CMOS 4-BIT MICROCONTROLLER

TMP47C440BN
TMP47C440BF

The 47C440B is high speed and high performance 4-bit single chip micro computers, integrating the 8-bit A/D converter and watchdog timer based on the TLCS-47 series.

PART No.	ROM	RAM	PACKAGE	OTP version
TMP47C440BN	4096 × 8-bit	256 × 4-bit	SDIP42-P-600-1.78	TMP47P440VN
TMP47C440BF			QFP44-P-1414-0.80D	TMP47P440VF

FEATURES

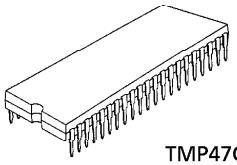
◆4-bit single chip microcomputer
◆Instruction execution time : 1.9 μs (at 4.2 MHz)
◆90 basic instructions
- Table look-up instructions
- 5-bit to 8-bit data conversion instruction

◆Subroutine nesting : 15 levels max.
◆6 interrupt sources (External : 2, Internal : 4)
All sources have independent latches each, and multiple interrupt control is available
◆I/O port (34 pins)
- Input 2 ports 5 pins
- Output 2 ports 8 pins
- I/O 6 ports 21 pins

◆Interval timer
◆Two 12-bit Timer/Counters
Timer, event counter, and pulse width measurement mode
◆Watchdog Timer
◆Serial Interface with 4-bit buffer
External/internal clock, leading/trailing edge shift mode
◆8-bit successive approximate type A/D converter
- With sample and hold
- 8 analog inputs
- Converting time : 48 μs (4 MHz)

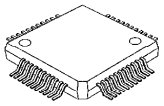
◆High current outputs
LED direct drive capability (typ. 20 mA × 8 bits)
◆Hold function
Battery/Capacitor back-up
◆Real Time Emulator : BM47214A

SDIP42-P-600-1.78



TMP47C440BN
TMP47P440BN

QFP44-P-1414-0.80D

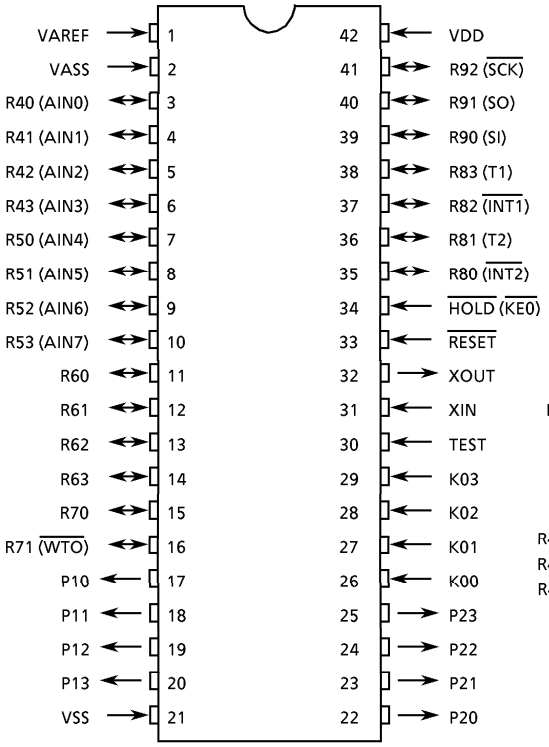


TMP47C440BF
TMP47P440BF

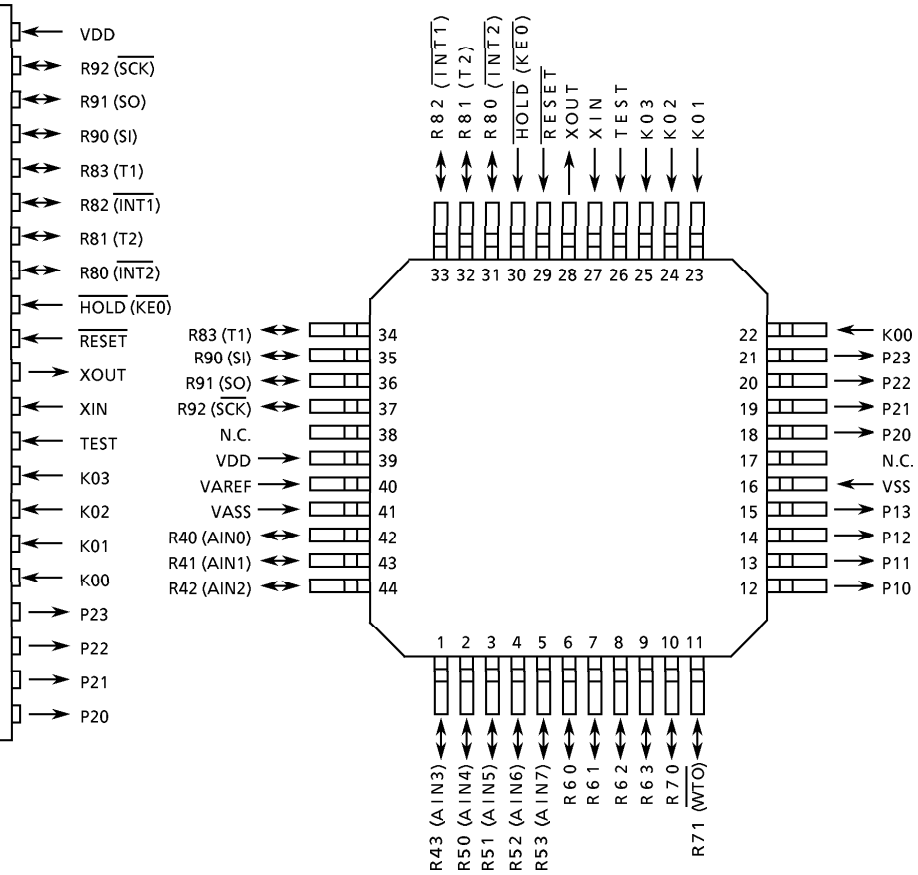
980901EBP1

PIN ASSIGNMENTS (TOP VIEW)

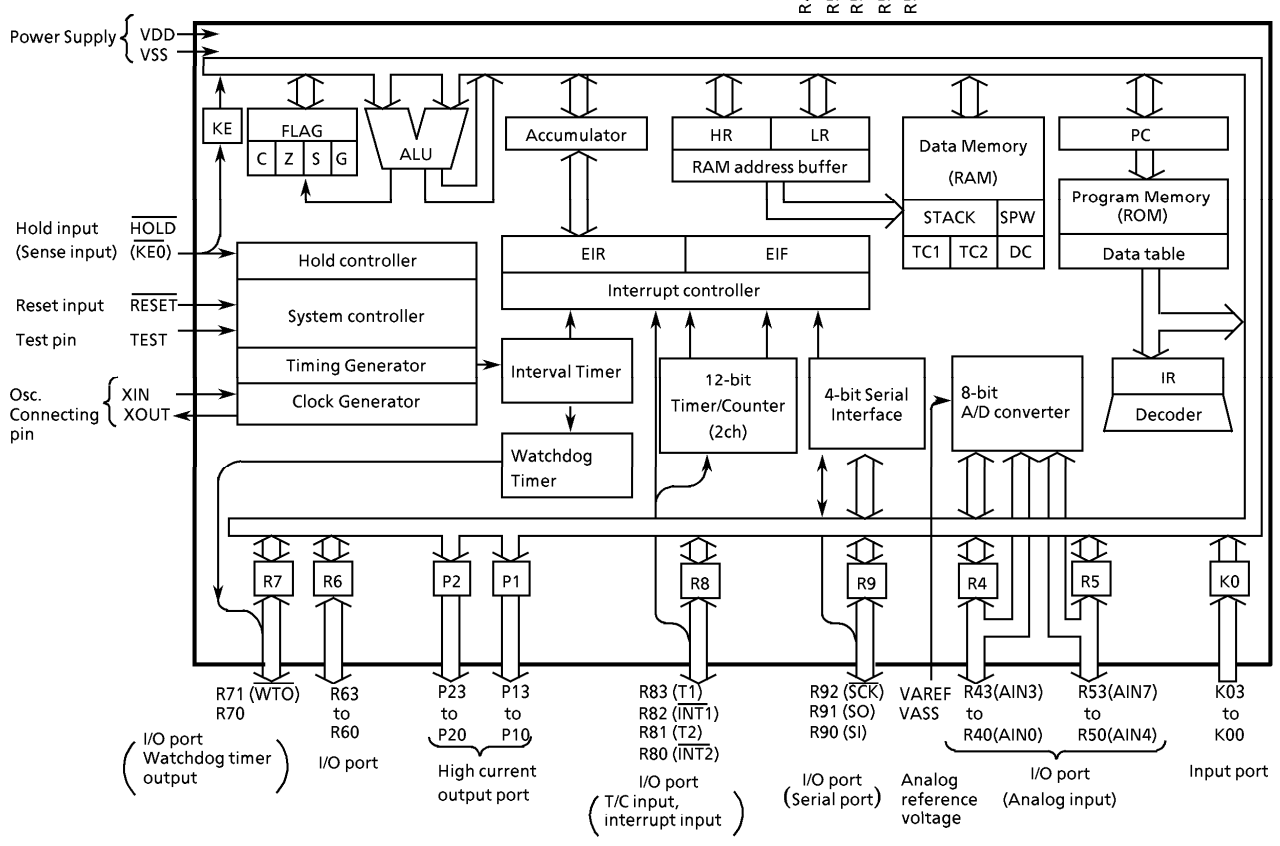
(1) SDIP42-P-600-1.78



(2) QFP44-P-1414-0.80D



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input / Output	FUNCTIONS	
K03 to K00	Input	4-bit input port	
P13 to P10	Output	4-bit output port with latch.	
P23 to P20		8-bit data are output by the 5-bit to 8-bit data conversion instruction [OUTB @HL].	
R43 (AIN3) to R40 (AIN0)	I/O (Input)	4-bit I/O port with latch. When used as input port or analog input, the latch must be set to "1".	A / D converter analog input
R53 (AIN7) to R50 (AIN4)			
R63 to R60	I/O	4-bit I/O port with latch	
R71 ($\overline{WTO}$)	I/O (Output)	2-bit I/O port with latch. When used as input port or watchdog timer output, the latch must be set to "1".	Watchdog timer output
R70	I/O		
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or timer/counter external input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 ($\overline{SCK}$)	I/O(I/O)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
XIN	Input	Resonator connecting pins. For inputting external clock, XIN is used and XOUT is opened.	
XOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)	HOLD request/release signal input	Sense input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power supply	+ 5V	
VSS		0V (GND)	
VAREF		A/D converter analog reference voltage (High)	
VASS		A/D converter analog reference voltage (Low)	

OPERATIONAL DESCRIPTION

Conserning the 47C440B, the hardware configuration and operation of hardwares are described.
As the description is porvided with priority on those parts deffering from the 47C400B, the technical data sheets for the 47C400B shall also be referred to.

1. SYSTEM CONFIGURATION

◆INTERNAL CPU FUNCTION

They are the same as those of the 47C440B.

◆PERIPHERAL HARDWARE FUNCTION

① I/O Port
② Interval Timer
③ Timer/Counters (TC1, TC2)
④ A/D Converter
⑤ Wachdog Timer
⑥ Serial Interface

The description has been provided with priority on functions (①, ④ and ⑤) added to and changed from the 47C400B.

2. PERIPHERAL HARDWARE FUNCTION

2.1 Ports

The 47C440B has 10 I/O ports (34 pins) each as follows :

① K0	;	4-bit input
② P1, P2	;	4-bit output
③ R4, R5	;	4-bit input/output (shared with the A/D converter analog inputs)
④ R6	;	4-bit input/output
⑤ R7	;	2-bit input/output (shared with the watchdog timer output)
⑥ R8	;	4-bit input/output(shared with external interrupt request input and timer/counter input)
⑦ R9	;	3-bit input/output (shared with serial port)
⑧ KE	;	1-bit sense input (shared with hold request/release signal input)

This section describes ports of ③ and ⑤ which are changed from the 47C400B.
Table 2-1 lists the port address assignments and the I/O instructions that can access the ports.

(1) Ports R4 (R43-R40), R5 (R53-R50)

Ports R4 and R5 are 4-bit I/O ports with latch shared by the analog inputs for A/D converter. When used as an input ports or analog inputs, the latch should be set to "1". If other port is used as an output, be careful not to execute the output instruction for any port during A/D conversion in order to keep accuracy of conversion. The latch is initialized to "1" and analog input is selected R40 (AIN0) pin during reset.

Port R4 (Port address OP04 / IP04)

3	2	1	0
R43 (AIN3)	R42 (AIN2)	R41 (AIN1)	R40 (AIN0)

Port R5 (Port address OP05 / IP05)

3	2	1	0
R53 (AIN7)	R52 (AIN6)	R51 (AIN5)	R50 (AIN4)

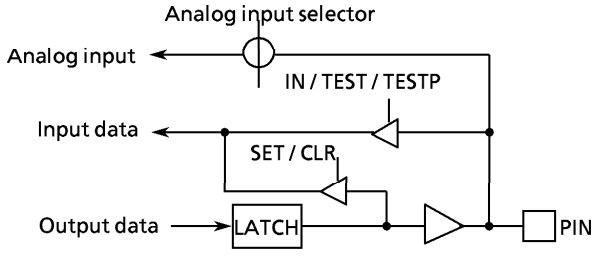


Figure 2-1. Port R4 and R5

(2) Port R7 (R71, R70)

Port R7 is 2-bits I/O port with latch. R71 pin is shared by the watchdog timer output. To use R71 pin for the watchdog timer output, the latch should be set to "1". The latch is initialized to "1" during reset. R70 pin is normal I/O pin. R72 and R73 pins do not exist actually but "1" is read when an input instruction is executed.

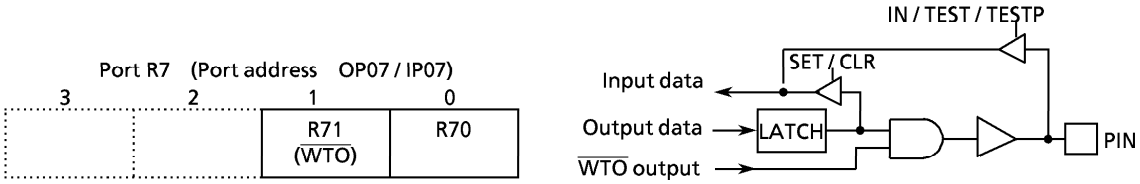


Figure 2-2. Port R7

Table 2-1. Port Address Assignments and Available I/O Instructions

Port Address (**)	Port		Input/Output instruction						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A,%p OUT @HL,%p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	K0 input port	——	○	–	–	–	–	○	–
01	P1 output latch	P1 output port	○	○	○	○ (Note 2)	○	○	–
02	P2 output latch	P2 output port	○	○	○		○	○	–
03	——	——	–	–	–	–	–	–	–
04	R4 input port (Analog input)	R4 output port	○	○	○	–	○	○	○
05	R5 input port (Analog input)	R5 output port	○	○	○	–	○	○	○
06	R6 input port	R6 output port	○	○	○	–	○	○	○
07	R7 input port	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	R9 input port	R9 output port	○	○	○	–	○	○	–
0A	——	——	–	–	–	–	–	–	–
0B	——	——	–	–	–	–	–	–	–
0C	A / D status input	——	○	–	–	–	–	○	–
0D	A / D converted value	——	○	–	–	–	–	–	–
0E	SIO, Hold status	——	○	–	–	–	–	○	–
0F	Serial recieve buffer	Serial transmit buffer	○	○	○	–	–	–	–
10_H	Undefined	Hold operating mode control	–	○	–	–	–	–	–
11	Undefined	——	–	–	–	–	–	–	–
12	Undefined	A / D analog input selector	–	○	–	–	–	–	–
13	Undefined	A / D start register	–	○	–	–	–	–	–
14	Undefined	——	–	–	–	–	–	–	–
15	Undefined	Watchdog Timer control	–	○	–	–	–	–	–
16	Undefined	——	–	–	–	–	–	–	–
17	Undefined	——	–	–	–	–	–	–	–
18	Undefined	——	–	–	–	–	–	–	–
19	Undefined	Interval Timer intrrupt control	–	○	–	–	–	–	–
1A	Undefined	——	–	–	–	–	–	–	–
1B	Undefined	——	–	–	–	–	–	–	–
1C	Undefined	Timer/Counter 1 control	–	○	–	–	–	–	–
1D	Undefined	Timer/Counter 2 control	–	○	–	–	–	–	–
1E	Undefined	——	–	–	–	–	–	–	–
1F	Undefined	Serial interface control	–	○	–	–	–	–	–

Note 1. *"——" means the reserved state. Unavailable for the user programs.*

Note 2. *The 5-bit to 8-bit data conversion instruction [OUTB @HL], automatic access to ports P1 and P2.*

2.2 A/D Converter

The 47C440B has a 8-bit successive approximate type A/D converter and is capable of processing 8 analog inputs.

2.2.1 Circuit configuration

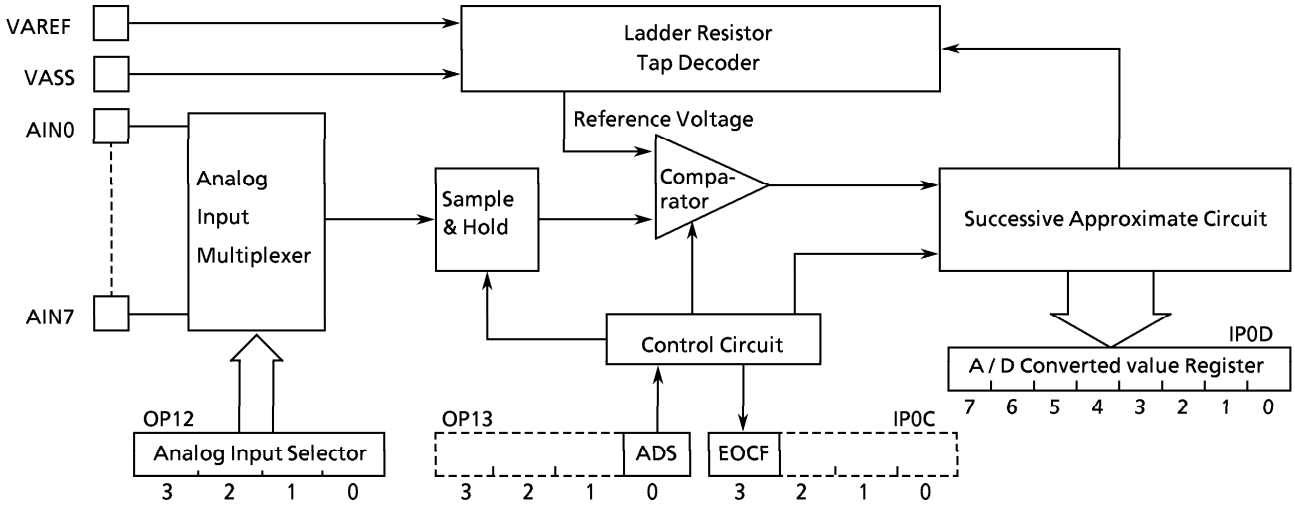


Figure 2-3. Block Diagram of A/D Converter

2.2.2 Control of A/D converter

The operation of A/D converter is controlled by a command register (OP12, OP13, IP0C, IP0D).

(1) Analog input selector (OP12)

Analog inputs (AIN0 through AIN7) are selected by values of this register.

Analog input select command register
(Port address OP12) (Initial value 0000)

3	2	1	0
SAIN			

SAIN	Analog input selection
0000:	R40(AIN0)
0001:	R41(AIN1)
0010:	R42(AIN2)
0011:	R43(AIN3)
0100:	R50(AIN4)
0101:	R51(AIN5)
0110:	R52(AIN6)
0111:	R53(AIN7)
1***:	Analog input is not selected.

*Note. * ; don't care*

Figure 2-4. Analog input selector

(2) Start of A/D conversion (OP13)

A/D conversion is started when ADS is set to "1" . After the conversion is started, ADS is cleared by hardware. If the restart is requested during the conversion, the conversion is started again at the time. Analog input voltage is hold by the sample hold circuit.

A / D conversion start command register
(Port address OP13) (Initial value 0000)

3	2	1	0
			ADS

ADS	A / D conversion enable

1: A/D conversion is started (clears after starting)

Figure 2-5. A/D conversion start register

(3) A/D converter and frag (IP0C)

End of Conversion Flag (EOCF) is a single bit flag showing the end of conversion and is set to "1" when conversion ended. When both upper 4 bits and lower 4 bits of a converted value are read or A/D conversion is started, EOCF is cleared to "0".

A / D converter status register
(Port address IP0C)

3	2	1	0
EOCF			

EOCF	End of conversion flag

0: Under A/D conversion or before A/D conversion

1: End of A/D conversion

Figure 2-6. A/D converter status register

(4) A/D converted value register (IP0D)

An A/D converted value is read by accessing port address IP0D. An A/D converted value is read by splitting into upper 4 bits and lower 4 bits by a value of LR_0 (LSB of the L registers).

A / D converted value register
(Port address IP0D)

3	2	1	0
D3	D2	D1	D0
D7	D6	D5	D4

D7 to D0	A/D converted value register

When $LR_0 = 0$, lower 4 bits of the converted value is read.

When $LR_0 = 1$, upper 4 bits of the converted value is read.

Figure 2-7. A/D converted value register

2.2.3 How to use A/D converter

Apply positive of analog reference voltage to the VAREF pin and negative to the VASS pin. The A/D conversion is carried out by splitting reference voltage between VAREF and VASS to bit corresponding voltage by a ladder resistor and making a judgement by comparing it with analog input voltage.

(1) Start of A / D conversion

Prior to conversion, select one of the analog input AIN0 through AIN7 by the analog input selector. Place output of the analog input, which is to be A/D converted, in the high impedance state by setting "1". If other port is used as an output, be careful not to execute the output instruction for any port during conversion in order to keep accuracy of conversion.

A/D conversion is started by setting ADS (bit 1 of the A/D conversion start register). When conversion ends after 24 instruction cycles, EOCF showing the end of conversion is set to "1".

Analog input voltage is sampled during the following 2 instruction cycles after setting conversion enable.

Note. The sample and hold circuit has capacitor (C_A = 12 pF typ.) with resister (RA = 5 kΩ typ.). See I/O circuitry table. This capacitor should be charged or discharged within 2 instruction cycles.

(2) Reading of an A/D converted value

After the end of conversion, read an A/D converted value is read by splitting into lower 4 bits and upper 4 bits by the A/D converted value register (IP0D).

Lower 4 bits of the A/D converted value can be read when LR_0 = 0 and upper 4 bits when LR_0 = 1. Usually an A/D converted value is stored in RAM by an instruction [IN %p, @HL]. Further, if an A/D converted value is read during the conversion, it becomes an indefinite value.

(3) A / D conversion with HOLD operation

When the HOLD operation is started during the conversion, the conversion is terminated and an A/D converted value becomes indefinite. Therefore, EOCF is kept clear to "0" after release from the HOLD operation. However, if the HOLD operation is started after the end of A/D conversion (after EOCF has been set), A/D converted value and status of EOCF are held.

Example: Selecting analog input (AIN3) , starting A/D conversion, monitoring EOCF and storing lower 4 bits and upper 4 bits of a converted value to RAM [10_H] and RAM [11_H] respectively.

```
        LD      A, #3H          ;  Selects analog input (AIN3)
        OUT     A, %OP12
        LD      A, #1H          ;  Start of A/D conversion
        OUT     A, %OP13
SLOOP : TEST    %IP0C, 3        ;  To wait until EOCF goes to "1"
        B       SLOOP
        LD      HL, #10H        ;  HL ← 10H
        IN      %IP0D, @HL      ;  RAM [10H] ← Lower 4 bits
        INC     L               ;  Increment of L registers
        IN      %IP0D, @HL      ;  RAM [11H] ← Upper 4 bits
```

2.3 Watchdog Timer (WDT)

The purpose of the watchdog timer is to detect the malfunction (ranaway) of program due to external noise or other causes and return the operation to the normal condition.

The watchdog timer output is output to R71 must be set to "1". Further, during reset, the output latch of R71 is set to "1", and the watchdog timer becomes disable state.

The initialization at time of runaway will become possible when the $\overline{WTO}$ pin and $\overline{RESET}$ pin are connected each other.

2.3.1 Configuration of Watchdog Timer

The watchdog timer consists of 3-stage binary counter, flip-flop (F/F), and its control circuit. The F/F is set to "1" during reset, and cleared to "0" at the rising edge of the binary counter output.

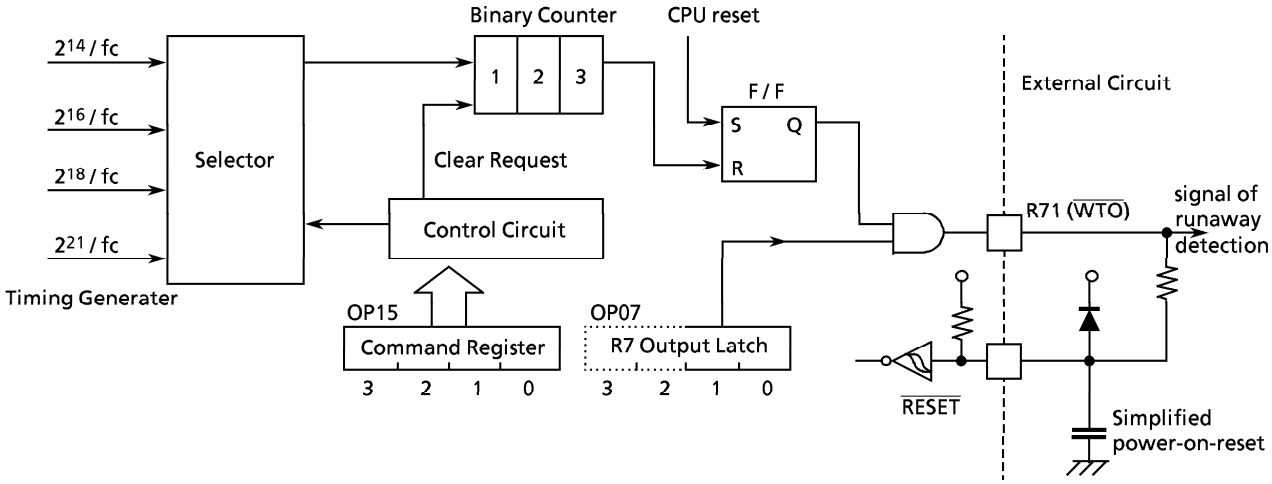


Figure 2-8. Watchdog Timer

2.3.2 Control of watchdog timer

The watchdog timer is controlled by the command register (OP15). This command register is initialized to "0000_B" during reset. The following are procedure to detect the malfunction (runaway) of CPU by the watchdog timer.

① At first, detection time of the watchdog timer should be set and binary counter should be cleared.

② The watchdog timer should be become enable.

③ Binary counter must be cleared before the detection time of the watchdog timer. When the runaway of CPU is taken place for some reason and binary counter is not cleared, the F/F is cleared to "0"at the rising edge of the binary counter and signal of runaway detection is become active ($\overline{WTO}$ output is "L").

Watchdog Timer control command register

(Port address OP15) (Initial value 1000)

3	2	1	0
RWT	EWT	TWT	

RWT	Clears binary counter

0 : Clears binary counter (After clear, automatically "1" is set)

EWT	Enable/Disable

0 : Disable

1 : Enable

TWT	Setting of watchdog timer detection time

Example : At fc = 4.19 MHz

00 : 2^{17} / fc [s] ····· 31.25 [ms]

01 : 2^{19} / fc ····· 125

10 : 2^{21} / fc ····· 500

11 : 2^{24} / fc ····· 4000

Note. fc ; Basic clock frequency [Hz]

Figure 2-9. Command Register

Example : To set the watchdog detection time (2^{21} / fc[s]). And to enable the watchdog timer.

```
        LD      A, #0010B       ; OP15 ← 0010B
                                  (Sets WDT detection time. Clears binary counter)
        OUT     A, %OP15
        LD      A, #0110B       ; OP15 ← 0110B (Enables WDT)
        OUT     A, %OP15
        :
        :
        :
        LD      A, #0110B       ; OP15 ← 0110B (Clears binary counter)
        OUT     A, %OP15
        :
        :
```

Within WDT detection time

Note. RWT can be operated only by clearing to "0". Note that both EWT (Enable Watchdog Timer) and RWT should not be set to "1" at the same time.

Port Condition by RESET Operation

The transition of Port condition by RESET operation is shown as below.

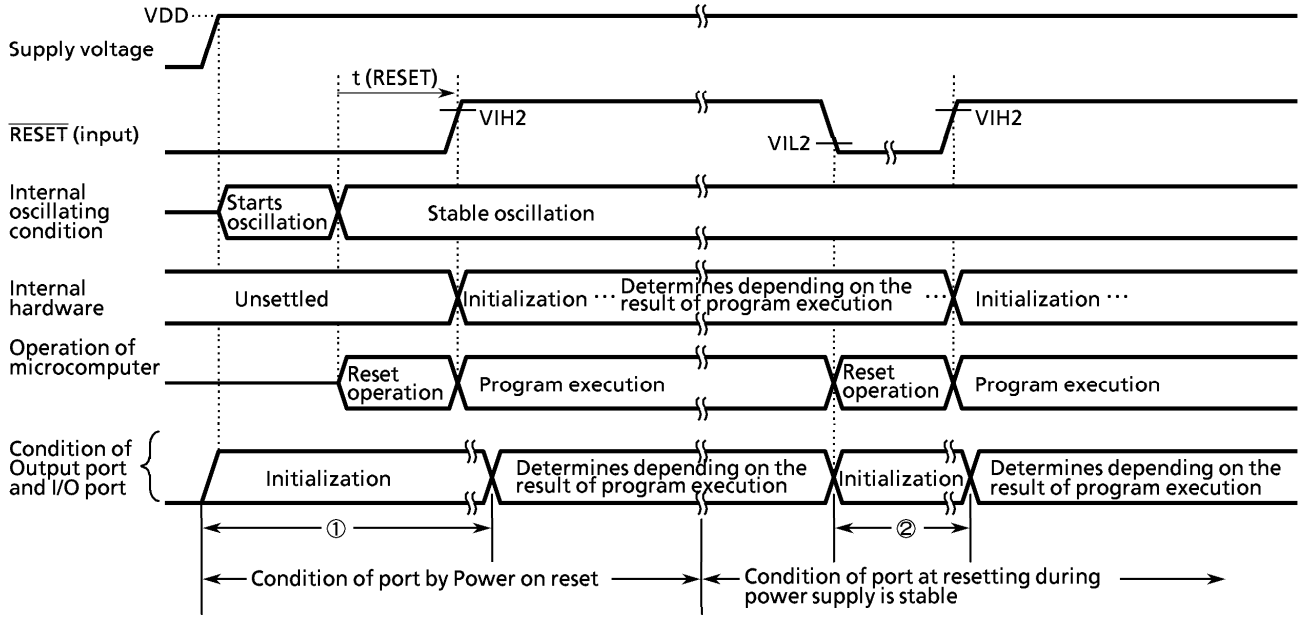


Figure 2-10. Port condition by Reset operation

Note 1: t (RESET) > 24/fc

Note 2: VIL2 : Stands for low level input voltage of RESET pin.
VIH2 : Stands for high level input voltage of RESET pin.

Note 3: The term from power on reset to the time program is executed (above ①) and also the term starting from reset operation during power supply is stable to the program is executed (above ②), the port is on the initial condition. The initial condition of Port differs from I/O circuit by each port, refer to the section of "INPUT/OUTPUT CIRCUITRY". Thus, when using Port as an output pin, in the term of the above ① and ②, the voltage level on the signal that connects with the output pin of Port to the input pin of external application circuit should be determined by the external circuitry such as pull-up resistor and / or pull-down resistor.

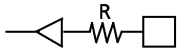
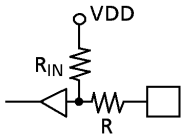
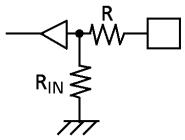
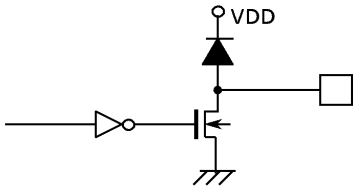
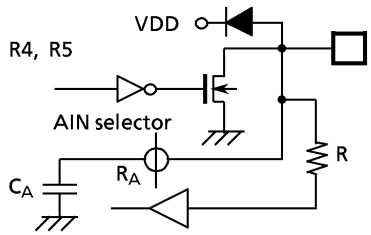
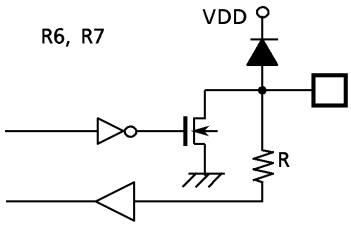
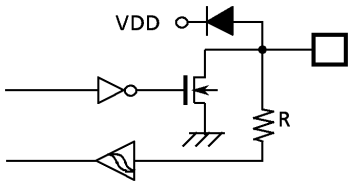
INPUT/OUTPUT CIRCUITRY

(1) Control pins

The input/output circuitries of the 47C440B control pins are similar to that of the 47C400B.

(2) I/O Ports

The input/output circuitries of the 47C440B I/O ports are shown below, any one of the circuitries can be chosen by a code (SA-SC) as a mask option.

PORT	I/O	INPUT/OUTPUT CIRCUITRY and CODE			REMARKS
		SA	SB	SC	
K0	Input				Pull-up / pull-down resistor R_{IN} = 70 kΩ (typ.) R = 1 kΩ (typ.)
P1 P2	Output				Sink open drain output Initial "Hi-Z" High current I_{OL} = 20 mA (typ.)
R4 R5 R6 R7	I/O				Sink open drain output Initial "Hi-Z" R = 1 kΩ (typ.) Analog input R_A = 5 kΩ (typ.) C_A = 12 pF (typ.)
R8 R9	I/O				Sink open drain output Initial "Hi-Z" Hysteresis input R = 1 kΩ (typ.)

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT}		– 0.3 to V_{DD} + 0.3	V
Output Current (Per 1 pin)	I_{OUT1}	Ports R	3.2	mA
	I_{OUT2}	Ports P1, P2	30	
Output Current (Total)	ΣI_{OUT}	Ports P1, P2	120	mA
Power Dissipation [T_{opr} = 70℃]	PD		600	mW
Soldering Temperature (time)	Tsld		260 (10 s)	℃
Storage Temperature	Tstg		– 55 to 125	℃
Operating Temperature	Topr		– 30 to 70	℃

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = – 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		fc = 6.0 MHz	4.5	5.5	V
			fc = 4.2 MHz	2.7		
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5$ V	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5$ V	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT		0.4	6.0	MHz

Note. Input voltage V_{IH3}, V_{IL3} : in the HOLD mode

D.C. CHARACTERISTICS

(V_{SS} = 0V, T_{opr} = – 30 to 70 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	—	—	± 2	μA
	I_{IN2}	Ports R (open drain)					
Low Input Current	I_{IL}	Ports R (push-pull)	V_{DD} = 5.5V, V_{IN} = 0.4V	—	—	– 2	mA
Input Resistance	R_{IN1}	Port K0 with pull-up/pull-down		30	70	150	kΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Ports R (open drain)	V_{DD} = 5.5V, V_{OUT} = 5.5V	—	—	2	μA
Output Low Voltage	V_{OL2}	Except XOUT, ports P	V_{DD} = 4.5V, I_{OL} = 1.6 mA	—	—	0.4	V
Low output Current	I_{OL1}	Ports P1, P2	V_{DD} = 4.5V, V_{OL} = 1.0V	—	20	—	mA
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5V, fc = 4 MHz	—	3	6	mA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5V	—	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25 °C, V_{DD} = 5V.

Note 2. Input Current I_{IN1} ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3. Supply Current I_{DD}, I_{DDH} ; V_{IN} = 5.3V/0.2V
The K0 port is open when the input resistor is contained. The voltage applied to the R port is within the valid range.

A / D CONVERSION CHARACTERISTICS

(T_{opr} = – 30 to 70 °C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Analog Reference Voltage	V_{AREF}		V_{DD} – 1.5	—	V_{DD}	V
	V_{ASS}		V_{SS}	—	1.5	
Analog Reference Voltage Range	ΔV_{AREF}	V_{AREF} – V_{ASS}	2.5	—	—	V
Analog Input Voltage	V_{AIN}		V_{ASS}	—	V_{AREF}	V
Analog Supply Current	I_{REF}		—	0.5	1.0	mA
Nonlinearity Error		V_{DD} = 5.0V, V_{SS} = 0.0V V_{AREF} = 5.000V V_{ASS} = 0.000V	—	—	± 1	LSB
Zero Point Error			—	—	± 1	
Full Scale Error			—	—	± 1	
Total Error			—	—	± 2	

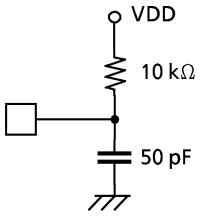
A. C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 4.5 to 5.5V, T_{opr} = – 30 to 70°C)

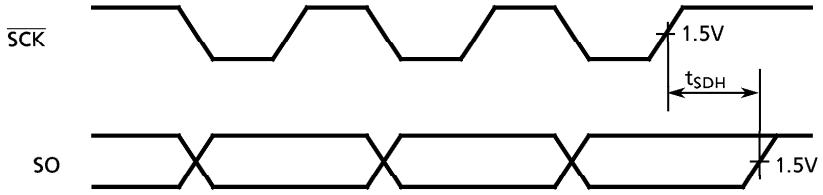
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}		1.9	—	20	μs
High level Clock pulse Width	t_{WCH}	External clock mode	80	—	—	ns
Low level Clock pulse Width	t_{WCL}					
A/D Sampling Time	t_{AIN}	fc = 4 MHz	—	4	—	μs
Shift Data Hold Time	t_{SDH}		0.5 t_{cy} – 300	—	—	ns

Note. Shift Data Hold Time

External circuit for $\overline{SCK}$ pin and SO pin



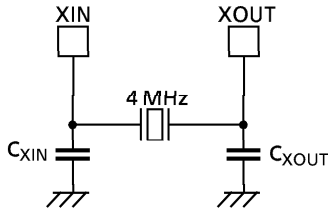
Serial port (completion of transmission)



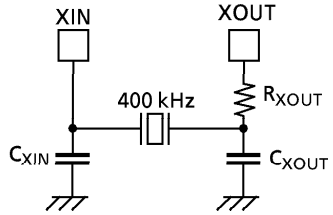
RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0V, V_{DD} = 4.5 to 5.5V, T_{opr} = – 30 to 70°C)

(1) 4MHz
Ceramic Resonator
CSA4. 00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 30 pF
KBR-4. 00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30 pF
Crystal Oscillator
204B-6F 4. 0000 (TOYOCOM) $C_{XIN} = C_{XOUT}$ = 20 pF



(2) 400kHz
Ceramic Resonator
CSB400B (MURATA) $C_{XIN} = C_{XOUT}$ = 220 pF, R_{XOUT} = 6.8 kΩ
KBR-400B (KYOCERA) $C_{XIN} = C_{XOUT}$ = 100 pF, R_{XOUT} = 10 kΩ



TYPICAL CHARACTERISTICS