OKI Semiconductor

MSM66201/66P201/66207/ 66P207

nX 66K CMOS 16-Bit Microcontroller

GENERAL DESCRIPTION

The MSM66201/66207 is a high-performance microcontroller implemented in silicon-gate complementary metal-oxide semiconductor (CMOS) technology. Integrated within this chip are a 16-bit ALU, 32K bytes of mask-program ROM, 1024 bytes of data RAM, 48 I/O lines, multifunction 16-bit timers, a 10-bit A/D converter, a serial I/O port, a pulse-width modulator (PWM), and an oscillator. The MSM66P201/66P207 is the OTP (One-Time Programmable) versions of the MSM66201/66207.

FEATURES

- 8-bit external data bus interface
- 16-bit internal architecture
- 64K address space for program memory
  - MSM66201 : 16K bytes of internal ROM
    Max. 48K bytes of external ROM
  - MSM66207 : 32K bytes of internal ROM
    Max. 32K bytes of external ROM
  - Internal ROMs of the MSM66P201/66P207 are OTP versions.
- 64K address space for data memory
  - MSM66201 : 512 bytes of internal RAM
    Max. 63.5K bytes of external RAM
  - MSM66207 : 1024 bytes of internal RAM
    Max. 63K bytes of external RAM
- High-speed execution
  - Minimum cycle for instruction : 400ns @ 10MHz
- Powerful instruction set : 8/16-bit data transfer instructions
  8/16-bit arithmetic instructions
  16(8)bits × 16(8)bits → 32(16)bits
  32(16)bits ÷ 16(8)bits → 32(16)bits
  16(8)bits ± 16(8)bits → 16(8)bits
  8/16-bit logic instructions
  Bit manipulation instructions
  ROM table reference instructions
- Numerous addressing modes
- I/O port : 6 ports, 48 bits

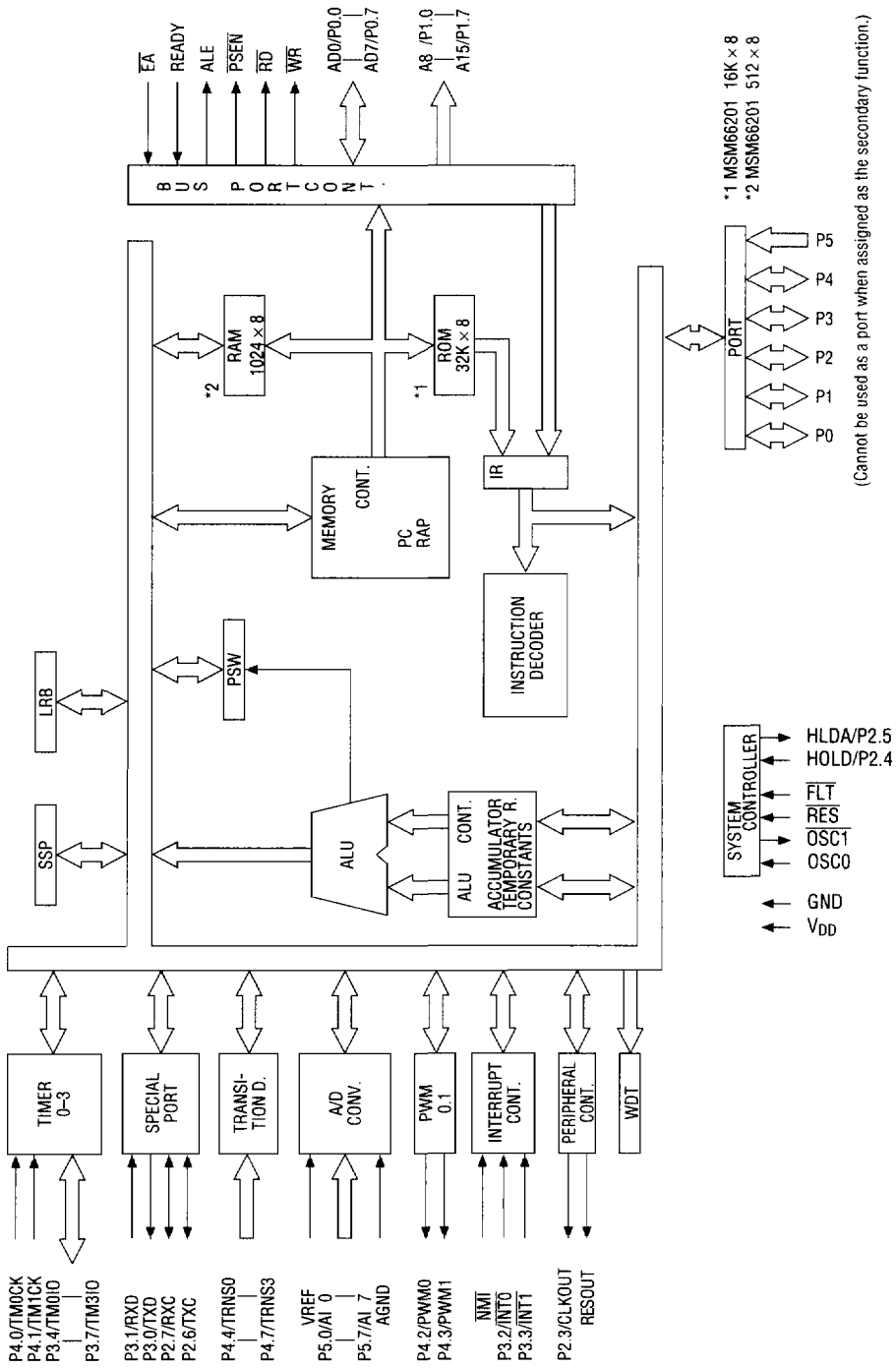
Input/output port	40 bits
Input	8 bits

- Multifunctional 16-bit timer × 4
  Each timer has the following 4 modes. : Auto-reload timer mode
  Clock output mode
  Capture register mode
  Real time output mode

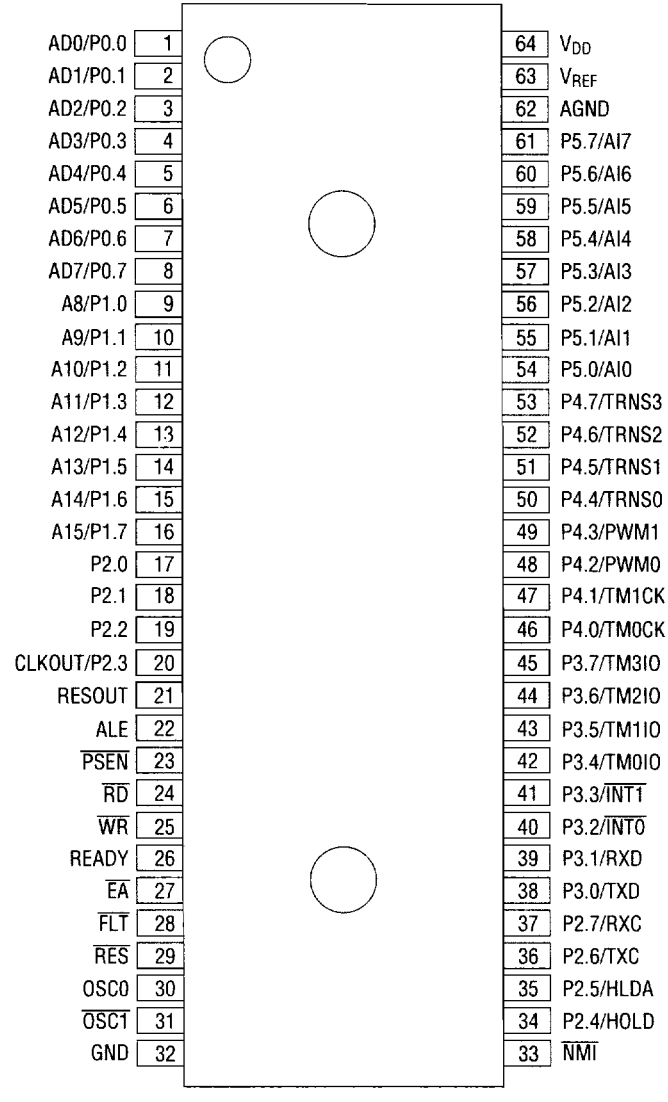
- Multifunctional serial port
  - : Baud rate generators independently used for transmit and receive
  - : Data length, parity, and stop bit setting
  - : Synchronous/asynchronous (UART) mode setting
  - : Multiprocessor communication mode/ normal mode setting
  - : Receive error status detection
- 16-bit pulse width modulator × 2
- Watchdog timer
- Transition detector × 4
- 10-Bit A/D converter (8 channels)
- 1 non-maskable interrupt, 16 maskable interrupts
- Stand-by function
  - STOP mode : Software clock stop mode
  - HALT mode : Software CPU stop mode
  - HOLD mode : Hardware CPU stop mode
- Package
  - 64-pin plastic shrink DIP (SDIP64-P-750) : (MSM66201-xxxSS) (MSM66P201-xxxSS) (MSM66207-xxxSS) (MSM66P207-xxxSS)
  - 64-pin plastic QFP (QFP64-P-1414-BK) : (MSM66201-xxxGS-BK) (MSM66P207-xxxGS-BK)
  - 68-pin plastic QFJ (PLCC) (QFJ68-P-S950) : (MSM66201-xxxJS) (MSM66P201-xxxJS) (MSM66207-xxxJS) (MSM66P207-xxxJS)
  - 64-pin ceramic piggyback : (MSM66G207VS)

* The piggyback type is used only for engineering samples.
xxx indicates the code number.

BLOCK DIAGRAM

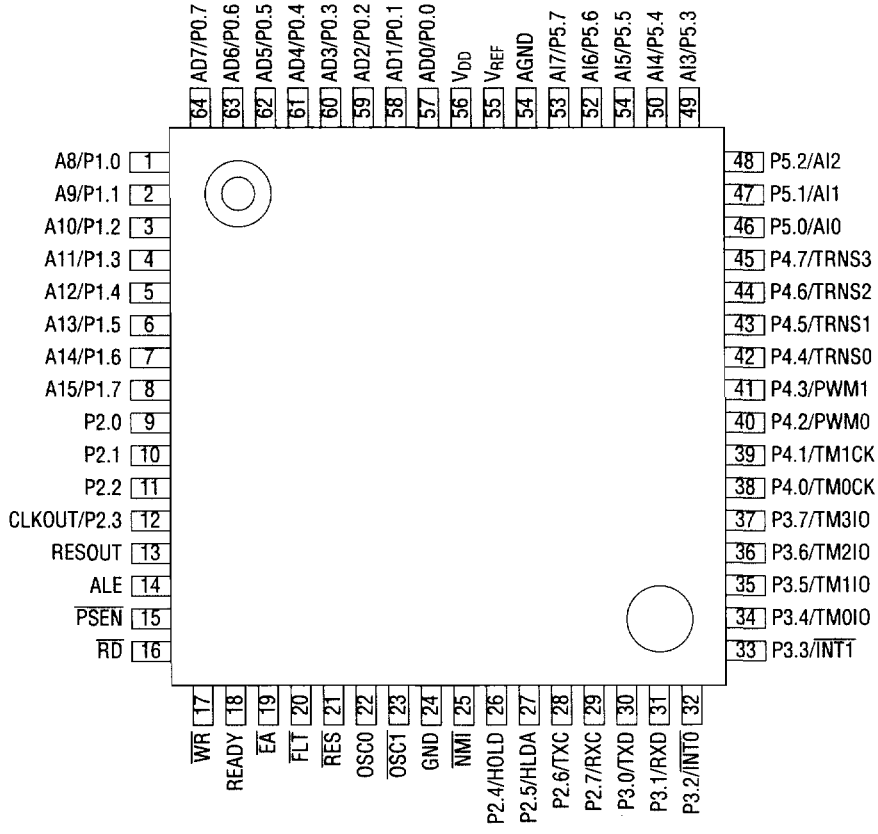


PIN CONFIGURATION (TOP VIEW)



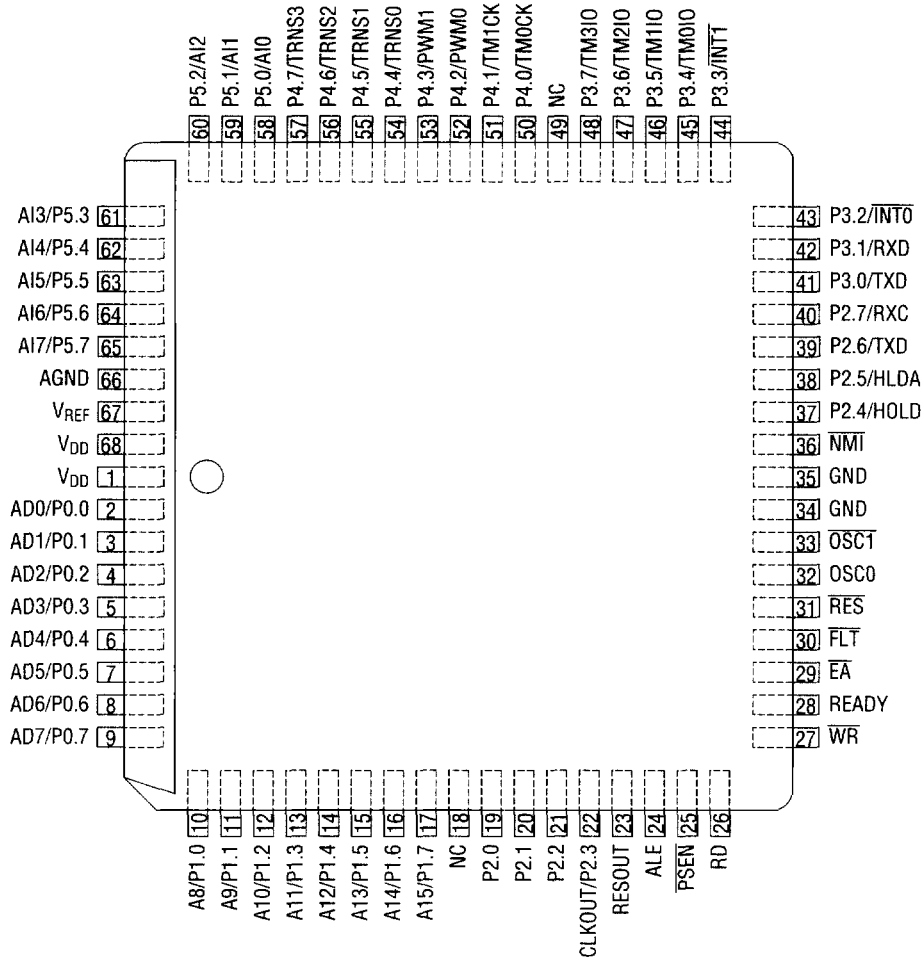
64-Pin Plastic Shrink DIP

PIN CONFIGURATION (TOP VIEW) (Continued)



64-Pin Plastic QFP

PIN CONFIGURATION (TOP VIEW) (Continued)



68-Pin Plastic QFJ (PLCC)

PIN DESCRIPTION

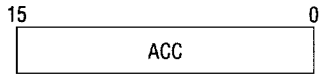
Symbol	Type	Description
P0.0–P0.7/ AD0–AD7	I/O	P0: 8-bit I/O port. Each bit can be assigned to input or output. AD: Outputs the lower 8 bits of program counter during external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. This pin also outputs the address and outputs or inputs data during an external data memory access instruction, under the control of ALE, $\overline{RD}$, and $\overline{WR}$.
P1.0–P1.7/ A8–A15	I/O	P1: 8-bit I/O port. Each bit can be assigned to input or output. A: Outputs the upper 8 bits of program counter (PC_{8-15}) during external program memory fetch. This pin also outputs the upper 8 bits of address during external data memory access instructions.
P2.0–P2.2	I/O	P2: 8-bit I/O port. Each bit can be assigned to input or output.
P2.3–CLKOUT		CLKOUT: Clock output pin. Output frequency range is equal to or twice the system clock.
P2.4/HOLD		HOLD: Input pin to request the CPU to enter the hardware power-down state.
P2.5/HLDA		HLDA: HOLD ACKNOWLEDGE: the HLDA signal appears in response to the HOLD signal and indicates that the CPU has entered the power-down state.
P2.6/T_XC		T_XC: Transmitter clock input/output pin.
P2.7/R_XC		R_XC: Receiver clock input/output pin.
P3.0/T_XD	I/O	P3: 8-bit I/O port. Each bit can be assigned to input or output.
P3.1/R_XD		T_XD: Transmitter data output pin.
P3.2/$\overline{INT0}$		R_XD: Receiver data input pin.
P3.3/$\overline{INT1}$		$\overline{INT}$: Interrupt request input pin. Falling edge trigger or level trigger is selectable.
P3.4/TM0IO		TM0IO-TM3IO: One of the following signals is output or input.
P3.5/TM1IO		• Clock at twice the frequency range of the 16-bit timer overflow
P3.6/TM2IO		• Load trigger signal to the capture register input
P3.7/TM3IO		• Setting value output
		Whether the signal is input or output depends on the mode.
P4.0/TM0CK	I/O	P4: 8-bit I/O port. Each bit can be assigned to input or output.
P4.1/TM1CK		TM0CK, TM1CK: Clock input pins of timer 0, timer 1.
P4.2/PWM0		TRANS: Transition detector.
P4.3/PWM1		The input pins which sense the falling edge and set the flag.
P4.4 – P4.7		PWM: 16-bit pulse-width modulator output pin.
TRANS0 – TRANS3		
P5.0 – P5.7/ AI0 –AI7	I	P5: 8-bit input port. AI: Analog signal input pin for A/D converter.

PIN DESCRIPTION (Continued)

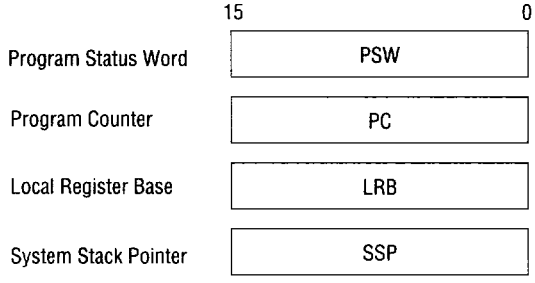
Symbol	Type	Description
RESOUT	Output	Outputs "H" level in the case of internal reset. Reset to"L" level by program.
ALE	Output	Address Latch Enable: The timing pulse to latch the lower 8 bits of the address output from port 0 when the CPU accesses the external memory.
$\overline{PSEN}$	Output	Program Strobe Enable: The strobe pulse to fetch to external program memory.
$\overline{RD}$	Output	Output strobe activated during a bus read cycle. Used to enable data onto the bus from the external data memory.
$\overline{WR}$	Output	Output strobe during a bus write cycle. Used as write strobe to external data memory.
READY	Input	Used when the CPU accesses low-speed peripherals.
$\overline{EA}$	Input	Normaly set to "H" level. If set to "L" level, the CPU fetches the code from external program memory.
$\overline{FLT}$	Input	If $\overline{FLT}$ is "H" level, ALE, $\overline{WR}$, $\overline{RD}$, $\overline{PSEN}$ are set to "H" level when reset. If $\overline{FLT}$ is set to "L", ALE, $\overline{WR}$, $\overline{RD}$, $\overline{PSEN}$ are set to floating level when reset.
$\overline{RES}$	Input	RESET input pin.
OSC0, $\overline{OSC1}$	Input/Output	Oscillation circuit input and output.
$\overline{NMI}$	Input	Non-maskable interrupt input pin (falling edge).
V_{REF}	—	Reference voltage input pin for A/D converter.
AGND	—	Ground for A/D converter.
V_{DD}	—	System power supply.
GND	—	Ground.

REGISTERS

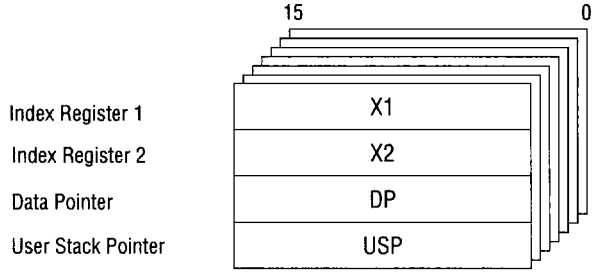
Accumulator



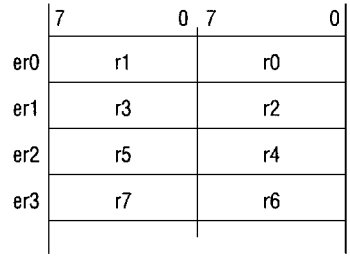
Control Register (CR)



Pointing Register (PR)



Local Register



SFR

Address (HEX)	Name	Symbol	R/W	8/16-bit Operation	Reset
0000	System stack printer	SSP (ASSP)	R/W	8/16	FFH
0001					FFH
0002	Local register base	LRB (ALRB)			undefined
0003					
0004	Program status word	PSWL (APSW)			C8H
0005		PSWH			0CH
0006	Accumulator	ACC			00H
0007					00H
0010	Standby control register	SBYCON		8	F8H
0011	Watchdog timer	WDT	W		00H/WDT is stopped
0012	Peripheral control register	PRPHF	R/W		FDH
0013	Stop code acceptor	STPACP	W		"0"
0018	Interrupt request flag	IRQ	R/W	8/16	00H
0019					00H
001A	Interrupt enable flag	IE			00H
001B					00H
001C	External linterrupt control register	EXICON		8	FCH
0020	Port 0 data register	P0			undefined
0021	Port 0 mode register	P0IO			00H
0022	Port 1 data register	P1			undefined
0023	Port 1 mode register	P1IO			00H
0024	Port 2 data register	P2			undefined
0025	Port 2 mode register	P2IO			00H
0026	Port 2 secondary function control register	P2SF			07H
0028	Port 3 data register	P3			undefined
0029	Port 3 mode register	P3IO			00H
002A	Port 3 secondary function control register	P3SF			00H
002C	Port 4 data register	P4			undefined
002D	Port 4 mode register	P4IO			00H
002E	Port 4 secondary function control register	P4SF			00H
002F	Port 5	P5	R		—
0030	Timer 0 counter	TM0	R/W	16	00H
0031					00H
0032	Timer 0 register	TMR0			00H
0033					00H
0034	Timer 1 counter	TM1			00H
0035					00H
0036	Timer 1 register	TMR1			00H
0037					00H

SFR (Continued)

Addres (HEX)	Name	Abbreviated Name	R/W	8/16-bit Operation	Reset
0038	Timer 2 counter	TM2	R/W	16	00H
0039					00H
003A	Timer 2 register	TMR2			00H
003B					00H
003C	Timer 3 counter	TM3			00H
003D					00H
003E	Timer 3 register	TMR3			00H
003F					00H
0040	Timer 0 control register	TCON0		8	00H
0041	Timer 1 control register	TCON1			00H
0042	Timer 2 control register	TCON2			00H
0043	Timer 3 control register	TCON3			00H
0046	Transition detector register	TRNSIT			undefined
0048	Serial port transmission baud rate generator counter	STTM			00H
0049	Serial port transmission baud rate generator register	STTMR			00H
004A	Serial port transmission baud rate generator control register	STTMC			0CH
004C	Serial port receiving baud rate generator counter	SRTM			00H
004D	Serial port receiving baud rate generator register	SRTMR			00H
004E	Serial port receiving baud rate generator control register	SRTMC			0EH
0050	Serial port transmission mode control register	STCON			80H
0051	Serial port transmission data buffer register	STBUF	W		undefined
0054	Serial port receiving mode control register	SRCON	R/W		00H
0055	Serial port receiving data buffer register	SRBUF	R		undefined
0056	Serial port receiving error register	SRSTAT	R/W		F0H
0058	A/D scan mode register	ADSCAN			80H
0059	A/D select mode register	ADSEL			A0H
0060	A/D conversion result register 0	ADCR0	R	8/16	undefined
0061					

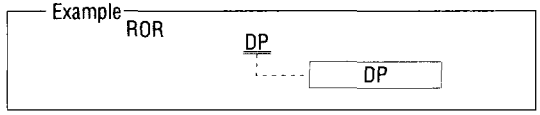
SFR (Continued)

Address (HEX)	Name	Abbreviated Name	R/W	8/16-bit operation	Reset
0062	A/D conversion result register 1	ADCR1	R	8/16	undefined
0063					
0064	A/D conversion result register 2	ADCR2			
0065					
0066	A/D conversion result register 3	ADCR3			
0067					
0068	A/D conversion result register 4	ADCR4			
0069					
006A	A/D conversion result register 5	ADCR5			
006B					
006C	A/D conversion result register 6	ADCR6			
006D					
006E	A/D conversion result register 7	ADCR7			
006F					
0070	PWM 0 counter	PWMC0	R/W		00H
0071					00H
0072	PWM 0 register	PWMR0			00H
0073					00H
0074	PWM 1 counter	PWMC1			00H
0075					00H
0076	PWM 1 register	PWMR1			00H
0077					00H
0078	PWM 0 control register	PWCON0		8	00H
007A	PWM 1 countrol register	PWCON1			00H

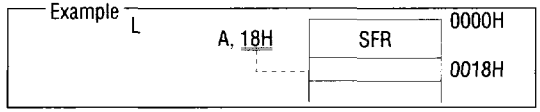
ADDRESSING MODES

The MSM66201/66207 supports 64KB of data space and 64KB of program space with various types of addressing modes. These modes are divided into the following types.

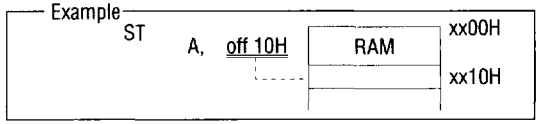
1. RAM Addressing (for data space)
1.1 Register Direct Addressing



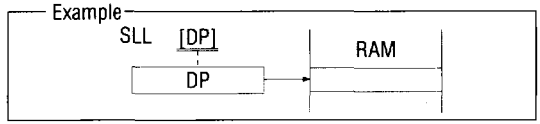
1.2 Displacement Addressing
a) Zero Page



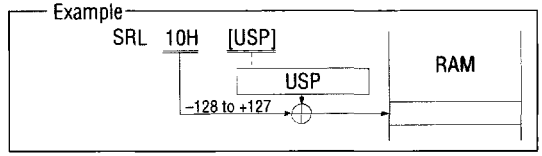
b) Direct Page



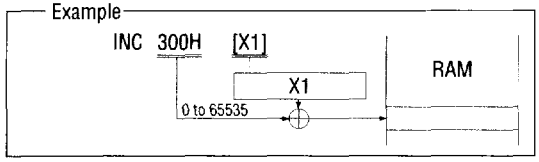
1.3 Pointing Register (PR) Indirect Addressing
a) Data Point (DP) Indirect



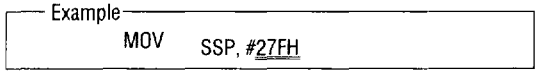
b) User Stack Pointer (USP) Indirect



c) Index Register (X1, X2) Indirect

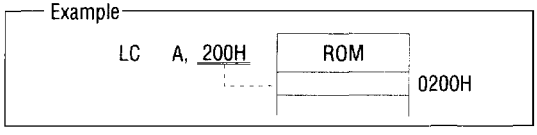


1.4 Immediate Addressing



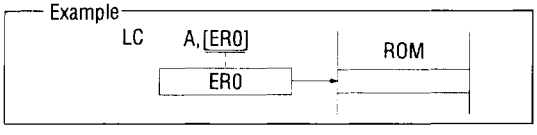
2. ROM Addressing (for program space)

2.1 Direct Addressing



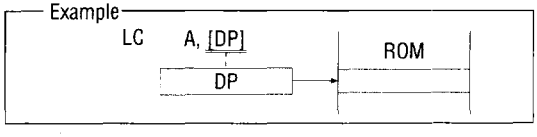
2.2 Simple Indirect Addressing

a) Local Register Indirect

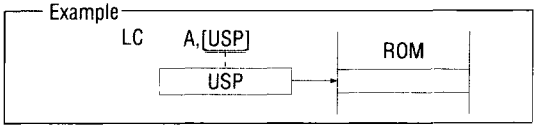


b) Pointing Register Indirect

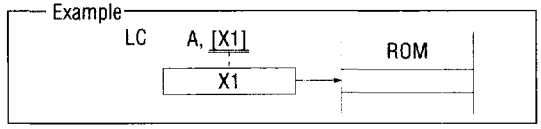
1) Data Pointer (DP) Indirect



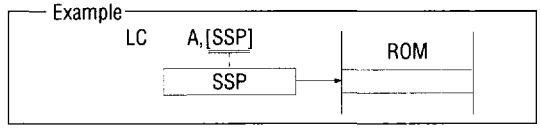
2) User Stack Pointer (USP) Indirect



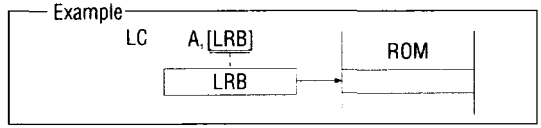
3) Index Register (X1, X2) Indirect



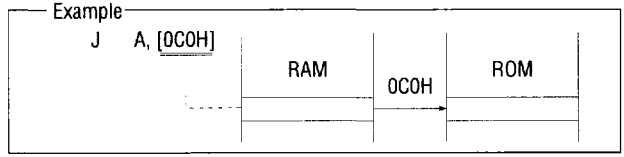
c) System Stack Pointer (SSP) Indirect



d) Local Register Base (LRB) Indirect

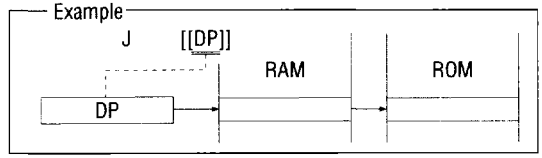


e) RAM Indirect

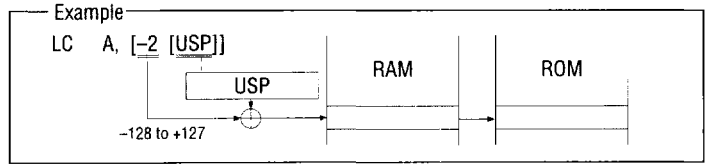


2.3 Double Indirect Addressing

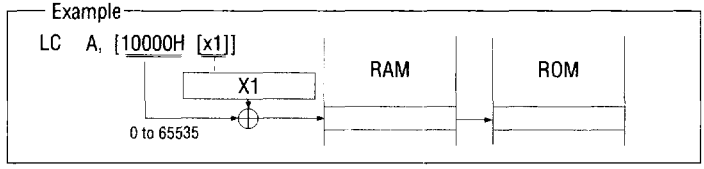
a) Data Pointer (DP) Double Indirect



b) User Stack Pointer (USP) Double Indirect



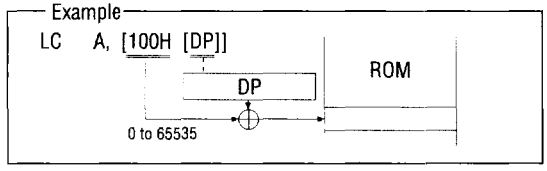
c) Index Register (X1, X2) Double Indirect



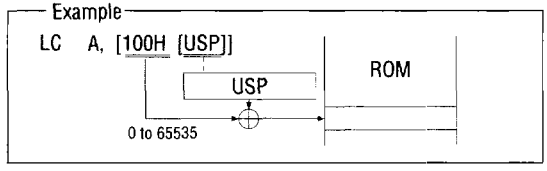
2.4 Indirect Addressing with 16-bit Offset

a) Pointing Register Indirect

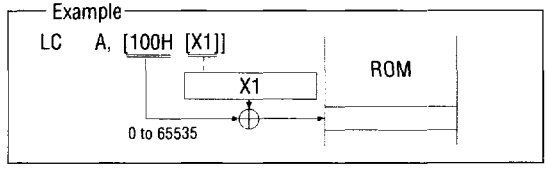
1) Data Pointer (DP) Indirect



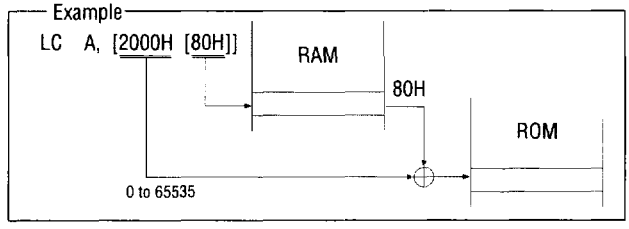
2) User Stack Pointer (USP) Indirect



3) Index Register (X1, X2) Indirect

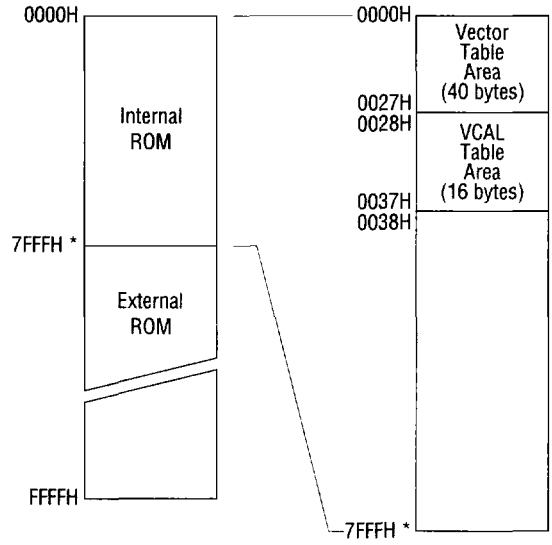


b) RAM Indirect



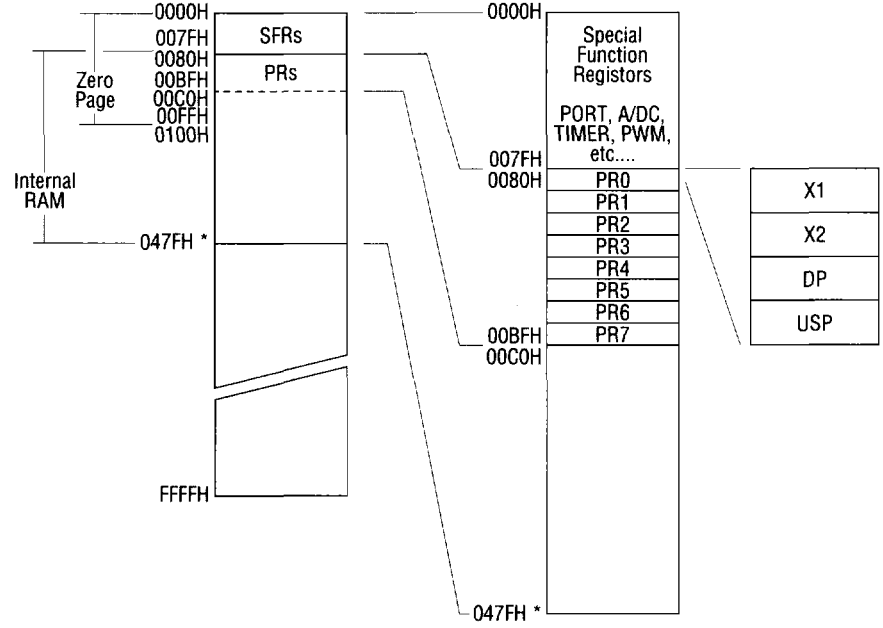
MEMORY MAPS

Program Memory Space



* MSM66201 : 3FFFH

Data Memory Space



* MSM66201 : 027FH

ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

Parameter	Symbol	Condition		Rating	Unit
Supply Voltage	V_{DD}	GND=AGND=0V		−0.3 to 7.0	V
Input Voltage	V_I			−0.3 to V_{DD}+0.3	V
Output Voltage	V_O			−0.3 to V_{DD}+0.3	V
Analog Ref. Voltage	V_R			−0.3 to V_{DD}+0.3	V
Analog Input Voltage	V_{AI}			−0.3 to V_R	V
Power Dissipation	P_D	Ta=85°C per Package	64-pin shrink DIP	930 MAX.	mW
			64-pin QFP	565 MAX.	
			68-pin QFJ	1120 MAX.	
Storage Temperature	T_{STG}	—		−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition		Range	Unit
Supply Voltage	V_{DD}	$f_{OSC} \leq$ 10MHz		4.5 to 5.5	V
Memory Hold Voltage	V_{DDH}	f_{OSC} = 0Hz		2.0 to 5.5	V
Operating Frequency	f_{OSC}	V_{DD} = 5V ±10%		0 to 10	MHz
Ambient Temperature	Ta	—		−40 to +85	°C
Fan Out	N	MOS load		20	—
		TTL load	P0	2	
			P1, P2, P3, P4	1	

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 5V ± 10%, Ta = −40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage 1, 3, 6	V_{IH}	—	2.4	—	V_{DD}+0.3	V
"H" Input Voltage 5, 7			4.0	—	V_{DD}+0.3	
"H" Input Voltage 8			4.2	—	V_{DD}+0.3	
"H" Input Voltage 2			3.6	—	V_{DD}+0.3	
"L" Input Voltage 1, 2, 3, 6	V_{IL}	—	−0.3	—	0.8	
"L" Input Voltage 5, 7			−0.3	—	0.8	
"L" Input Voltage 8			−0.3	—	0.4	
"H" Output Voltage 1, 4	V_{OH}	I_O = −400μA	4.2	—	—	
"H" Output Voltage 2		I_O = −200μA	4.2	—	—	
"L" Output Voltage 1, 4	V_{OL}	I_O = 3.2mA	—	—	0.4	
"L" Output Voltage 2		I_O = 1.6mA	—	—	0.4	
Input Leakage Current 3, 6, 7	I_{IH}/I_{IL}	V_I = V_{DD}/0V	—	—	1/−1	μA
Input Current 5			—	—	1/−20	
Input Current 8			—	—	10/−10	
"H" Output Current 1	I_{OH}	V_O = 2.4V	−2	—	—	mA
"H" Output Current 2			−1	—	—	
"L" Output Current 1	I_{OL}		10	—	—	
"L" Output Current 2			5	—	—	
Output Leakage Current 1, 2, 4	I_{LO}	V_O = V_{DD}/0V	—	—	±2	μA
Input Capacitance	C_I	f = 1MHz Ta = 25°C	—	5	—	pF
Output Capacitance	C_O		—	7	—	
Analog Reference Power Supply Current	I_{REF}	In A/D converter operation	—	0.3	2	mA
		In A/D converter halt	—	0.5	10	μA
Current Consumption (during STOP) *	I_{DDS}	V_{DD} = 2V	—	0.2	10	μA
		—	—	1	100	
Current Consumption (during HALT)	I_{DDH}	f_{OSC} = 10MHz No Load	—	6	10	mA
			**—	8	15	
Current Consumption	I_{DD}		—	20	35	
			**—	30	40	

Note: 1 Applied to P0
2 Applied to P1, P2, P3 and P4
3 Applied to P5
4 Applied to ALE, $\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$ and RESOUT
5 Applied to $\overline{RES}$ and $\overline{NMI}$
6 Applied to READY and $\overline{EA}$
7 Applied to $\overline{FLT}$
8 Applied to OSC_0
* V_{DD} or 0V for ports serving as the input pin. No load for any other.
** Applied to MSM66P201/66P207

AC Characteristics

• External program memory control

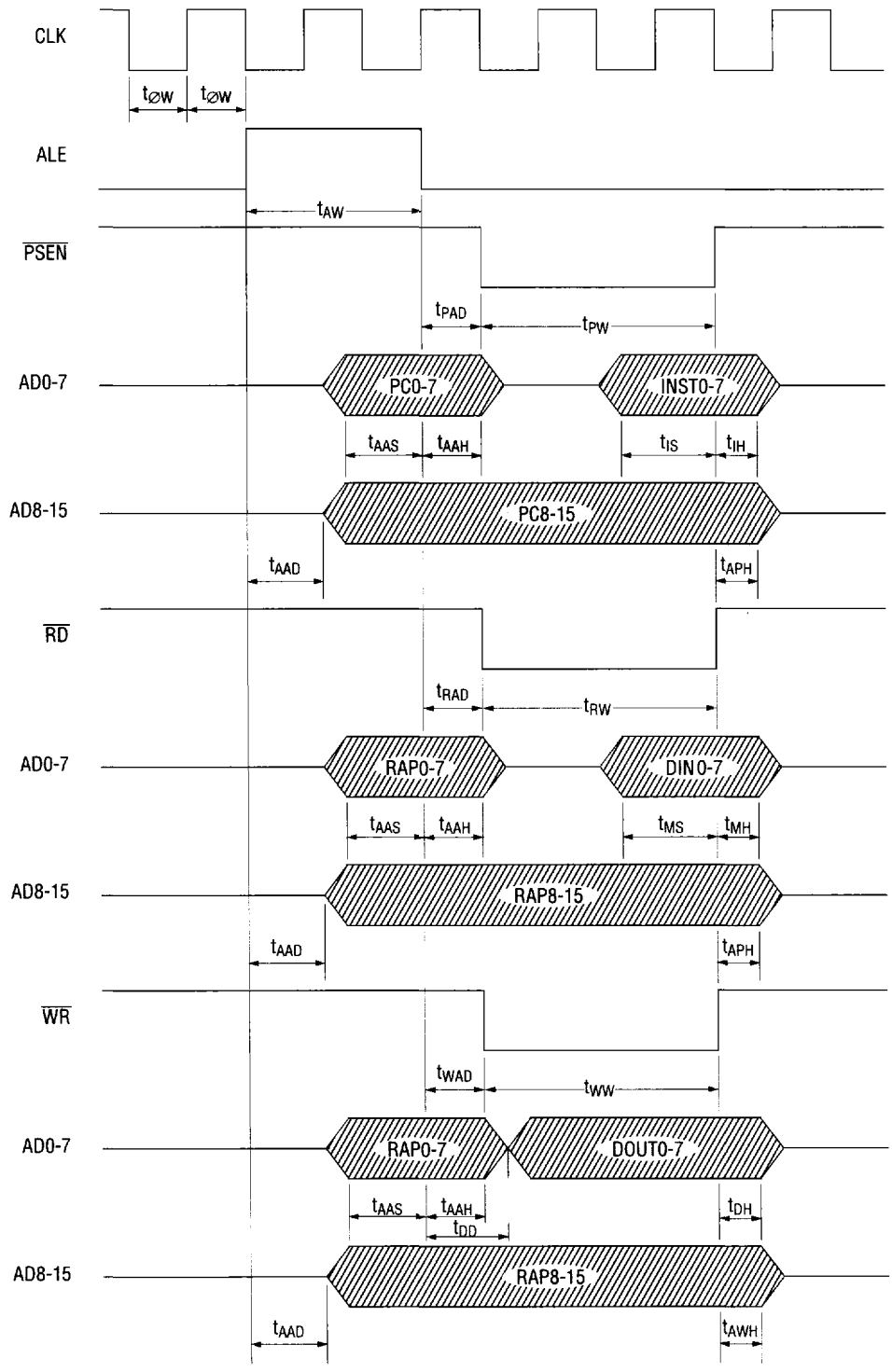
(V_{DD}=5V±10%, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock (OSC) Pulse	$t_{\phi W}$	—	50	—	ns
ALE Pulse Width	t_{AW}	C_L = 50pF	$3t_{\phi W}$–20	—	
$\overline{PSEN}$ Pulse Width	t_{PW}		$4t_{\phi W}$–20	—	
$\overline{PSEN}$ Pulse Delay Time	t_{PAD}		$t_{\phi W}$–20	$t_{\phi W}$+20	
Low Address Setup time	t_{AAS}		$2t_{\phi W}$–35	$2t_{\phi W}$+20	
Low Address Hold Time	t_{AAH}		$t_{\phi W}$–20	$t_{\phi W}$+40	
High Address Delay Time	t_{AAD}		$t_{\phi W}$–20	$t_{\phi W}$+40	
High Address Hold Time	t_{APH}		$t_{\phi W}$–20	$t_{\phi W}$+40	
Instruction Setup Time	t_{IS}		100	—	
Instruction Hold Time	t_{IH}		0	$t_{\phi W}$–20	

• External data memory control

(V_{DD}=5V±10%, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock (OSC) Pulse	$t_{\phi W}$	—	50	—	ns
ALE Pulse Width	t_{AW}	C_L = 50pF	$3t_{\phi W}$–20	—	
$\overline{RD}$ Pulse Width	t_{RW}		$4t_{\phi W}$–20	—	
$\overline{WR}$ Pulse Width	t_{WW}		$4t_{\phi W}$–20	—	
$\overline{RD}$ Pulse Delay Time	t_{RAD}		$t_{\phi W}$–20	$t_{\phi W}$+20	
$\overline{WR}$ Pulse Delay Time	t_{WAD}		$t_{\phi W}$–20	$t_{\phi W}$+20	
Low Address Setup Time	t_{AAS}		$2t_{\phi W}$–35	$2t_{\phi W}$+20	
Low Address Hold Time	t_{AAH}		$t_{\phi W}$–20	$t_{\phi W}$+40	
High Address Delay Time	t_{AAD}		$t_{\phi W}$–20	$t_{\phi W}$+40	
High Address Hold Time	t_{ARH}		$t_{\phi W}$–20	$t_{\phi W}$+40	
High Address Hold Time	t_{AWH}		$t_{\phi W}$–20	$t_{\phi W}$+40	
Memory Data Setup Time	t_{MS}		100	—	
Memory Data Hold Time	t_{MH}		0	$t_{\phi W}$–20	
Data Delay Time	t_{DD}		$t_{\phi W}$–20	$t_{\phi W}$+40	
Data Hold Time	t_{DH}		$t_{\phi W}$–20	$t_{\phi W}$+40	


CLK
tøw
tøw
ALE
tAW
PSEN
tPAD
tPW
AD0-7
PC0-7
INST0-7
tAAS
tAAH
tIS
tIH
AD8-15
PC8-15
tAAD
tAPH
RD
tRAD
tRW
AD0-7
RAP0-7
DIN0-7
tAAS
tAAH
tMS
tMH
AD8-15
RAP8-15
tAAD
tAPH
WR
tWAD
tWW
AD0-7
RAP0-7
DOUT0-7
tAAS
tAAH
tDD
tDH
AD8-15
RAP8-15
tAAD
tAWH

- **Serial port control**

Master mode

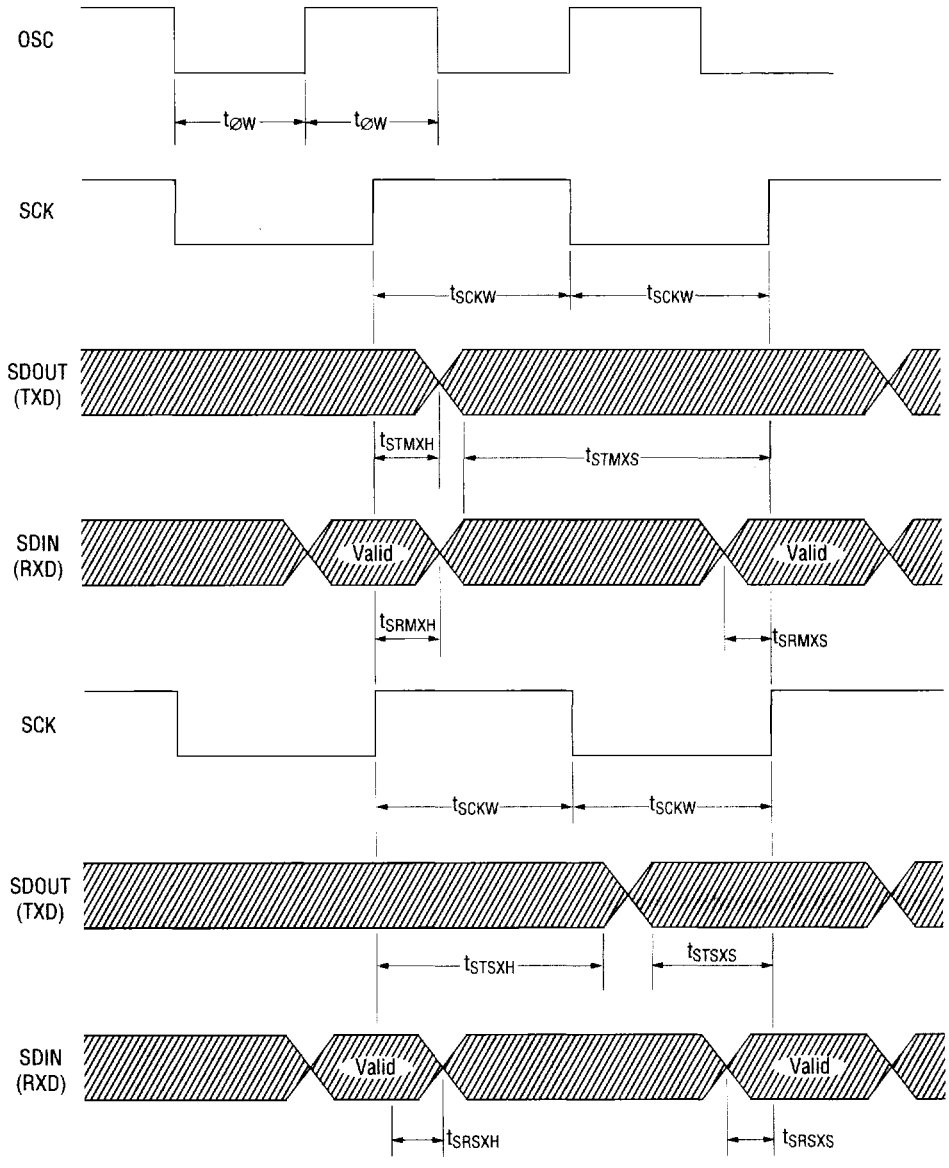
(V_{DD}=5V±10%, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock (OSC) Pulse Width	$t_{\phi W}$	—	50	—	ns
Serial Clock Pulse Width	t_{SCKW}	—	$8t_{\phi W}$	—	
Data Setup Time	t_{STMXS}	C_L=50pF	$8t_{\phi W}$+40	—	
Data Hold Time	t_{STMXH}		$6t_{\phi W}$–20	—	
Input Data Setup Time	t_{SRMXS}		$2t_{\phi W}$+10	—	
Input Data Hold Time	t_{SRMXH}		50	—	

Slave mode

(V_{DD}=5V±10%, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock (OSC) Pulse Width	$t_{\phi W}$	—	50	—	ns
Serial Clock Pulse Width	t_{SCKW}	—	$8t_{\phi W}$	—	
Data Setup Time	t_{STSXS}	C_L=50pF	$6t_{\phi W}$+40	—	
Data Hold Time	t_{STSXH}		$6t_{\phi W}$–20	—	
Input Data Setup Time	t_{SRSXS}		100	—	
Input Data Hold Time	t_{SRSXH}		100	—	


OSC
tøw
tøw
SCK
tSCKW
tSCKW
SDOUT
(TXD)
tSTMXH
tSTMXS
SDIN
(RXD)
Valid
Valid
tSRMXH
tSRMXS
SCK
tSCKW
tSCKW
SDOUT
(TXD)
tSTSXH
tSTSXS
SDIN
(RXD)
Valid
Valid
tSRSXH
tSRSXS

A/D CONVERTER CHARACTERISTICS

Operating Range

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	$f_{OSC} \leq 10MHz$	4.5	—	5.5	V
Analog Reference Voltage	V_R	V_{AG} = GND = 0V	4.5	—	V_{DD}	V
Analog Input Voltage	V_{AI}	V_{AG} = GND = 0V	V_{AG}	—	V_R	V
Analog Reference Power Voltage Resistance	R_R	V_{AG} = GND = 0V	—	16	—	kΩ
Operating Temperature	T_{OP}	V_{DD} = 5V ± 10%	–40	—	85	°C

A/D Converter Accuracy

- **Normal operation mode**

(V_{DD}=5V±10%, f_{OSC}=10MHz, Ta=–40 to 85°C)

Parameter	Symbol	Condition	Min.		Typ.		Max.		Unit
				*		*		*	
Resolution	n	See the recommended circuit V_R=V_{DD} V_{AG}=GND=0V Analog input source impedance ≤5kΩ One channel conversion time t_C=64μs	—	—	—	—	10	10	Bit
Absolute Error	E_A		—	—	—	—	$^{+3.0}_{-3.5}$	$^{+2.0}_{-3.5}$	LSB
Relative Error	E_R		—	—	—	—	±1.5	±1.0	LSB
Zero Point Error	E_Z		0	0	—	—	+3.0	+2.0	LSB
Full Scale Error	E_F		–0.5	–1.0	—	—	–3.5	–3.5	LSB
Differential Linearity Error	E_D		—	—	—	—	+3.0	+2.0	LSB
Crosstalk	E_C		—	—	±0.5	±0.5	—	—	LSB

* V_{DD}=5V, Ta=25°C

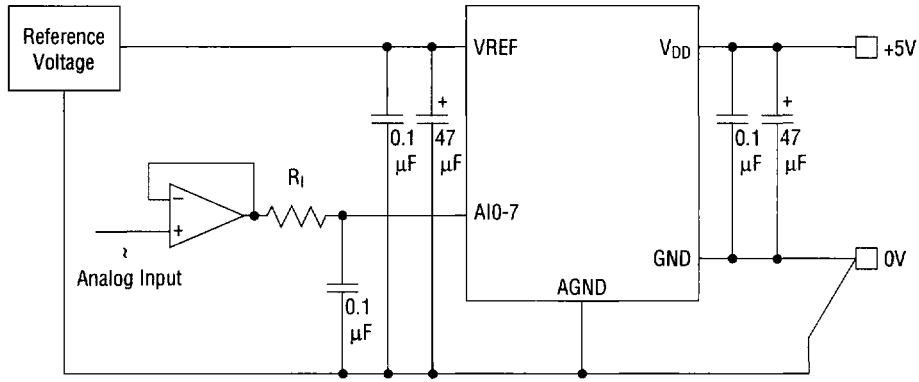
- **HALT/HOLD operation mode**

(V_{DD}=5V±10%, f_{OSC}=10MHz, Ta=–40 to 85°C)

Parameter	Symbol	Condition	Min.		Typ.		Max.		Unit
				*		*		*	
Resolution	n	See the recommended circuit V_R=V_{DD} V_{AG}=GND=0V Analog input source impedance ≤5kΩ One channel conversion time t_C=64μs	—	—	—	—	10	10	Bit
Absolute Error	E_A		—	—	—	—	$^{+2.0}_{-3.5}$	$^{+1.0}_{-2.0}$	LSB
Relative Error	E_R		—	—	—	—	±1.0	±0.5	LSB
Zero Point Error	E_Z		+0.5	+0.5	—	—	+2.0	+1.0	LSB
Full Scale Error	E_F		–1.0	–1.5	—	—	–3.5	–2.0	LSB
Differential Linearity Error	E_D		—	—	—	—	+2.0	+1.0	LSB
Crosstalk	E_C		—	—	±0.5	±0.5	—	—	LSB

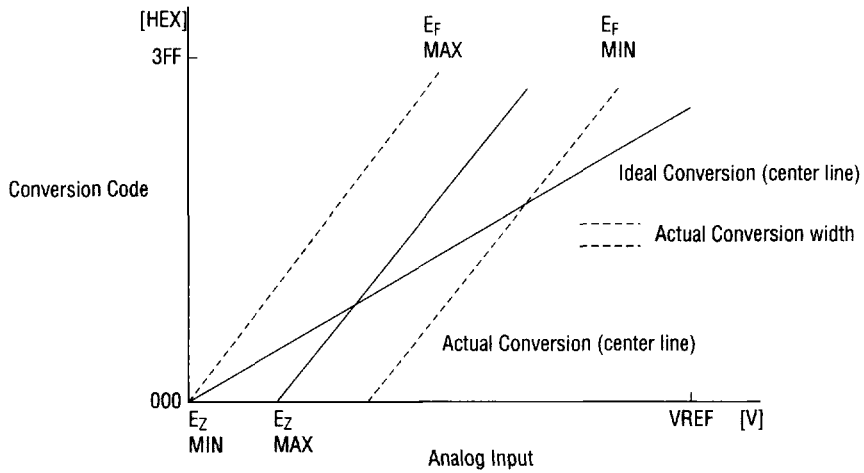
* V_{DD}=5V, Ta=25°C

Recommended Circuit



RI (Analog input source impedance) ≤ 5kΩ

A/D Converter Conversion Characteristics 1



Conversion Characteristics Diagram 1

Absolute error (Ea)

The absolute error indicates a difference between actual conversion and ideal conversion, excluding a quantizing error. The absolute error of the A/D converter gets larger as it approaches the zero point or full scale. (Refer to Conversion Characteristics Diagram 1.)

Relative error (Er)

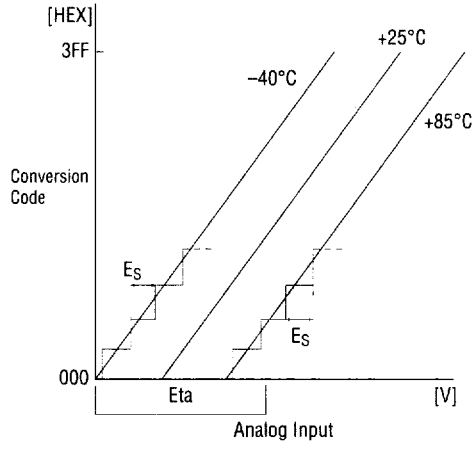
The relative error indicates a deviation from a line which connects the center point of the zero point conversion width with that of the full scale conversion width, excluding a quantizing error.

The relative error of this A/D converter is almost due to a differential linearity error.

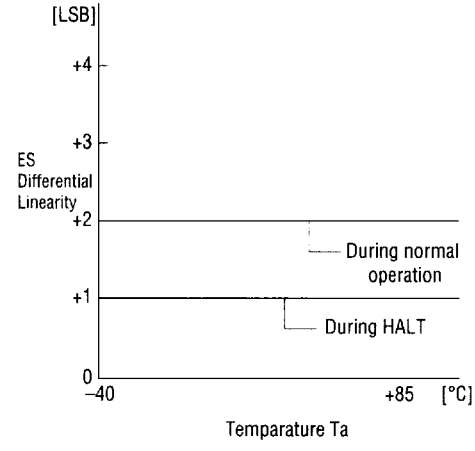
Zero point error (Ez) and full scale error (Ef)

The zero point error and full scale error indicate a difference between actual conversion and ideal conversion at the zero point and full scale, respectively. (Refer to Conversion Characteristics Diagram 1.)

A/D Converter Conversion Characteristics 2 (temperature characteristics)



Conversion Characteristics Diagram 2-1



Conversion Characteristics Diagram 2-2

Differential linearity error

The differential linearity error indicates a difference between the actual conversion width (actual step width) and ideal value (1LSB).

With this A/D converter, a voltage for actual conversion is shifted and the inclination of a voltage is changed, with changes of temperature (see Conversion Characteristics Diagram 2-1). Specifications described in the foregoing tables are established from Eta shown in Conversion Characteristics Diagram 2-1 (ED=Eta−1LSB). Conversion Characteristics Diagram 2-2 shows temperature characteristics of differential linearity of Es in Conversion Characteristics Diagram 2-1.