T-46-23-10

SHARP

NEW PRODUCT INFORMATION
PRELIMINARY

LH101504 High-Speed BiCMOS 256K (64K×4) ECL Static RAM
LH101510 High-Speed BiCMOS 1M (1M×1) ECL Static RAM

Description

The LH101504/LH101510 is a 256K/1M-bit high speed BiCMOS ECL static RAM organized as 64K×4 and 1M×1 respectively, fully compatible with ECL 101K I/O levels. It is fabricated using 0.8μm design rule and features advanced circuit technology that result in high speed access times.

Designed for high speed applications, it is applicable to the main memory of super computers and the cache memory of high performance work stations.

Features

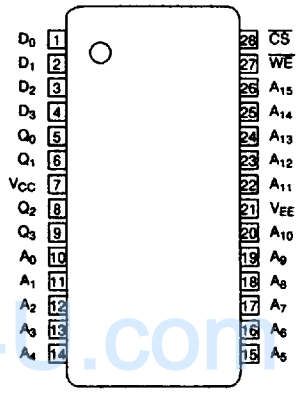
1. 0.8μm BiCMOS process
2. Memory organization
   65,536×4 bits (LH101504)
   1,048,576×1 bit (LH101510)
3. Access times:
   7/8/10ns MAX. (LH101504)
   8/10/12ns MAX. (LH101510)
4. Balanced read and write cycle times
5. Power consumption:
   1.6W MAX. f_O = 100MHz (LH101504)
   1.4W MAX. f_O = 100MHz (LH101510)
6. Fully 101K compatible ECL I/O
7. Power supply: −5.2V ± 10%
8. Package: 28-pin ceramic flat package

Pin Description

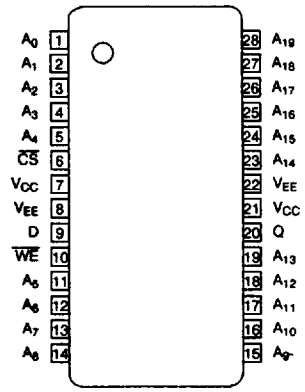
Signal		Pin name
LH101504	LH101510	
A_0-A_{15}	A_0-A_{19}	Address inputs
Q_0-Q_3	Q	Data output
D_0-D_3	D	Data input
$\overline{CS}$		Chip select
$\overline{WE}$		Write enable
V_{EE}		Power supply
V_{CC}		Ground

Pin Connections

LH101504



LH101510



Top View

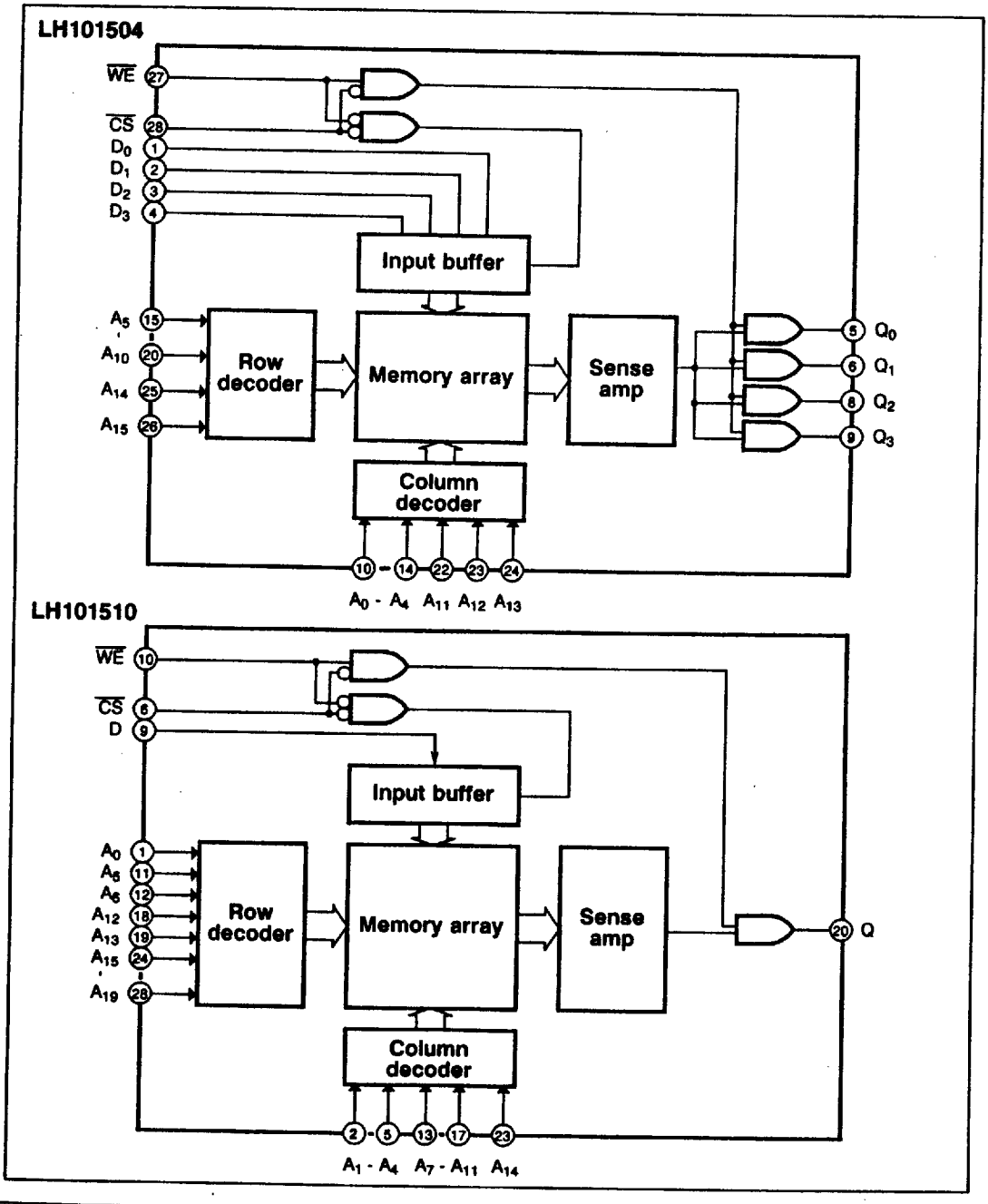
Truth Table

$\overline{CS}$	$\overline{WE}$	D	Q	Mode
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	Q	Read

I·C

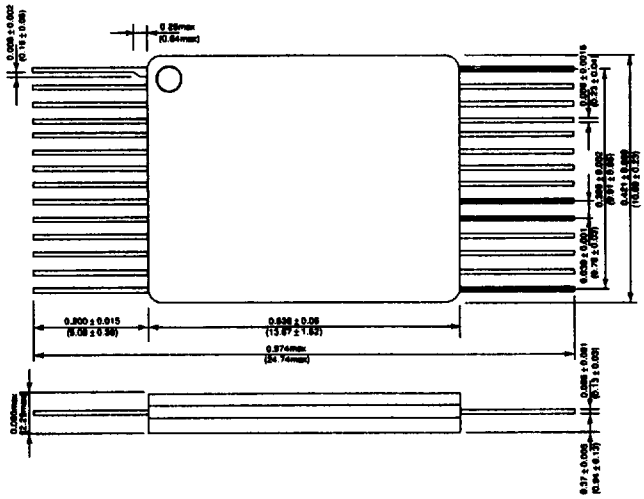
LH101504 High-Speed BiCMOS 256K (64K×4) ECL Static RAM
LH101510 High-Speed BiCMOS 1M (1M×1) ECL Static RAM

Block Diagrams

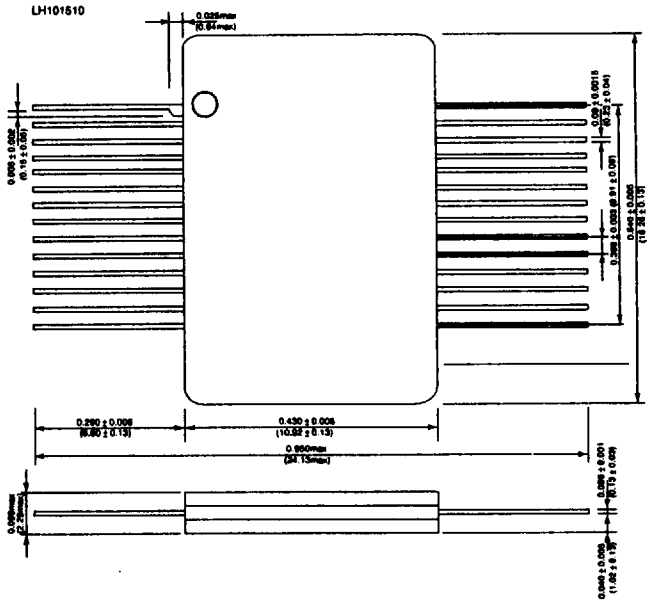


■ **Package Dimensions (28-pin ceramic flat package)**

LH101504



LH101510



Dimensions in inches (mm)

LH101504 High-Speed BiCMOS 256K (64K×4) ECL Static RAM
LH101510 High-Speed BiCMOS 1M (1M×1) ECL Static RAM

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
VEE pin potential to ground	V_{EE}	−7.0 to +0.0	V
Input voltage (DC)	V_{IN}	V_{EE} to +0.0	V
Output current (DC output HIGH)	I_{OH}	−50	mA
Operating temperature	Topr	0 to +85	°C
Storage temperature	Tstg	−55 to +150	°C
Maximum junction temperature	Tj	+150	°C

DC Characteristics

(T_C = 0 to +85°C, V_{CC} = Ground, V_{EE} = −5.2V ± 10%)

Parameter	Symbol	Test Condition		MIN.	MAX.	Unit
Output HIGH voltage	V_{OH}	$V_{IN} = V_{IH}$ (MAX.) or V_{IL} (MIN.) Loading with 50 ohms to −2.0V		−1025	−880	mV
Output LOW voltage	V_{OL}			−1810	−1620	mV
Input HIGH voltage	V_{IH}			−1165	−880	mV
Input LOW voltage	V_{IL}			−1810	−1475	mV
Output HIGH voltage	V_{OHC}	$V_{IN} = V_{IH}$ (MIN.) or V_{IL} (MAX.) Loading with 50 ohms to −2.0V		−1025		mV
Output LOW voltage	V_{OLC}				−1620	mV
Input HIGH current	I_{IH}	$V_{IN} = V_{IH}$(MAX.)			220	μA
Input LOW current	I_{IL}	$V_{IN} = V_{IL}$(MAX.)		−50	170	μA
Power supply current	I_{EE}	f_O = 100MHz	LH101504	−270		mA
			LH101510	−240		

Note: T_C = Case Temperature

Capacitance (Note 1)

Parameter	Symbol	LH101504		LH101510		Unit
		MIN.	MAX.	MIN.	MAX.	
Input capacitance	C_{IN}		5.0		7.0	pF
Output capacitance	C_{OUT}		8.0		8.0	pF

Note 1: Sample tested only

Switching Characteristics Read Cycle

V_{EE} = −5.2V ± 10%, V_{CC} = Ground, Tc = 0°C to +85°C

Parameter	Symbol	LH101504N-07		LH101510N-08		LH101510N-10		Unit
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Address valid to address invalid	T_{AVAX}	7		8		10		ns
Address valid to output valid	T_{AVQV}		7		8		10	ns
Address invalid to output invalid	T_{AXQX}	4	7	5	7	5	8	ns
Chip select LOW to chip select HIGH	T_{ELEH}	4		5		6		ns
Chip select LOW to output valid	T_{ELQV}		4		4		4	ns
Chip select HIGH to output LOW	T_{EHQL}		4		4		4	ns
Write cycle 1								
Address valid to address invalid	T_{AVAX}	7		8		10		ns
Write enable LOW to chip select HIGH	T_{WLEH}	4		5		6		ns
Write HIGH to address don't care	T_{WHAX}	0		0		0		ns
Write LOW to write HIGH (Setup & holds)	T_{WLWH}	4		5		6		ns
Address valid to write LOW	T_{AVWL}	0		0		0		ns
Data valid to write HIGH	T_{DVWH}	4		5		6		ns
Write HIGH to data don't care	T_{WHDX}	0		0		0		ns
Write LOW to output LOW	T_{WLQL}		4		4		4	ns
Write HIGH to output valid	T_{WHQV}		7		8		10	ns
Write cycle 2								
Address valid to chip select LOW	T_{AVEL}	0		0		0		ns
Chip select LOW to chip select HIGH	T_{ELEH}	4		5		6		ns
Chip select HIGH to address don't care	T_{EHAX}	0		0		0		ns
Chip select LOW to write enable HIGH	T_{ELWH}	4		5		6		ns
Data valid to chip select HIGH	T_{DVEH}	4		5		6		ns
Chip select HIGH to data don't care	T_{EHDX}	0		0		0		ns
Consecutive write cycle								
Write enable HIGH to write enable LOW	T_{WHWL}	4		4		4		ns
Chip select HIGH to chip select LOW	T_{EHEL}	4		4		4		ns

Note: Tc = Case Temperature

AC Test Conditions

Input rise and fall times	1.5ns
Output reference levels	−1.33V
Input reference levels	−1.33V
AC test circuit	Figure 2

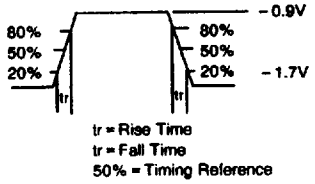


Figure 1

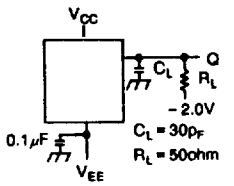
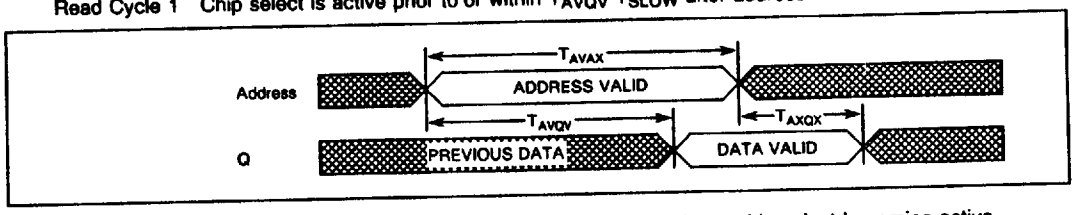


Figure 2 AC Test Circuit

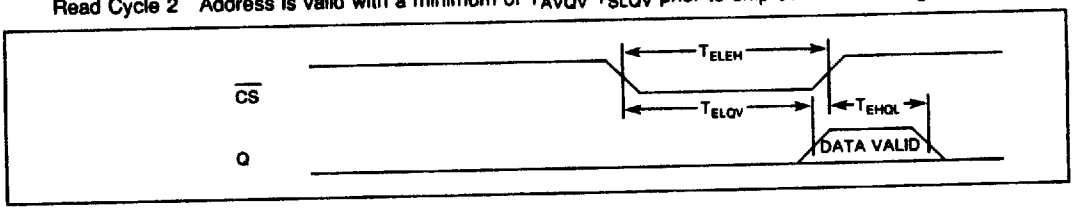
LH101504 High-Speed BiCMOS 256K (64K×4) ECL Static RAM
LH101510 High-Speed BiCMOS 1M (1M×1) ECL Static RAM

Timming Diagram

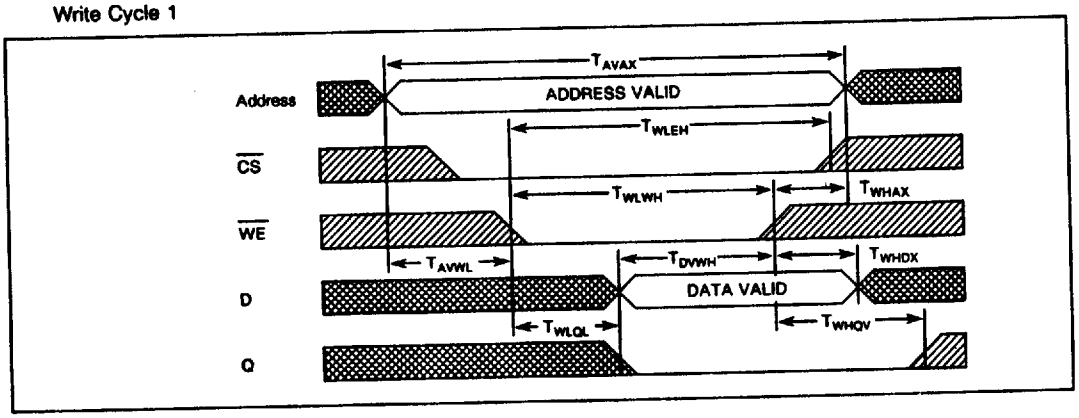
Read Cycle 1 Chip select is active prior to or within T_{AVQV}-T_{SLOW} after address valid.



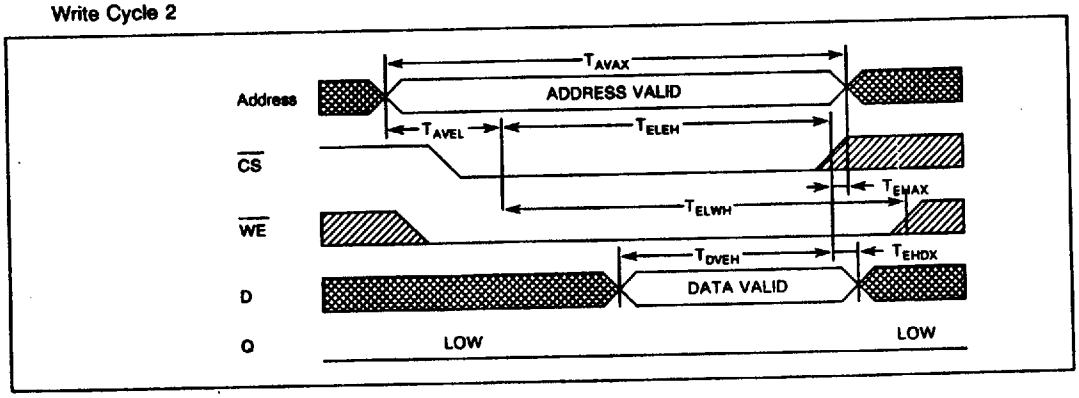
Read Cycle 2 Address is valid with a minimum of T_{AVQV}-T_{SLQV} prior to chip select becoming active.



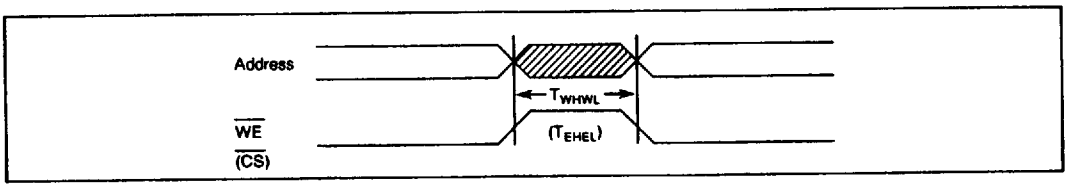
Write Cycle 1



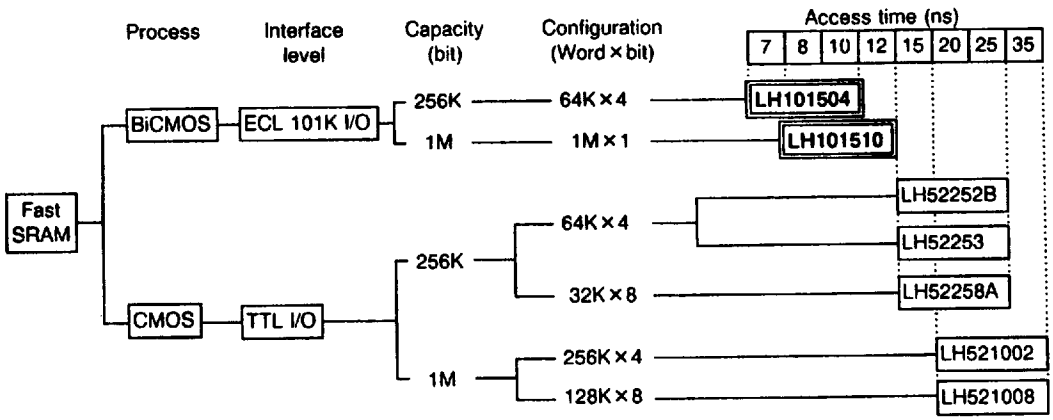
Write Cycle 2



Consecutive Write Cycle (Minimum write (select) pulse disable)



Sharp's Product Lineup (Fast SRAM)



LH101504 High-Speed BiCMOS 256K (64K×4) ECL Static RAM
LH101510 High-Speed BiCMOS 1M (1M×1) ECL Static RAM

NEW PRODUCT INFORMATION
PRELIMINARY

Ordering Information

LH101504 X - XX

- Access times
  - 08: 8ns
  - 10: 10ns
  - 12: 12ns
- Package
  - N: 28-pin ceramic flat package
- Model No.
  - 256K (64K×4) bit ECL I/O static RAM

LH101510 X - XX

- Access times
  - 07: 7ns
  - 08: 8ns
  - 10: 10ns
- Package
  - N: 28-pin ceramic flat package
- Model No.
  - 1M (1M×1) bit ECL I/O static RAM

Development Schedule

	(LH101504)	(LH101510)
Sample	May, '92	July, '92
Mass Production Start	August, '92	October, '92

The information described herein is intended to introduce descriptions for products that are in development, and specifications and circuitry are subject to change upon final characterization.

SHARP

SHARP CORPORATION Japan
IC SALES DEPARTMENT
INTERNATIONAL SALES & MARKETING GROUP
-IC/ELECTRONIC COMPONENTS
2613-1 ICHINOMOTO-CHO TENRI-CITY NARA 632, JAPAN
PHONE: (07436) 5-1321
TELEX: LABOMETA-B J63428
FACSIMILE: (07436) 5-1532

NORTH AMERICA: SHARP ELECTRONICS CORPORATION
Microelectronics Group
5700 Northwest Pacific Rim Boulevard Suite 20
Camas, Washington 98607, U.S.A.
PHONE: (206) 834-2500
TELEX: 49608472 (SHARPCAM)
FACSIMILE: (206) 834-8903

EUROPE: SHARP ELECTRONICS (EUROPE) GmbH
Microelectronics Division
Sonninstraße 3, 2000 Hamburg 1, F.R. Germany
PHONE: (040) 2376-2286
TELEX: 2161867 (HEEG D)
FACSIMILE: (040) 2378-2232

HONG KONG: SHARP-ROXY (HONG KONG) LTD.
3rd Business Division
Room 1701-1710, Admiralty Centre, Tower 1,
18 Harcourt Road, Hong Kong
PHONE: 8229311/8229348
TELEX: 74256 SRHL HX
FACSIMILE: 5297561/8660779

SINGAPORE: SHARP-ROXY SALES (SINGAPORE) PTE. LTD.
100G Pasir Panjang Road, Singapore 0511
PHONE: 4731911
TELEX: 55504 (SRSSIN RS)
FACSIMILE: 4794105

KOREA: SHARP ELECTRONICS INDUSTRIAL CORPORATION
4F Dae San Bldg 14-27 Yeoyido-dong,
Young Deung Po-ku, Seoul, Korea
PHONE: 782-8637 ~ 40
TELEX: SHARPEI K26754
FACSIMILE: (02) 782-5070

Distributed by:

Ref. No. NP098C