Features

- Generates an EMI optimized clocking signal at output.
- Input frequency – 25 MHz.
- Frequency outputs:
  - 60 MHz (unmodulated)
  - 2 x 48 MHz (unmodulated)
  - 66.6 MHz (modulated) -1.7% down spread
- Modulation rate: 30 KHz.
- Supply voltage range 3.3V (± 0.3V).
- Available in 8-pin SOIC package.
- Commercial and Industrial Temperature range.

Product Description

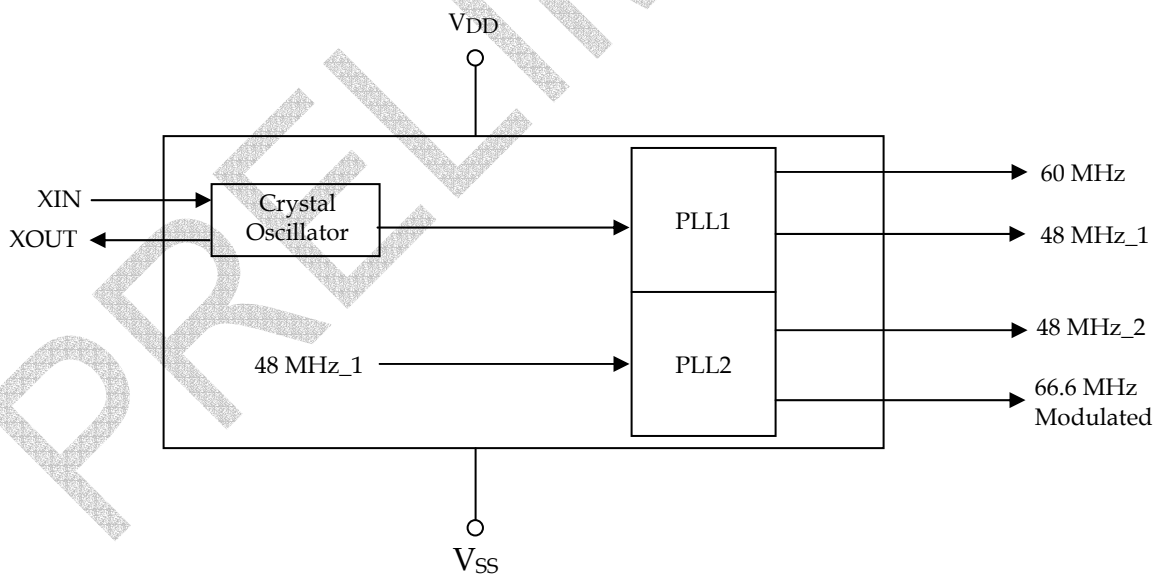
The ASM3P2111A is a versatile spread spectrum frequency modulator. The ASM3P2111A reduces electromagnetic interference (EMI) at the clock source.

The ASM3P2111A allows significant system cost savings by reducing the number of circuit board layers and shielding that are required to pass EMI regulations. The ASM3P2111A modulates the output of PLL in order to spread the bandwidth of a synthesized clock, thereby decreasing the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most clock generators. Lowering EMI by increasing a signal's bandwidth is called spread spectrum clock generation.

Applications

ASM3P2111A is targeted towards EMI management for high speed digital applications such as PC peripheral devices, consumer electronics and embedded controller systems.

Block Diagram



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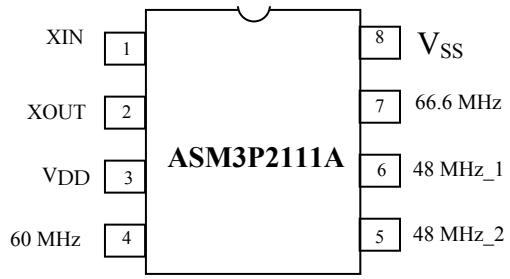
Pin Configuration



Pin Description

Pin Name	Type	Description
XIN	I	Connection to crystal
XOUT	O	Connection to crystal
V_{DD}	P	Power supply for the analog and digital blocks
60 MHz	O	Clock output-1 60 MHz unmodulated
48 MHz_2	O	Clock output-2 48 MHz_2 unmodulated
48 MHz_1	I/O	Clock output-3 48 MHz_1 unmodulated
66.6 MHz	I	Clock output-4 66.6 MHz modulated
V_{SS}	P	Ground to entire chip

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Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}	Supply voltage, DC	(V_{SS} – 0.5) to 7	V
V_I	Input voltage, DC	(V_{SS}-0.5) to (V_{DD}+0.5)	V
V_O	Output voltage, DC	(V_{SS}-0.5) to (V_{DD} + 0.5)	V
I_{IK}	Input clamp current (V_I<0 or V_I>V_{DD})	-50 to +50	mA
I_{OK}	Output clamp current (V_I<0 or V_I>V_{DD})	-50 to +50	mA
T_S	Storage temperature	-65 to +125	°C
T_A	Ambient temperature range, under bias	-55 to 125	°C
T_J	Junction temperature	150	°C
	Lead temperature (soldering 10 sec)	260	°C
	Input static discharge voltage protection (MIL –STD 883E, Method 3015.7)	2	kV
Note: These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.			

Operating Conditions

Parameter	Symbol	Condition / Description	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.3V ± 10%	3	3.3	3.6	V
Ambient Operating Temperature Range	T_A		-10		+70	°C
Crystal Resonator Frequency	F_{XIN}			25		MHz
Output Driver Load Capacitance	C_L				15	pF

Crystal Specifications

Fundamental AT cut parallel resonant crystal	
Nominal frequency	25 MHz
Frequency tolerance	± 50 ppm or better at 25°C
Operating temperature range	-25°C to +85°C
Storage temperature	-40°C to +85°C
Load capacitance	18pF
Shunt capacitance	7pF maximum
ESR	25 Ω

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DC Electrical Characteristics

Parameter	Symbol	Conditions / Description	Min	Typ	Max	Unit
						Overall
Supply Current, Dynamic	I_{DD}	V_{DD}=3.3V, F_{CLK}=25MHz, C_L=15pF		43		mA
Supply Current, Static	I_{DDL}	V_{DD} = 3.3V, Software Power Down		TBD		mA
						All input pins
High-Level Input Voltage	V_{IH}	V_{DD}=3.3V	2.0		V_{DD}+0.3	V
Low-Level Input Voltage	V_{IL}	V_{DD}=3.3V	V_{SS}-0.3		0.8	V
High-Level Input Current	I_{IH}		-1		1	μA
Low-Level Input Current (pull-up)	I_{IL}		-20	-36	-80	μA
High-Level Output Source Current	I_{xOH}	V_{DD}=V(XIN) = 3.3V, V_O=0V	10	21	30	mA
Low-Level Output Source Current	I_{xOL}	V_{DD}=3.3V, V(XIN)=V_O=5.5V	-10	-21	-30	mA
						Clock Outputs
High-Level Output Source Current	I_{OH}	V_O=2.4V		-20		mA
Low-Level Output Sink Current	I_{OL}	V_O=0.4V		23		mA
Output Impedance	Z_{OH}	V_O=0.5V_{DD}; output driving high		29		Ω
	Z_{OL}	Vo=0.5V_{DD}; output driving low		27		

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AC Electrical Characteristics

Parameter	Symbol	Conditions/ Description	Min	Typ	Max	Unit
Rise Time	t_r	V_O = 0.3V to 3.0V; C_L = 15pF		2.1		ns
Fall Time	t_f	V_O = 3.0V to 0.3V; C_L = 15pF		1.9		ns
Clock Duty Cycle		Ratio of pulse width (as measured from rising edge to next falling edge at 2.5V) to one clock period	45		55	%
Jitter, Long Term	$Tj_{(LT)}$	On rising edges 500 µs apart at 2.5 V relative to an ideal clock, PLL B inactive *		45		ps
		On rising edges 500 µs apart at 2.5 V relative to an ideal clock, PLL B active *		165		
Jitter, peak to peak	$Tj_{(\Delta T)}$	From rising edge to next rising edge at 2.5 V, PLL B inactive *		110		ps
		From rising edge to next rising edge at 2.5 V, PLL B active *		390		
* CL = 15 pF, Input clock frequency = 12.75 MHz, Output frequency = 51 MHz						

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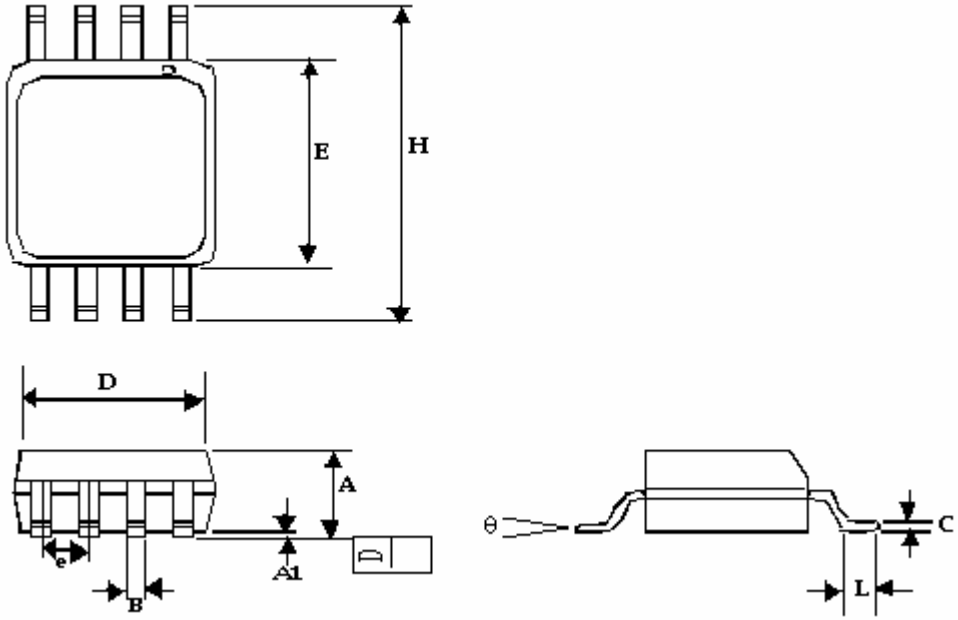
Package Information

8-Pin SOIC package



Symbol	Dimensions in inches		Dimensions in millimeters	
	Min	Max	Min	Max
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.013	0.022	0.33	0.53
C	0.007	0.012	0.18	0.27
D	0.188	0.197	4.78	5.00
E	0.150	0.158	3.80	4.01
H	0.228	0.244	5.80	6.20
e	0.050 BSC		1.27 BSC	
L	0.016	0.035	0.40	0.89
θ	0°	8°	0°	8°

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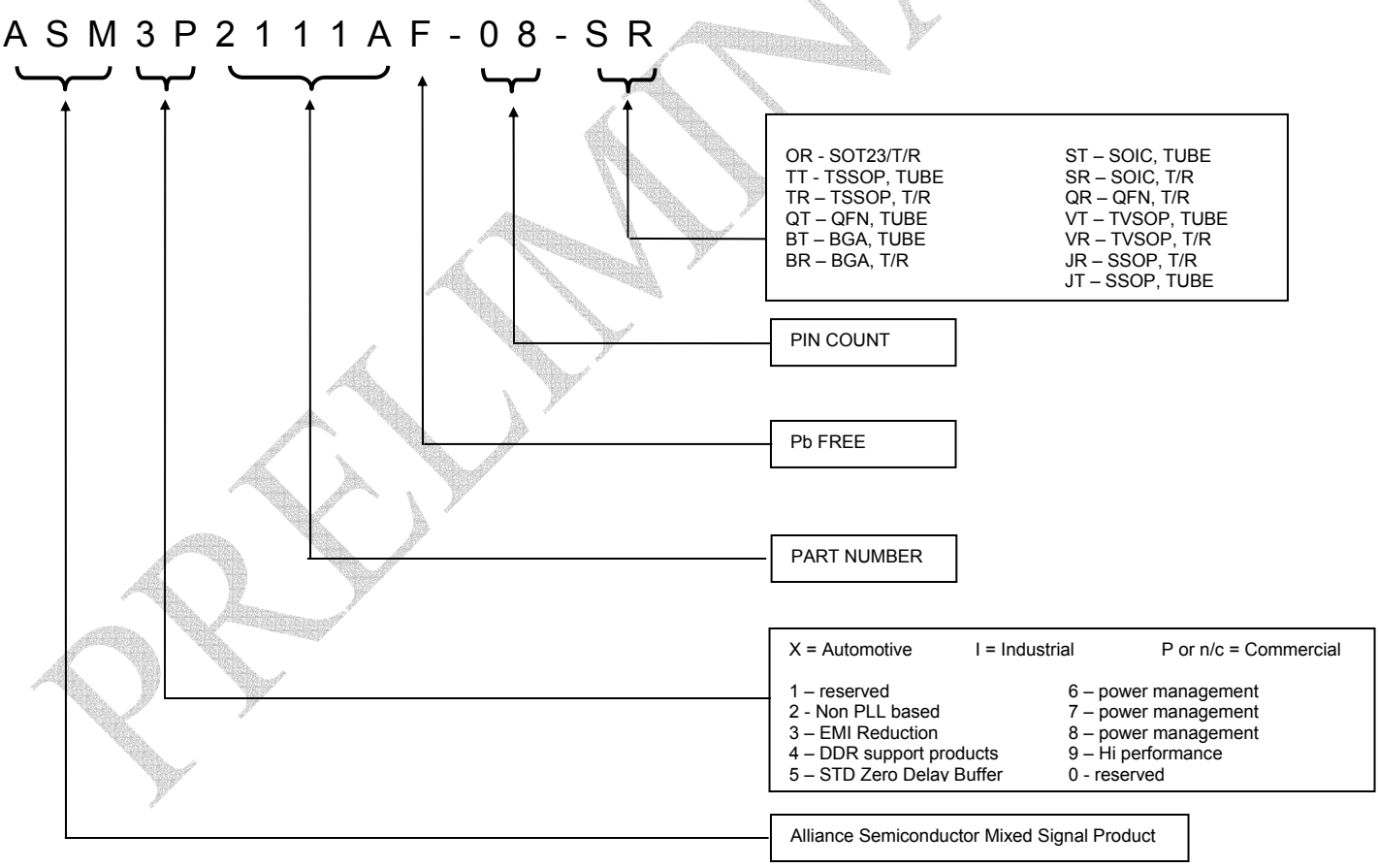
Ordering Codes

Part number	Package Configuration	Temperature Range
ASM3P2111AF-08-ST	08-pin SOIC TUBE	Commercial
ASM3P2111AF-08-SR	08-pin SOIC TAPE & REEL	Commercial
ASM3I2111AF-08-ST	08-pin SOIC TUBE	Industrial
ASM3I2111AF-08-SR	08-pin SOIC TAPE & REEL	Industrial

Ordering Information



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Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.

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Preliminary Information
Part Number: ASM3P2111A
Document Version: v1.1

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to Dan Hariton / Alliance Semiconductor, dated 11-11-2003

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