# 32 K × 8 / 3.3 Volts Very Low Power CMOS SRAM



## Introduction

The L65656 is a very low power CMOS static RAM organized as 32 768 × 8 bits. It is manufactured using the TEMIC high performance SCMOS technology.

The L65656 provides fast access time of 70 ns for a 3 volts power supply.

Utilizing an array of six transistors (6T) memory cells, the L65656 combines an extremely low standby supply current (Typical value = 0.1 µA) with a fast access time at 70 ns in commercial temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

Extra protection against heavy ions is given by the use of an epitaxial layer of a P substrate.

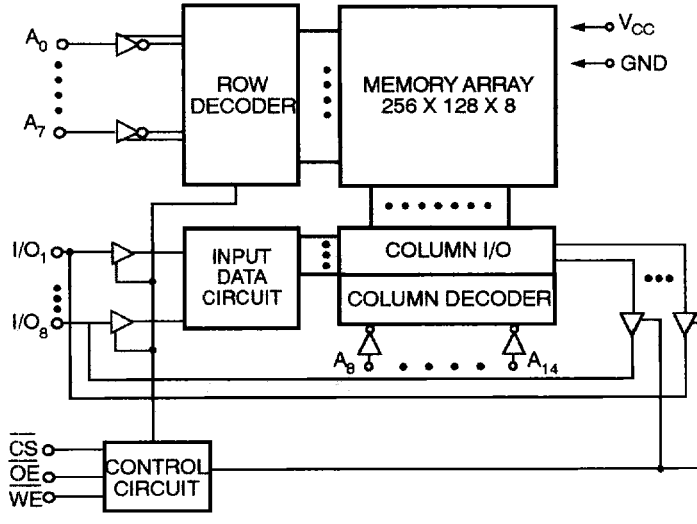
The L65656 is processed following the test methods of MIL STD 883C and/or ESA/SCC 9000, making it ideally suitable for military/space applications that demand superior levels of performance and reliability.

## Features

- Single supply 3.3 ± 0.3 volts
- Access time
  Commercial : 70/80/100 ns (max)
  Military/industrial : 80/100 ns (max)
- Very low power consumption
  Active : 200 mW (typ)
  Standby : 0.3 µW (typ)
  Data retention : 0.2 µW (typ)
- Wide temperature range : – 55 to + 125 °C
- Asynchronous
- Equal cycle and access time
- Gated inputs : no pull-up/dow resistors are required

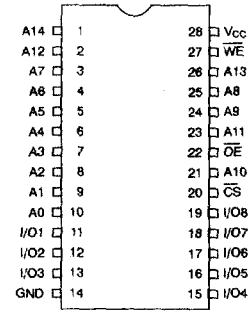
## Interface

### Block Diagram



## Pin Configuration

**Pinout DIL/SO/FP 28 pins (top view)**




## Pin Description

| | | | | | |
|---|---|---|---|---|---|
| A0-A14 | : | Address inputs | $\overline{CS}$ (bar) : | Chip-Select |
| I/O0-I/O7 | : | Input/Output | $\overline{W}$ (bar) : | Write Enable |
| Vcc | : | Power | $\overline{OE}$ (bar) : | Output Enable |
| Gnd | : | Ground | | |

## Truth Table

| $\overline{CS}$ (bar) | $\overline{W}$ (bar) | $\overline{OE}$ (bar) | MEMORY OPERATION | MODE |
|---|---|---|---|---|
| H | X | X | Z | Deselect/ POWER-DOWN |
| L | H | L | DATA OUT | Read |
| L | L | X | DATA IN | Write |
| L | H | H | Z | Output disable |

L = low, H = high, X = H or L, Z = high impedance.

# Electrical Characteristics

## Absolute Maximum Ratings

Supply voltage to GND potential : ..... –0.5 V to + 7.0 V
Input or Output voltage applied : ..... (Gnd – 0.3 V) to (Vcc + 0.3 V)
Storage temperature : ..... –65 °C to + 150 °C

## Operating Range

| | SUPPLY VOLTAGE | OPERATING TEMPERATURE |
|---|---|---|
| Military | 3.3 V ± 0.3 V | – 55 °C to + 125 °C |
| Industrial | 3.3 V ± 0.3 V | – 40 °C to + 85 °C |
| Commercial | 3.3 V ± 0.3 V | 0 °C to + 70 °C |

## DC Operating Conditions

| PARAMETER | DESCRIPTION | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| Vcc | Supply voltage | 3 | 3.3 | 3.6 | V |
| Gnd | Ground | 0.0 | 0.0 | 0.0 | V |
| VIL (1) | Input low voltage | – 0.3 | 0.0 | 0.6 | V |
| VIH | Input high voltage | 1.8 | – | Vcc + 0.3 V | V |

**Note :** 1. VIL min = –0.3 V or –1.0 V pulse width 50 ns.

## Capacitance

| PARAMETER | DESCRIPTION | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| Cin (2) | Input capacitance | – | – | 8 | pF |
| Cout (2) | Output capacitance | – | – | 8 | pF |

**Note :** 2. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not tested.

## DC Parameter

| PARAMETER | DESCRIPTION | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| IIX (3) | Input leakage current | – 1.0 | – | 1 | µA |
| IOZ (3) | Output leakage current | – 1.0 | – | 1.0 | µA |
| VOL (4) | Output low voltage | – | – | 0.4 | V |
| VOH (4) | Output high voltage | 2 | – | – | V |

**Notes :** 3. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
4. Vcc min, IOL = 6 mA, IOH = –1.0 mA.

## Consumption for Commercial Specification

| SYMBOL | PARAMETER | L 65656 V–70 | L 65656 L–70 | L 65656 V–85 | L 65656 L–85 | L 65656 V–100 | L 65656 L–100 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|---|---|
| ICCSB (5) | Standby supply current | 1 | 5 | 1 | 5 | 1 | 5 | mA | max |
| ICCSB1 (6) | Standby supply current | 4 | 70 | 4 | 70 | 4 | 70 | µA | max |
| ICCOP (7) | Operating supply current | 100 | 120 | 95 | 115 | 90 | 110 | mA | max |

## Consumption for Industrial Specification

| SYMBOL | PARAMETER | L 65656 V–80 | L 65656 L–80 | L 65656 V–85 | L 65656 L–85 | L 65656 V–100 | L 65656 L–100 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|---|---|
| ICCSB (5) | Standby supply current | 5 | 10 | 5 | 10 | 5 | 10 | mA | max |
| ICCSB1 (6) | Standby supply current | 9 | 90 | 9 | 90 | 9 | 90 | µA | max |
| ICCOP (7) | Operating supply current | 95 | 115 | 95 | 115 | 90 | 110 | mA | max |

## Consumption for Military Specification

| SYMBOL | PARAMETER | L 65656 V–80 | L 65656 L–80 | L 65656 V–100 | L 65656 L–100 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|
| ICCSB (5) | Standby supply current | 5 | 10 | 5 | 10 | mA | max |
| ICCSB1 (6) | Standby supply current | 90 | 400 | 90 | 400 | µA | max |
| ICCOP (7) | Operating supply current | 95 | 115 | 90 | 110 | mA | max |

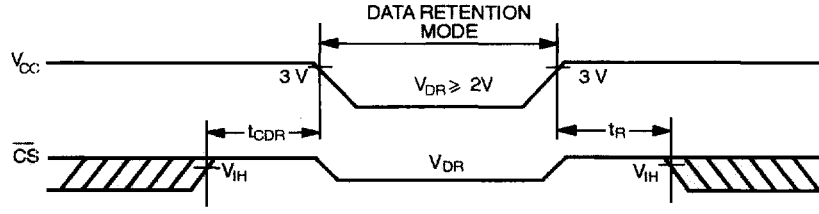
**Notes :** 5. $\overline{CS} \geq VIH$, Vin ≥ VIH or Vin ≤ VIL.
6. $\overline{CS} \geq$ Vcc – 0.3 V, Iout = 0 mA. Vin ≥ Vcc – 0.3 V or Vin ≤ 0.3 V.
7. Vcc max, Iout = 0 mA, f = max, Vin = Gnd/Vcc. Duty cycle 100 %.
For Low frequency application consult us for power consumption.

## Data Retention Mode

MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ($\overline{CS}$) must be held high during data retention ; within Vcc to Vcc – 0.2 V.
2. Output Enable ($\overline{OE}$) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. $\overline{CS}$ and $\overline{OE}$ must be kept between Vcc + 0.3 V and 70 % of Vcc during the power up and power down transitions.
4. The RAM can begin operation > 80 ns after Vcc reaches the minimum operating voltage (3 V).

## Timing




## Data Retention Characteristics

| PARAMETER | DESCRIPTION | MINIMUM | TYPICAL (8) | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| VCCDR | Vcc for data retention | 2.0 | – | – | V |
| TCDR | Chip deselect to data retention time | 0.0 | – | – | ns |
| TR | Operation recovery time | TAVAV (9) | – | – | ns |
| ICCDR1 (10) | Data retention current | | | | |
| | @ 2.0 V : CL-65656V-70/80/100 | – | 0.1 | 3 | µA |
| | CL-65656L-70/80/100 | – | 0.1 | 60 | µA |
| | IL-65656V-80/85/100 | – | 0.1 | 8 | µA |
| | IL-65656L-80/85/100 | – | 0.1 | 80 | µA |
| | ML-65656V-80/85/100 | – | 0.1 | 80 | µA |
| | ML-65656-80/85/100 | – | 0.1 | 300 | µA |

**Notes :** 8. TA = 25°C.
9. TAVAV = Read cycle time.
10. $\overline{CS}$ = Vcc, Vin = Gnd/Vcc.

# AC Parameters

## AC Conditions

Input pulse levels : ..... Gnd to 3.0 V
Input rise : ..... 5 ns
Input timing reference levels : ..... 1.2 V
Output load : ..... See fig. 1a, 1b



## Write Cycle : Commercial Specification (note 12)

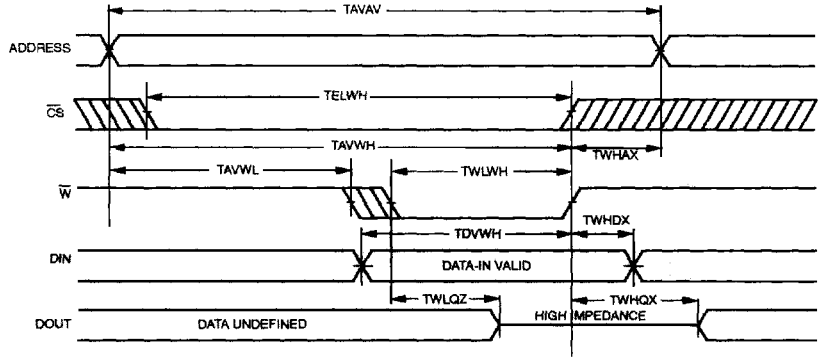
| SYMBOL | PARAMETER | L-65656 L-70 | L-65656 L-70 | L-65656 V-80 | L-65656 L-80 | L-65656 V-100 | L-65656 L-100 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|---|---|
| TAVAV | Write cycle time | 70 | 70 | 80 | 80 | 100 | 100 | ns | min |
| TAVWL | Address set-up time | 0 | 0 | 0 | 0 | 0 | 0 | ns | min |
| TAVWH | Address valid to end of write | 55 | 55 | 65 | 65 | 85 | 85 | ns | min |
| TDVWH | Data set-up time | 45 | 45 | 55 | 55 | 65 | 65 | ns | min |
| TELWH | $\overline{CS}$ low to write end | 55 | 55 | 65 | 65 | 85 | 85 | ns | min |
| TWLQZ (11) | Write low to high Z | 25 | 25 | 25 | 25 | 30 | 30 | ns | max |
| TWLWH | Write pulse width | 60 | 60 | 70 | 70 | 90 | 90 | ns | min |
| TWHAX | Address hold to end of write | 0 | 0 | 0 | 0 | 0 | 0 | ns | min |
| TWHDX | Data hold time | 0 | 0 | 0 | 0 | 0 | 0 | ns | min |
| TWHQX (11) | Write high to low Z | 0 | 0 | 0 | 0 | 0 | 0 | ns | min |

## Write Cycle : Industrial and Military Specification (note 12)

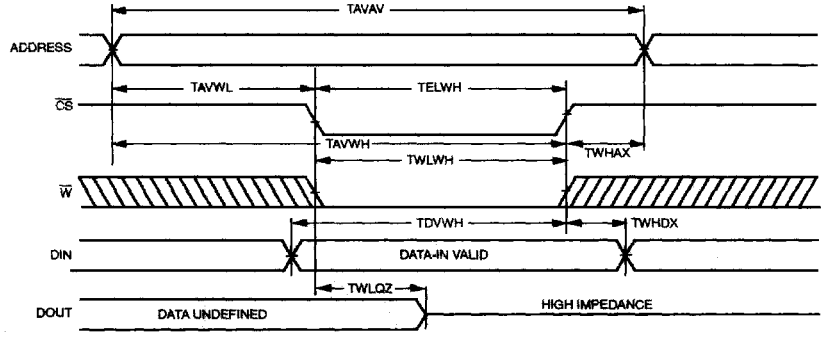
| SYMBOL | PARAMETER | L-65656 V-80 | L-65656 L-80 | L-65656 V-100 | L-65656 L-100 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|
| TAVAV | Write cycle time | 80 | 80 | 100 | 100 | ns | min |
| TAVWL | Address set-up time | 0 | 0 | 0 | 0 | ns | min |
| TAVWH | Address valid to end of write | 65 | 65 | 85 | 85 | ns | min |
| TDVWH | Data set-up time | 55 | 55 | 65 | 65 | ns | min |
| TELWH | $\overline{CS}$ low to write end | 65 | 65 | 85 | 85 | ns | min |
| TWLQZ (11) | Write low to high Z | 25 | 25 | 30 | 30 | ns | max |
| TWLWH | Write pulse width | 70 | 70 | 90 | 90 | ns | min |
| TWHAX | Address hold to end of write | 0 | 0 | 0 | 0 | ns | min |
| TWHDX | Data hold time | 0 | 0 | 0 | 0 | ns | min |
| TWHQX (11) | Write high to low Z | 0 | 0 | 0 | 0 | ns | min |

**Note :** 11. Specified with $C_L$ = 5 pF (see figure 1b). Guaranteed. Not tested.

## Write Cycle 1 : $\overline{W}$ Controlled (note 12)




## Write Cycle 2 : $\overline{CS}$ Controlled (note 12)




**Note :** 12. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
Data out is high impedance if $\overline{OE}$ = VIH.

## AC Test Loads and Waveforms

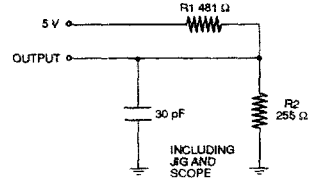



**Figure 1 a**

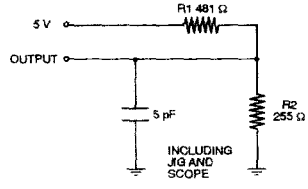



**Figure 1 b**

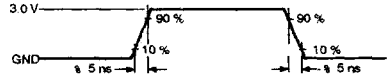
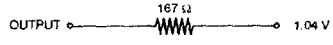



**Figure 2**

Equivalent to : THEVENIN EQUIVALENT



## Read Cycle : Commercial Specification

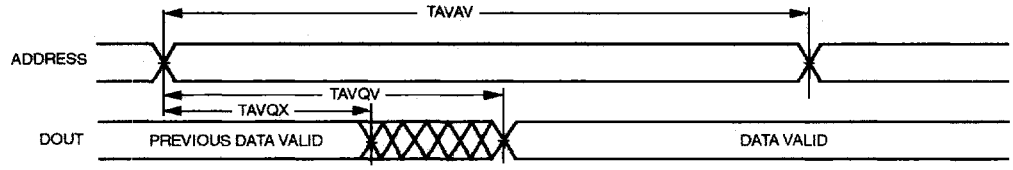
| SYMBOL | PARAMETER | L-65656 V-70 | L-65656 L-70 | L-65656 V-80 | L-65656 L-80 | L-65656 V-100 | L-65656 L-100 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|---|---|
| TAVAV | Write cycle time | 70 | 70 | 80 | 80 | 100 | 100 | ns | min |
| TAVQV | Address access time | 70 | 70 | 80 | 80 | 100 | 100 | ns | max |
| TAVQX | Address valid to low Z | 10 | 10 | 10 | 10 | 10 | 10 | ns | min |
| TELQV | Chip–select access time | 70 | 70 | 80 | 80 | 100 | 100 | ns | max |
| TELQX (13) | $\overline{CS}$ low to low Z | 10 | 10 | 10 | 10 | 10 | 10 | ns | min |
| TEHQZ (13) | $\overline{CS}$ high to high Z | 40 | 40 | 40 | 40 | 60 | 60 | ns | max |
| TGLQV | Output Enable access time | 35 | 35 | 35 | 35 | 40 | 40 | ns | max |
| TGLQX (13) | $\overline{OE}$ low to low Z | 10 | 10 | 10 | 10 | 10 | 10 | ns | min |
| TGHQZ (13) | $\overline{OE}$ high to high Z | 30 | 30 | 30 | 30 | 40 | 40 | ns | max |

## Read Cycle : Industrial and Military Specification

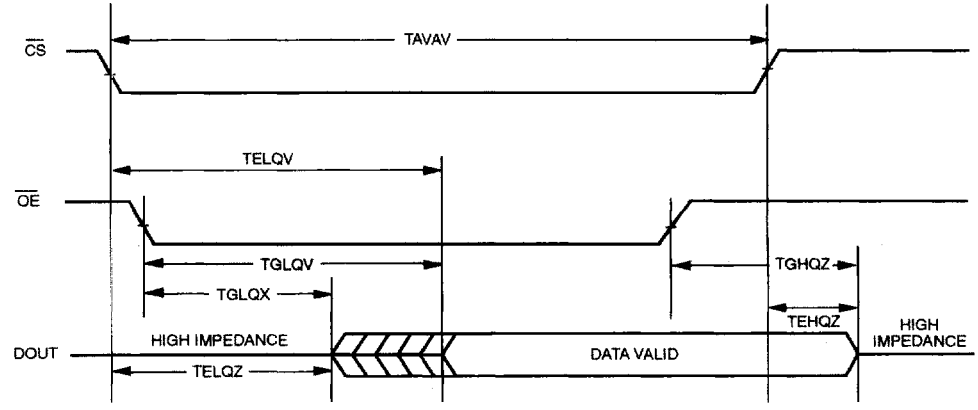
| SYMBOL | PARAMETER | L-65656 V-80 | L-65656 L-80 | L-65656 V-100 | L-65656 L-100 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|
| TAVAV | Read cycle time | 80 | 80 | 100 | 100 | ns | min |
| TAVQV | Address access time | 80 | 80 | 100 | 100 | ns | max |
| TAVQX | Address valid to low Z | 10 | 10 | 10 | 10 | ns | min |
| TELQV | Chip–select access time | 80 | 80 | 100 | 100 | ns | max |
| TELQX (13) | $\overline{CS}$ low to low Z | 10 | 10 | 10 | 10 | ns | min |
| TEHQZ (13) | $\overline{CS}$ high to high Z | 40 | 40 | 60 | 60 | ns | max |
| TGLQV | Output Enable access time | 35 | 35 | 45 | 45 | ns | max |
| TGLQX (13) | $\overline{OE}$ low to low Z | 10 | 10 | 10 | 10 | ns | min |
| TGHQZ (13) | $\overline{OE}$ high to high Z | 30 | 30 | 40 | 40 | ns | max |

**Note :** 13. Guaranteed but not tested.

## Read Cycle nb 1 (notes 14, 15)

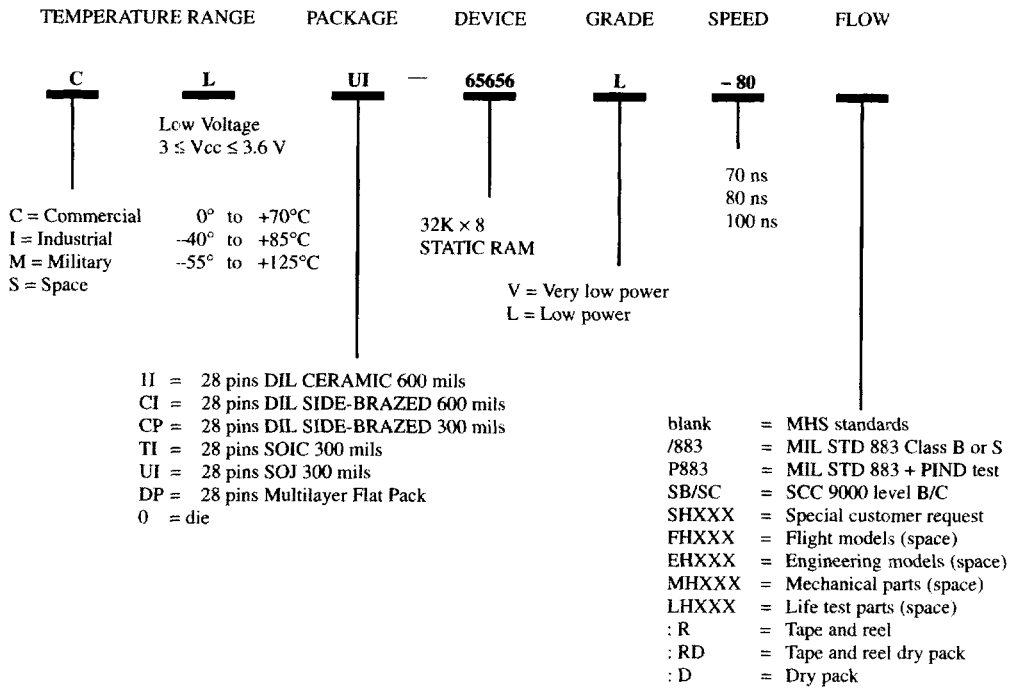



## Read Cycle nb 2 (notes 14, 16)




**Notes :** 14. $\overline{W}$ is high for read cycle.
15. Device is continuously selected, $\overline{CS}$ & $\overline{OE}$ = VIL.
16. Address valid prior to or coincident with $\overline{CS}$ transition low.

## Ordering Information




## Military and Space Versions

The following table gives package/consumption/access time/process flow available combinations

| Temp. range | Packages | Consumption | | Access Time (ns) | | | Std process 5962-9XXXX | RT process 5962-9XXXX | |
|---|---|---|---|---|---|---|---|---|---|
| | | V | L | 80 | 85 | 100 | Mil flows | Mil flows | Space flows |
| M | II | • | • | X | • | • | • | | |
| | CI | • | • | X | • | • | • | | |
| | CP | • | • | X | • | • | • | | |
| | DP | • | • | X | • | • | • | | |
| | 0 | X | • | X | X | • | • | | |
| S | CI | • | • | X | • | • | | • | • |
| | CP | • | | X | • | • | | • | • |
| | DP | • | | X | • | • | | • | • |
| | 0 | X | | X | X | • | | • | • |

• = product in production

X = call sales office for availibility