FAIRCHILD SEMICONDUCTOR TM

February 2002

FDC5614P

60V P-Channel Logic Level PowerTrench® MOSFET

General Description

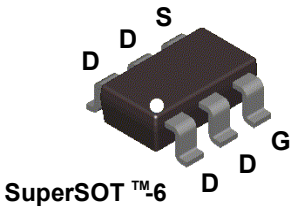
This 60V P-Channel MOSFET uses Fairchild's high voltage PowerTrench process. It has been optimized for power management applications.

Applications

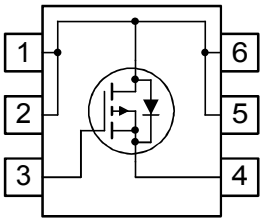
- DC-DC converters
- Load switch
- Power management

Features

- –3 A, –60 V. $R_{DS(ON)}$ = 0.105 Ω @ V_{GS} = –10 V
  $R_{DS(ON)}$ = 0.135 Ω @ V_{GS} = –4.5 V
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$



SuperSOT ™-6



Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		–60	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current – Continuous	(Note 1a)	–3	A
	– Pulsed		–20	
P_D	Maximum Power Dissipation	(Note 1a)	1.6	W
		(Note 1b)	0.8	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	30	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.564	FDC5614P	7''	8mm	3000 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 μA	–60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 μA, Referenced to 25°C		–49		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –48 V, V_{GS} = 0 V			–1	μA
I_{GSSF}	Gate–Body Leakage, Forward	V_{GS} = 20V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	V_{GS} = –20 V V_{DS} = 0 V			–100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 μA	–1	–1.6	–3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = –250 μA,Referenced to 25°C		4		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = –10 V, I_D = –3 A V_{GS} = –4.5 V, I_D = –2.7 A V_{GS} = –10 V, I_D = –3 A T_J=125°C		82 105 130	105 135 190	mΩ
$I_{D(on)}$	On–State Drain Current	V_{GS} = –10 V, V_{DS} = –5 V	–20			A
g_{FS}	Forward Transconductance	V_{DS} = –5 V, I_D = –3 A		8		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = –30 V, V_{GS} = 0 V, f = 1.0 MHz		759		pF
C_{oss}	Output Capacitance			90		pF
C_{rss}	Reverse Transfer Capacitance			39		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = –30 V, I_D = –1 A, V_{GS} = –10 V, R_{GEN} = 6 Ω		7	14	ns
t_r	Turn–On Rise Time			10	20	ns
$t_{d(off)}$	Turn–Off Delay Time			19	34	ns
t_f	Turn–Off Fall Time			12	22	ns
Q_g	Total Gate Charge	V_{DS} = –30V, I_D = –3.0 A, V_{GS} = –10 V		15	24	nC
Q_{gs}	Gate–Source Charge			2.5		nC
Q_{gd}	Gate–Drain Charge			3.0		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				–1.3	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = –1.3 A (Note 2)		–0.8	–1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a. 78°C/W when mounted on a 1in^2 pad of 2oz copper on FR-4 board.

b. 156°C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

Typical Characteristics

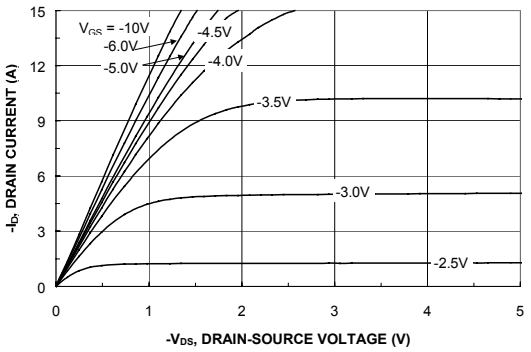


Figure 1. On-Region Characteristics.

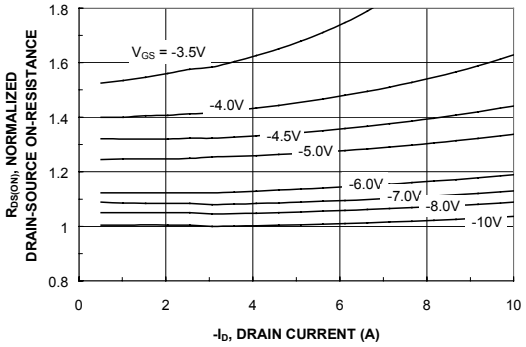


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

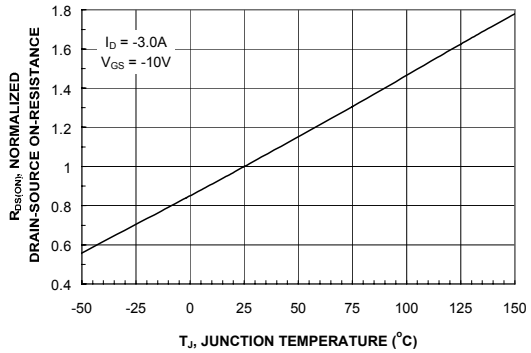


Figure 3. On-Resistance Variation with Temperature.

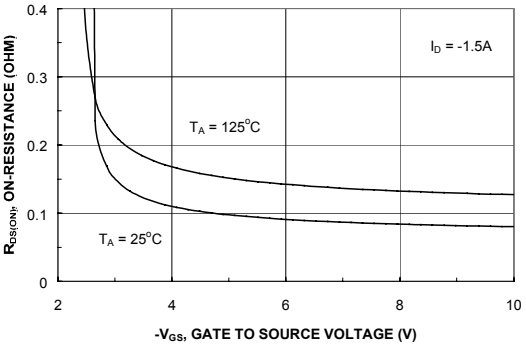


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

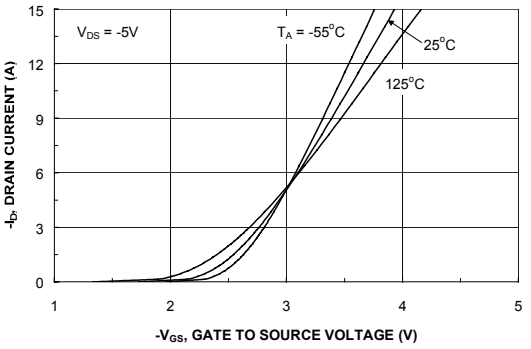


Figure 5. Transfer Characteristics.

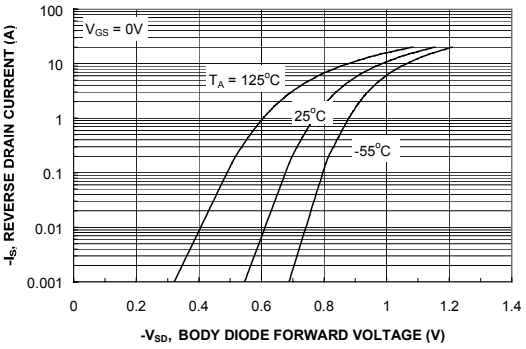


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

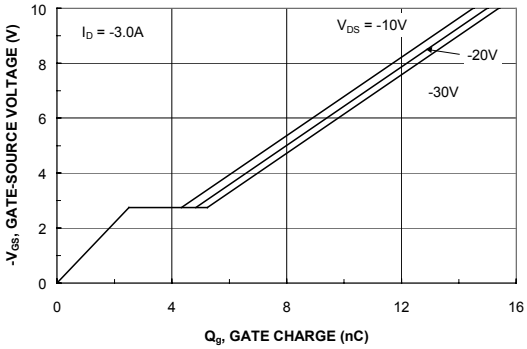


Figure 7. Gate Charge Characteristics.

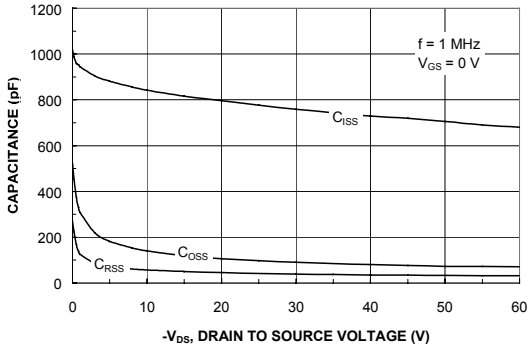


Figure 8. Capacitance Characteristics.

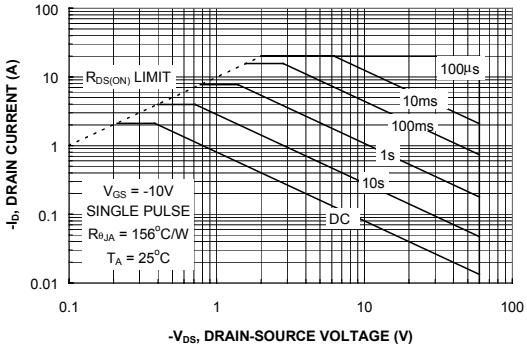


Figure 9. Maximum Safe Operating Area.

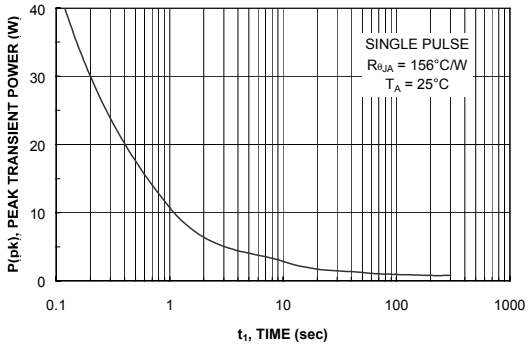


Figure 10. Single Pulse Maximum Power Dissipation.

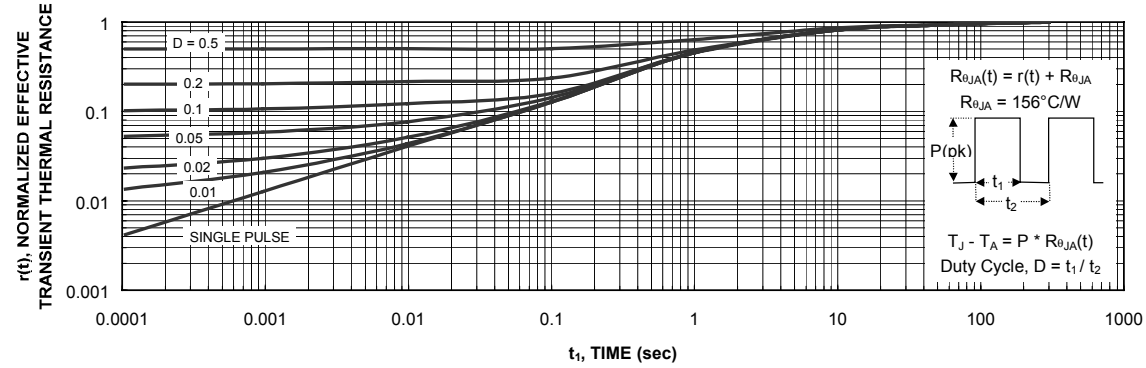


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient themal response will change depending on the circuit board design.

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FAST ®	OPTOLOGIC™	SMART START™	VCX™
Bottomless™	FASTr™	OPTOPLANAR™	STAR*POWER™	
CoolFET™	FRFET™	PACMAN™	Stealth™	
CROSSVOLT™	GlobalOptoisolator™	POP™	SuperSOT™-3	
DenseTrench™	GTO™	Power247™	SuperSOT™-6	
DOME™	HiSeC™	PowerTrench®	SuperSOT™-8	
EcoSPARK™	ISOPLANAR™	QFET™	SyncFET™	
E^2CMOS™	LittleFET™	QS™	TinyLogic™	
EnSigna™	MicroFET™	QT Optoelectronics™	TruTranslation™	
FACT™	MicroPak™	Quiet Series™	UHC™	
FACT Quiet Series™	MICROWIRE™	SILENT SWITCHER®	UltraFET®	

STAR*POWER is used under license

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.
As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

FDC5614P

60V P-Channel Logic Level PowerTrench MOSFET

Contents

BUY

Datasheet
Download this datasheet

e-mail this datasheet

This page
Print version

This product
Use in FETBench Analysis

Related Links

- Request samples
- How to order products
- Product Change Notices (PCNs)
- Support
- Sales support
- Quality and reliability
- Design center

General description

This 60V P-Channel MOSFET uses Fairchild's high voltage PowerTrench process. It has been optimized for power management applications.

back to top

Features

- -3 A, -60 V. $R_{DS(on)}$ = 0.105 Ω @ V_{GS} = -10 V, $R_{DS(on)}$ = 0.135 Ω @ V_{GS} = -4.5 V
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$.

back to top

Applications

- DC-DC converters
- Load switch
- Power management

back to top

Product status/pricing/packaging

BUY

Product	Product status	Pb-free Status	Pricing*	Package type	Leads	Packing method	Package Marking Convention**
FDC5614P	Full Production	Full Production	$0.402	SSOT-6	6	TAPE REEL	Line 1: &E&**Y** (Binary Calendar Year Coding) Line 2: .564
FDC5614P_NF073	Full Production	Full Production	N/A	SSOT-6	6	TAPE REEL	Line 1: &E&**Y** (Binary Calendar Year Coding) Line 2: .564

* Fairchild 1,000 piece Budgetary Pricing
** A sample button will appear if the part is available through Fairchild's on-line samples program. If there is no sample button, please contact a Fairchild distributor to obtain samples

Indicates product with Pb-free second-level interconnect. For more information click here.

Package marking information for product FDC5614P is available. Click here for more information .

back to top

Models

Package & leads	Condition	Temperature range	Software version	Revision date
PSPICE				
SSOT-6-6	Electrical	25°C to 125°C	Orcad 9.1	Jan 30, 2000

back to top

Qualification Support

Click on a product for detailed qualification data

Product
FDC5614P
FDC5614P_NF073

back to top