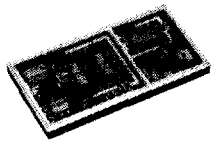
BU-65170/61580 AND BU-61585

MIL-STD-1553A/B NOTICE 2 RT and BC/RT/MT, ADVANCED COMMUNICATION ENGINE (ACE)



ACE User's Guide Also Available

DESCRIPTION

DDC's BU-65170, BU-61580 and BU-61585 BC/RT/MT Advanced Communication Engine (ACE) terminal comprises a complete integrated interface between a host processor and a MIL-STD-1553 A and B or STANAG 3838 bus.

The ACE series is packaged in a 1.9 square inch 70-pin, low-profile, cofired MCM ceramic package that is well suited for applications with stringent height requirements.

The BU-61585 ACE integrates dual transceiver, protocol, memory management, processor interface logic, and a total of 12K words of RAM in a choice of DIP or flat pack packages. The BU-61585 requires +5 V power and either -15 V or -12 V power.

The BU-61585 internal RAM can be configured as 12K x 16 or 8K x 17.

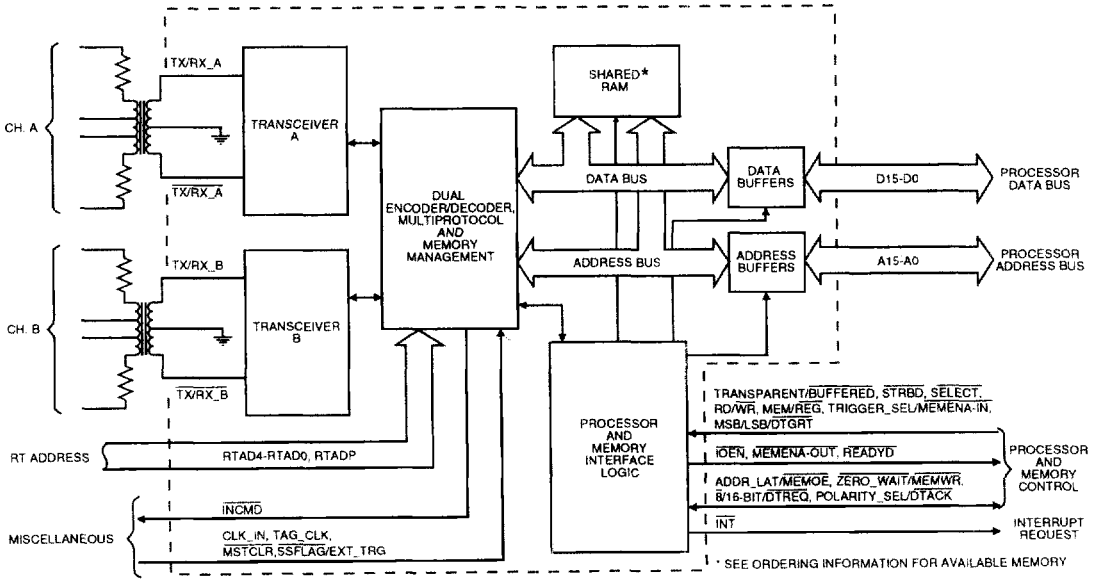
The 8K x 17 RAM feature provides capability for memory integrity checking by implementing RAM parity generation and verification on all accesses. To minimize board space and "glue" logic, the ACE provides ultimate flexibility in interfacing to a host processor and internal/external RAM.

The advanced functional architecture of the ACE terminals provides software compatibility to DDC's AIM series hybrids, while incorporating a multiplicity of architectural enhancements. It allows flexible operation while off-loading the host processor, ensuring data sample consistency, and supporting bulk data transfers.

The ACE hybrids may be operated at either 12 or 16 MHz. Wire bond options allow for programmable RT address (hardwired is standard) and external transmitter inhibit inputs.

FEATURES

- ***Fully Integrated MIL-STD-1553 Interface Terminal***
- ***Flexible Processor/Memory Interface***
- ***Standard 4K x 16 RAM and Optional 12K x 16 or 8K x 17 RAM Available***
- ***Optional RAM Parity Generation/Checking***
- ***Automatic BC Retries***
- ***Programmable BC Gap Times***
- ***BC Frame Auto-Repeat***
- ***Flexible RT Data Buffering***
- ***Programmable Illegalization***
- ***Selective Message Monitor***
- ***Simultaneous RT/Monitor Mode***



ACE BLOCK DIAGRAM

J

BU-65170/65171, BU-61580/61581/61585/61586 PIN LISTINGS (S OR V PACKAGE)	
PIN	**NAME**
1	TX/RX-A
2	TX/RX-A*
3	SELECT*
4	STRBD*
5	MEM/REG*
6	RD/WR*
7	MSTCLR*
8	A15
9	A14
10	A13
11	A12
12	A11
13	A10
14	A09
15	A08
16	A07
17	A06
18	GND
19	CLK
20	A05
21	A04
22	A03
23	A02
24	A01
25	A00
26	DTGRT*/MSB/LSB
27	SSFLAG*/EXT_TRIG
28	MEMENA_OUT*
29	MEMOE*/ADDR_LAT
30	MEMWR*/ZERO_WAIT*
31	DTREQ/16/8*
32	DTACK*/POLARITY_SEL
33	MEMENA_IN*/TRIGGER_SEL
34	TX/RX-B
35	TX/RX-B*

BU-65170/65171, BU-61580/61581/61585/61586 PIN LISTINGS (S OR V PACKAGE)	
PIN	**NAME**
36	-VB (see note)
37	GNDB
38	+5VB
39	RTAD0
40	RTAD1
41	RTAD2
42	RTAD3
43	RTAD4
44	RTADP
45	INCMD*
46	D00
47	D01
48	D02
49	D03
50	D04
51	D05
52	D06
53	D07
54	+5V Logic
55	D08
56	D09
57	D10
58	D11
59	D12
60	D13
61	D14
62	D15
63	TAG_CLK
64	TRANSPARENT/BUFFERED*
65	INT*
66	READYD*
67	IOEN*
68	+5VA
69	GNDA
70	-VA (see note)

Notes:

-15V for BU-65170/61580X1.
-12V for BU-65170/61580X2.
N/C for BU-65170/61580X3.

For BU-65170/61580X6.
pin 36 is TX_INH_B
pin 70 is TX_INH_A

ORDERING INFORMATION

BU-XXXXXXX-XX0X

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = Pull Test
- Q = Pull Test and Pre-Cap Inspection
- Blank = None of the Above

Process Requirements:
- 0 = Standard DDC practices, no Burn-In (See page xiii.)
- 1 = MIL-PRF-38534 Compliant
- 2 = B*
- 3 = MIL-PRF-38534 Compliant with PIND Testing
- 4 = MIL-PRF-38534 Compliant with Solder Dip
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip
- 6 = B* with PIND Testing
- 7 = B* with Solder Dip
- 8 = B* with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In (See page xiii.)

Temperature Range/Data Requirements:
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 8 = 0°C to +70°C with Variables Test Data

Voltage/Transceiver Option:
- 0 = Transceiverless
- 1 = +5 Volts and -15 Volts (1760 Compliant)
- 2 = +5 Volts and -12 Volts
- 3 = +5 Volts only
- 5 = +5/+15/-15V Sinusoidal (McAir)
- 6 = +5 Volts only with TX Inhibit inputs brought out on negative supply pins

Package Type:
- D = DIP (replaced by "S" package)
- F = Flat Pack (replaced by "V" package)
- J = J Lead
- S = Small DIP
- V = Very Small Flat Pack
- P = PGA
- G = "Gull Wing" (Formed Lead) - ("Process Requirements" must include solder dip.)

Product Type:
- 65170 = 70-pin RT
- 65171 = 70-pin RT with Latchable RT Address Option
- 65178 = 72-pin Quad Flat Pack/81-pin PGA RT only Mini-ACE
- 61580 = 70-pin BC/RT/MT
- 61581 = 70-pin BC/RT/MT with Latchable RT address Option
- 61582 = Rad Hard 70-pin BC/RT/MT with 16K x 16 RAM
- 61583 = Rad Hard 70-pin BC/RT/MT with 16K x 16 RAM and Latchable RT Address Option
- 61585 = 70-pin BC/RT/MT 8K x 17 with RAM
- 61586 = 70-pin BC/RT/MT 8K x 17 with RAM and RT Address Option
- 61588 = 72-pin Quad Flatpack/81-pin PGA BC/RT/MT Mini-ACE
- 61590 = 78-pin Universal BC/RT/MT with 4K x 16 RAM
- 65620 = 144-pin Monolithic BC/RT/MT with 4K x 16 RAM and no transceivers
- 65621 = 172-pin Rad Hard monolithic with no RAM and no tranceivers

Note: The ACE series is also available to DESC drawing number 5962-93065.

*Standard DDC Processing with burn-in and full temperature test, see table on page xiii.

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