

IGLOO PLUS Low Power Flash FPGAs with Flash*Freeze Technology



Features and Benefits

Low Power

- 1.2 V to 1.5 V Core Voltage Support for Low Power
- Supports Single-Voltage System Operation
- 5 μ W Power Consumption in Flash*Freeze Mode
- Low Power Active FPGA Operation
- Flash*Freeze Technology Enables Ultra-Low Power Consumption while Maintaining FPGA Content
- Configurable Hold Previous State, Tristate, HIGH, or LOW State per I/O in Flash*Freeze Mode
- Easy Entry To / Exit From Ultra-Low Power Flash*Freeze Mode

Feature Rich

- 30 k to 125 k System Gates
- Up to 36 kbits of True Dual-Port SRAM
- Up to 212 User I/Os

Reprogrammable Flash Technology

- 130-nm, 7-Layer Metal, Flash-Based CMOS Process
- Live-at-Power-Up (LAPU) Level 0 Support
- Single-Chip Solution
- Retains Programmed Design When Powered Off
- 250 MHz (1.5 V systems) and 160 MHz (1.2 V systems) System Performance

In-System Programming (ISP) and Security

- Secure ISP Using On-Chip 128-Bit Advanced Encryption Standard (AES) Decryption via JTAG (IEEE 1532-compliant)[†]
- FlashLock[®] to Secure FPGA Contents

High-Performance Routing Hierarchy

- Segmented, Hierarchical Routing and Clock Structure

Table 1 • IGLOO PLUS Product Family

IGLOO PLUS Devices	AGLP030	AGLP060	AGLP125
System Gates	30,000	60,000	125,000
Typical Equivalent Macrocells	256	512	1,024
VersaTiles (D-flip-flops)	792	1,584	3,120
Flash*Freeze Mode (typical, μ W)	5	10	16
RAM Kbits (1,024 bits)	–	18	36
4,608-Bit Blocks	–	4	8
Secure (AES) ISP	–	Yes	Yes
FlashROM Kbits	1	1	1
Integrated PLL in CCCs ¹	–	1	1
VersaNet Globals ²	6	18	18
I/O Banks	4	4	4
Maximum User I/Os	120	157	212
Package Pins			
CS	CS201, CS289	CS201, CS289	CS281, CS289
VQ	VQ128	VQ176	

Notes:

1. AGLP060 in CS201 does not support the PLL.
2. Six chip (main) and twelve quadrant global networks are available for AGLP060 and AGLP125.

[†] The AGLP030 device does not support this feature.

I/Os Per Package ¹

IGLOO PLUS Devices	AGLP030	AGLP060	AGLP125
Package	Single-Ended I/Os		
CS201	120	157	–
CS281	–	–	212
CS289	120	157	212
VQ128	101	–	–
VQ176	–	137	–

Note: When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.

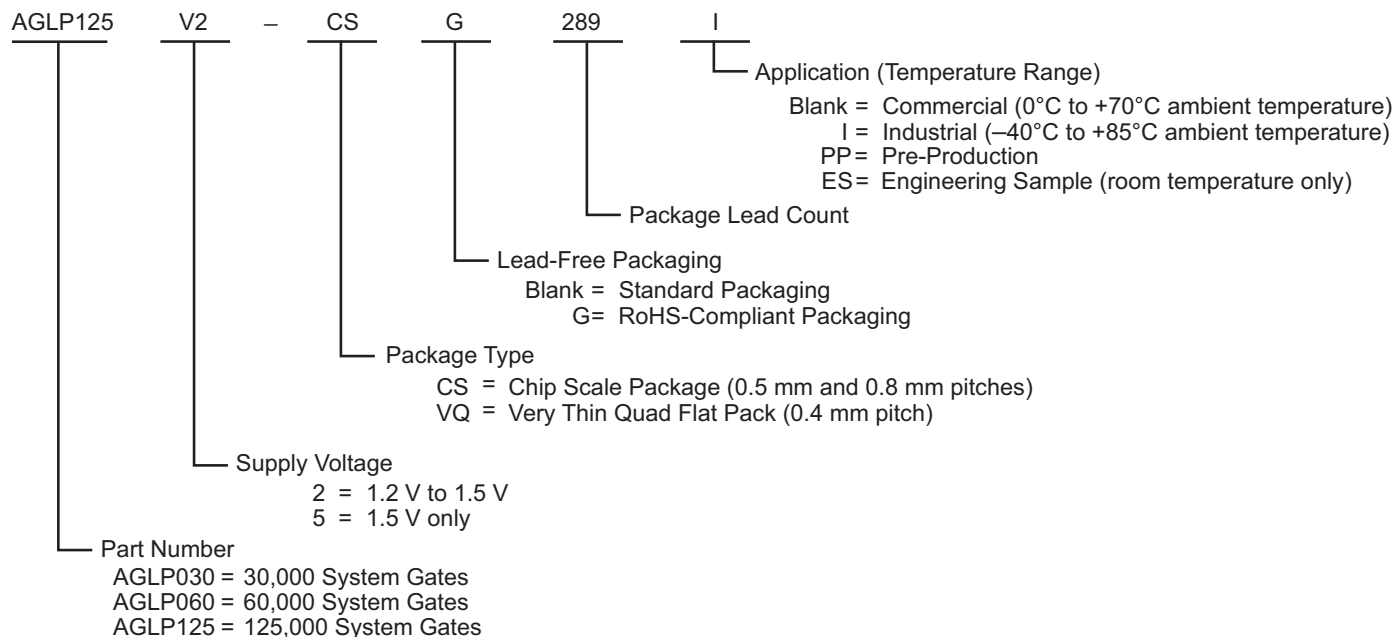
Table 2 • IGLOO PLUS FPGAs Package Size Dimensions

Package	CS201	CS281	CS289	VQ128	VQ176
Length × Width (mm/mm)	8 × 8	10 × 10	14 × 14	14 × 14	20 × 20
Nominal Area (mm²)	64	100	196	196	400
Pitch (mm)	0.5	0.5	0.8	0.4	0.4
Height (mm)	0.89	1.05	1.20	1.0	1.0

IGLOO PLUS Device Status

IGLOO PLUS Device	Status
AGLP030	Production
AGLP060	Production
AGLP125	Production

IGLOO PLUS Ordering Information



Notes:

1. Marking information: IGLOO PLUS V2 devices do not have a V2 marking, but IGLOO PLUS V5 devices are marked accordingly.
2. "G" indicates RoHS-compliant packages.

Temperature Grade Offerings

Package	AGLP030	AGLP060	AGLP125
CS201	C, I	C, I	–
CS281	–	–	C, I
CS289	C, I	C, I	C, I
VQ128	C, I	–	–
VQ176	–	C, I	–

Notes:

1. C = Commercial temperature range: 0°C to 70°C ambient temperature.
2. I = Industrial temperature range: –40°C to 85°C ambient temperature.

Contact your local Actel representative for device availability: <http://www.actel.com/company/contact/default.aspx>.

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1 – IGLOO PLUS Device Family Overview

General Description

The IGLOO PLUS family of flash FPGAs, based on a 130 nm flash process, offers the lowest power FPGA, a single-chip solution, small-footprint packages, reprogrammability, and an abundance of advanced features.

The Flash*Freeze technology used in IGLOO PLUS devices enables entering and exiting an ultra-low power mode that consumes as little as 5 μ W while retaining the design information, SRAM content, registers, and I/O states. Flash*Freeze technology simplifies power management through I/O and clock management with rapid recovery to operation mode.

The Low Power Active capability (static idle) allows for ultra-low power consumption while the IGLOO PLUS device is completely functional in the system. This allows the IGLOO PLUS device to control system power management based on external inputs (e.g., scanning for keyboard stimulus) while consuming minimal power.

Nonvolatile flash technology gives IGLOO PLUS devices the advantage of being a secure, low power, single-chip solution that is live at power-up (LAPU). IGLOO PLUS is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

IGLOO PLUS devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on an integrated phase-locked loop (PLL). IGLOO PLUS devices have up to 125 k system gates, supported with up to 36 kbits of true dual-port SRAM and up to 212 user I/Os. The AGLP030 devices have no PLL or RAM support.

Flash*Freeze Technology

The IGLOO PLUS device offers unique Flash*Freeze technology, allowing the device to enter and exit ultra-low power Flash*Freeze mode. IGLOO PLUS devices do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, registers, and I/O states. Flash*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of IGLOO PLUS V2 devices to support a wide range of core and I/O voltages (1.2 V to 1.5 V) allows further reduction in power consumption, thus achieving the lowest total system power.

During Flash*Freeze mode, each I/O can be set to the following configurations: hold previous state, tristate, or set as HIGH or LOW.

The availability of low power modes, combined with reprogrammability, a single-chip and single-voltage solution, and availability of small-footprint, high-pin-count packages, make IGLOO PLUS devices the best fit for portable electronics.

Flash Advantages

Low Power

IGLOO PLUS devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. IGLOO PLUS devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

IGLOO PLUS devices also have low dynamic power consumption to further maximize power savings; power is even further reduced by the use of a 1.2 V core voltage.

Low dynamic power consumption, combined with low static power consumption and Flash*Freeze technology, gives the IGLOO PLUS device the lowest total system power offered by any FPGA.

Security

The nonvolatile, flash-based IGLOO PLUS devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. IGLOO PLUS devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

IGLOO PLUS devices (except AGLP030) utilize a 128-bit flash-based lock and a separate AES key to secure programmed intellectual property and configuration data. In addition, all FlashROM data in IGLOO PLUS devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. IGLOO PLUS devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. IGLOO PLUS devices with AES-based security allow for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. The contents of a programmed IGLOO PLUS device cannot be read back, although secure design verification is possible.

Security, built into the FPGA fabric, is an inherent component of the IGLOO PLUS family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The IGLOO PLUS family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected and secure, making remote ISP possible. An IGLOO PLUS device provides the most impenetrable security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based IGLOO PLUS FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

The IGLOO PLUS devices can be operated with a 1.2 V or 1.5 V single-voltage supply for core and I/Os, eliminating the need for additional supplies while minimizing total power consumption.

Live at Power-Up

The Actel flash-based IGLOO PLUS devices support Level 0 of the LAPU classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The LAPU feature of flash-based IGLOO PLUS devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the IGLOO PLUS device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based IGLOO PLUS devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

IGLOO PLUS flash FPGAs allow the user to quickly enter and exit Flash*Freeze mode. This is done almost instantly (within 1 μ s), and the device retains configuration and data in registers and RAM. Unlike SRAM-based FPGAs, the device does not need to reload configuration and design state from external memory components; instead, it retains all necessary information to resume operation immediately.

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based IGLOO PLUS devices allow all functionality to be live at power-up; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the

industry-standard AES algorithm. The IGLOO PLUS family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the IGLOO PLUS family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/communications, computing, and avionics markets.

Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of IGLOO PLUS flash-based FPGAs. Once it is programmed, the flash cell configuration element of IGLOO PLUS FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Advanced Flash Technology

The IGLOO PLUS family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130 nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

IGLOO PLUS family FPGAs utilize design and process techniques to minimize power consumption in all modes of operation.

Advanced Architecture

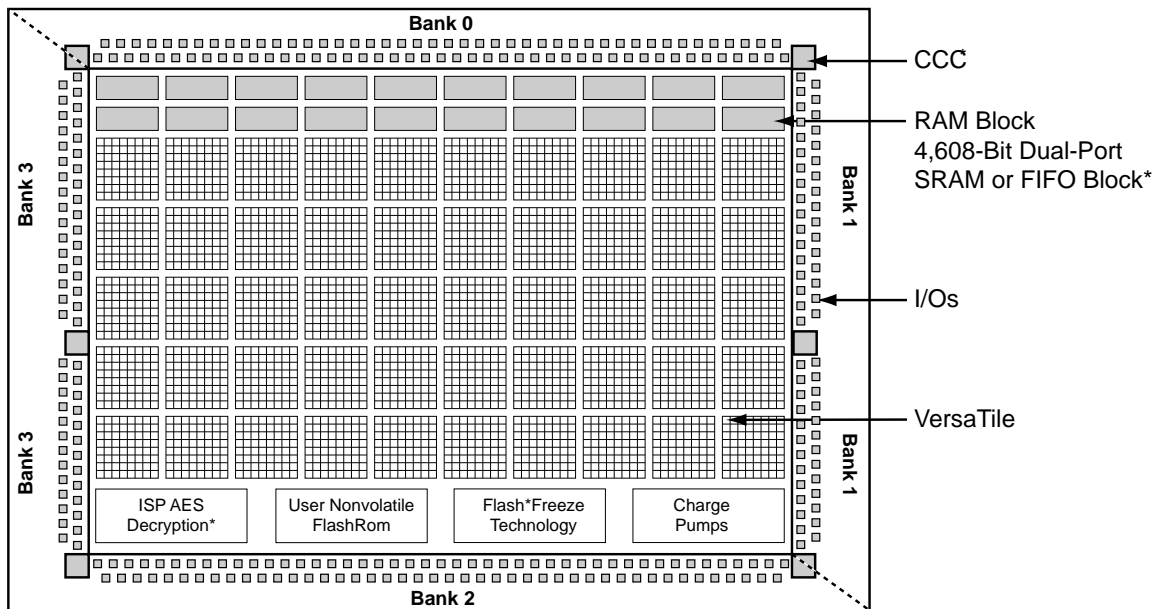
The proprietary IGLOO PLUS architecture provides granularity comparable to standard-cell ASICs. The IGLOO PLUS device consists of five distinct and programmable architectural features (Figure 1-1 on page 1-4):

- Flash*Freeze technology
- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory†
- Extensive CCCs and PLLs†
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the IGLOO PLUS core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Actel ProASIC family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of IGLOO PLUS devices via an IEEE 1532 JTAG interface.

† The AGLP030 device does not support PLL or SRAM.



* Not supported by AGLP030 devices

Figure 1-1 • IGLOO PLUS Device Architecture Overview with Four I/O Banks (AGLP030, AGLP060, and AGLP125)

Flash*Freeze Technology

The IGLOO PLUS device has an ultra-low power static mode, called Flash*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash*Freeze technology enables the user to quickly (within 1 μ s) enter and exit Flash*Freeze mode by activating the Flash*Freeze pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption, clocks can still be driven or can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and I/O states. I/Os can be individually configured to either hold their previous state or be tristated during Flash*Freeze mode. Alternatively, they can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL, and the device consumes as little as 5 μ W in this mode.

Flash*Freeze technology allows the user to switch to Active mode on demand, thus simplifying the power management of the device.

The Flash*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. Refer to [Figure 1-2](#) for an illustration of entering/exiting Flash*Freeze mode. It is also possible to use the Flash*Freeze pin as a regular I/O if Flash*Freeze mode usage is not planned.

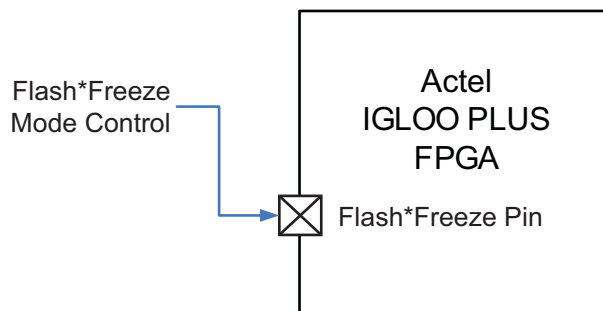


Figure 1-2 • IGLOO PLUS Flash*Freeze Mode

VersaTiles

The IGLOO PLUS core consists of VersaTiles, which have been enhanced beyond the ProASIC^{PLUS}® core tiles. The IGLOO PLUS VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to [Figure 1-3](#) for VersaTile configurations.

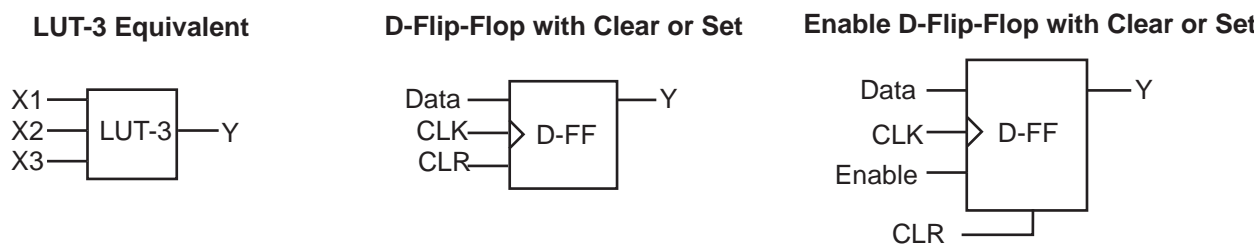


Figure 1-3 • VersaTile Configurations

User Nonvolatile FlashROM

Actel IGLOO PLUS devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard IGLOO PLUS IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in AGLP030 devices), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The Actel IGLOO PLUS development software solutions, Libero[®] Integrated Design Environment (IDE) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Actel Libero IDE and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

IGLOO PLUS devices (except AGLP030 devices) have embedded SRAM blocks along their north side. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256x18, 512x9, 1kx4, 2kx2, and 4kx1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in AGLP030 devices).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

IGLOO PLUS devices provide designers with very flexible clock conditioning circuit (CCC) capabilities. Each member of the IGLOO PLUS family contains six CCCs. One CCC (center west side) has a PLL. The AGLP030 device does not have a PLL or CCCs; it contains only inputs to six globals.

The six CCC blocks are located at the four corners and the centers of the east and west sides. One CCC (center west side) has a PLL.

The four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz up to 250 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time is 300 μs (for PLL only)
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases (for PLL only) is 40 ps × 250 MHz / f_{OUT_CCC}

Global Clocking

IGLOO PLUS devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

I/Os with Advanced I/O Standards

The IGLOO PLUS family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V wide range, and 3.3 V). IGLOO PLUS FPGAs support many different I/O standards.

The I/Os are organized into four banks. All devices in IGLOO PLUS have four banks. The configuration of these banks determines the I/O standards supported.

Each I/O module contains several input, output, and output enable registers.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

Wide Range I/O Support

Actel IGLOO PLUS devices support JEDEC-defined wide range I/O operation. IGLOO PLUS devices support both the JESD8-B specification, covering 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V, and JESD8-12 with its 1.2 V nominal, supporting an effective operating range of 1.14 V to 1.575 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

2 – IGLOO PLUS DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in [Table 2-1](#) may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in [Table 2-2](#) on [page 2-2](#) is not implied.

Table 2-1 • Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	-0.3 to 1.65	V
VJTAG	JTAG DC voltage	-0.3 to 3.75	V
VPUMP	Programming voltage	-0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	-0.3 to 1.65	V
VCCI	DC I/O buffer supply voltage	-0.3 to 3.75	V
VI ¹	I/O input voltage	-0.3 V to 3.6 V	V
T _{STG} ²	Storage temperature	-65 to +150	°C
T _J ²	Junction temperature	+125	°C

Notes:

- 1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in [Table 2-4](#) on [page 2-3](#).*
- 2. For flash programming and retention maximum limits, refer to [Table 2-3](#) on [page 2-2](#), and for recommended operating limits, refer to [Table 2-2](#) on [page 2-2](#).*

Table 2-2 • Recommended Operating Conditions^{1,2}

Symbol	Parameter		Commercial	Industrial	Units
T _A	Ambient temperature		0 to +70	–40 to +85	°C
T _J	Junction temperature ²		0 to +85	–40 to +100	°C
VCC ³	1.5 V DC core supply voltage ⁴		1.425 to 1.575	1.425 to 1.575	V
	1.2 V–1.5 V wide range core voltage ^{5,6}		1.14 to 1.575	1.14 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP ⁷	Programming voltage	Programming mode	3.15 to 3.45	3.15 to 3.45	V
		Operation	0 to 3.6	0 to 3.6	V
VCCPLL ⁸	Analog power supply (PLL)	1.5 V DC core supply voltage ⁴	1.425 to 1.575	1.425 to 1.575	V
		1.2 V–1.5 V wide range core voltage ⁵	1.14 to 1.575	1.14 to 1.575	V
VCCI	1.2 V DC supply voltage ⁵		1.14 to 1.26	1.14 to 1.26	V
	1.2 V DC wide range supply voltage ⁵		1.14 to 1.575	1.14 to 1.575	V
	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V wide range DC supply voltage ⁹		2.7 to 3.6	2.7 to 3.6	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V

Notes:

1. All parameters representing voltages are measured with respect to GND unless otherwise specified.
2. To ensure targeted reliability standards are met across ambient and junction operating temperatures, Actel recommends that the user follow best design practices using Actel's timing and power simulation tools.
3. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in [Table 2-21 on page 2-19](#). VCCI should be at the same voltage within a given I/O bank.
4. For IGLOO[®] PLUS V5 devices
5. For IGLOO PLUS V2 devices only, operating at $VCCI \geq VCC$.
6. All IGLOO PLUS devices (V5 and V2) must be programmed with the VCC core voltage at 1.5 V. Applications using V2 devices powered by a 1.2 V supply must switch the core supply to 1.5 V for in-system programming.
7. VPUMP can be left floating during operation (not programming mode).
8. VCCPLL pins should be tied to VCC pins. See the Pin Descriptions chapter of the [IGLOO PLUS FPGA Fabric User's Guide](#) for further information.
9. 3.3 V wide range is compliant to the JDEC8b specification and supports 3.0 V VCCI operation.

Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature¹

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T _{STG} (°C) ²	Maximum Operating Junction Temperature T _J (°C) ²
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Notes:

1. This is a stress rating only; functional operation at any condition other than those indicated is not implied.
2. These limits apply for program/data retention only. Refer to [Table 2-1 on page 2-1](#) and [Table 2-2](#) for device operating conditions and absolute limits.

Table 2-4 • Overshoot and Undershoot Limits¹

VCCI	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle ²	Maximum Overshoot/Undershoot ²
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. Based on reliability requirements at 85°C.
2. The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every IGLOO PLUS device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in [Figure 2-1 on page 2-4](#).

There are five regions to consider during power-up.

IGLOO PLUS I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points ([Figure 2-1](#) and [Figure 2-2 on page 2-5](#)).
2. $VCCI > VCC - 0.75\text{ V}$ (typical)
3. Chip is in the operating mode.

VCCI Trip Point:

Ramping up (V5 devices): $0.6\text{ V} < \text{trip_point_up} < 1.2\text{ V}$

Ramping down (V5 devices): $0.5\text{ V} < \text{trip_point_down} < 1.1\text{ V}$

Ramping up (V2 devices): $0.75\text{ V} < \text{trip_point_up} < 1.05\text{ V}$

Ramping down (V2 devices): $0.65\text{ V} < \text{trip_point_down} < 0.95\text{ V}$

VCC Trip Point:

Ramping up (V5 devices): $0.6\text{ V} < \text{trip_point_up} < 1.1\text{ V}$

Ramping down (V5 devices): $0.5\text{ V} < \text{trip_point_down} < 1.0\text{ V}$

Ramping up (V2 devices): $0.65\text{ V} < \text{trip_point_up} < 1.05\text{ V}$

Ramping down (V2 devices): $0.55\text{ V} < \text{trip_point_down} < 0.95\text{ V}$

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

Actel recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLX exceed brownout activation levels (see Figure 2-1 and Figure 2-2 on page 2-5 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels ($0.75\text{ V} \pm 0.25\text{ V}$ for V5 devices, and $0.75\text{ V} \pm 0.2\text{ V}$ for V2 devices), the PLL output lock signal goes Low and/or the output clock is lost. Refer to the "Brownout Voltage" section in the "Power-Up/Down Behavior of Low Power Flash Devices" chapter of the *IGLOO PLUS Device Family User's Guide* for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

To make sure the transition from input buffers to output buffers is clean, ensure that there is no path longer than 100 ns from input buffer to output buffer in your design.

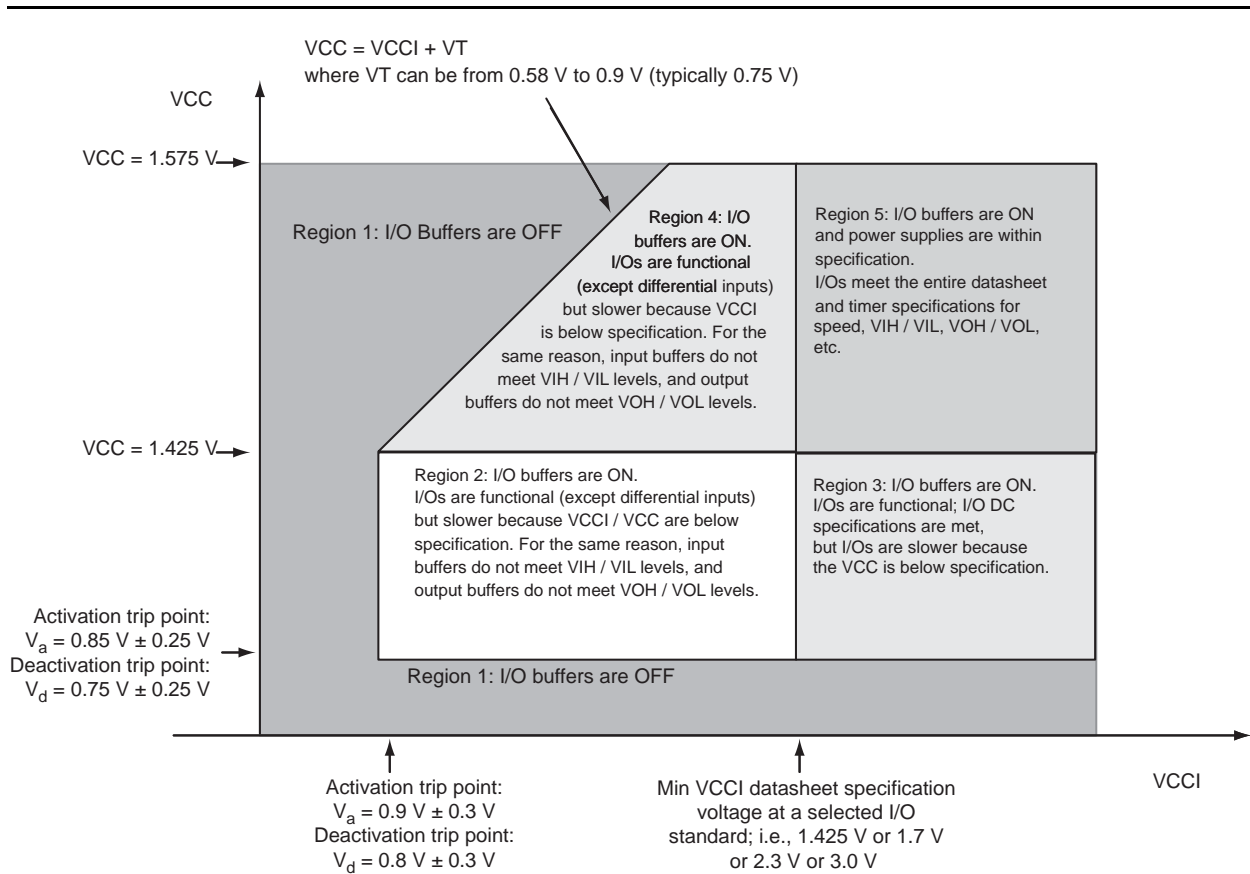


Figure 2-1 • V5 Devices – I/O State as a Function of VCCI and VCC Voltage Levels

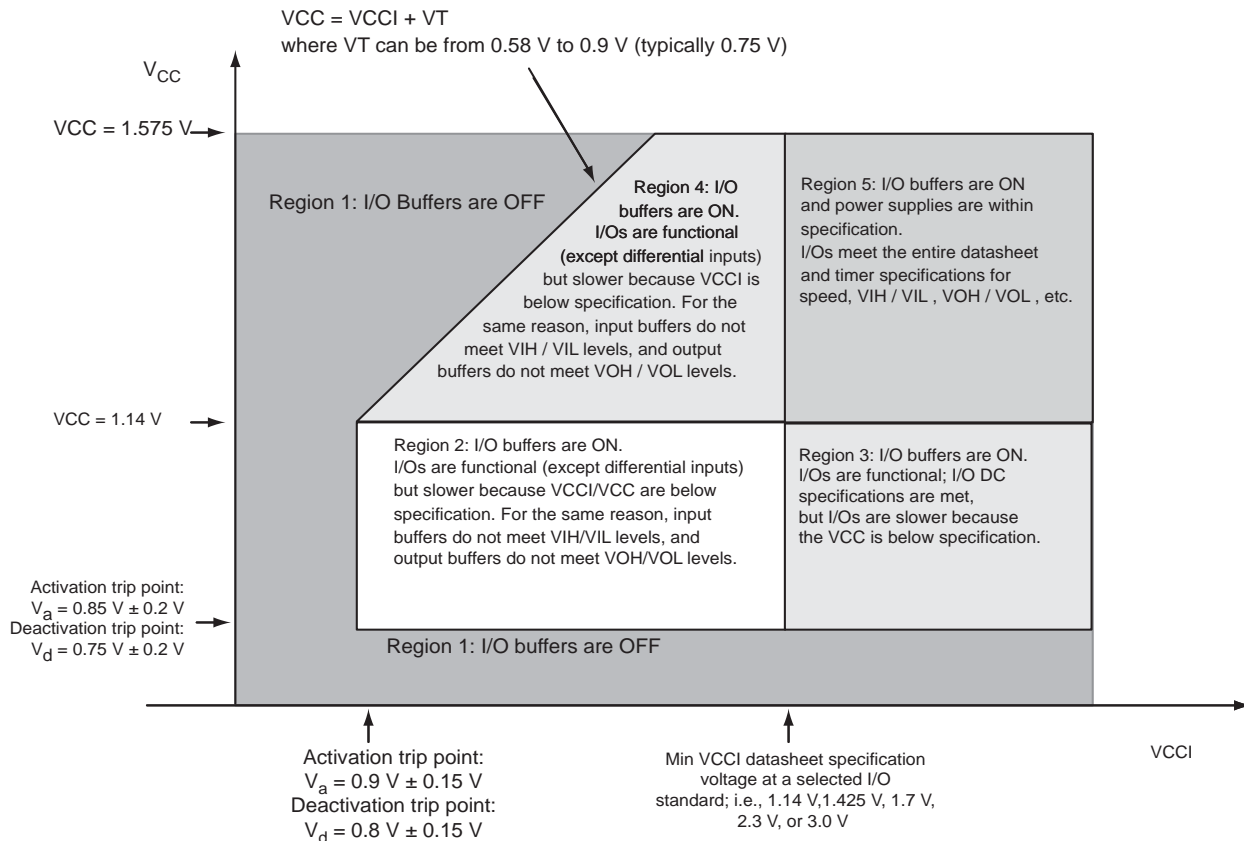


Figure 2-2 • V2 Devices – I/O State as a Function of VCCI and VCC Voltage Levels

Thermal Characteristics

Introduction

The temperature variable in the Actel Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction temperature to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

EQ 1

where:

T_A = Ambient temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Figure 2-5.

P = Power dissipation

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja} . The thermal characteristics for θ_{ja} are shown for two air flow rates. The maximum operating junction temperature is 100°C. EQ 2 shows a sample calculation of the maximum operating power dissipation allowed for a 484-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (}^\circ\text{C)} - \text{Max. ambient temp. (}^\circ\text{C)}}{\theta_{ja}(\text{}^\circ\text{C/W)}} = \frac{100^\circ\text{C} - 70^\circ\text{C}}{20.5^\circ\text{C/W}} = 1.46 \text{ W}$$

EQ 2

Table 2-5 • Package Thermal Resistivities

Package Type	Pin Count	θ_{jc}	θ_{ja}			Units
			Still Air	200 ft./min.	500 ft./min.	
Chip Scale Package (CSP)	201	TBD	TBD	TBD	TBD	C/W
	281	TBD	TBD	TBD	TBD	C/W
	289	TBD	TBD	TBD	TBD	C/W
Very Thin Quad Flat Package (VQFP)	128	TBD	TBD	TBD	TBD	C/W
	176	TBD	TBD	TBD	TBD	C/W

Temperature and Voltage Derating Factors

**Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425 \text{ V}$)
For IGLoo PLUS V2 or V5 devices, 1.5 V DC Core Supply Voltage**

Array Voltage VCC (V)	Junction Temperature ($^\circ\text{C}$)					
	-40°C	0°C	25°C	70°C	85°C	100°C
1.425	0.934	0.953	0.971	1.000	1.007	1.013
1.5	0.855	0.874	0.891	0.917	0.924	0.929
1.575	0.799	0.816	0.832	0.857	0.864	0.868

**Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$)
For IGLOO PLUS V2, 1.2 V DC Core Supply Voltage**

Array Voltage VCC (V)	Junction Temperature ($^\circ\text{C}$)					
	-40°C	0°C	25°C	70°C	85°C	100°C
1.14	0.963	0.975	0.989	1.000	1.007	1.011
1.2	0.853	0.865	.0877	0.893	0.893	0.897
1.26	0.781	0.792	0.803	0.813	0.819	0.822

Calculating Power Dissipation

Quiescent Supply Current

Quiescent supply current (I_{DD}) calculation depends on multiple factors, including operating voltages (VCC, VCCI, and VJTAG), operating temperature, system clock frequency, and power mode usage. Actel recommends using the Power Calculator and SmartPower software estimation tools to evaluate the projected static and active power based on the user design, power mode usage, operating voltage, and temperature.

Table 2-8 • Power Supply State per Mode

Modes/Power Supplies	Power Supply Configurations				
	VCC	VCCPLL	VCCI	VJTAG	VPUMP
Flash*Freeze	On	On	On	On	On/off/floating
Sleep	Off	Off	On	Off	Off
Shutdown	Off	Off	Off	Off	Off
No Flash*Freeze	On	On	On	On	On/off/floating

Note: Off: Power Supply level = 0 V

Table 2-9 • Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Flash*Freeze Mode*

	Core Voltage	AGLP030	AGLP060	AGLP125	Units
Typical (25°C)	1.2 V	4	8	13	μA
	1.5 V	6	10	18	μA

* I_{DD} includes VCC, VPUMP, VCCI, VJTAG, and VCCPLL currents.

Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Sleep Mode*

ICCI Current	Core Voltage	AGLP030	AGLP060	AGLP125	Units
VCCI = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	μA
VCCI = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	μA
VCCI = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	μA
VCCI = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	μA
VCCI = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	μA

Note: * $I_{DD} = N_{BANKS} * ICCI$

Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Shutdown Mode

	Core Voltage	AGLP030	AGLP060	AGLP125	Units
Typical (25°C)	1.2 V / 1.5 V	0	0	0	μA

Table 2-12 • Quiescent Supply Current (IDD), No IGLOO PLUS Flash*Freeze Mode¹

	Core Voltage	AGLP030	AGLP060	AGLP125	Units
ICCA Current²					
Typical (25°C)	1.2 V	6	10	13	μA
	1.5 V	16	20	28	μA
ICCI or IJTAG Current					
VCCI / VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	μA
VCCI / VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	μA
VCCI / VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	μA
VCCI / VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	μA
VCCI / VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	μA

Notes:

1. $IDD = N_{BANKS} * ICCI + ICCA$. JTAG counts as one bank when powered.
2. Includes VCC, VCCPLL, and VPUMP currents.

Power per I/O Pin

Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings

	VCCI (V)	Dynamic Power PAC9 (μW/MHz) ¹
Single-Ended		
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	16.26
3.3 V LVTTTL / 3.3 V LVCMOS – Schmitt Trigger	3.3	18.95
3.3 V LVCMOS Wide Range ²	3.3	16.26
3.3 V LVCMOS Wide Range ² – Schmitt Trigger	3.3	18.95
2.5 V LVCMOS	2.5	4.59
2.5 V LVCMOS – Schmitt Trigger	2.5	6.01
1.8 V LVCMOS	1.8	1.61
1.8 V LVCMOS – Schmitt Trigger	1.8	1.70
1.5 V LVCMOS (JESD8-11)	1.5	0.96
1.5 V LVCMOS (JESD8-11) – Schmitt Trigger	1.5	0.90
1.2 V LVCMOS ³	1.2	0.55
1.2 V LVCMOS ³ – Schmitt Trigger	1.2	0.47
1.2 V LVCMOS Wide Range ³	1.2	0.55
1.2 V LVCMOS Wide Range ³ – Schmitt Trigger	1.2	0.47

Notes:

1. PAC9 is the total dynamic power measured on VCCI.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
3. Applicable for IGLOO PLUS V2 devices only, operating at VCCI ≥ VCC.

Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings¹

	C _{LOAD} (pF)	VCCI (V)	Dynamic Power PAC10 (μW/MHz) ²
Single-Ended			
3.3 V LVTTTL / 3.3 V LVCMOS	5	3.3	127.11
3.3 V LVCMOS Wide Range ³	5	3.3	127.11
2.5 V LVCMOS	5	2.5	70.71
1.8 V LVCMOS	5	1.8	35.57
1.5 V LVCMOS (JESD8-11)	5	1.5	24.30
1.2 V LVCMOS ⁴	5	1.2	15.22
1.2 V LVCMOS Wide Range ⁴	5	1.2	15.22

Notes:

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.
2. PAC10 is the total dynamic power measured on VCCI.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
4. Applicable for IGLOO PLUS V2 devices only, operating at VCCI ≥ VCC.

Power Consumption of Various Internal Resources

Table 2-15 • Different Components Contributing to Dynamic Power Consumption in IGLOO PLUS Devices For IGLOO PLUS V2 or V5 Devices, 1.5 V Core Supply Voltage

Parameter	Definition	Device Specific Dynamic Power (μW/MHz)		
		AGLP125	AGLP060	AGLP030
PAC1	Clock contribution of a Global Rib	11.03	9.3	9.3
PAC2	Clock contribution of a Global Spine	0.81	0.81	0.41
PAC3	Clock contribution of a VersaTile row	0.81		
PAC4	Clock contribution of a VersaTile used as a sequential module	0.11		
PAC5	First contribution of a VersaTile used as a sequential module	0.057		
PAC6	Second contribution of a VersaTile used as a sequential module	0.207		
PAC7	Contribution of a VersaTile used as a combinatorial module	0.17		
PAC8	Average contribution of a routing net	0.7		
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-13 on page 2-9 .		
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-14 on page 2-9 .		
PAC11	Average contribution of a RAM block during a read operation	25.00		
PAC12	Average contribution of a RAM block during a write operation	30.00		
PAC13	Dynamic contribution for PLL	2.70		

Table 2-16 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices For IGLOO PLUS V2 or V5 Devices, 1.5 V Core Supply Voltage

Parameter	Definition	Device-Specific Static Power (mW)		
		AGLP125	AGLP060	AGLP030
PDC1	Array static power in Active mode	See Table 2-12 on page 2-8		
PDC2	Array static power in Static (Idle) mode	See Table 2-11 on page 2-8		
PDC3	Array static power in Flash*Freeze mode	See Table 2-9 on page 2-7		
PDC4	Static PLL contribution	1.84 ¹		
PDC5	Bank quiescent power (VCCI-dependent)	See Table 2-12 on page 2-8		

Notes:

1. This is the minimum contribution of the PLL when operating at lowest frequency.
2. For a different output load, drive strength, or slew rate, Actel recommends using the Actel power spreadsheet calculator or the SmartPower tool in Actel Libero[®] Integrated Design Environment (IDE) software.

Table 2-17 • Different Components Contributing to Dynamic Power Consumption in IGLOO PLUS Devices For IGLOO PLUS V2 Devices, 1.2 V Core Supply Voltage

Parameter	Definition	Device-Specific Dynamic Power (μW/MHz)		
		AGLP125	AGLP060	AGLP030
PAC1	Clock contribution of a Global Rib	7.07	5.96	5.96
PAC2	Clock contribution of a Global Spine	0.52	0.52	0.26
PAC3	Clock contribution of a VersaTile row	0.52		
PAC4	Clock contribution of a VersaTile used as a sequential module	0.07		
PAC5	First contribution of a VersaTile used as a sequential module	0.045		
PAC6	Second contribution of a VersaTile used as a sequential module	0.186		
PAC7	Contribution of a VersaTile used as a combinatorial module	0.11		
PAC8	Average contribution of a routing net	0.45		
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-13 on page 2-9		
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-14 on page 2-9		
PAC11	Average contribution of a RAM block during a read operation	25.00		
PAC12	Average contribution of a RAM block during a write operation	30.00		
PAC13	Dynamic contribution for PLL	2.10		

Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLoo PLUS Devices For IGLoo PLUS V2 Devices, 1.2 V Core Supply Voltage

Parameter	Definition	Device-Specific Static Power (mW)		
		AGLP125	AGLP060	AGLP030
PDC1	Array static power in Active mode	See Table 2-12 on page 2-8		
PDC2	Array static power in Static (Idle) mode	See Table 2-11 on page 2-8		
PDC3	Array static power in Flash*Freeze mode	See Table 2-9 on page 2-7		
PDC4	Static PLL contribution	0.90 ¹		
PDC5	Bank quiescent power (VCCI-dependent)	See Table 2-12 on page 2-8		

Notes:

1. This is the minimum contribution of the PLL when operating at lowest frequency.
2. For a different output load, drive strength, or slew rate, Actel recommends using the Actel power spreadsheet calculator or the SmartPower tool in Actel Libero IDE software.

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Actel Libero IDE software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-19 on page 2-14.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-20 on page 2-14.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-20 on page 2-14. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption— P_{TOTAL}

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption— P_{STAT}

$$P_{STAT} = (P_{DC1} \text{ or } P_{DC2} \text{ or } P_{DC3}) + N_{BANKS} * P_{DC5}$$

N_{BANKS} is the number of I/O banks powered in the design.

Total Dynamic Power Consumption— P_{DYN}

$$P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$$

Global Clock Contribution— P_{CLOCK}

$$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * P_{AC3} + N_{S-CELL} * P_{AC4}) * F_{CLK}$$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in Table 2-19 on page 2-14.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in Table 2-19 on page 2-14.

F_{CLK} is the global clock signal frequency.

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

P_{AC1} , P_{AC2} , P_{AC3} , and P_{AC4} are device-dependent.

Sequential Cells Contribution— P_{S-CELL}

$$P_{S-CELL} = N_{S-CELL} * (P_{AC5} + \alpha_1 / 2 * P_{AC6}) * F_{CLK}$$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-19 on page 2-14](#).

F_{CLK} is the global clock signal frequency.

Combinatorial Cells Contribution— P_{C-CELL}

$$P_{C-CELL} = N_{C-CELL} * \alpha_1 / 2 * P_{AC7} * F_{CLK}$$

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-19 on page 2-14](#).

F_{CLK} is the global clock signal frequency.

Routing Net Contribution— P_{NET}

$$P_{NET} = (N_{S-CELL} + N_{C-CELL}) * \alpha_1 / 2 * P_{AC8} * F_{CLK}$$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-19 on page 2-14](#).

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution— P_{INPUTS}

$$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 2-19 on page 2-14](#).

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution— $P_{OUTPUTS}$

$$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * P_{AC10} * F_{CLK}$$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 2-19 on page 2-14](#).

β_1 is the I/O buffer enable rate—guidelines are provided in [Table 2-20 on page 2-14](#).

F_{CLK} is the global clock signal frequency.

RAM Contribution— P_{MEMORY}

$$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ-CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE-CLOCK} * \beta_3$$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ-CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE-CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in [Table 2-20 on page 2-14](#).

PLL Contribution— P_{PLL}

$$P_{PLL} = P_{DC4} + P_{AC13} * F_{CLKOUT}$$

F_{CLKOUT} is the output clock frequency.¹

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
 - Bit 0 (LSB) = 100%
 - Bit 1 = 50%
 - Bit 2 = 25%
 - ...
 - Bit 7 (MSB) = 0.78125%
 - Average toggle rate = $(100\% + 50\% + 25\% + 12.5\% + \dots + 0.78125\%) / 8$

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-19 • Toggle Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 2-20 • Enable Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

1. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC13} * F_{CLKOUT}$ product) to the total PLL contribution.

User I/O Characteristics

Timing Model

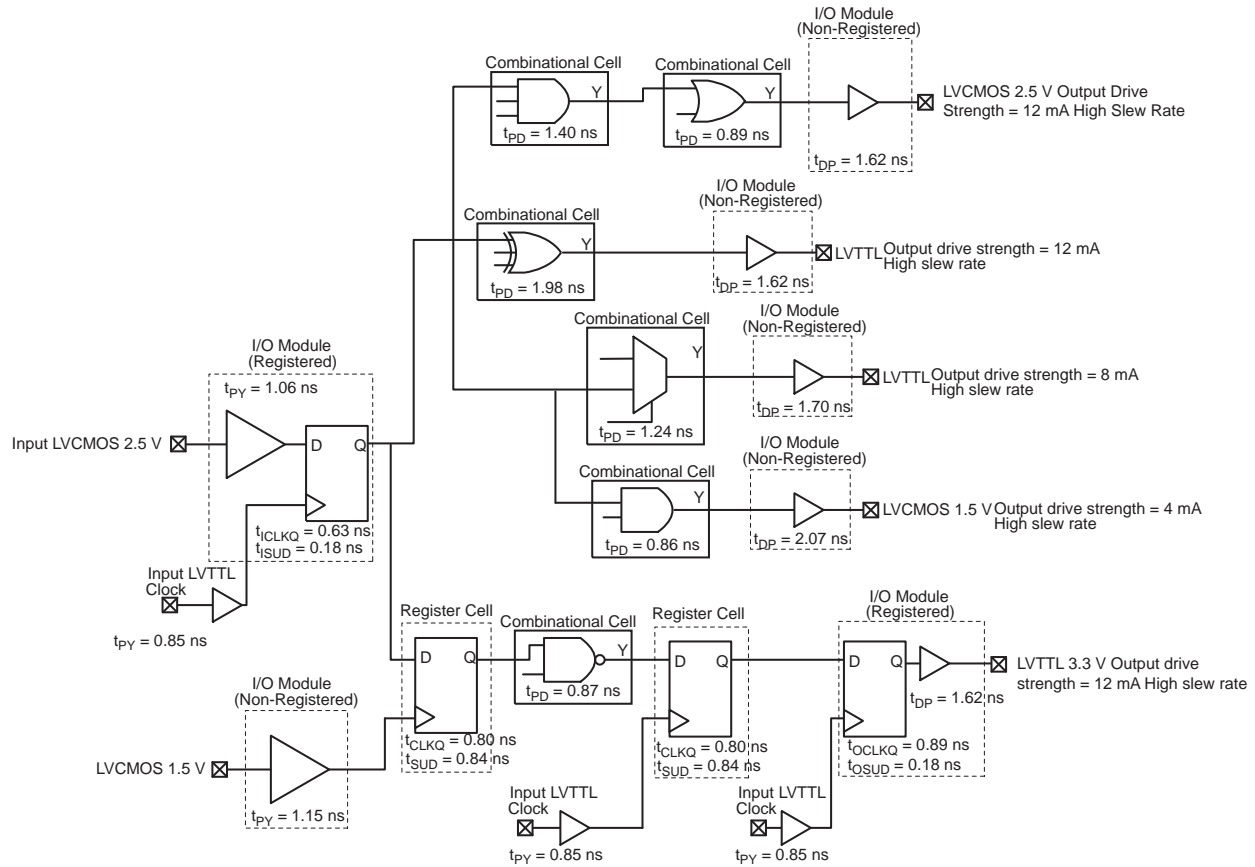


Figure 2-3 • Timing Model

Operating Conditions: STD Speed, Commercial Temperature Range ($T_J = 70^\circ\text{C}$), Worst-Case $V_{CC} = 1.425$ V, for DC 1.5 V Core Voltage, Applicable to V2 and V5 Devices

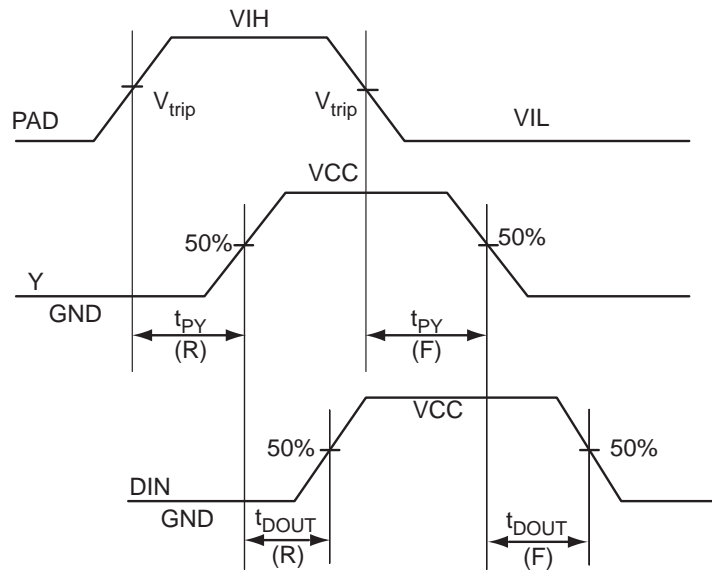
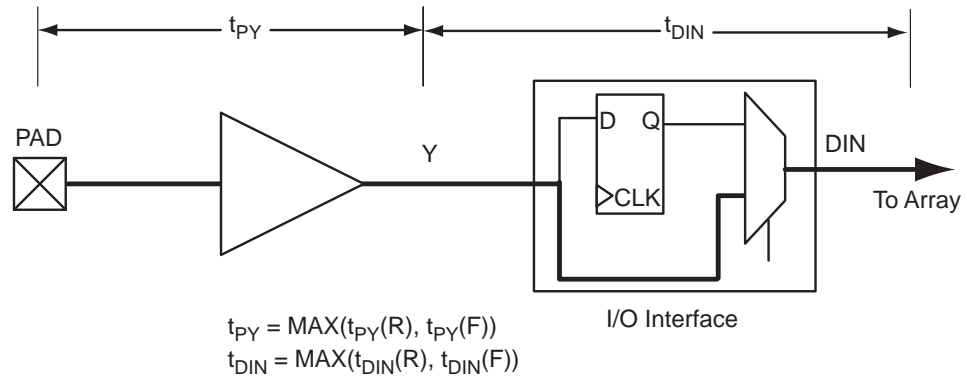


Figure 2-4 • Input Buffer Timing Model and Delays (example)

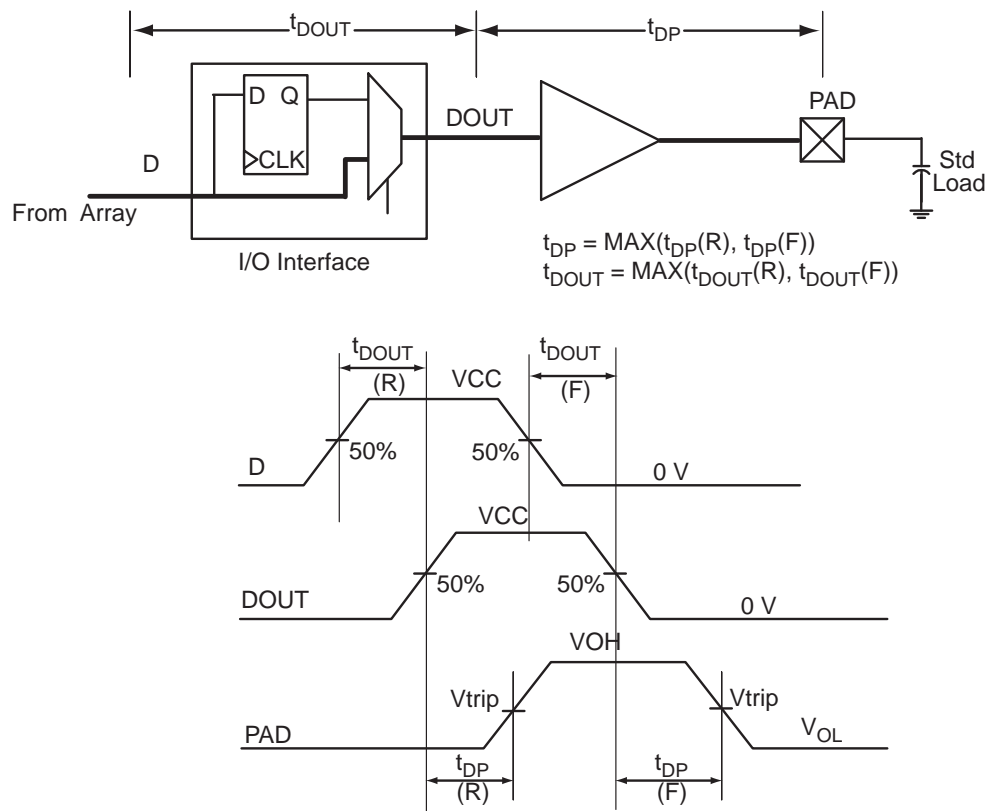


Figure 2-5 • Output Buffer Model and Delays (example)

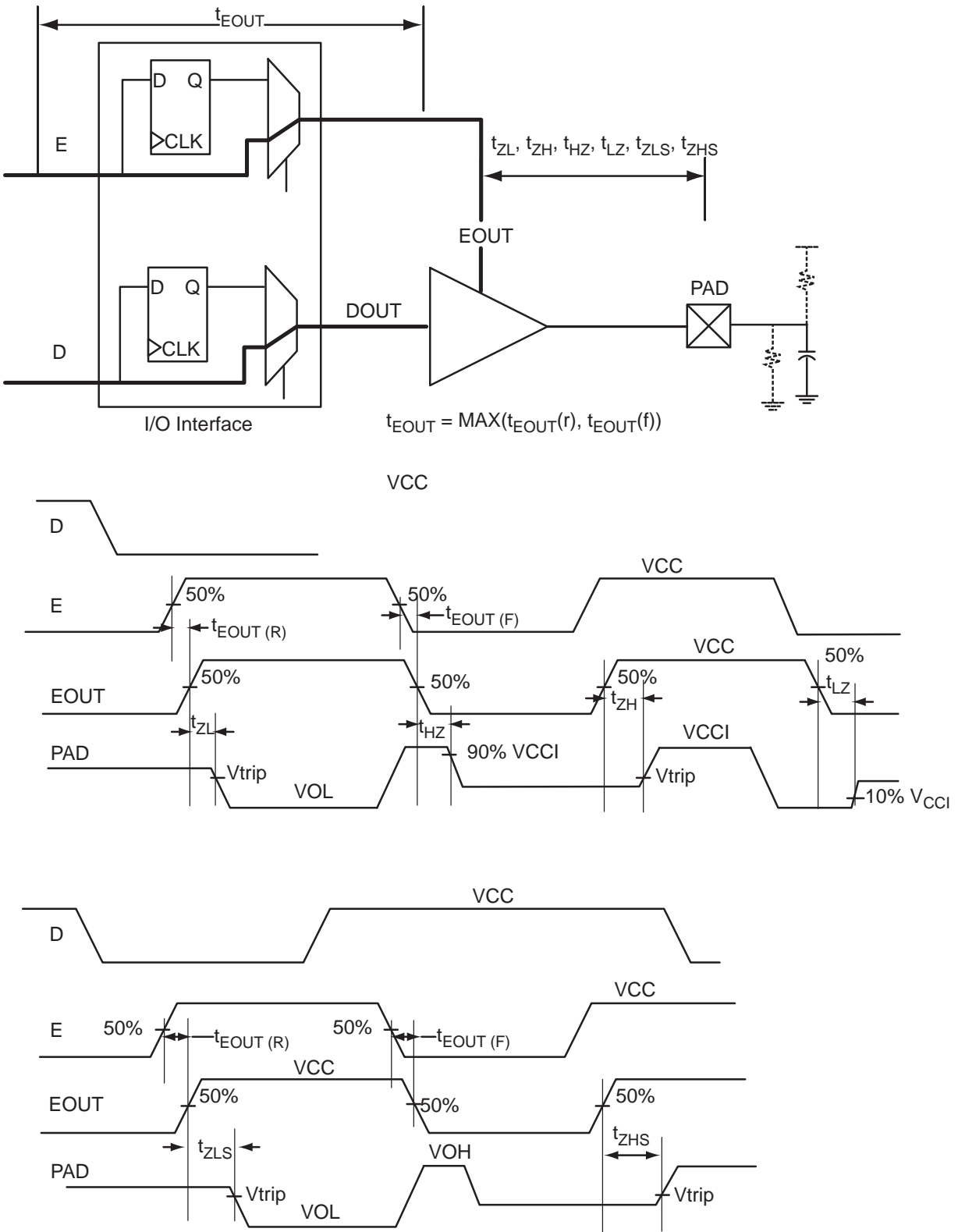


Figure 2-6 • Tristate Output Buffer Timing Model and Delays (example)

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option ²	Slew Rate	VIL		VIH		VOL	VOH	I _{OL} ¹	I _{OH} ¹
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12 mA	High	-0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range ³	100 µA	12 mA	High	-0.3	0.8	2	3.6	0.2	VDD 3 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12 mA	High	-0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	8 mA	8 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI - 0.45	8	8
1.5 V LVCMOS	4 mA	4 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	4	4
1.2 V LVCMOS ⁴	2 mA	2 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2
1.2 V LVCMOS Wide Range ^{4,5}	100 µA	2 mA	High	-0.3	0.3 * VCCI	0.7 * VCCI	3.6	0.1	VCCI - 0.1	0.1	0.1

Notes:

1. Currents are measured at 85°C junction temperature.
2. Note that 1.2 V LVCMOS and 3.3 V LVCMOS wide range are applicable to 100 µA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
4. Applicable to IGLOO PLUS V2 devices operating at $V_{CCI} \geq V_{CC}$.
5. All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.

**Table 2-22 • Summary of Maximum and Minimum DC Input Levels
Applicable to Commercial and Industrial Conditions**

DC I/O Standards	Commercial ¹		Industrial ²	
	IIL ³	IIH ⁴	IIL ³	IIH ⁴
	μA	μA	μA	μA
3.3 V LVTTTL / 3.3 V LVCMOS	10	10	15	15
3.3 V LVCMOS Wide Range	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
1.2 V LVCMOS ⁵	10	10	15	15
1.2 V LVCMOS Wide Range ⁵	10	10	15	15

Notes:

1. Commercial range ($0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$)
2. Industrial range ($-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$)
3. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
4. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
5. Applicable to IGLOO PLUS V2 devices operating at $V_{CCI} \geq V_{CC}$.

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-23 • Summary of AC Measuring Points

Standard	Measuring Trip Point (Vtrip)
3.3 V LVTTTL / 3.3 V LVCMOS	1.4 V
3.3 V LVCMOS Wide Range	1.4 V
2.5 V LVCMOS	1.2 V
1.8 V LVCMOS	0.90 V
1.5 V LVCMOS	0.75 V
1.2 V LVCMOS	0.60 V
1.2 V LVCMOS Wide Range	0.60 V

Table 2-24 • I/O AC Parameter Definitions

Parameter	Parameter Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{HZ}	Enable to Pad delay through the Output Buffer—High to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to High
t_{LZ}	Enable to Pad delay through the Output Buffer—Low to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to Low
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to High
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to Low

Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade, Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option ¹	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12 mA	High	5 pF	–	0.97	1.76	0.18	0.85	1.15	0.66	1.80	1.39	2.20	2.64	ns
3.3 V LVCMOS Wide Range ²	100 μA	12 mA	High	5 pF	–	0.97	2.47	0.18	1.18	1.64	0.66	2.48	1.91	3.16	3.76	ns
2.5 V LVCMOS	12 mA	12 mA	High	5 pF	–	0.97	1.77	0.18	1.06	1.22	0.66	1.81	1.51	2.22	2.56	ns
1.8 V LVCMOS	8 mA	8 mA	High	5 pF	–	0.97	2.00	0.18	1.00	1.43	0.66	2.04	1.76	2.29	2.55	ns
1.5 V LVCMOS	4 mA	4 mA	High	5 pF	–	0.97	2.29	0.18	1.16	1.62	0.66	2.33	2.00	2.37	2.57	ns

Notes:

1. Note that 3.3 V LVCMOS wide range is applicable to 100 μA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option ¹	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12 mA	High	5 pF	–	0.98	2.31	0.19	0.99	1.37	0.67	2.34	1.86	2.65	3.38	ns
3.3 V LVCMOS Wide Range ²	100 μA	12 mA	High	5 pF	–	0.98	3.21	0.19	1.32	1.92	0.67	3.21	2.52	3.73	4.73	ns
2.5 V LVCMOS	12 mA	12 mA	High	5 pF	–	0.98	2.29	0.19	1.19	1.40	0.67	2.32	1.94	2.65	3.27	ns
1.8 V LVCMOS	8 mA	8 mA	High	5 pF	–	0.98	2.45	0.19	1.12	1.61	0.67	2.48	2.16	2.71	3.16	ns
1.5 V LVCMOS	4 mA	4 mA	High	5 pF	–	0.98	2.71	0.19	1.26	1.80	0.67	2.75	2.39	2.78	3.15	ns
1.2 V LVCMOS	2 mA	2 mA	High	5 pF	–	0.98	3.38	0.19	1.57	2.34	0.67	3.26	2.78	2.99	3.24	ns
1.2 V LVCMOS Wide Range ³	100 μA	2 mA	High	5 pF	–	0.98	3.38	0.19	1.57	2.34	0.67	3.26	2.78	2.99	3.24	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\ \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
3. All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.
4. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Detailed I/O DC Characteristics

Table 2-27 • Input Capacitance

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	$V_{IN} = 0, f = 1.0 \text{ MHz}$		8	pF
C_{INCLK}	Input capacitance on the clock pin	$V_{IN} = 0, f = 1.0 \text{ MHz}$		8	pF

Table 2-28 • I/O Output Buffer Maximum Resistances ¹

Standard	Drive Strength	$R_{PULL-DOWN}$ (Ω) ²	$R_{PULL-UP}$ (Ω) ³
3.3 V LVTTTL / 3.3V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	25	75
3.3 V LVCMOS Wide Range	100 μ A	Same as equivalent software default drive	
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
1.2 V LVCMOS	2 mA	157.5	163.8
1.2 V LVCMOS Wide Range ⁴	100 μ A	157.5	163.8

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI} , drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS model on the Actel website at <http://www.actel.com/download/ibis/default.aspx>.
2. $R_{(PULL-DOWN-MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$
4. Applicable to IGLOO PLUS V2 devices operating at $V_{CCI} \geq V_{CC}$.

Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

VCCI	$R_{(WEAK\ PULL-UP)}^1$ (Ω)		$R_{(WEAK\ PULL-DOWN)}^2$ (Ω)	
	Min.	Max.	Min.	Max.
3.3 V	10 K	45 K	10 K	45 K
3.3 V (wide range I/Os)	10 K	45 K	10 K	45 K
2.5 V	11 K	55 K	12 K	74 K
1.8 V	18 K	70 K	17 K	110 K
1.5 V	19 K	90 K	19 K	140 K
1.2 V	25 K	110 K	25 K	150 K
1.2 V (wide range I/Os)	19 K	110 K	19 K	150 K

Notes:

- $R_{(WEAK\ PULL-UP-MAX)} = (VCCImax - VOHspec) / I_{(WEAK\ PULL-UP-MIN)}$
- $R_{(WEAK\ PULLDOWN-MAX)} = (VOLspec) / I_{(WEAK\ PULLDOWN-MIN)}$

Table 2-30 • I/O Short Currents I_{OSH}/I_{OSL}

	Drive Strength	I_{OSL} (mA)*	I_{OSH} (mA)*
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	109	103
3.3 V LVCMOS Wide Range	100 μ A	Same as equivalent software default drive	
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
	12 mA	74	65
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	44	35
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
1.2 V LVCMOS	2 mA	26	20
1.2 V LVCMOS Wide Range	100 μ A	26	20

 * $T_J = 100^\circ\text{C}$

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-31 • Duration of Short Circuit Event before Failure

Temperature	Time before Failure
-40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months

Table 2-32 • Schmitt Trigger Input Hysteresis Hysteresis Voltage Value (Typ.) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typ.)
3.3 V LVTTTL/LVCMOS (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV
1.2 V LVCMOS (Schmitt trigger mode)	40 mV

Table 2-33 • I/O Input Rise Time, Fall Time, and Related I/O Reliability

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTTL/LVCMOS (Schmitt trigger disabled)	No requirement	10 ns *	20 years (100°C)
LVTTTL/LVCMOS (Schmitt trigger enabled)	No requirement	No requirement, but input noise voltage cannot exceed Schmitt hysteresis.	20 years (100°C)

* The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Actel recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.

Single-Ended I/O Characteristics

3.3 V LVTTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTTL input buffer and push-pull output buffer.

Table 2-34 • Minimum and Maximum DC Input and Output Levels

3.3 V LVTTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IO _L	IO _H	I _{OSL}	I _{OSH}	I _{IL} ¹	I _{IH} ²
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	-0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	-0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	-0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10
12 mA	-0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	10	10
16 mA	-0.3	0.8	2	3.6	0.4	2.4	16	16	103	109	10	10

Notes:

1. I_{IL} is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. I_{IH} is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

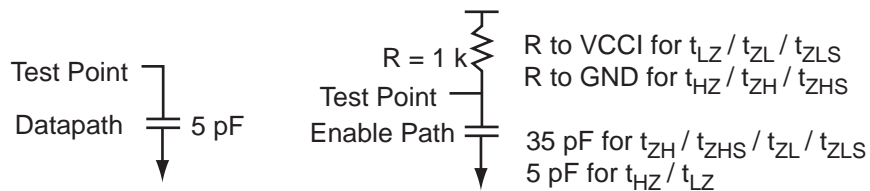


Figure 2-7 • AC Loading

Table 2-35 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	3.3	1.4	5

* Measuring point = V_{trip} . See Table 2-23 on page 2-21 for a complete table of trip points.

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-36 • 3.3 V LVTTTL / 3.3 V LVC MOS Low Slew – Applies to 1.5 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
4 mA	STD	0.97	3.94	0.18	0.85	1.15	0.66	4.02	3.46	1.82	1.87	ns
6 mA	STD	0.97	3.20	0.18	0.85	1.15	0.66	3.27	2.94	2.04	2.27	ns
8 mA	STD	0.97	3.20	0.18	0.85	1.15	0.66	3.27	2.94	2.04	2.27	ns
12 mA	STD	0.97	2.72	0.18	0.85	1.15	0.66	2.78	2.57	2.20	2.53	ns
16 mA	STD	0.97	2.72	0.18	0.85	1.15	0.66	2.78	2.57	2.20	2.53	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-37 • 3.3 V LVTTTL / 3.3 V LVC MOS High Slew – Applies to 1.5 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
4 mA	STD	0.97	2.36	0.18	0.85	1.15	0.66	2.41	1.90	1.82	1.98	ns
6 mA	STD	0.97	1.96	0.18	0.85	1.15	0.66	2.01	1.56	2.04	2.38	ns
8 mA	STD	0.97	1.96	0.18	0.85	1.15	0.66	2.01	1.56	2.04	2.38	ns
12 mA	STD	0.97	1.76	0.18	0.85	1.15	0.66	1.80	1.39	2.20	2.64	ns
16 mA	STD	0.97	1.76	0.18	0.85	1.15	0.66	1.80	1.39	2.20	2.64	ns

Notes:

- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.
- Software default selection highlighted in gray.

Applies to 1.2 V DC Core Voltage

Table 2-38 • 3.3 V LVTTTL / 3.3 V LVC MOS Low Slew – Applies to 1.2 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
4 mA	STD	0.98	4.56	0.19	0.99	1.37	0.67	4.63	3.98	2.26	2.57	ns
6 mA	STD	0.98	3.80	0.19	0.99	1.37	0.67	3.96	3.45	2.49	2.98	ns
8 mA	STD	0.98	3.80	0.19	0.99	1.37	0.67	3.86	3.45	2.49	2.98	ns
12 mA	STD	0.98	3.31	0.19	0.99	1.37	0.67	3.36	3.07	2.65	3.25	ns
16 mA	STD	0.98	3.31	0.19	0.99	1.37	0.67	3.36	3.07	2.65	3.25	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-39 • 3.3 V LVTTTL / 3.3 V LVC MOS High Slew – Applies to 1.2 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
4 mA	STD	0.98	2.92	0.19	0.99	1.37	0.67	2.97	2.38	2.25	2.70	ns
6 mA	STD	0.98	2.52	0.19	0.99	1.37	0.67	2.56	2.03	2.49	3.11	ns
8 mA	STD	0.98	2.52	0.19	0.99	1.37	0.67	2.56	2.03	2.49	3.11	ns
12 mA	STD	0.98	2.31	0.19	0.99	1.37	0.67	2.34	1.86	2.65	3.38	ns
16 mA	STD	0.98	2.31	0.19	0.99	1.37	0.67	2.34	1.86	2.65	3.38	ns

Notes:

- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.
- Software default selection highlighted in gray.

3.3 V LVCMOS Wide Range

Table 2-40 • Minimum and Maximum DC Input and Output Levels

3.3 V LVCMOS Wide Range	Equivalent Software Default Drive Strength Option ¹	VIL		VIH		VOL	VOH	I _{OL}	I _{OH}	I _{OSL}	I _{OSH}	I _{IL} ²	I _{IH} ³
		Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	μA	μA	Max. μA ⁴	Max. μA ⁴	μA ⁵	μA ⁵
100 μA	2 mA	-0.3	0.8	2	3.6	0.2	VDD - 0.2	100	100	25	27	10	10
100 μA	4 mA	-0.3	0.8	2	3.6	0.4	VDD - 0.2	100	100	25	27	10	10
100 μA	6 mA	-0.3	0.8	2	3.6	0.4	VDD - 0.2	100	100	51	54	10	10
100 μA	8 mA	-0.3	0.8	2	3.6	0.4	VDD - 0.2	100	100	51	54	10	10
100 μA	12 mA	-0.3	0.8	2	3.6	0.4	VDD - 0.2	100	100	103	109	10	10
100 μA	16 mA	-0.3	0.8	2	3.6	0.4	VDD - 0.2	100	100	103	109	10	10

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 μA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. I_{IL} is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < V_{IN} < VIL.
3. I_{IH} is the input leakage current per I/O pin over recommended operating conditions V_{IH} < V_{IN} < V_{CCI}. Input current is larger when operating outside recommended ranges.
4. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
5. Currents are measured at 85°C junction temperature.
6. Software default selection highlighted in gray.

Table 2-41 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	3.3	1.4	5

* Measuring point = V_{trip}. See [Table 2-23 on page 2-21](#) for a complete table of trip points.

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-42 • 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.5 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.7\text{ V}$

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 μA	4 mA	STD	0.97	5.85	0.18	1.18	1.64	0.66	5.86	5.05	2.57	2.57	ns
100 μA	6 mA	STD	0.97	4.70	0.18	1.18	1.64	0.66	4.72	4.27	2.92	3.19	ns
100 μA	8 mA	STD	0.97	4.70	0.18	1.18	1.64	0.66	4.72	4.27	2.92	3.19	ns
100 μA	12 mA	STD	0.97	3.96	0.18	1.18	1.64	0.66	3.98	3.70	3.16	3.59	ns
100 μA	16 mA	STD	0.97	3.96	0.18	1.18	1.64	0.66	3.98	3.70	3.16	3.59	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\ \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-43 • 3.3 V LVCMOS Wide Range High Slew – Applies to 1.5 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.7\text{ V}$

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 μA	4 mA	STD	0.97	3.39	0.18	1.18	1.64	0.66	3.41	2.69	2.57	2.73	ns
100 μA	6 mA	STD	0.97	2.79	0.18	1.18	1.64	0.66	2.80	2.17	2.92	3.36	ns
100 μA	8 mA	STD	0.97	2.79	0.18	1.18	1.64	0.66	2.80	2.17	2.92	3.36	ns
100 μA	12 mA	STD	0.97	2.47	0.18	1.18	1.64	0.66	2.48	1.91	3.16	3.76	ns
100 μA	16 mA	STD	0.97	2.47	0.18	1.18	1.64	0.66	2.48	1.91	3.16	3.76	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\ \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.
3. Software default selection highlighted in gray.

Applies to 1.2 V DC Core Voltage

Table 2-44 • 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.7\text{ V}$

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 μA	4 mA	STD	0.98	6.68	0.19	1.32	1.92	0.67	6.68	5.74	3.13	3.47	ns
100 μA	6 mA	STD	0.98	5.51	0.19	1.32	1.92	0.67	5.51	4.94	3.48	4.11	ns
100 μA	8 mA	STD	0.98	5.51	0.19	1.32	1.92	0.67	5.51	4.94	3.48	4.11	ns
100 μA	12 mA	STD	0.98	4.75	0.19	1.32	1.92	0.67	4.75	4.36	3.73	4.52	ns
100 μA	16 mA	STD	0.98	4.75	0.19	1.32	1.92	0.67	4.75	4.36	3.73	4.52	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\ \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-45 • 3.3 V LVCMOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.7\text{ V}$

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 μA	4 mA	STD	0.98	4.16	0.19	1.32	1.92	0.67	4.16	3.32	3.12	3.66	ns
100 μA	6 mA	STD	0.98	3.54	0.19	1.32	1.92	0.67	3.54	2.79	3.48	4.31	ns
100 μA	8 mA	STD	0.98	3.54	0.19	1.32	1.92	0.67	3.54	2.79	3.48	4.31	ns
100 μA	12 mA	STD	0.98	3.21	0.19	1.32	1.92	0.67	3.21	2.52	3.73	4.73	ns
100 μA	16 mA	STD	0.98	3.21	0.19	1.32	1.92	0.67	3.21	2.52	3.73	4.73	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\ \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.
3. Software default selection highlighted in gray.

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-46 • Minimum and Maximum DC Input and Output Levels

2.5 V LVCMOS Drive Strength	VIL		VIH		VOL	VOH	I _{OL}	I _{OH}	I _{OSL}	I _{OSH}	I _{IL} ¹	I _{IH} ²
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.7	1.7	3.6	0.7	1.7	2	2	16	18	10	10
4 mA	-0.3	0.7	1.7	3.6	0.7	1.7	4	4	16	18	10	10
6 mA	-0.3	0.7	1.7	3.6	0.7	1.7	6	6	32	37	10	10
8 mA	-0.3	0.7	1.7	3.6	0.7	1.7	8	8	32	37	10	10
12 mA	-0.3	0.7	1.7	3.6	0.7	1.7	12	12	65	74	10	10

Notes:

1. I_{IL} is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. I_{IH} is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

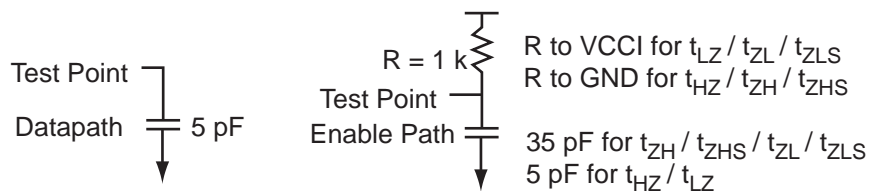


Figure 2-8 • AC Loading

Table 2-47 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	2.5	1.2	5

* Measuring point = V_{trip} . See Table 2-23 on page 2-21 for a complete table of trip points.

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-48 • 2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
4 mA	STD	0.97	4.44	0.18	1.06	1.22	0.66	4.53	4.15	1.80	1.70	ns
6 mA	STD	0.97	3.61	0.18	1.06	1.22	0.66	3.69	3.50	2.05	2.18	ns
8 mA	STD	0.97	3.61	0.18	1.06	1.22	0.66	3.69	3.50	2.05	2.18	ns
12 mA	STD	0.97	3.07	0.18	1.06	1.22	0.66	3.14	3.03	2.22	2.48	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-49 • 2.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
4 mA	STD	0.97	2.41	0.18	1.06	1.22	0.66	2.47	2.22	1.79	1.77	ns
6 mA	STD	0.97	1.99	0.18	1.06	1.22	0.66	2.04	1.75	2.04	2.25	ns
8 mA	STD	0.97	1.99	0.18	1.06	1.22	0.66	2.04	1.75	2.04	2.25	ns
12 mA	STD	0.97	1.77	0.18	1.06	1.22	0.66	1.81	1.51	2.22	2.56	ns

Notes:

- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.
- Software default selection highlighted in gray.

Applies to 1.2 V DC Core Voltage

Table 2-50 • 2.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
4 mA	STD	0.98	5.04	0.19	1.19	1.40	0.67	5.12	4.65	2.22	2.36	ns
6 mA	STD	0.98	4.19	0.19	1.19	1.40	0.67	4.25	3.98	2.48	2.85	ns
8 mA	STD	0.98	4.19	0.19	1.19	1.40	0.67	4.25	3.98	2.48	2.85	ns
12 mA	STD	0.98	3.63	0.19	1.19	1.40	0.67	3.69	3.50	2.66	3.16	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-51 • 2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
4 mA	STD	0.98	2.96	0.19	1.19	1.40	0.67	3.00	2.67	2.22	2.46	ns
6 mA	STD	0.98	2.52	0.19	1.19	1.40	0.67	2.56	2.18	2.47	2.95	ns
8 mA	STD	0.98	2.52	0.19	1.19	1.40	0.67	2.56	2.18	2.47	2.95	ns
12 mA	STD	0.98	2.29	0.19	1.19	1.40	0.67	2.32	1.94	2.65	3.27	ns

Notes:

- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.
- Software default selection highlighted in gray.

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-52 • Minimum and Maximum DC Input and Output Levels

1.8 V LVCMOS	VIL		VIH		VOL	VOH	I _{OL}	I _{OH}	I _{OSL}	I _{OSH}	I _{IL} ¹	I _{IH} ²
	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA ³	Max., mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI - 0.45	2	2	9	11	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI - 0.45	4	4	17	22	10	10
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI - 0.45	6	6	35	44	10	10
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI - 0.45	8	8	35	44	10	10

Notes:

1. I_{IL} is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < V_{IN} < V_{IL}.
2. I_{IH} is the input leakage current per I/O pin over recommended operating conditions V_{IH} < V_{IN} < V_{CCI}. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

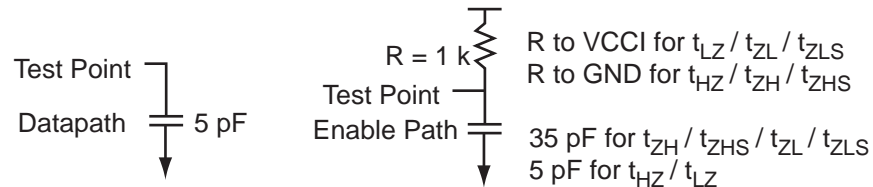


Figure 2-9 • AC Loading

Table 2-53 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	1.8	0.9	5

* Measuring point = V_{trip}. See Table 2-23 on page 2-21 for a complete table of trip points.

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-54 • 1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	5.89	0.18	1.00	1.43	0.66	6.01	5.43	1.78	1.30	ns
4 mA	STD	0.97	4.82	0.18	1.00	1.43	0.66	4.92	4.56	2.08	2.08	ns
6 mA	STD	0.97	4.13	0.18	1.00	1.43	0.66	4.21	3.96	2.30	2.46	ns
8 mA	STD	0.97	4.13	0.18	1.00	1.43	0.66	4.21	3.96	2.30	2.46	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-55 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	2.82	0.18	1.00	1.43	0.66	2.88	2.78	1.78	1.35	ns
4 mA	STD	0.97	2.30	0.18	1.00	1.43	0.66	2.35	2.11	2.08	2.15	ns
6 mA	STD	0.97	2.00	0.18	1.00	1.43	0.66	2.04	1.76	2.29	2.55	ns
8 mA	STD	0.97	2.00	0.18	1.00	1.43	0.66	2.04	1.76	2.29	2.55	ns

Notes:

- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.
- Software default selection highlighted in gray.

Applies to 1.2 V DC Core Voltage

Table 2-56 • 1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.98	6.43	0.19	1.12	1.61	0.67	6.54	5.93	2.19	1.88	ns
4 mA	STD	0.98	5.33	0.19	1.12	1.61	0.67	5.41	5.03	2.50	2.68	ns
6 mA	STD	0.98	4.61	0.19	1.12	1.61	0.67	4.69	4.41	2.72	3.07	ns
8 mA	STD	0.98	4.61	0.19	1.12	1.61	0.67	4.69	4.41	2.72	3.07	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-57 • 1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.98	3.30	0.19	1.12	1.61	0.67	3.34	3.21	2.19	1.93	ns
4 mA	STD	0.98	2.76	0.19	1.12	1.61	0.67	2.79	2.51	2.50	2.76	ns
6 mA	STD	0.98	2.45	0.19	1.12	1.61	0.67	2.48	2.16	2.71	3.16	ns
8 mA	STD	0.98	2.45	0.19	1.12	1.61	0.67	2.48	2.16	2.71	3.16	ns

Notes:

- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.
- Software default selection highlighted in gray.

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-58 • Minimum and Maximum DC Input and Output Levels

1.5 V LVCMOS	VIL		VIH		VOL	VOH	I _{OL}	I _{OH}	I _{OSL}	I _{OSH}	I _{IL} ¹	I _{IH} ²
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.35 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10
4 mA	-0.3	0.35 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	4	4	25	33	10	10

Notes:

1. I_{IL} is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. I_{IH} is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

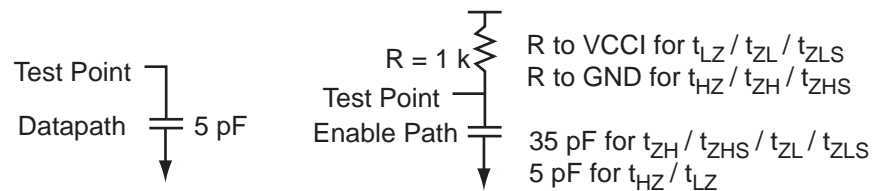


Figure 2-10 • AC Loading

Table 2-59 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	1.5	0.75	5

* Measuring point = V_{trip}. See [Table 2-23 on page 2-21](#) for a complete table of trip points.

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-60 • 1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	6.07	0.18	1.16	1.62	0.66	6.19	5.53	2.13	2.02	ns
4 mA	STD	0.97	5.24	0.18	1.16	1.62	0.66	5.34	4.81	2.37	2.47	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-61 • 1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	2.65	0.18	1.16	1.62	0.66	2.71	2.43	2.13	2.11	ns
4 mA	STD	0.97	2.29	0.18	1.16	1.62	0.66	2.33	2.00	2.37	2.57	ns

Notes:

- For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.
- Software default selection highlighted in gray.

Applies to 1.2 V DC Core Voltage

Table 2-62 • 1.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.98	6.57	0.19	1.26	1.80	0.67	6.68	6.01	2.54	2.59	ns
4 mA	STD	0.98	5.72	0.19	1.26	1.80	0.67	5.81	5.27	2.79	3.05	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-63 • 1.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.98	3.08	0.19	1.26	1.80	0.67	3.13	2.82	2.53	2.68	ns
4 mA	STD	0.98	2.71	0.19	1.26	1.80	0.67	2.75	2.39	2.78	3.15	ns

Notes:

- For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.
- Software default selection highlighted in gray.

1.2 V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer.

Table 2-64 • Minimum and Maximum DC Input and Output Levels

1.2 V LVCMOS ¹	V _{IL}		V _{IH}		V _{OL}	V _{OH}	I _{OL}	I _{OH}	I _{OSL}	I _{OSH}	I _{IL} ²	I _{IH} ³
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ⁴	Max. mA ⁴	μA ⁵	μA ⁵
2 mA	-0.3	0.35 * V _{CCI}	0.65 * V _{CCI}	3.6	0.25 * V _{CCI}	0.75 * V _{CCI}	2	2	20	26	10	10

Notes:

1. Applicable to IGL00 nano V2 devices operating at V_{CCI} ≥ V_{CC}.
2. I_{IL} is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < V_{IN} < V_{IL}.
3. I_{IH} is the input leakage current per I/O pin over recommended operating conditions V_{IH} < V_{IN} < V_{CCI}. Input current is larger when operating outside recommended ranges.
4. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
5. Currents are measured at 85°C junction temperature.
6. Software default selection highlighted in gray.

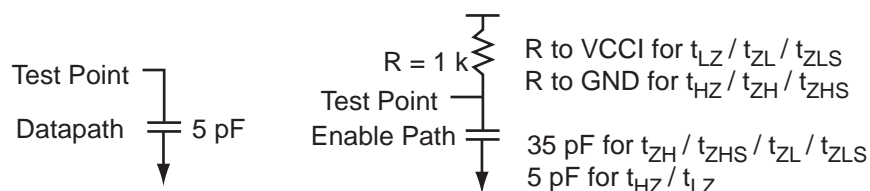


Figure 2-11 • AC Loading

Table 2-65 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	1.2	0.6	5

* Measuring point = V_{trip}. See Table 2-23 on page 2-21 for a complete table of trip points.

Timing Characteristics

Applies to 1.2 V DC Core Voltage

Table 2-66 • 1.2 V LVCMOS Low Slew

Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.14 V

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	Units
2 mA	STD	0.98	8.27	0.19	1.57	2.34	0.67	7.94	6.77	3.00	3.11	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-67 • 1.2 V LVCMOS High Slew

Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.14 V

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	Units
2 mA	STD	0.98	3.38	0.19	1.57	2.34	0.67	3.26	2.78	2.99	3.24	ns

Notes:

1. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.
2. Software default selection highlighted in gray.

1.2 V LVCMOS Wide Range

Table 2-68 • Minimum and Maximum DC Input and Output Levels

1.2 V LVCMOS Wide Range ¹		V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL} ³	I_{IH} ⁴
Drive Strength	Equivalent Software Default Drive Strength Option ²	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ⁵	Max. mA ⁵	μA ⁶	μA ⁶
100 μA	2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	20	26	10	10

Notes:

1. Applicable to V2 devices only.
2. The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is $\pm 100 \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
3. I_{IL} is the input leakage current per I/O pin over recommended operation conditions where $-0.3 \text{ V} < V_{IN} < V_{IL}$.
4. I_{IH} is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
5. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
6. Currents are measured at 85°C junction temperature.
7. Software default selection highlighted in gray.

Table 2-69 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.2	0.6	5

* Measuring point = V_{trip} . See Table 2-23 on page 2-21 for a complete table of trip points.

Timing Characteristics

Applies to 1.2 V DC Core Voltage

Table 2-70 • 1.2 V LVC MOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 1.14\text{ V}$

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 μA	2 mA	STD	0.98	8.27	0.19	1.57	2.34	0.67	7.94	6.77	3.00	3.11	ns

Notes:

1. The minimum drive strength for any LVC MOS 1.2 V software configuration when run in wide range is $\pm 100\ \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-71 • 1.2 V LVC MOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 1.14\text{ V}$

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 μA	2 mA	STD	0.98	3.38	0.19	1.57	2.34	0.67	3.26	2.78	2.99	3.24	ns

Notes:

1. The minimum drive strength for any LVC MOS 1.2 V software configuration when run in wide range is $\pm 100\ \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.
3. Software default selection highlighted in gray.

I/O Register Specifications

Fully Registered I/O Buffers with Asynchronous Preset

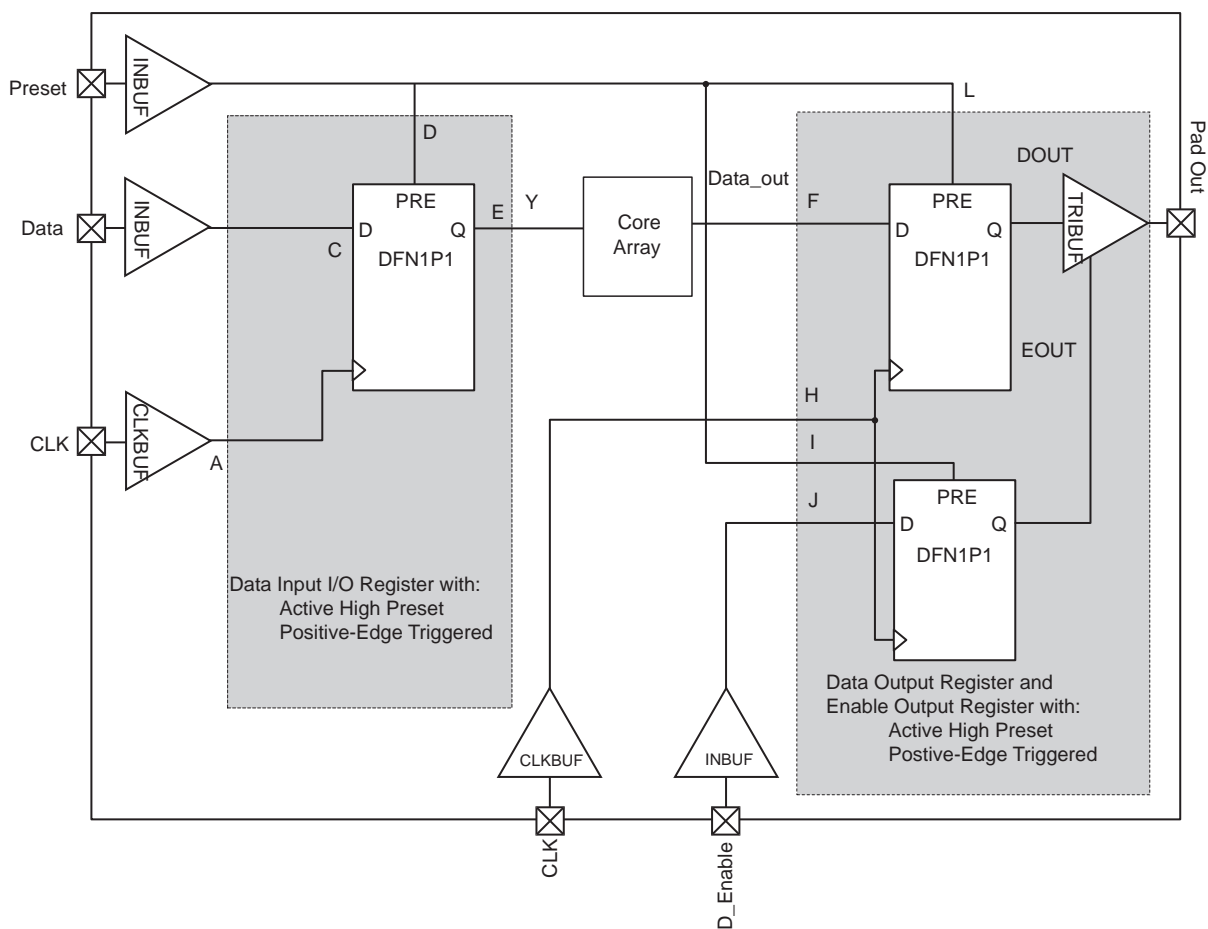


Figure 2-12 • Timing Model of Registered I/O Buffers with Asynchronous Preset

Table 2-72 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t _{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t _{OSUD}	Data Setup Time for the Output Data Register	F, H
t _{OHD}	Data Hold Time for the Output Data Register	F, H
t _{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
t _{OEMPRES}	Asynchronous Preset Removal Time for the Output Data Register	L, H
t _{ORECPRES}	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t _{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t _{OESUD}	Data Setup Time for the Output Enable Register	J, H
t _{OEH}	Data Hold Time for the Output Enable Register	J, H
t _{OEPRE2Q}	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
t _{OEREMPRE}	Asynchronous Preset Removal Time for the Output Enable Register	I, H
t _{OERECPRE}	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t _{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t _{ISUD}	Data Setup Time for the Input Data Register	C, A
t _{IHD}	Data Hold Time for the Input Data Register	C, A
t _{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
t _{IEMPRE}	Asynchronous Preset Removal Time for the Input Data Register	D, A
t _{IRECPRE}	Asynchronous Preset Recovery Time for the Input Data Register	D, A

* See Figure 2-12 on page 2-41 for more information.

Fully Registered I/O Buffers with Asynchronous Clear

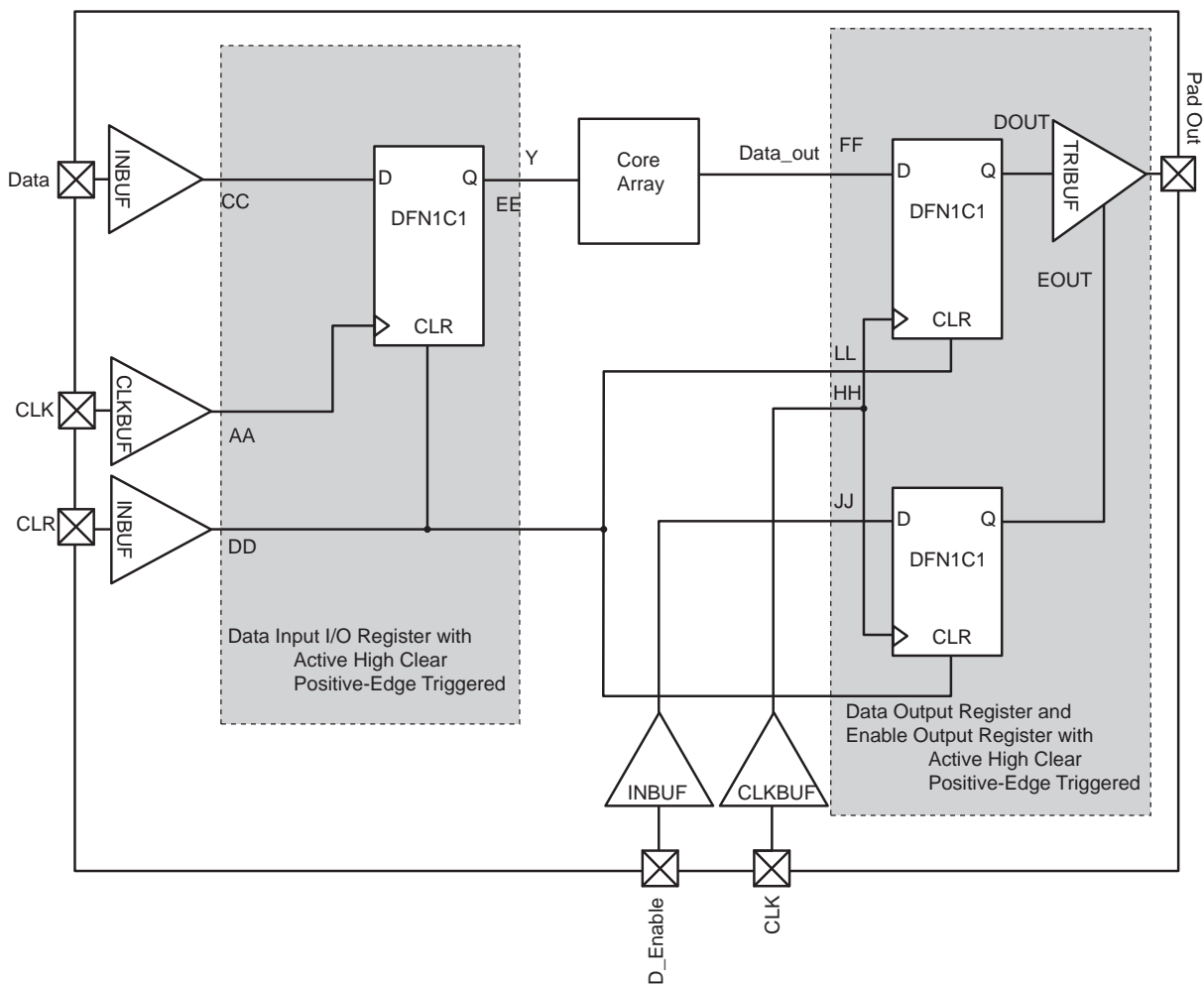


Figure 2-13 • Timing Model of the Registered I/O Buffers with Asynchronous Clear

Table 2-73 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t _{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t _{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t _{OHD}	Data Hold Time for the Output Data Register	FF, HH
t _{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
t _{OEMCLR}	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
t _{OECCLR}	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t _{OCLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t _{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t _{OEH}	Data Hold Time for the Output Enable Register	JJ, HH
t _{OCLR2Q}	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
t _{OEMCLR}	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
t _{OECCLR}	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t _{ICKQ}	Clock-to-Q of the Input Data Register	AA, EE
t _{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t _{IHD}	Data Hold Time for the Input Data Register	CC, AA
t _{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
t _{IEMCLR}	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
t _{IECCLR}	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

* See Figure 2-13 on page 2-43 for more information.

Input Register

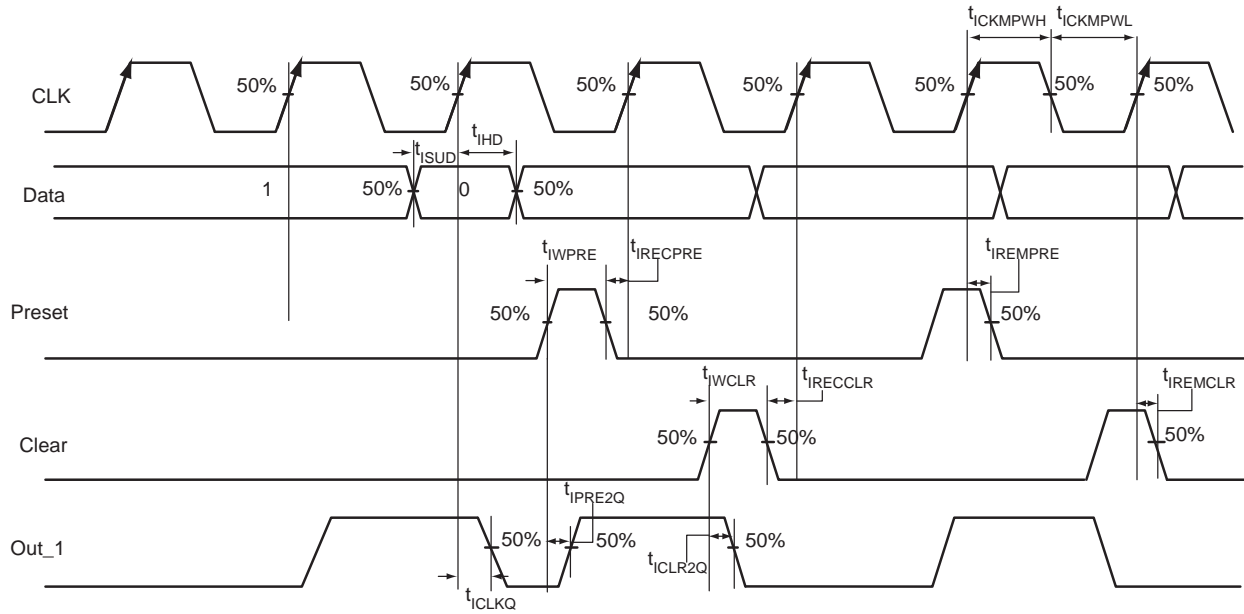


Figure 2-14 • Input Register Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-74 • Input Data Register Propagation Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Input Data Register	0.41	ns
t_{SUD}	Data Setup Time for the Input Data Register	0.32	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.57	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.57	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
t_{ICKMPWH}	Clock Minimum Pulse Width High for the Input Data Register	0.31	ns
t_{ICKMPWL}	Clock Minimum Pulse Width Low for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-75 • Input Data Register Propagation Delays
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{iCLKQ}	Clock-to-Q of the Input Data Register	0.66	ns
t_{iSUD}	Data Setup Time for the Input Data Register	0.43	ns
t_{iHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{iCLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.86	ns
t_{iPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.86	ns
$t_{iREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{iRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{iREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{iRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{iWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{iWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{iCKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.31	ns
$t_{iCKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

Output Register

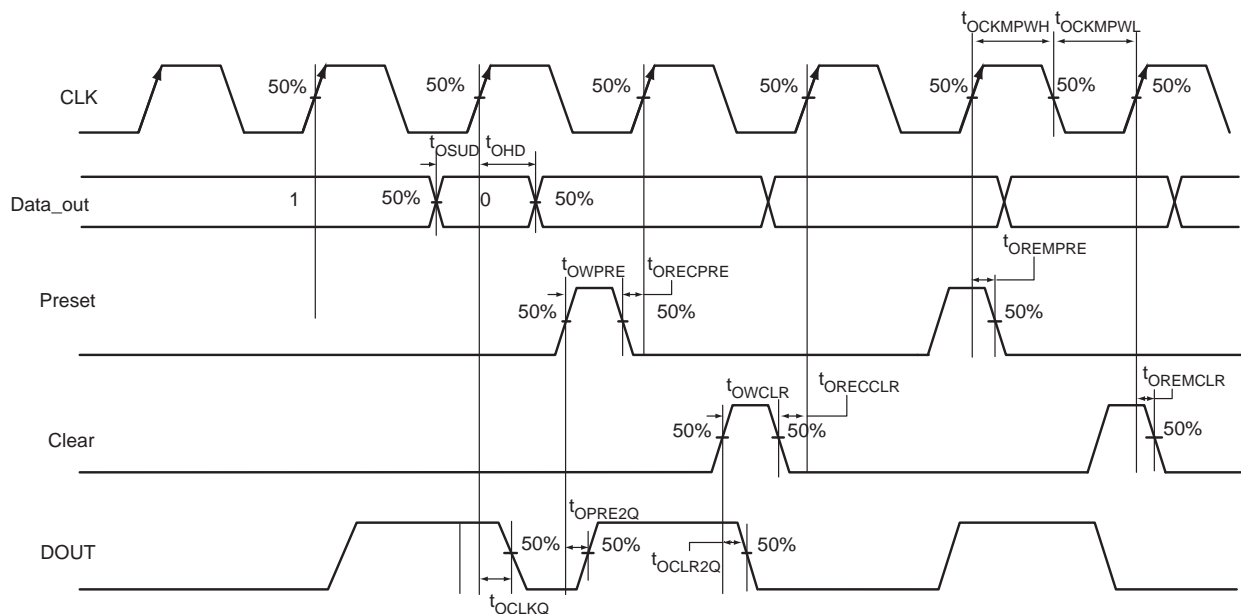


Figure 2-15 • Output Register Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-76 • Output Data Register Propagation Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.66	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.33	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.82	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.88	ns
t_{OEMCLR}	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
t_{OECCLR}	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
t_{OEMPRE}	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
t_{OECPRE}	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OCKMPWH}	Clock Minimum Pulse Width High for the Output Data Register	0.31	ns
t_{OCKMPWL}	Clock Minimum Pulse Width Low for the Output Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-77 • Output Data Register Propagation Delays
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	1.03	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.52	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	1.22	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	1.31	ns
t_{OREMCLR}	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
t_{ORECCLR}	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
t_{OREMPRE}	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
t_{ORECPRE}	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OCKMPWH}	Clock Minimum Pulse Width High for the Output Data Register	0.31	ns
t_{OCKMPWL}	Clock Minimum Pulse Width Low for the Output Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

Output Enable Register

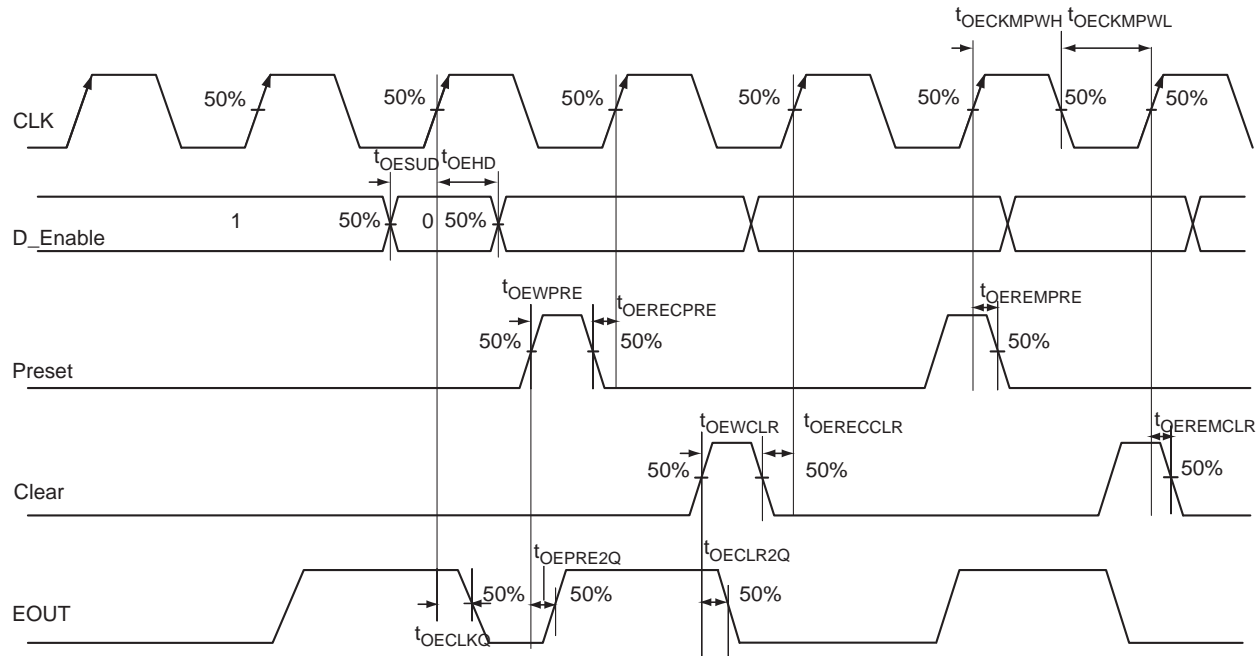


Figure 2-16 • Output Enable Register Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-78 • Output Enable Register Propagation Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.68	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.33	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.84	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.91	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.31	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-79 • Output Enable Register Propagation Delays
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	1.06	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.52	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	1.25	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	1.36	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	ns
$t_{OEWCCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OEWPRES}$	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.31	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The IGLOO PLUS library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/ E Macro Library Guide*.

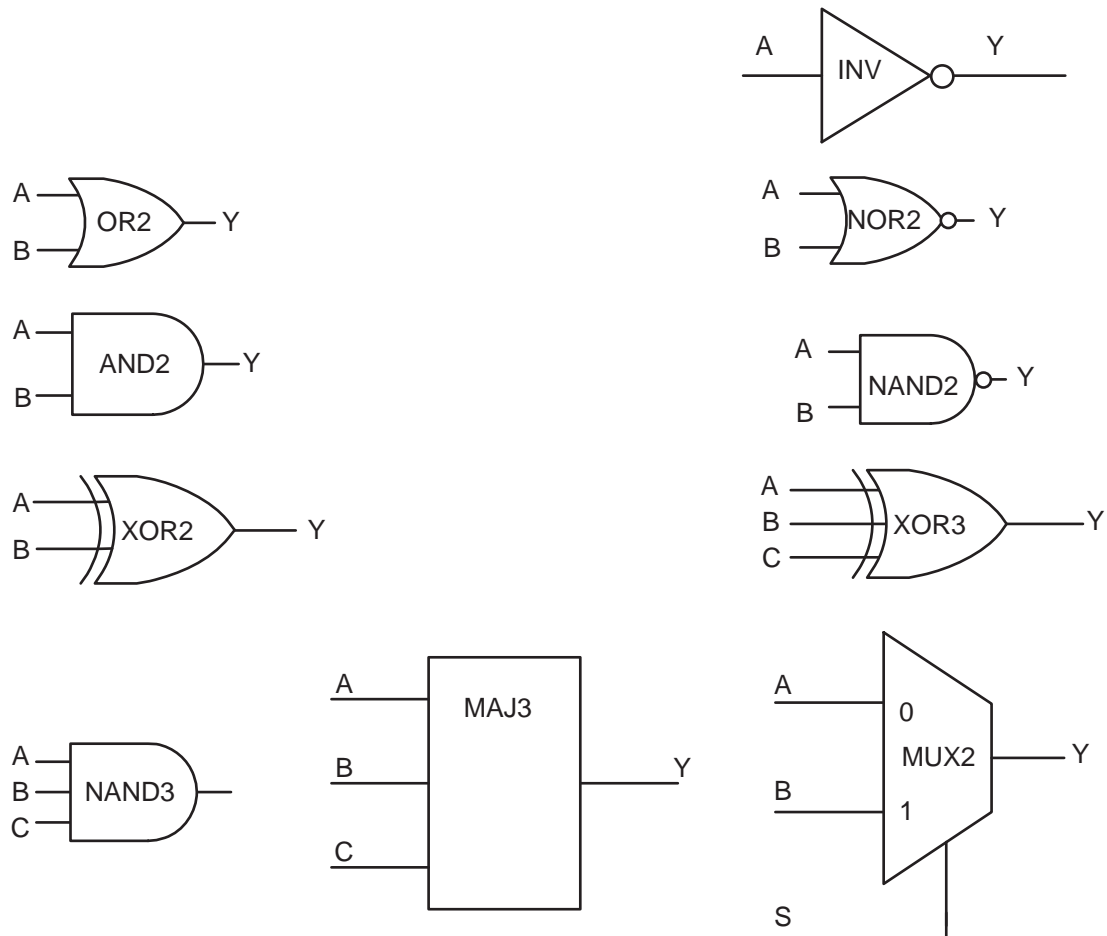


Figure 2-17 • Sample of Combinatorial Cells

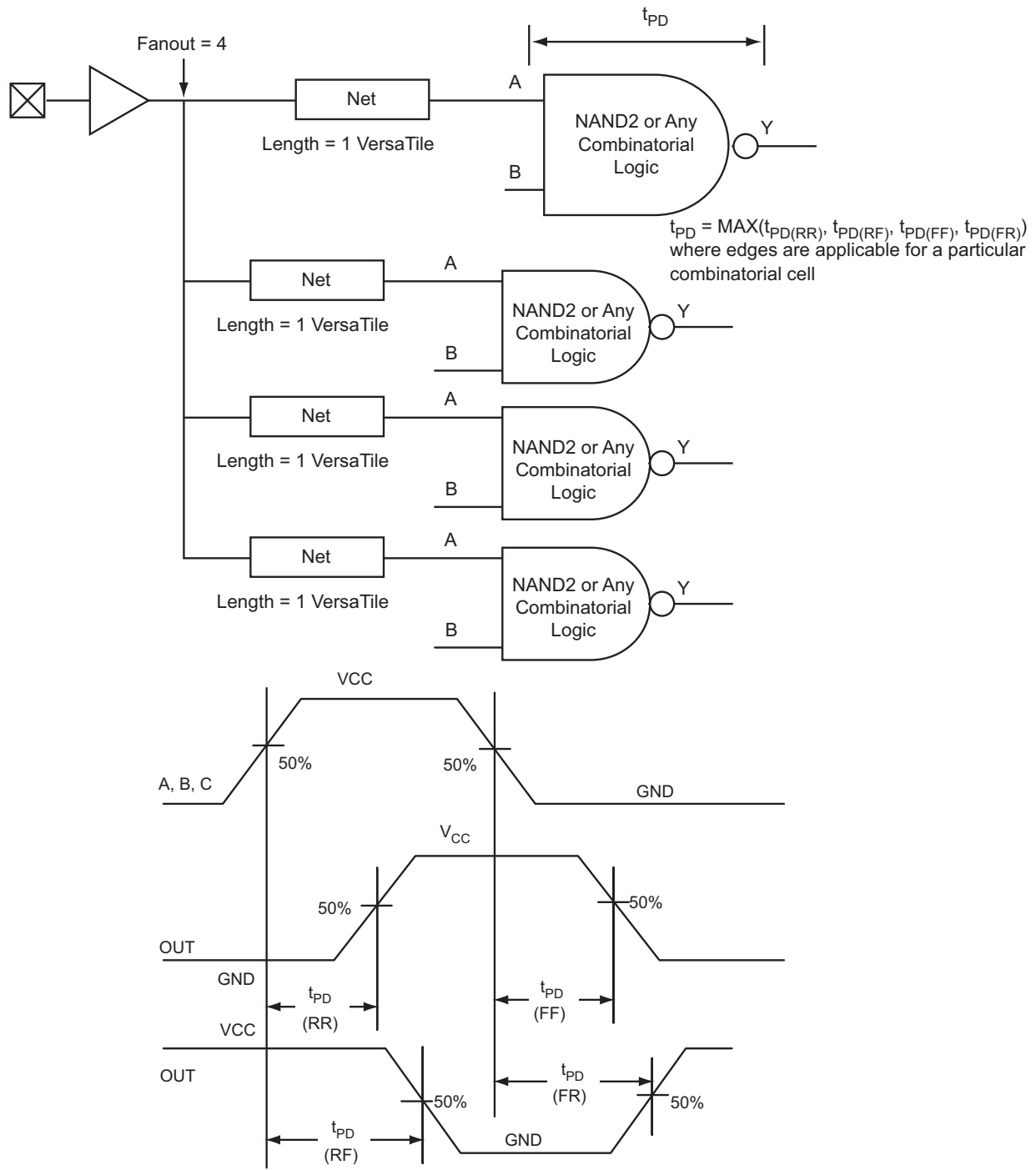


Figure 2-18 • Timing Model and Waveforms

Timing Characteristics

1.5 V DC Core Voltage

Table 2-80 • Combinatorial Cell Propagation Delays

 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	$Y = !A$	t_{PD}	0.72	ns
AND2	$Y = A \cdot B$	t_{PD}	0.86	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	1.00	ns
OR2	$Y = A + B$	t_{PD}	1.26	ns
NOR2	$Y = !(A + B)$	t_{PD}	1.16	ns
XOR2	$Y = A \oplus B$	t_{PD}	1.46	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	t_{PD}	1.47	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	2.12	ns
MUX2	$Y = A !S + B S$	t_{PD}	1.24	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	1.40	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

1.2 V DC Core Voltage

Table 2-81 • Combinatorial Cell Propagation Delays

 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	$Y = !A$	t_{PD}	1.26	ns
AND2	$Y = A \cdot B$	t_{PD}	1.46	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	1.78	ns
OR2	$Y = A + B$	t_{PD}	2.47	ns
NOR2	$Y = !(A + B)$	t_{PD}	2.17	ns
XOR2	$Y = A \oplus B$	t_{PD}	2.62	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	t_{PD}	2.66	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	3.77	ns
MUX2	$Y = A !S + B S$	t_{PD}	2.20	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	2.49	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

VersaTile Specifications as a Sequential Module

The IGLOO PLUS library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/E Macro Library Guide*.

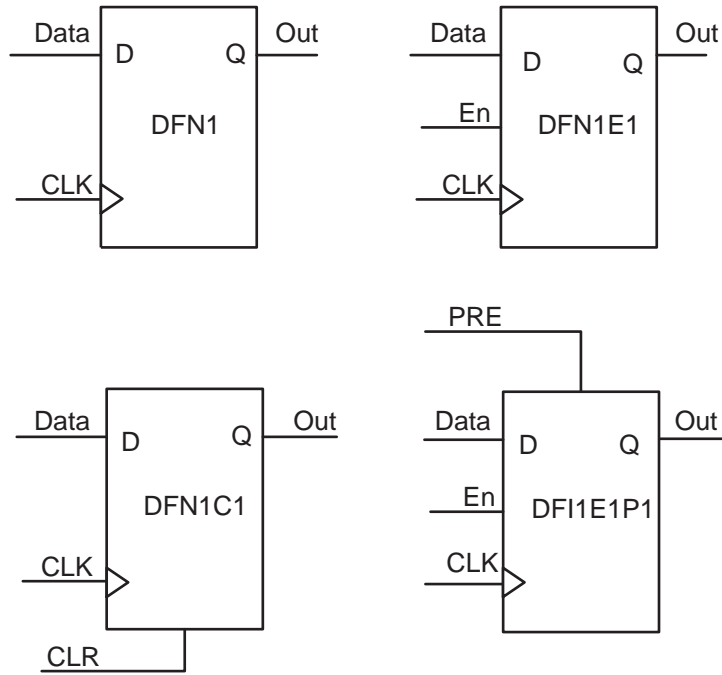
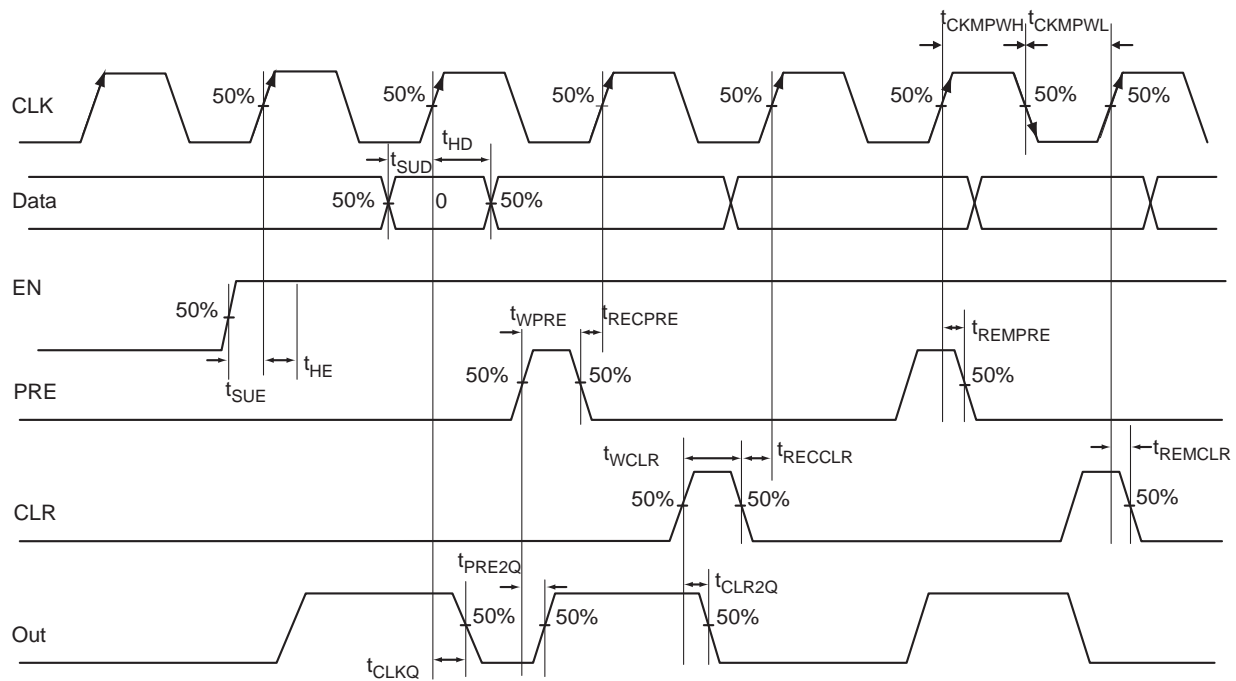


Figure 2-19 • Sample of Sequential Cells


Figure 2-20 • Timing Model and Waveforms

Timing Characteristics

1.5 V DC Core Voltage

Table 2-82 • Register Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.89	ns
t_{SUD}	Data Setup Time for the Core Register	0.81	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.73	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.60	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.62	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.23	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.56	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.56	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

1.2 V DC Core Voltage

Table 2-83 • Register Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	1.61	ns
t_{SUD}	Data Setup Time for the Core Register	1.17	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	1.29	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.87	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.89	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.24	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.46	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.46	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.95	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.95	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

Global Resource Characteristics

AGLP125 Clock Tree Topology

Clock delays are device-specific. Figure 2-21 is an example of a global tree used for clock routing. The global tree presented in Figure 2-21 is driven by a CCC located on the west side of the AGLP125 device. It is used to drive all D-flip-flops in the device.

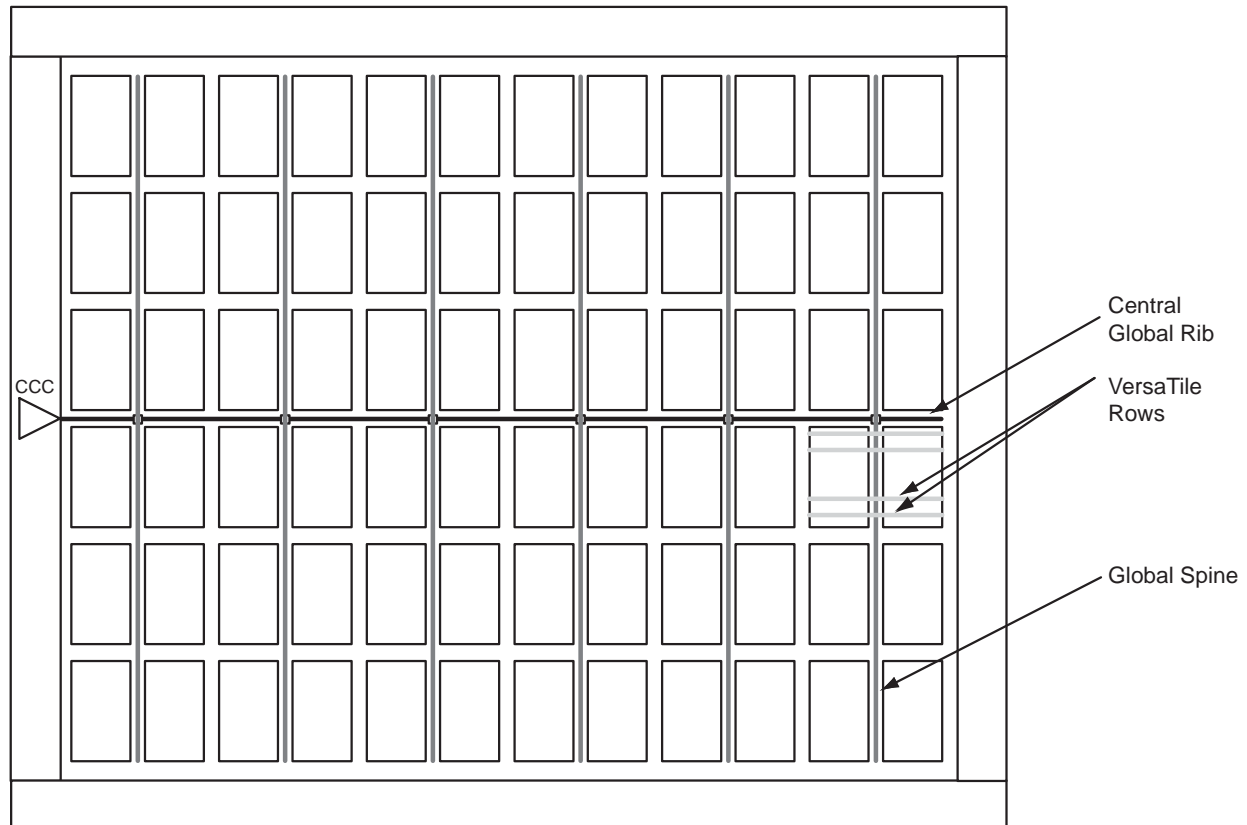


Figure 2-21 • Example of Global Tree Use in an AGLP125 Device for Clock Routing

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard-dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-61. Table 2-84 to Table 2-89 on page 2-60 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-84 • AGLP030 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.21	1.42	ns
t_{RCKH}	Input High Delay for Global Clock	1.23	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-85 • AGLP060 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.32	1.62	ns
t_{RCKH}	Input High Delay for Global Clock	1.34	1.72	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.38	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-86 • AGLP125 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.36	1.71	ns
t_{RCKH}	Input High Delay for Global Clock	1.39	1.82	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

1.2 V DC Core Voltage

Table 2-87 • AGLP030 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.80	2.09	ns
t_{RCKH}	Input High Delay for Global Clock	1.88	2.27	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.39	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

Table 2-88 • AGLP060 Global Resource
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	2.02	2.43	ns
t_{RCKH}	Input High Delay for Global Clock	2.09	2.65	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.56	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

Table 2-89 • AGLP125 Global Resource
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	2.08	2.54	ns
t_{RCKH}	Input High Delay for Global Clock	2.15	2.77	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.62	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

Table 2-90 • IGLOO PLUS CCC/PLL Specification
For IGLOO PLUS V2 or V5 devices, 1.5 V DC Core Supply Voltage

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		250	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		250	MHz
Delay Increments in Programmable Delay Blocks ^{1,2}		360		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL ^{3,4}				
Input Cycle-to-Cycle Jitter (peak magnitude)			100	MHz
Acquisition Time			300	μ s
				6.0
Tracking Jitter ⁵			2.5	
				1.5
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 ^{1,2}	1.25		15.65	ns
Delay Range in Block: Programmable Delay 2 ^{1,2}	0.469		15.65	ns
Delay Range in Block: Fixed Delay ^{1,2}		3.5		ns
VCO Output Peak-to-Peak Period Jitter F_{CCC_OUT} ⁶	Maximum Peak-to-Peak Period Jitter ^{6,7,8}			
	SSO \leq 2	SSO \leq 4	SSO \leq 8	SSO \leq 16
0.75 MHz to 50 MHz	0.50%	0.60%	0.80%	1.20%
50 MHz to 250 MHz	2.50%	4.00%	6.00%	12.00%

Notes:

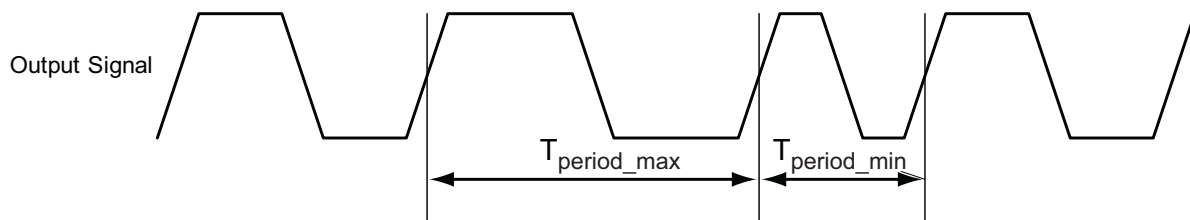
1. This delay is a function of voltage and temperature. See [Table 2-6 on page 2-6](#) and [Table 2-7 on page 2-7](#) for deratings.
2. $T_J = 25^\circ\text{C}$, $V_{CC} = 1.5\text{ V}$
3. Maximum value obtained for a STD speed grade device in Worst Case Commercial Conditions. For specific junction temperature and voltage supply, refer to [Table 2-6 on page 2-6](#) and [Table 2-7 on page 2-7](#) for derating values.
4. The AGLP030 device does not support a PLL.
5. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.
6. VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the per cent jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps, regardless of the output divider settings.
7. Measurements done with LVTTTL 3.3 V 8 mA I/O drive strength and high slew rate, $V_{CC}/V_{CCPLL} = 1.14\text{ V}$, $V_{CCI} = 3.3\text{ V}$, VQ/PQ/TQ type of packages, 20 pF load.
8. SSO are outputs that are synchronous to a single clock domain and have clock-to-out times that are within $\pm 200\text{ ps}$ of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "ProASIC3/E SSO and Pin Placement Guidelines" chapter of the *ProASIC3 FPGA Fabric User's Guide*.

Table 2-91 • IGLOO PLUS CCC/PLL Specification
For IGLOO PLUS V2 Devices, 1.2 V DC Core Supply Voltage

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		160	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		160	MHz
Delay Increments in Programmable Delay Blocks ^{1, 2}		580		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL ^{3, 4}				
Input Cycle-to-Cycle Jitter (peak magnitude)			60	MHz
Acquisition Time				
	LockControl = 0		300	μs
	LockControl = 1		6.0	ms
Tracking Jitter ⁵				
	LockControl = 0		4	ns
	LockControl = 1		3	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 ^{1, 2}	2.3		20.86	ns
Delay Range in Block: Programmable Delay 2 ^{1, 2}	0.025		20.86	ns
Delay Range in Block: Fixed Delay ^{1, 2}		5.7		ns
VCO Output Peak-to-Peak Period Jitter F_{CCC_OUT} ⁶	Maximum Peak-to-Peak Period Jitter ^{6, 7, 8}			
	SSO ≤ 2	SSO ≤ 4	SSO ≤ 8	SSO ≤ 16
0.75 MHz to 50 MHz	0.50%	1.20%	2.00%	3.00%
50 MHz to 160 MHz	2.50%	5.00%	7.00%	15.00%

Notes:

1. This delay is a function of voltage and temperature. See [Table 2-6 on page 2-6](#) and [Table 2-7 on page 2-7](#) for deratings.
2. $T_J = 25^\circ\text{C}$, $V_{CC} = 1.2\text{ V}$
3. Maximum value obtained for a STD speed grade device in Worst Case Commercial Conditions. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) and [Table 2-7 on page 2-7](#) for derating values.
4. The AGLP030 device does not support PLL.
5. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by period jitter parameter.
6. VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the per cent jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps, regardless of the output divider settings.
7. Measurements are done with LVTTTL 3.3 V, 8 mA, I/O drive strength and high slew rate. $V_{CC}/V_{CCPLL} = 1.14\text{ V}$, $V_{CCI} = 3.3\text{ V}$, VQ/PQ/TQ type of packages, 20 pF load.
8. SSO are outputs that are synchronous to a single clock domain, and have their clock-to-out times within $\pm 200\text{ ps}$ of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "ProASIC3/E SSO and Pin Placement Guidelines" chapter of the [ProASIC3 FPGA Fabric User's Guide](#).



Note: Peak-to-peak jitter measurements are defined by $T_{\text{peak-to-peak}} = T_{\text{period_max}} - T_{\text{period_min}}$.

Figure 2-22 • Peak-to-Peak Jitter Definition

Embedded SRAM and FIFO Characteristics

SRAM

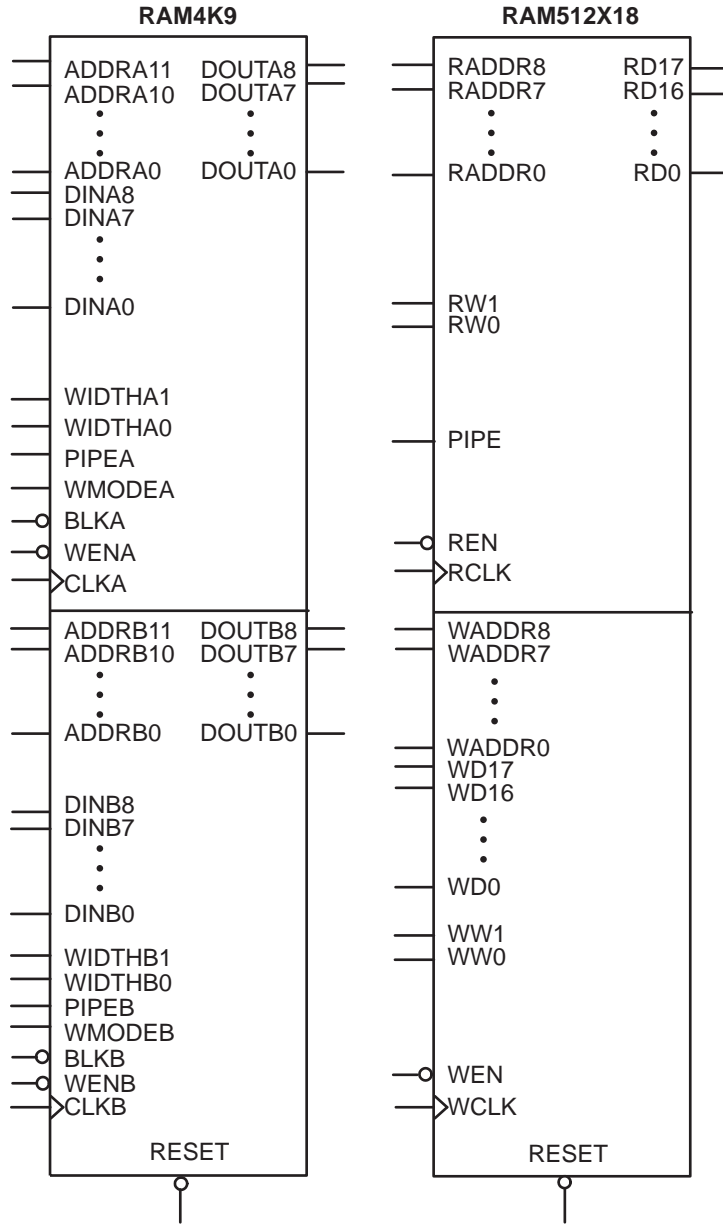


Figure 2-23 • RAM Models

Timing Waveforms

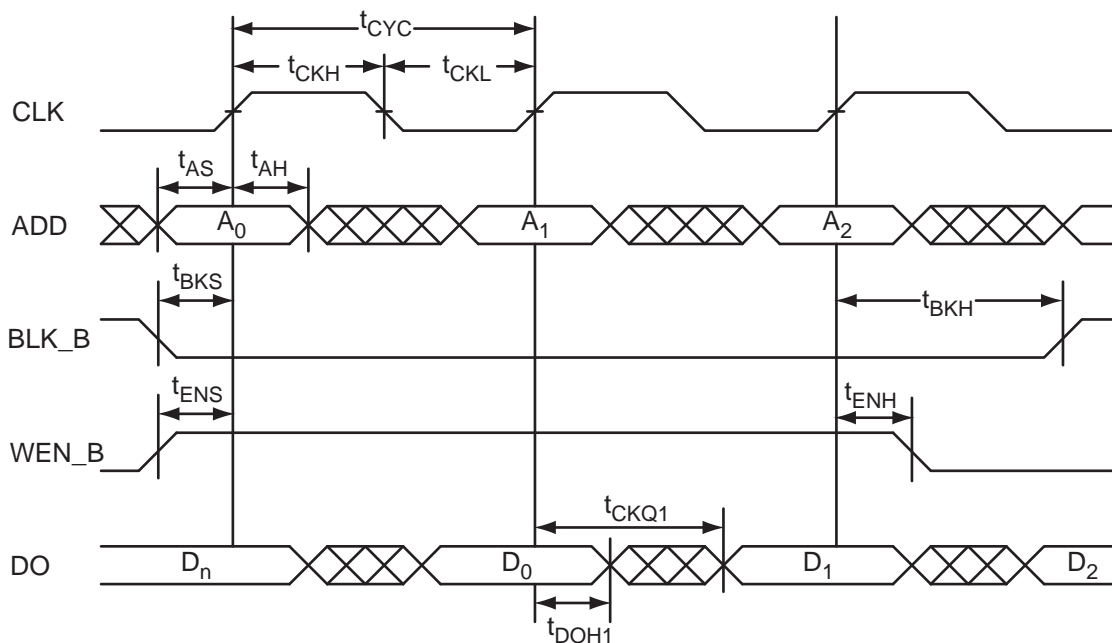


Figure 2-24 • RAM Read for Pass-Through Output

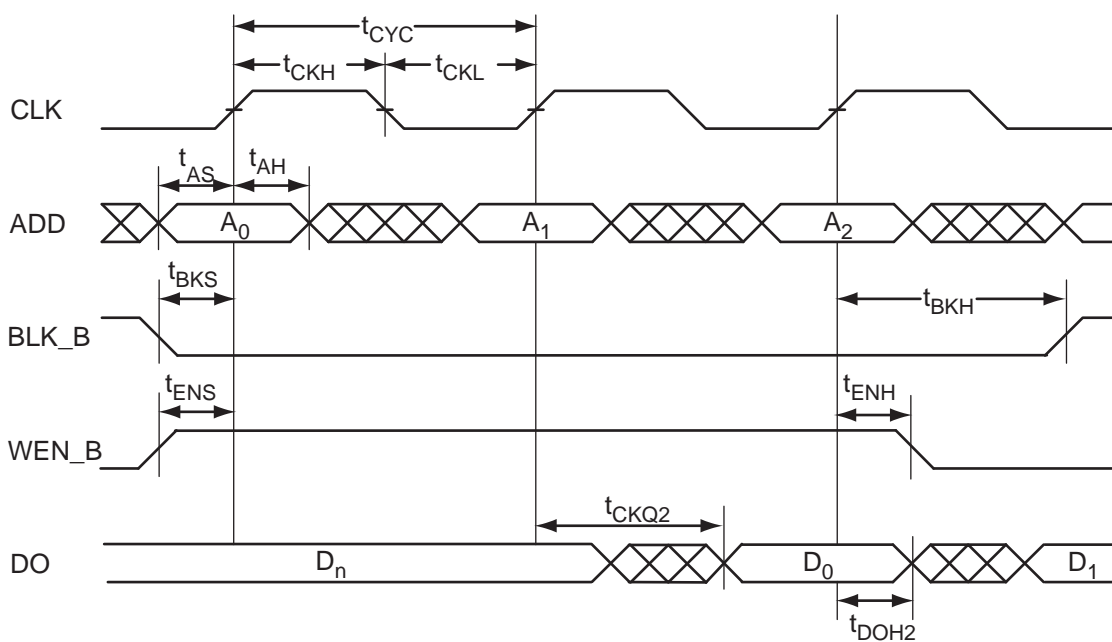
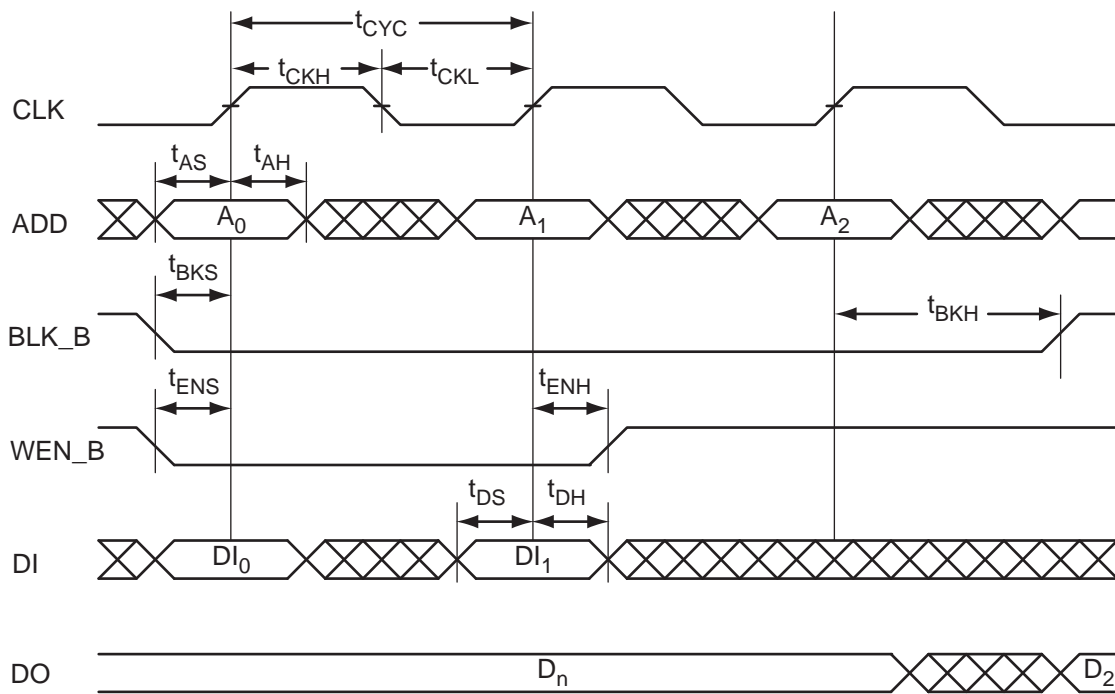
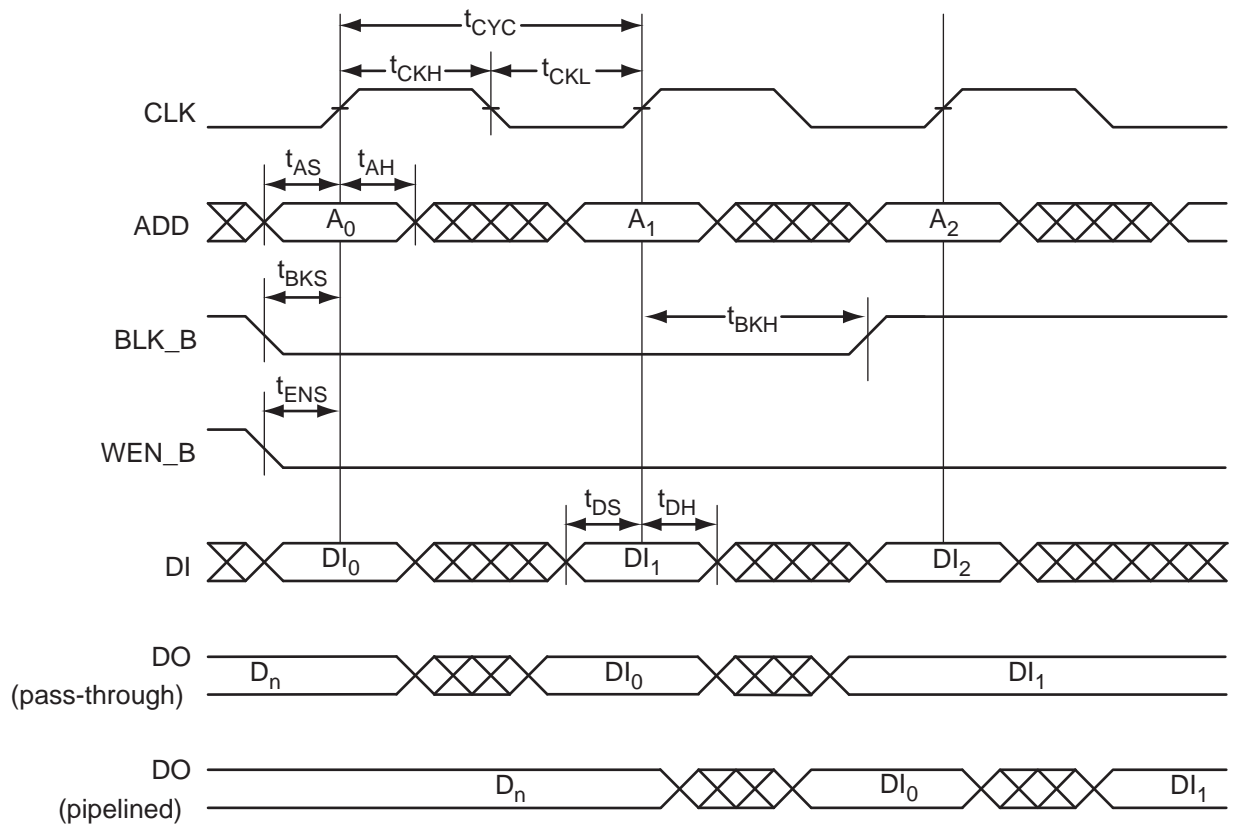


Figure 2-25 • RAM Read for Pipelined Output


Figure 2-26 • RAM Write, Output Retained (WMODE = 0)

Figure 2-27 • RAM Write, Output as Write Data (WMODE = 1)

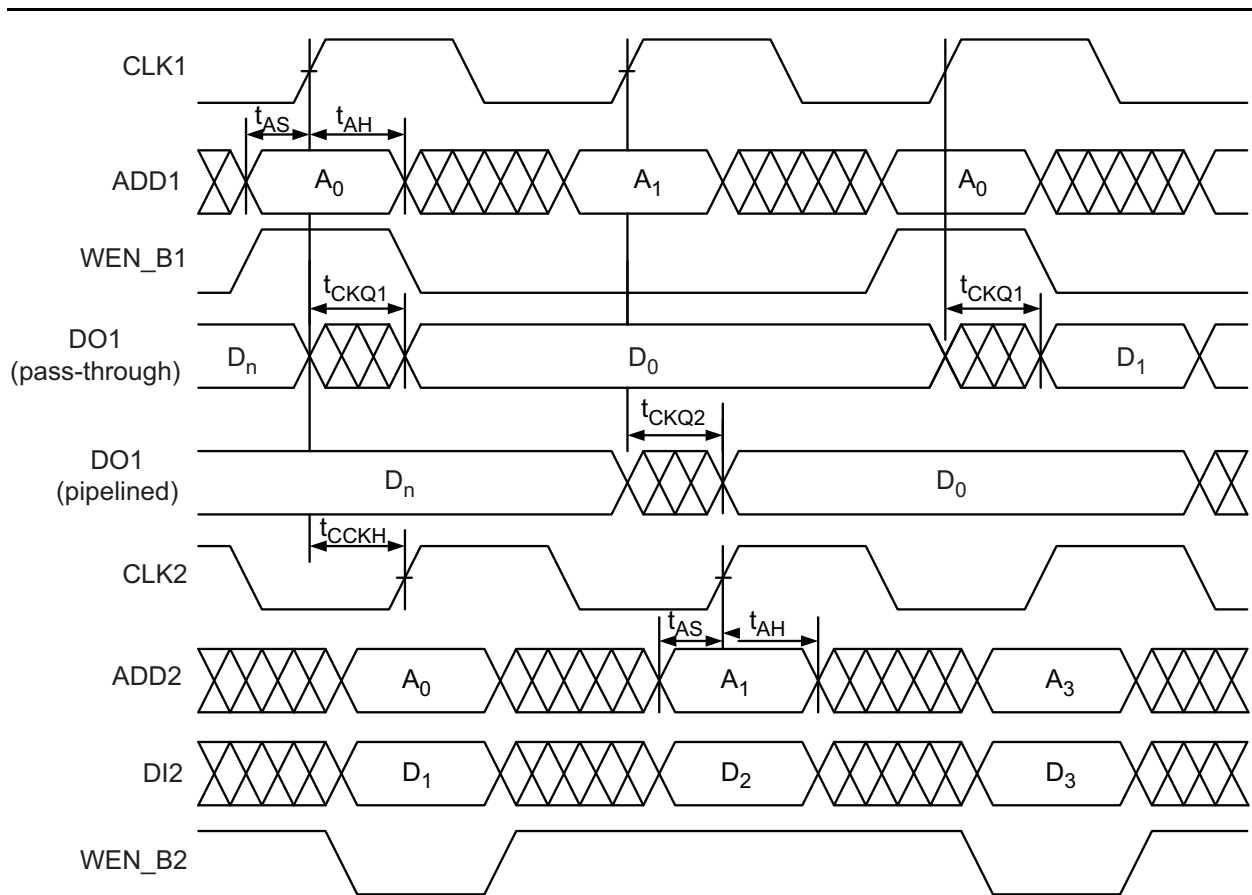


Figure 2-28 • Write Access after Read onto Same Address

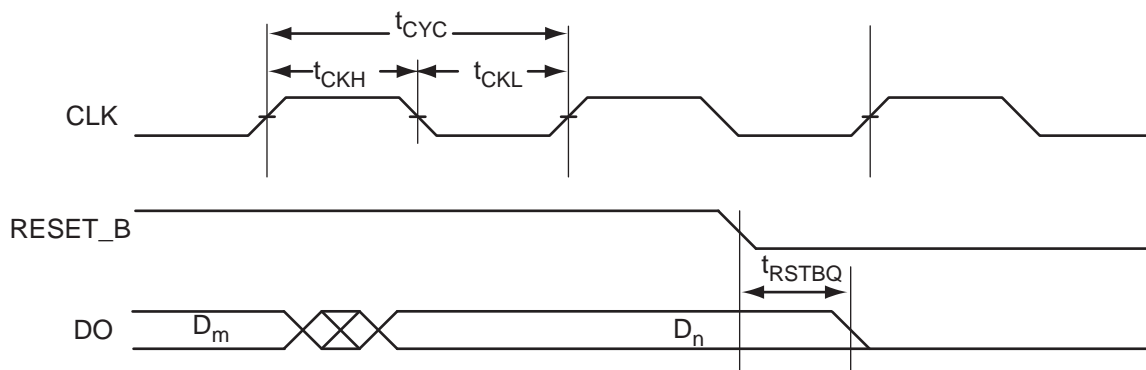


Figure 2-29 • RAM Reset

Timing Characteristics

1.5 V DC Core Voltage

Table 2-92 • RAM4K9
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	0.69	ns
t_{AH}	Address hold time	0.13	ns
t_{ENS}	REN_B, WEN_B setup time	0.68	ns
t_{ENH}	REN_B, WEN_B hold time	0.13	ns
t_{BKS}	BLK_B setup time	1.37	ns
t_{BKH}	BLK_B hold time	0.13	ns
t_{DS}	Input data (DI) setup time	0.59	ns
t_{DH}	Input data (DI) hold time	0.30	ns
t_{CKQ1}	Clock High to new data valid on DO (output retained, WMODE = 0)	2.94	ns
	Clock High to new data valid on DO (flow-through, WMODE = 1)	2.55	ns
t_{CKQ2}	Clock High to new data valid on DO (pipelined)	1.51	ns
t_{C2CWWL}	Address collision clk-to-clk delay for reliable write after write on same address – applicable to closing edge	0.29	ns
t_{C2CRWH}	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.24	ns
t_{C2CWRH}	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.40	ns
t_{RSTBQ}	RESET_B Low to data out Low on DO (flow-through)	1.72	ns
	RESET_B Low to data out Low on DO (pipelined)	1.72	ns
$t_{REMRSTB}$	RESET_B removal	0.51	ns
$t_{RECRSTB}$	RESET_B recovery	2.68	ns
$t_{MPWRSTB}$	RESET_B minimum pulse width	0.68	ns
t_{CYC}	Clock cycle time	6.24	ns
F_{MAX}	Maximum frequency	160	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-93 • RAM512X18**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$**

Parameter	Description	Std.	Units
t_{AS}	Address setup time	0.69	ns
t_{AH}	Address hold time	0.13	ns
t_{ENS}	REN_B, WEN_B setup time	0.61	ns
t_{ENH}	REN_B, WEN_B hold time	0.07	ns
t_{DS}	Input data (DI) setup time	0.59	ns
t_{DH}	Input data (DI) hold time	0.30	ns
t_{CKQ1}	Clock High to new data valid on DO (output retained, WMODE = 0)	3.51	ns
t_{CKQ2}	Clock High to new data valid on DO (pipelined)	1.43	ns
t_{C2CRWH}	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.21	ns
t_{C2CWRH}	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.25	ns
t_{RSTBQ}	RESET_B Low to data out Low on DO (flow-through)	1.72	ns
	RESET_B Low to data out Low on DO (pipelined)	1.72	ns
$t_{REMRSTB}$	RESET_B removal	0.51	ns
$t_{RECRSTB}$	RESET_B recovery	2.68	ns
$t_{MPWRSTB}$	RESET_B minimum pulse width	0.68	ns
t_{CYC}	Clock cycle time	6.24	ns
F_{MAX}	Maximum frequency	160	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

1.2 V DC Core Voltage

Table 2-94 • RAM4K9

 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{AS}	Address setup time	1.28	ns
t_{AH}	Address hold time	0.25	ns
t_{ENS}	REN_B, WEN_B setup time	1.25	ns
t_{ENH}	REN_B, WEN_B hold time	0.25	ns
t_{BKS}	BLK_B setup time	2.54	ns
t_{BKH}	BLK_B hold time	0.25	ns
t_{DS}	Input data (DI) setup time	1.10	ns
t_{DH}	Input data (DI) hold time	0.55	ns
t_{CKQ1}	Clock High to new data valid on DO (output retained, WMODE = 0)	5.51	ns
	Clock High to new data valid on DO (flow-through, WMODE = 1)	4.77	ns
t_{CKQ2}	Clock High to new data valid on DO (pipelined)	2.82	ns
t_{C2CWWL}	Address collision clk-to-clk delay for reliable write after write on same address – applicable to closing edge	0.30	ns
t_{C2CRWH}	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.32	ns
t_{C2CWRH}	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.44	ns
t_{RSTBQ}	RESET_B Low to data out Low on DO (flow-through)	3.21	ns
	RESET_B Low to data out Low on DO (pipelined)	3.21	ns
$t_{REMRSTB}$	RESET_B removal	0.93	ns
$t_{RECRSTB}$	RESET_B recovery	4.94	ns
$t_{MPWRSTB}$	RESET_B minimum pulse width	1.18	ns
t_{CYC}	Clock cycle time	10.90	ns
F_{MAX}	Maximum frequency	92	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

Table 2-95 • RAM512X18**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.	Units
t_{AS}	Address setup time	1.28	ns
t_{AH}	Address hold time	0.25	ns
t_{ENS}	REN_B, WEN_B setup time	1.13	ns
t_{ENH}	REN_B, WEN_B hold time	0.13	ns
t_{DS}	Input data (DI) setup time	1.10	ns
t_{DH}	Input data (DI) hold time	0.55	ns
t_{CKQ1}	Clock High to new data valid on DO (output retained, WMODE = 0)	6.56	ns
t_{CKQ2}	Clock High to new data valid on DO (pipelined)	2.67	ns
t_{C2CRWH}	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.29	ns
t_{C2CWRH}	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.36	ns
t_{RSTBQ}	RESET_B Low to data out Low on DO (flow through)	3.21	ns
	RESET_B Low to data out Low on DO (pipelined)	3.21	ns
$t_{REMRSTB}$	RESET_B removal	0.93	ns
$t_{RECRSTB}$	RESET_B recovery	4.94	ns
$t_{MPWRSTB}$	RESET_B minimum pulse width	1.18	ns
t_{CYC}	Clock cycle time	10.90	ns
F_{MAX}	Maximum frequency	92	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

FIFO

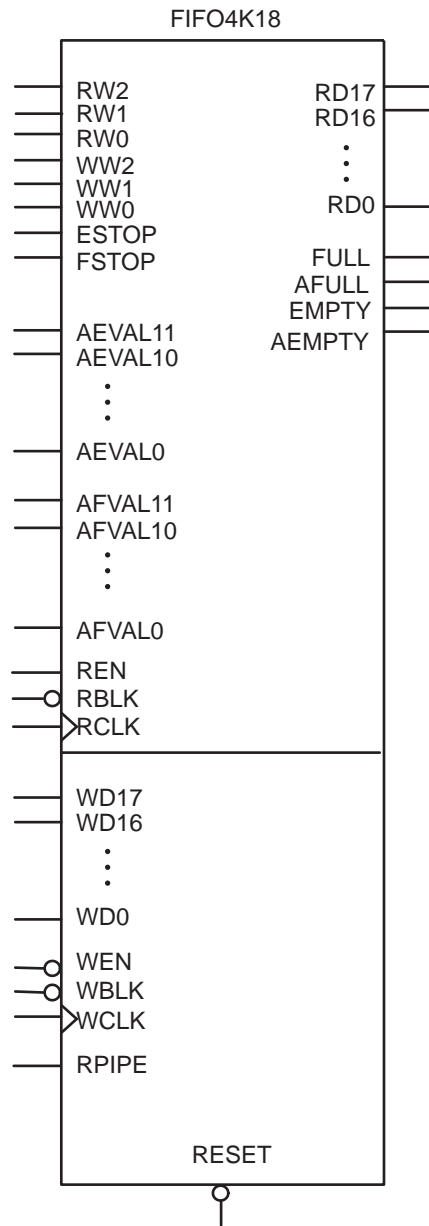


Figure 2-30 • FIFO Model

Timing Waveforms

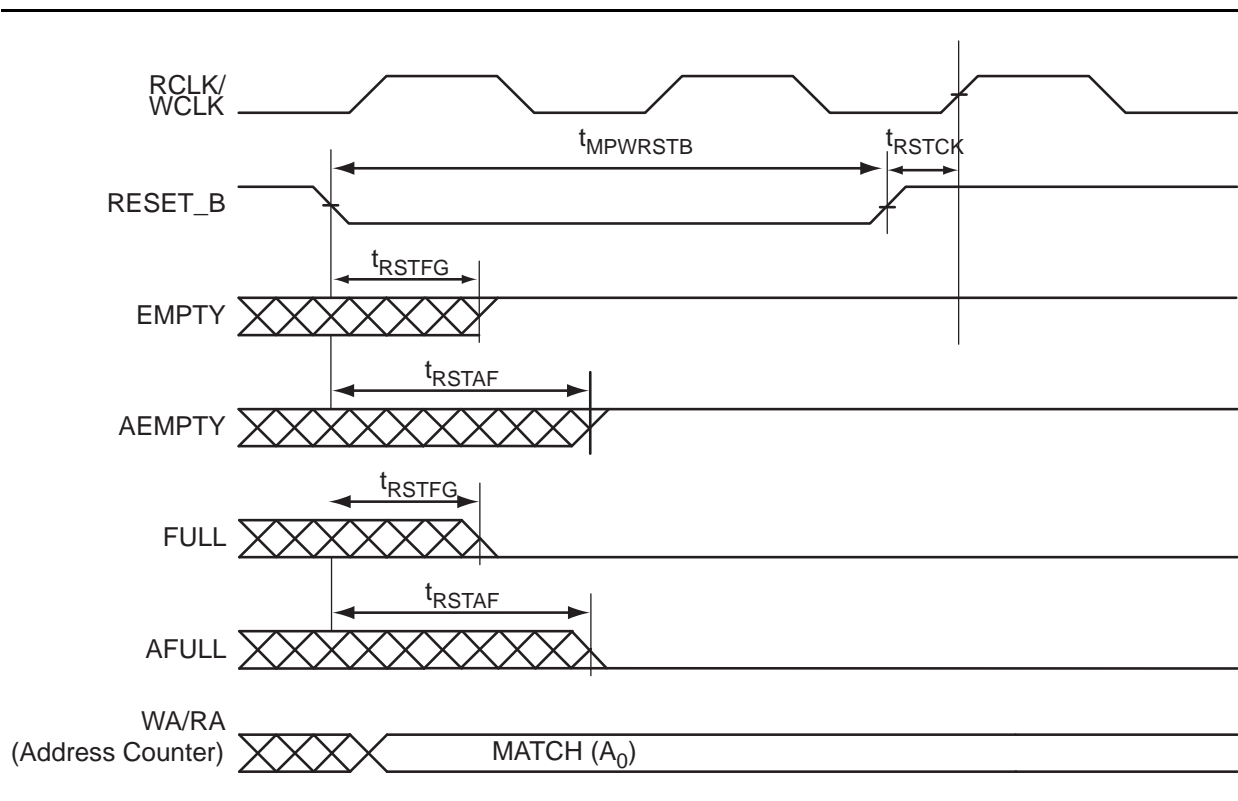


Figure 2-31 • FIFO Reset

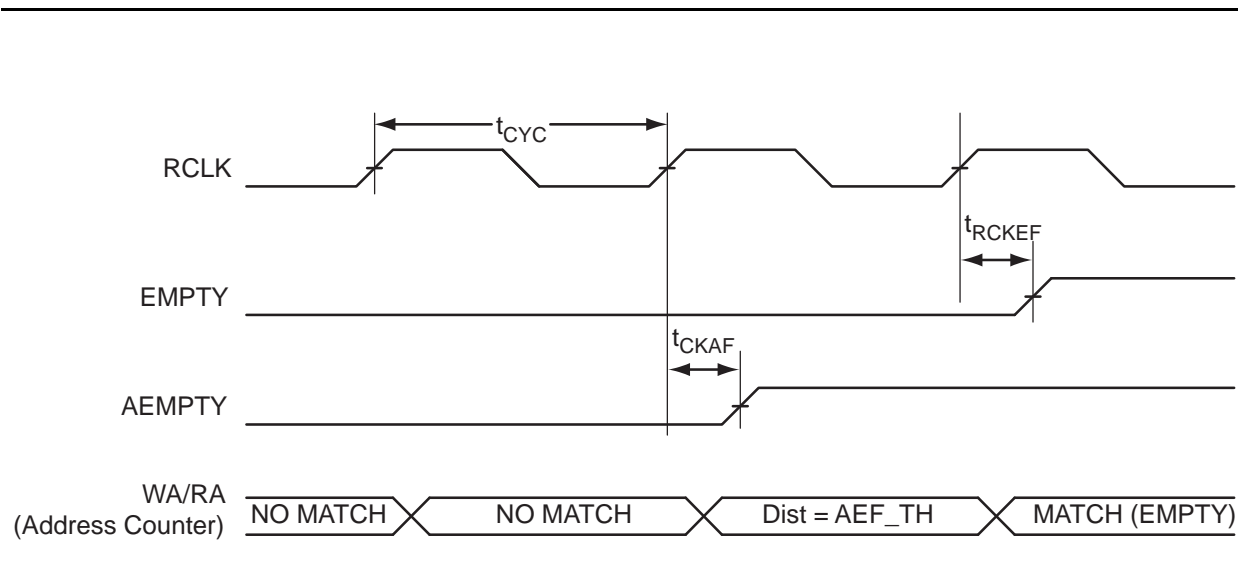


Figure 2-32 • FIFO EMPTY Flag and AEMPTY Flag Assertion

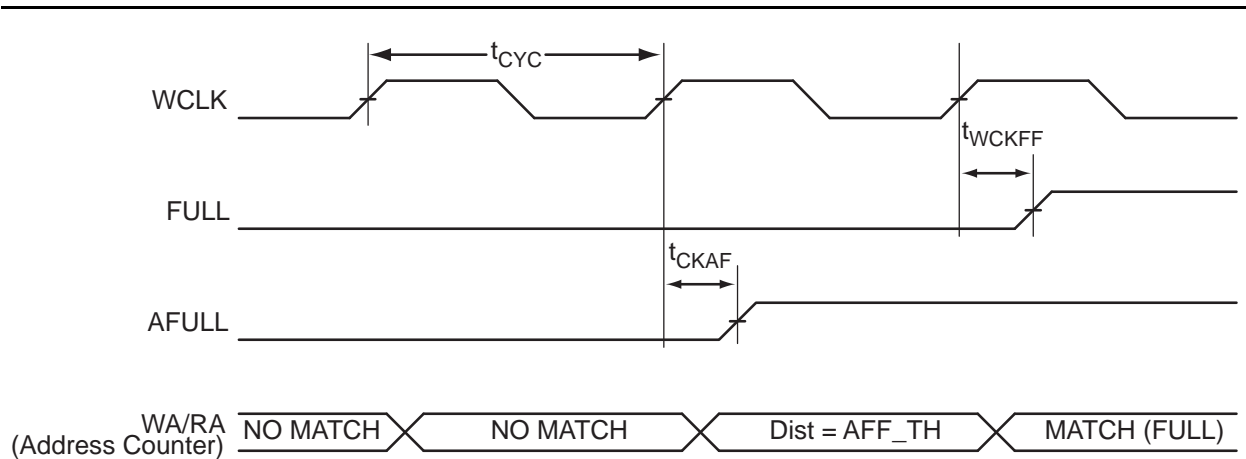


Figure 2-33 • FIFO FULL Flag and AFULL Flag Assertion

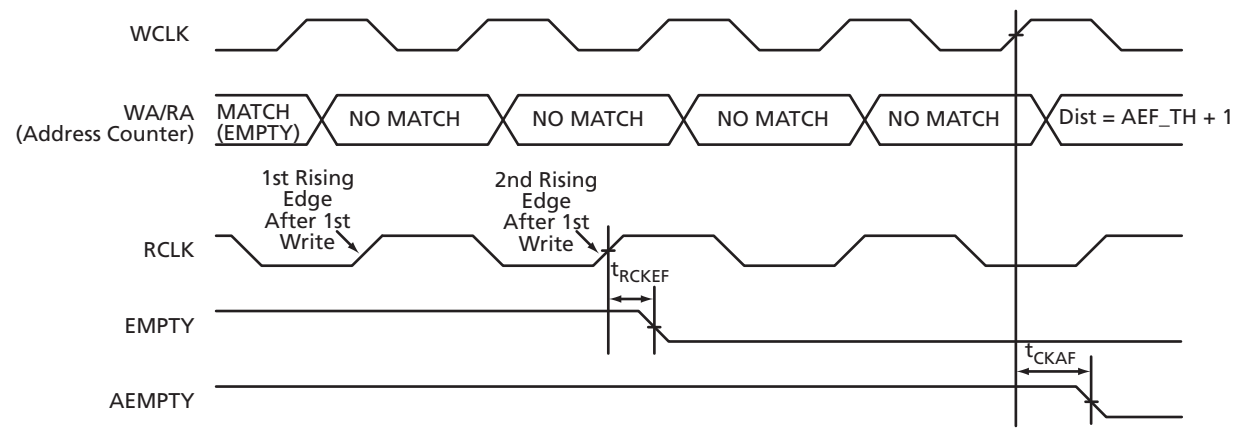


Figure 2-34 • FIFO EMPTY Flag and AEMPTY Flag Deassertion

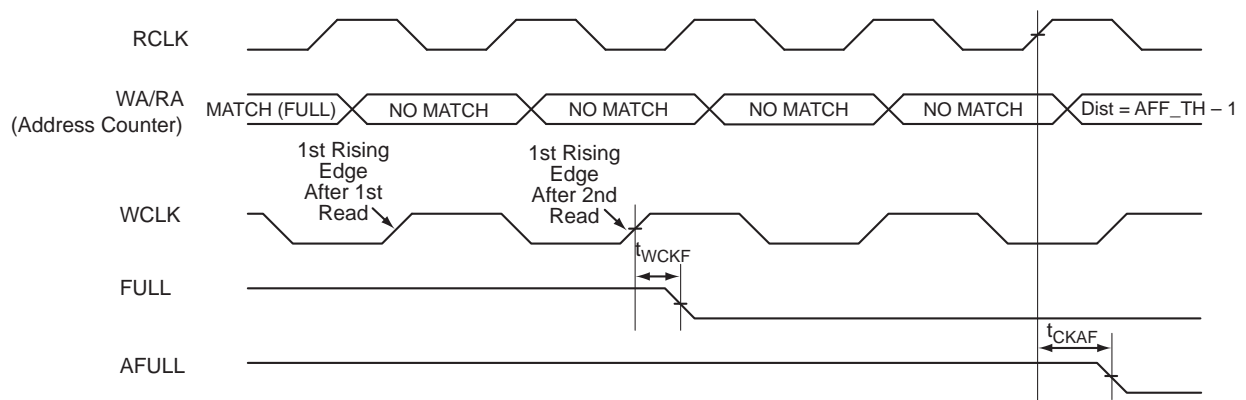


Figure 2-35 • FIFO FULL Flag and AFULL Flag Deassertion

Timing Characteristics

1.5 V DC Core Voltage

Table 2-96 • FIFO

 Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{ENS}	REN_B, WEN_B Setup Time	1.66	ns
t_{ENH}	REN_B, WEN_B Hold Time	0.13	ns
t_{BKS}	BLK_B Setup Time	0.30	ns
t_{BKH}	BLK_B Hold Time	0.00	ns
t_{DS}	Input Data (DI) Setup Time	0.63	ns
t_{DH}	Input Data (DI) Hold Time	0.20	ns
t_{CKQ1}	Clock High to New Data Valid on DO (flow-through)	2.77	ns
t_{CKQ2}	Clock High to New Data Valid on DO (pipelined)	1.50	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	2.94	ns
t_{WCKFF}	WCLK High to Full Flag Valid	2.79	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	10.71	ns
t_{RSTFG}	RESET_B Low to Empty/Full Flag Valid	2.90	ns
t_{RSTAF}	RESET_B Low to Almost Empty/Full Flag Valid	10.60	ns
t_{RSTBQ}	RESET_B Low to Data Out Low on DO (flow-through)	1.68	ns
	RESET_B Low to Data Out Low on DO (pipelined)	1.68	ns
$t_{REMRSTB}$	RESET_B Removal	0.51	ns
$t_{RECRSTB}$	RESET_B Recovery	2.68	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.68	ns
t_{CYC}	Clock Cycle Time	6.24	ns
F_{MAX}	Maximum Frequency for FIFO	160	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-97 • FIFO
Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{ENS}	REN_B, WEN_B Setup Time	3.44	ns
t_{ENH}	REN_B, WEN_B Hold Time	0.26	ns
t_{BKS}	BLK_B Setup Time	0.30	ns
t_{BKH}	BLK_B Hold Time	0.00	ns
t_{DS}	Input Data (DI) Setup Time	1.30	ns
t_{DH}	Input Data (DI) Hold Time	0.41	ns
t_{CKQ1}	Clock High to New Data Valid on DO (flow-through)	5.67	ns
t_{CKQ2}	Clock High to New Data Valid on DO (pipelined)	3.02	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	6.02	ns
t_{WCKFF}	WCLK High to Full Flag Valid	5.71	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	22.17	ns
t_{RSTFG}	RESET_B Low to Empty/Full Flag Valid	5.93	ns
t_{RSTAF}	RESET_B Low to Almost Empty/Full Flag Valid	21.94	ns
t_{RSTBQ}	RESET_B Low to Data Out Low on DO (flow-through)	3.41	ns
	RESET_B Low to Data Out Low on DO (pipelined)	3.41	ns
$t_{REMRSTB}$	RESET_B Removal	1.02	ns
$t_{RECRSTB}$	RESET_B Recovery	5.48	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	1.18	ns
t_{CYC}	Clock Cycle Time	10.90	ns
F_{MAX}	Maximum Frequency for FIFO	92	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

Embedded FlashROM Characteristics

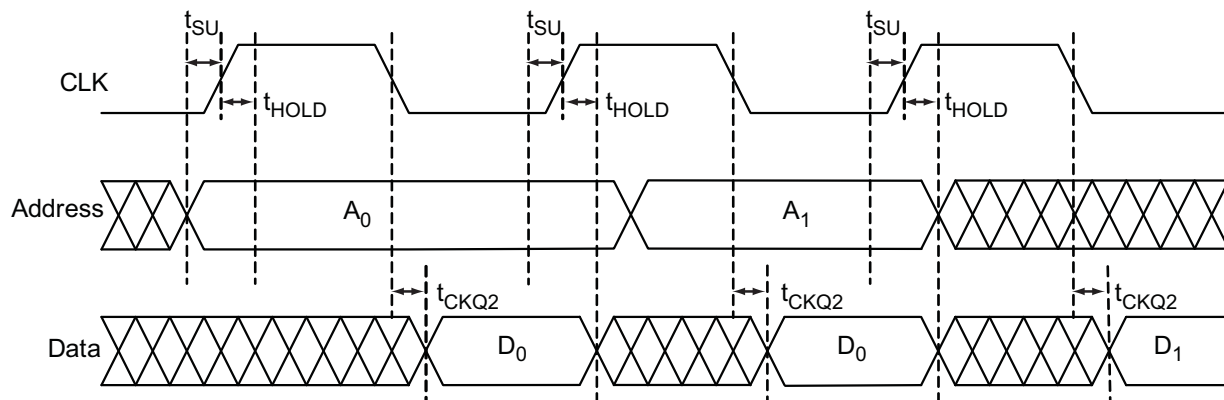


Figure 2-36 • Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-98 • Embedded FlashROM Access Time

Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.57	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	17.58	ns
F_{MAX}	Maximum Clock Frequency	15	MHz

1.2 V DC Core Voltage

Table 2-99 • Embedded FlashROM Access Time

Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.59	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	30.94	ns
F_{MAX}	Maximum Clock Frequency	10	MHz

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-15 for more details.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-100 • JTAG 1532

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.00	ns
t_{DIHD}	Test Data Input Hold Time	2.00	ns
t_{TMSU}	Test Mode Select Setup Time	1.00	ns
t_{TMDHD}	Test Mode Select Hold Time	2.00	ns
t_{TCK2Q}	Clock to Q (data out)	8.00	ns
t_{RSTB2Q}	Reset to Q (data out)	25.00	ns
F_{TCKMAX}	TCK Maximum Frequency	15	MHz
t_{TRSTREM}	ResetB Removal Time	0.58	ns
t_{TRSTREC}	ResetB Recovery Time	0.00	ns
t_{TRSTMPW}	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-101 • JTAG 1532

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.50	ns
t_{DIHD}	Test Data Input Hold Time	3.00	ns
t_{TMSU}	Test Mode Select Setup Time	1.50	ns
t_{TMDHD}	Test Mode Select Hold Time	3.00	ns
t_{TCK2Q}	Clock to Q (data out)	11.00	ns
t_{RSTB2Q}	Reset to Q (data out)	30.00	ns
F_{TCKMAX}	TCK Maximum Frequency	9.00	MHz
t_{TRSTREM}	ResetB Removal Time	1.18	ns
t_{TRSTREC}	ResetB Recovery Time	0.00	ns
t_{TRSTMPW}	ResetB Minimum Pulse	TBD	ns

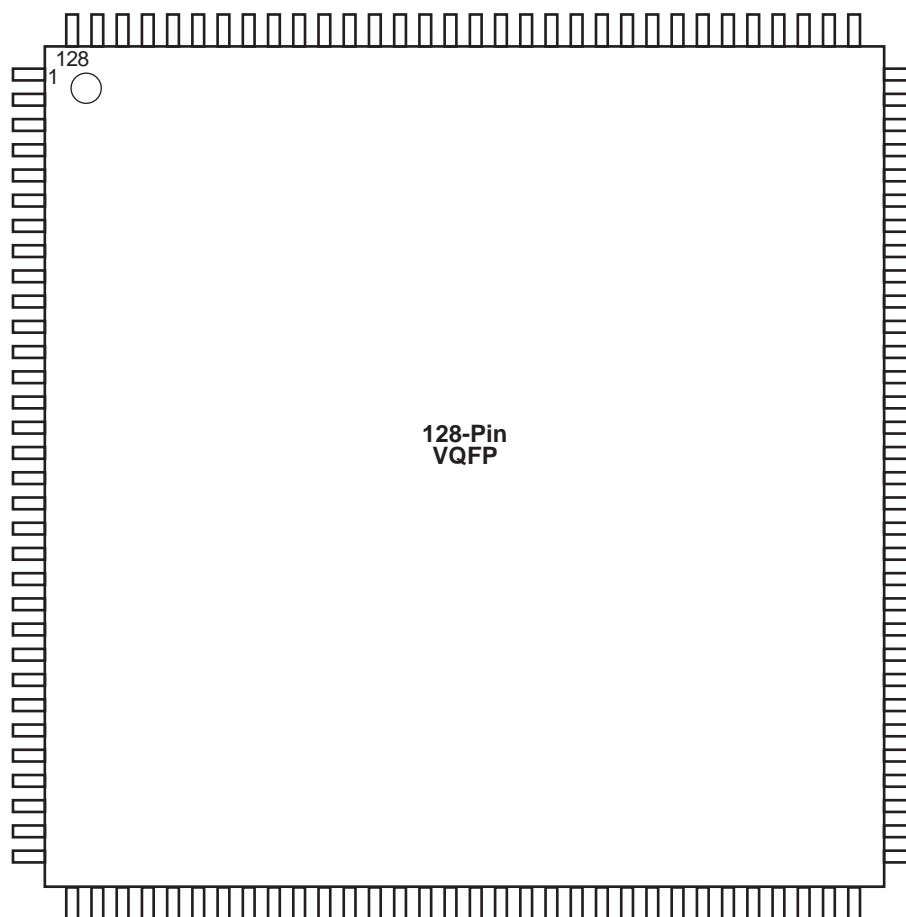
Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Actel Safety Critical, Life Support, and High-Reliability Applications Policy

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3 – Package Pin Assignments

128-Pin VQFP



Note: This is the bottom view of the package.

Note

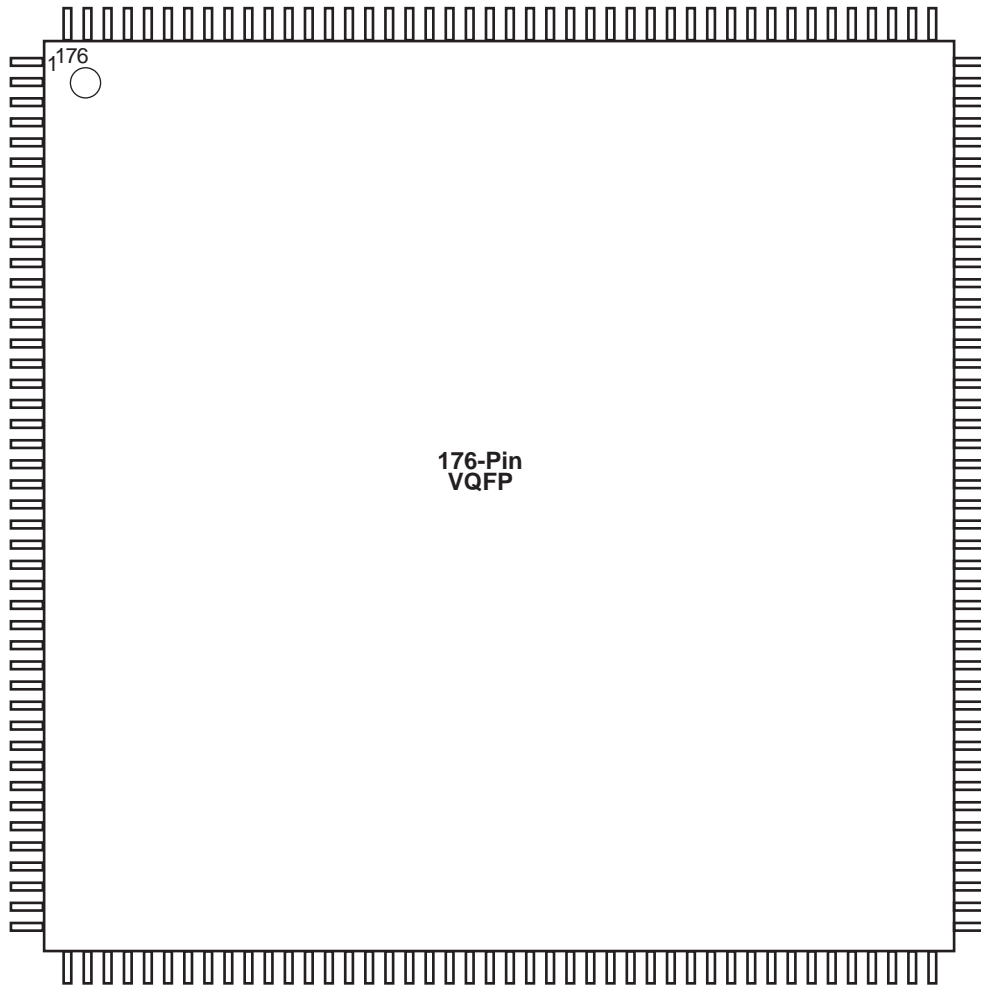
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Pin information is in the "Pin Descriptions" chapter of the *IGLOO PLUS FPGA Fabric User's Guide*.

128-Pin VQFP		128-Pin VQFP		128-Pin VQFP	
Pin Number	AGLP030 Function	Pin Number	AGLP030 Function	Pin Number	AGLP030 Function
1	IO119RSB3	36	IO88RSB2	71	IO57RSB1
2	IO118RSB3	37	IO86RSB2	72	VCCIB1
3	IO117RSB3	38	IO84RSB2	73	GND
4	IO115RSB3	39	IO83RSB2	74	IO55RSB1
5	IO116RSB3	40	GND	75	IO54RSB1
6	IO113RSB3	41	VCCIB2	76	IO53RSB1
7	IO114RSB3	42	IO82RSB2	77	IO52RSB1
8	GND	43	IO81RSB2	78	IO51RSB1
9	VCCIB3	44	IO79RSB2	79	IO50RSB1
10	IO112RSB3	45	IO78RSB2	80	IO49RSB1
11	IO111RSB3	46	IO77RSB2	81	VCC
12	IO110RSB3	47	IO75RSB2	82	GDB0/IO48RSB1
13	IO109RSB3	48	IO74RSB2	83	GDA0/IO47RSB1
14	GEC0/IO108RSB3	49	VCC	84	GDC0/IO46RSB1
15	GEA0/IO107RSB3	50	IO73RSB2	85	IO45RSB1
16	GEB0/IO106RSB3	51	IO72RSB2	86	IO44RSB1
17	VCC	52	IO70RSB2	87	IO43RSB1
18	IO104RSB3	53	IO69RSB2	88	IO42RSB1
19	IO103RSB3	54	IO68RSB2	89	VCCIB1
20	IO102RSB3	55	IO66RSB2	90	GND
21	IO101RSB3	56	IO65RSB2	91	IO40RSB1
22	IO100RSB3	57	GND	92	IO41RSB1
23	IO99RSB3	58	VCCIB2	93	IO39RSB1
24	GND	59	IO63RSB2	94	IO38RSB1
25	VCCIB3	60	IO61RSB2	95	IO37RSB1
26	IO97RSB3	61	IO59RSB2	96	IO36RSB1
27	IO98RSB3	62	TCK	97	IO35RSB0
28	IO95RSB3	63	TDI	98	IO34RSB0
29	IO96RSB3	64	TMS	99	IO33RSB0
30	IO94RSB3	65	VPUMP	100	IO32RSB0
31	IO93RSB3	66	TDO	101	IO30RSB0
32	IO92RSB3	67	TRST	102	IO28RSB0
33	IO91RSB2	68	IO58RSB1	103	IO27RSB0
34	FF/IO90RSB2	69	VJTAG	104	VCCIB0
35	IO89RSB2	70	IO56RSB1	105	GND

128-Pin VQFP	
Pin Number	AGLP030 Function
106	IO26RSB0
107	IO25RSB0
108	IO23RSB0
109	IO22RSB0
110	IO21RSB0
111	IO19RSB0
112	IO18RSB0
113	VCC
114	IO17RSB0
115	IO16RSB0
116	IO14RSB0
117	IO13RSB0
118	IO12RSB0
119	IO10RSB0
120	IO09RSB0
121	VCCIB0
122	GND
123	IO07RSB0
124	IO05RSB0
125	IO03RSB0
126	IO02RSB0
127	IO01RSB0
128	IO00RSB0

176-Pin VQFP



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

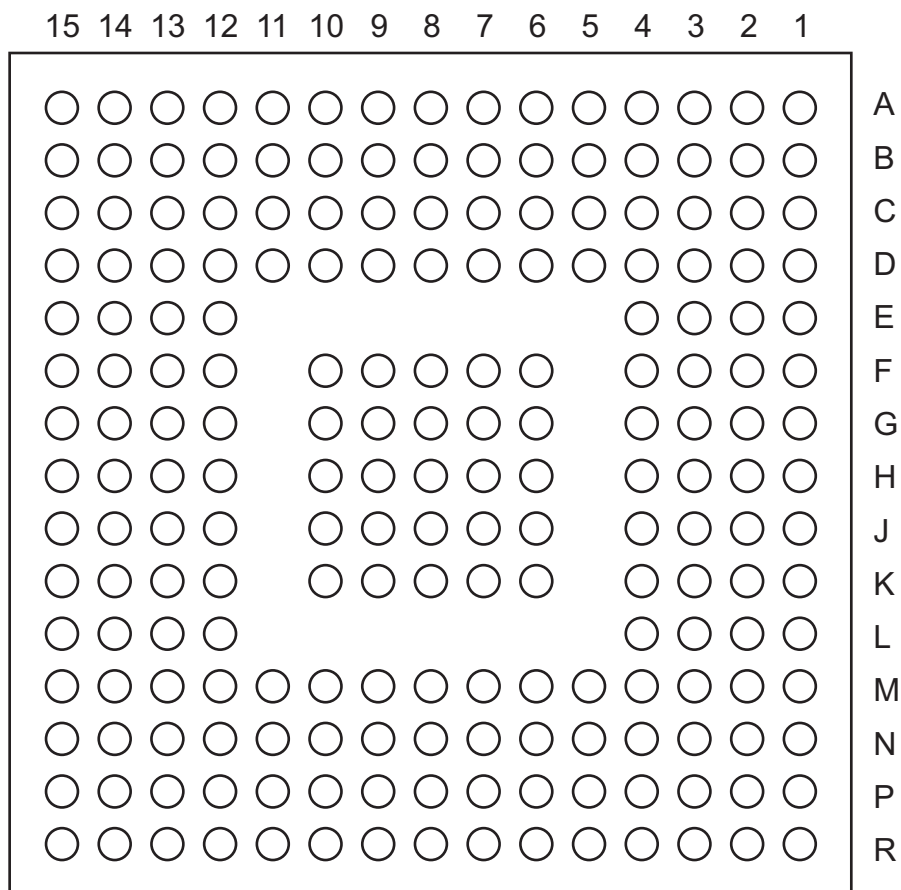
176-Pin VQFP		176-Pin VQFP		176-Pin VQFP	
Pin Number	AGLP060 Function	Pin Number	AGLP060 Function	Pin Number	AGLP060 Function
1	GAA2/IO156RSB3	36	IO119RSB3	70	IO89RSB2
2	IO155RSB3	37	GND	71	IO88RSB2
3	GAB2/IO154RSB3	38	VCCIB3	72	IO87RSB2
4	IO153RSB3	39	GEC1/IO116RSB3	73	IO86RSB2
5	GAC2/IO152RSB3	40	GEB1/IO114RSB3	74	IO85RSB2
6	GND	41	GEC0/IO115RSB3	75	IO84RSB2
7	VCCIB3	42	GEB0/IO113RSB3	76	GND
8	IO149RSB3	43	GEA1/IO112RSB3	77	VCCIB2
9	IO147RSB3	44	GEA0/IO111RSB3	78	IO83RSB2
10	IO145RSB3	45	GEA2/IO110RSB2	79	IO82RSB2
11	IO144RSB3	46	NC	80	GDC2/IO80RSB2
12	IO143RSB3	47	FF/GEB2/IO109RSB2	81	IO81RSB2
13	VCC	48	GEC2/IO108RSB2	82	GDA2/IO78RSB2
14	IO141RSB3	49	IO106RSB2	83	GDB2/IO79RSB2
15	GFC1/IO140RSB3	50	IO107RSB2	84	NC
16	GFB1/IO138RSB3	51	IO104RSB2	85	NC
17	GFB0/IO137RSB3	52	IO105RSB2	86	TCK
18	VCOMPLF	53	IO102RSB2	87	TDI
19	GFA1/IO136RSB3	54	IO103RSB2	88	TMS
20	VCCPLF	55	GND	89	VPUMP
21	GFA0/IO135RSB3	56	VCCIB2	90	TDO
22	GND	57	IO101RSB2	91	TRST
23	VCCIB3	58	IO100RSB2	92	VJTAG
24	GFA2/IO134RSB3	59	IO99RSB2	93	GDA1/IO76RSB1
25	GFB2/IO133RSB3	60	IO98RSB2	94	GDC0/IO73RSB1
26	GFC2/IO132RSB3	61	IO97RSB2	95	GDB1/IO74RSB1
27	IO131RSB3	62	IO96RSB2	96	GDC1/IO72RSB1
28	IO130RSB3	63	IO95RSB2	97	VCCIB1
29	IO129RSB3	64	IO94RSB2	98	GND
30	IO127RSB3	65	IO93RSB2	99	IO70RSB1
31	IO126RSB3	66	VCC	100	IO69RSB1
32	IO125RSB3	67	IO92RSB2	101	IO67RSB1
33	IO123RSB3	68	IO91RSB2	102	IO66RSB1
34	IO122RSB3	69	IO90RSB2	103	IO65RSB1
35	IO121RSB3			104	IO63RSB1

176-Pin VQFP	
Pin Number	AGLP060 Function
105	IO62RSB1
106	IO61RSB1
107	GCC2/IO60RSB1
108	GCB2/IO59RSB1
109	GCA2/IO58RSB1
110	GCA0/IO57RSB1
111	GCA1/IO56RSB1
112	VCCIB1
113	GND
114	GCB0/IO55RSB1
115	GCB1/IO54RSB1
116	GCC0/IO53RSB1
117	GCC1/IO52RSB1
118	IO51RSB1
119	IO50RSB1
120	VCC
121	IO48RSB1
122	IO47RSB1
123	IO45RSB1
124	IO44RSB1
125	IO43RSB1
126	VCCIB1
127	GND
128	GBC2/IO40RSB1
129	IO39RSB1
130	GBB2/IO38RSB1
131	IO37RSB1
132	GBA2/IO36RSB1
133	GBA1/IO35RSB0
134	NC
135	GBA0/IO34RSB0
136	NC
137	GBB1/IO33RSB0
138	NC
139	GBC1/IO31RSB0

176-Pin VQFP	
Pin Number	AGLP060 Function
140	GBB0/IO32RSB0
141	GBC0/IO30RSB0
142	IO29RSB0
143	IO28RSB0
144	IO27RSB0
145	VCCIB0
146	GND
147	IO26RSB0
148	IO25RSB0
149	IO24RSB0
150	IO23RSB0
151	IO22RSB0
152	IO21RSB0
153	IO20RSB0
154	IO19RSB0
155	IO18RSB0
156	VCC
157	IO17RSB0
158	IO16RSB0
159	IO15RSB0
160	IO14RSB0
161	IO13RSB0
162	IO12RSB0
163	IO11RSB0
164	IO10RSB0
165	IO09RSB0
166	VCCIB0
167	GND
168	IO07RSB0
169	IO08RSB0
170	GAC1/IO05RSB0
171	IO06RSB0
172	GAB1/IO03RSB0
173	GAC0/IO04RSB0
174	GAB0/IO02RSB0

176-Pin VQFP	
Pin Number	AGLP060 Function
175	GAA1/IO01RSB0
176	GAA0/IO00RSB0

201-Pin CSP



Note: This is the bottom view of the package.

Note

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201-Pin CSP		201-Pin CSP		201-Pin CSP	
Pin Number	AGLP030 Function	Pin Number	AGLP030 Function	Pin Number	AGLP030 Function
A1	NC	C6	IO12RSB0	F3	IO119RSB3
A2	IO04RSB0	C7	IO23RSB0	F4	IO111RSB3
A3	IO06RSB0	C8	IO19RSB0	F6	GND
A4	IO09RSB0	C9	IO28RSB0	F7	VCC
A5	IO11RSB0	C10	IO32RSB0	F8	VCCIB0
A6	IO13RSB0	C11	IO35RSB0	F9	VCCIB0
A7	IO17RSB0	C12	NC	F10	VCCIB0
A8	IO18RSB0	C13	GND	F12	NC
A9	IO24RSB0	C14	IO41RSB1	F13	NC
A10	IO26RSB0	C15	IO37RSB1	F14	IO40RSB1
A11	IO27RSB0	D1	IO117RSB3	F15	IO38RSB1
A12	IO31RSB0	D2	IO118RSB3	G1	NC
A13	NC	D3	NC	G2	IO112RSB3
A14	NC	D4	GND	G3	IO110RSB3
A15	NC	D5	IO01RSB0	G4	IO109RSB3
B1	NC	D6	IO03RSB0	G6	VCCIB3
B2	NC	D7	IO10RSB0	G7	GND
B3	IO08RSB0	D8	IO21RSB0	G8	VCC
B4	IO05RSB0	D9	IO25RSB0	G9	GND
B5	IO07RSB0	D10	IO30RSB0	G10	GND
B6	IO15RSB0	D11	IO33RSB0	G12	NC
B7	IO14RSB0	D12	GND	G13	NC
B8	IO16RSB0	D13	NC	G14	IO42RSB1
B9	IO20RSB0	D14	IO36RSB1	G15	IO44RSB1
B10	IO22RSB0	D15	IO39RSB1	H1	NC
B11	IO34RSB0	E1	IO115RSB3	H2	GEB0/IO106RSB3
B12	IO29RSB0	E2	IO114RSB3	H3	GEC0/IO108RSB3
B13	NC	E3	NC	H4	NC
B14	NC	E4	NC	H6	VCCIB3
B15	NC	E12	NC	H7	GND
C1	NC	E13	NC	H8	VCC
C2	NC	E14	GDC0/IO46RSB1	H9	GND
C3	GND	E15	GDB0/IO48RSB1	H10	VCCIB1
C4	IO00RSB0	F1	IO113RSB3	H12	IO54RSB1
C5	IO02RSB0	F2	IO116RSB3	H13	GDA0/IO47RSB1

201-Pin CSP		201-Pin CSP		201-Pin CSP	
Pin Number	AGLP030 Function	Pin Number	AGLP030 Function	Pin Number	AGLP030 Function
H14	IO45RSB1	L15	IO58RSB1	P5	IO87RSB2
H15	IO43RSB1	M1	IO93RSB3	P6	IO86RSB2
J1	GEOA0/IO107RSB3	M2	IO92RSB3	P7	IO84RSB2
J2	IO105RSB3	M3	IO97RSB3	P8	IO80RSB2
J3	IO104RSB3	M4	GND	P9	IO74RSB2
J4	IO102RSB3	M5	NC	P10	IO73RSB2
J6	VCCIB3	M6	IO79RSB2	P11	IO76RSB2
J7	GND	M7	IO77RSB2	P12	IO67RSB2
J8	VCC	M8	IO72RSB2	P13	IO64RSB2
J9	GND	M9	IO70RSB2	P14	VPUMP
J10	VCCIB1	M10	IO61RSB2	P15	TRST
J12	NC	M11	IO59RSB2	R1	NC
J13	NC	M12	GND	R2	NC
J14	IO52RSB1	M13	NC	R3	IO91RSB2
J15	IO50RSB1	M14	IO55RSB1	R4	FF/IO90RSB2
K1	IO103RSB3	M15	IO56RSB1	R5	IO89RSB2
K2	IO101RSB3	N1	NC	R6	IO83RSB2
K3	IO99RSB3	N2	NC	R7	IO82RSB2
K4	IO100RSB3	N3	GND	R8	IO85RSB2
K6	GND	N4	NC	R9	IO78RSB2
K7	VCCIB2	N5	IO88RSB2	R10	IO69RSB2
K8	VCCIB2	N6	IO81RSB2	R11	IO62RSB2
K9	VCCIB2	N7	IO75RSB2	R12	IO60RSB2
K10	VCCIB1	N8	IO68RSB2	R13	TMS
K12	NC	N9	IO66RSB2	R14	TDI
K13	IO57RSB1	N10	IO65RSB2	R15	TCK
K14	IO49RSB1	N11	IO71RSB2		
K15	IO53RSB1	N12	IO63RSB2		
L1	IO96RSB3	N13	GND		
L2	IO98RSB3	N14	TDO		
L3	IO95RSB3	N15	VJTAG		
L4	IO94RSB3	P1	NC		
L12	NC	P2	NC		
L13	NC	P3	NC		
L14	IO51RSB1	P4	NC		

201-Pin CSP		201-Pin CSP		201-Pin CSP	
Pin Number	AGLP060 Function	Pin Number	AGLP060 Function	Pin Number	AGLP060 Function
A1	IO150RSB3	C6	IO07RSB0	F3	IO145RSB3
A2	GAA0/IO00RSB0	C7	IO16RSB0	F4	IO147RSB3
A3	GAC0/IO04RSB0	C8	IO21RSB0	F6	GND
A4	IO08RSB0	C9	IO28RSB0	F7	VCC
A5	IO11RSB0	C10	GBB1/IO33RSB0	F8	VCCIB0
A6	IO15RSB0	C11	GBA1/IO35RSB0	F9	VCCIB0
A7	IO17RSB0	C12	GBB2/IO38RSB1	F10	VCCIB0
A8	IO18RSB0	C13	GND	F12	IO47RSB1
A9	IO22RSB0	C14	IO48RSB1	F13	IO45RSB1
A10	IO26RSB0	C15	IO39RSB1	F14	GCC1/IO52RSB1
A11	IO29RSB0	D1	IO146RSB3	F15	GCA1/IO56RSB1
A12	GBC1/IO31RSB0	D2	IO144RSB3	G1*	VCOMPLF
A13	GBA2/IO36RSB1	D3	IO148RSB3	G2	GFB0/IO137RSB3
A14	IO41RSB1	D4	GND	G3	GFC0/IO139RSB3
A15	NC	D5	GAB0/IO02RSB0	G4	IO143RSB3
B1	IO151RSB3	D6	GAC1/IO05RSB0	G6	VCCIB3
B2	GAB2/IO154RSB3	D7	IO14RSB0	G7	GND
B3	IO06RSB0	D8	IO19RSB0	G8	VCC
B4	IO09RSB0	D9	GBC0/IO30RSB0	G9	GND
B5	IO13RSB0	D10	GBB0/IO32RSB0	G10	GND
B6	IO10RSB0	D11	GBA0/IO34RSB0	G12	IO50RSB1
B7	IO12RSB0	D12	GND	G13	GCB1/IO54RSB1
B8	IO20RSB0	D13	GBC2/IO40RSB1	G14	GCC2/IO60RSB1
B9	IO23RSB0	D14	IO51RSB1	G15	GCA2/IO58RSB1
B10	IO25RSB0	D15	IO44RSB1	H1*	VCCPLF
B11	IO24RSB0	E1	IO142RSB3	H2	GFA1/IO136RSB3
B12	IO27RSB0	E2	IO149RSB3	H3	GFB1/IO138RSB3
B13	IO37RSB1	E3	IO153RSB3	H4	NC
B14	IO46RSB1	E4	GAC2/IO152RSB3	H6	VCCIB3
B15	IO42RSB1	E12	IO43RSB1	H7	GND
C1	IO155RSB3	E13	IO49RSB1	H8	VCC
C2	GAA2/IO156RSB3	E14	GCC0/IO53RSB1	H9	GND
C3	GND	E15	GCB0/IO55RSB1	H10	VCCIB1
C4	GAA1/IO01RSB0	F1	IO141RSB3	H12	GCB2/IO59RSB1
C5	GAB1/IO03RSB0	F2	GFC1/IO140RSB3	H13	GCA0/IO57RSB1

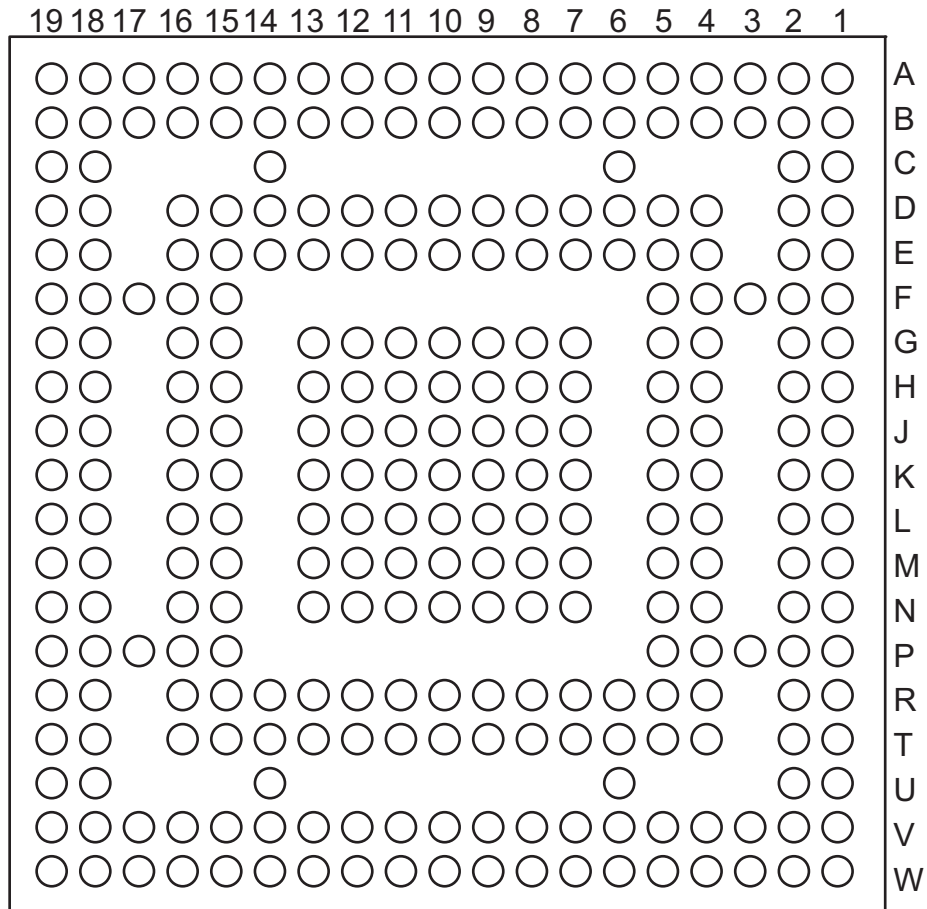
* Pin numbers G1 and H1 must be connected to ground because a PLL is not supported for AGLP060-CS/G201.

201-Pin CSP	
Pin Number	AGLP060 Function
H14	IO64RSB1
H15	IO62RSB1
J1	GFA2/IO134RSB3
J2	GFA0/IO135RSB3
J3	GFB2/IO133RSB3
J4	IO131RSB3
J6	VCCIB3
J7	GND
J8	VCC
J9	GND
J10	VCCIB1
J12	IO61RSB1
J13	IO63RSB1
J14	IO68RSB1
J15	IO66RSB1
K1	IO130RSB3
K2	GFC2/IO132RSB3
K3	IO127RSB3
K4	IO129RSB3
K6	GND
K7	VCCIB2
K8	VCCIB2
K9	VCCIB2
K10	VCCIB1
K12	IO65RSB1
K13	IO67RSB1
K14	IO69RSB1
K15	IO70RSB1
L1	IO126RSB3
L2	IO128RSB3
L3	IO121RSB3
L4	IO123RSB3
L12	GDB1/IO74RSB1
L13	GDC1/IO72RSB1
L14	IO71RSB1

201-Pin CSP	
Pin Number	AGLP060 Function
L15	GDC0/IO73RSB1
M1	IO122RSB3
M2	IO124RSB3
M3	IO119RSB3
M4	GND
M5	IO125RSB3
M6	IO98RSB2
M7	IO96RSB2
M8	IO91RSB2
M9	IO89RSB2
M10	IO82RSB2
M11	GDA2/IO78RSB2
M12	GND
M13	GDA1/IO76RSB1
M14	GDA0/IO77RSB1
M15	GDB0/IO75RSB1
N1	IO117RSB3
N2	IO120RSB3
N3	GND
N4	GEB1/IO114RSB3
N5	IO107RSB2
N6	IO100RSB2
N7	IO94RSB2
N8	IO87RSB2
N9	IO85RSB2
N10	GDC2/IO80RSB2
N11	IO90RSB2
N12	IO84RSB2
N13	GND
N14	TDO
N15	VJTAG
P1	GEC0/IO115RSB3
P2	GEC1/IO116RSB3
P3	GEA0/IO111RSB3
P4	GEA1/IO112RSB3

201-Pin CSP	
Pin Number	AGLP060 Function
P5	IO106RSB2
P6	IO105RSB2
P7	IO103RSB2
P8	IO99RSB2
P9	IO93RSB2
P10	IO92RSB2
P11	IO95RSB2
P12	IO86RSB2
P13	IO83RSB2
P14	VPUMP
P15	TRST
R1	IO118RSB3
R2	GEB0/IO113RSB3
R3	GEA2/IO110RSB2
R4	FF/GEB2/IO109RSB2
R5	GEC2/IO108RSB2
R6	IO102RSB2
R7	IO101RSB2
R8	IO104RSB2
R9	IO97RSB2
R10	IO88RSB2
R11	IO81RSB2
R12	GDB2/IO79RSB2
R13	TMS
R14	TDI
R15	TCK

281-Pin CSP



Note: This is the bottom view of the package.

Note

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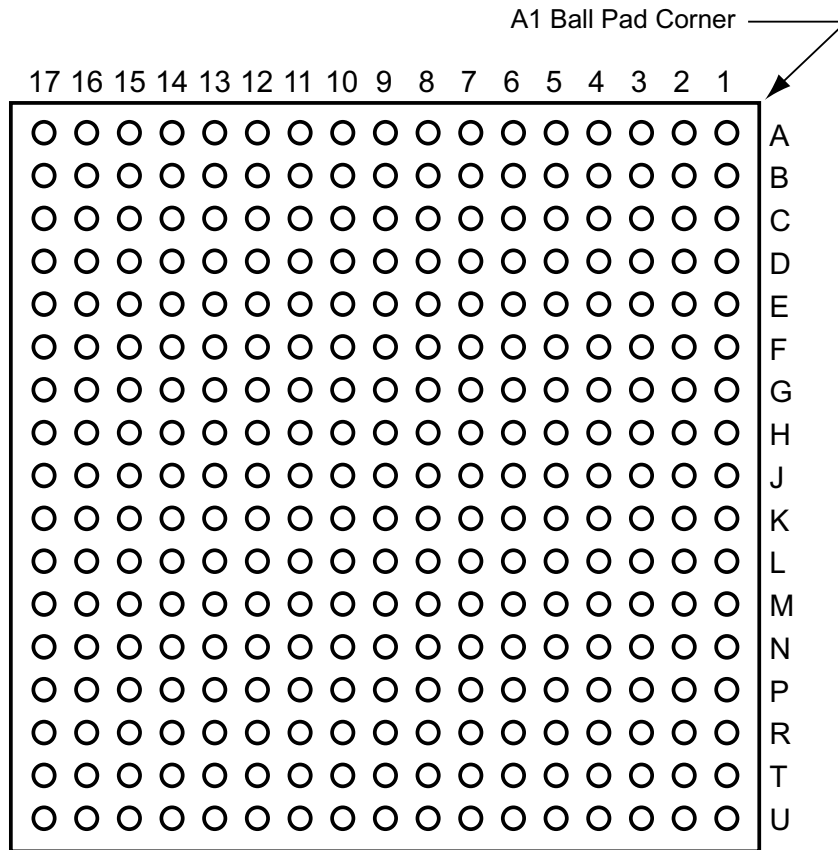
281-Pin CSP		281-Pin CSP		281-Pin CSP	
Pin Number	AGLP125 Function	Pin Number	AGLP125 Function	Pin Number	AGLP125 Function
A1	GND	B18	VCCIB1	E13	IO48RSB0
A2	GAB0/IO02RSB0	B19	IO64RSB1	E14	GBB1/IO60RSB0
A3	GAC1/IO05RSB0	C1	GAB2/IO209RSB3	E15	IO53RSB0
A4	IO09RSB0	C2	IO210RSB3	E16	IO69RSB1
A5	IO13RSB0	C6	IO12RSB0	E18	IO68RSB1
A6	IO15RSB0	C14	IO47RSB0	E19	IO71RSB1
A7	IO18RSB0	C18	IO54RSB0	F1	IO198RSB3
A8	IO23RSB0	C19	GBB2/IO65RSB1	F2	GND
A9	IO25RSB0	D1	IO206RSB3	F3	IO201RSB3
A10	VCCIB0	D2	IO208RSB3	F4	IO204RSB3
A11	IO33RSB0	D4	GAA0/IO00RSB0	F5	IO16RSB0
A12	IO41RSB0	D5	GAA1/IO01RSB0	F15	IO50RSB0
A13	IO43RSB0	D6	IO10RSB0	F16	IO74RSB1
A14	IO46RSB0	D7	IO17RSB0	F17	IO72RSB1
A15	IO55RSB0	D8	IO24RSB0	F18	GND
A16	IO56RSB0	D9	IO27RSB0	F19	IO73RSB1
A17	GBC1/IO58RSB0	D10	GND	G1	IO195RSB3
A18	GBA0/IO61RSB0	D11	IO31RSB0	G2	IO200RSB3
A19	GND	D12	IO40RSB0	G4	IO202RSB3
B1	GAA2/IO211RSB3	D13	IO49RSB0	G5	IO08RSB0
B2	VCCIB0	D14	IO45RSB0	G7	GAC2/IO207RSB3
B3	GAB1/IO03RSB0	D15	GBB0/IO59RSB0	G8	VCCIB0
B4	GAC0/IO04RSB0	D16	GBA2/IO63RSB1	G9	IO26RSB0
B5	IO11RSB0	D18	GBC2/IO67RSB1	G10	IO35RSB0
B6	GND	D19	IO66RSB1	G11	IO44RSB0
B7	IO21RSB0	E1	IO203RSB3	G12	VCCIB0
B8	IO22RSB0	E2	IO205RSB3	G13	IO51RSB0
B9	IO28RSB0	E4	IO07RSB0	G15	IO70RSB1
B10	IO32RSB0	E5	IO06RSB0	G16	IO75RSB1
B11	IO36RSB0	E6	IO14RSB0	G18	GCC0/IO80RSB1
B12	IO39RSB0	E7	IO20RSB0	G19	GCB1/IO81RSB1
B13	IO42RSB0	E8	IO29RSB0	H1	GFB0/IO191RSB3
B14	GND	E9	IO34RSB0	H2	IO196RSB3
B15	IO52RSB0	E10	IO30RSB0	H4	GFC1/IO194RSB3
B16	GBC0/IO57RSB0	E11	IO37RSB0	H5	GFB1/IO192RSB3
B17	GBA1/IO62RSB0	E12	IO38RSB0	H7	VCCIB3

281-Pin CSP		281-Pin CSP		281-Pin CSP	
Pin Number	AGLP125 Function	Pin Number	AGLP125 Function	Pin Number	AGLP125 Function
H8	VCC	K15	IO89RSB1	N4	IO182RSB3
H9	VCCIB0	K16	GND	N5	IO161RSB2
H10	VCC	K18	IO88RSB1	N7	GEA2/IO164RSB2
H11	VCCIB0	K19	VCCIB1	N8	VCCIB2
H12	VCC	L1	GFB2/IO187RSB3	N9	IO137RSB2
H13	VCCIB1	L2	IO185RSB3	N10	IO135RSB2
H15	IO77RSB1	L4	GFC2/IO186RSB3	N11	IO131RSB2
H16	GCB0/IO82RSB1	L5	IO184RSB3	N12	VCCIB2
H18	GCA1/IO83RSB1	L7	IO199RSB3	N13	VPUMP
H19	GCA2/IO85RSB1	L8	VCCIB3	N15	IO117RSB2
J1	VCOMPLF	L9	GND	N16	IO96RSB1
J2	GFA0/IO189RSB3	L10	GND	N18	IO98RSB1
J4	VCCPLF	L11	GND	N19	IO94RSB1
J5	GFC0/IO193RSB3	L12	VCCIB1	P1	IO174RSB3
J7	GFA2/IO188RSB3	L13	IO95RSB1	P2	GND
J8	VCCIB3	L15	IO91RSB1	P3	IO176RSB3
J9	GND	L16	NC	P4	IO177RSB3
J10	GND	L18	IO90RSB1	P5	GEA0/IO165RSB3
J11	GND	L19	NC	P15	IO111RSB2
J12	VCCIB1	M1	IO180RSB3	P16	IO108RSB2
J13	GCC1/IO79RSB1	M2	IO179RSB3	P17	GDC1/IO99RSB1
J15	GCA0/IO84RSB1	M4	IO181RSB3	P18	GND
J16	GCB2/IO86RSB1	M5	IO183RSB3	P19	IO97RSB1
J18	IO76RSB1	M7	VCCIB3	R1	IO173RSB3
J19	IO78RSB1	M8	VCC	R2	IO172RSB3
K1	VCCIB3	M9	VCCIB2	R4	GEC1/IO170RSB3
K2	GFA1/IO190RSB3	M10	VCC	R5	GEB1/IO168RSB3
K4	GND	M11	VCCIB2	R6	IO154RSB2
K5	IO19RSB0	M12	VCC	R7	IO149RSB2
K7	IO197RSB3	M13	VCCIB1	R8	IO146RSB2
K8	VCC	M15	IO122RSB2	R9	IO138RSB2
K9	GND	M16	IO93RSB1	R10	IO134RSB2
K10	GND	M18	IO92RSB1	R11	IO132RSB2
K11	GND	M19	NC	R12	IO130RSB2
K12	VCC	N1	IO178RSB3	R13	IO118RSB2
K13	GCC2/IO87RSB1	N2	IO175RSB3	R14	IO112RSB2

281-Pin CSP	
Pin Number	AGLP125 Function
R15	IO109RSB2
R16	GDA1/IO103RSB1
R18	GDB0/IO102RSB1
R19	GDC0/IO100RSB1
T1	IO171RSB3
T2	GEC0/IO169RSB3
T4	GEB0/IO167RSB3
T5	IO157RSB2
T6	IO158RSB2
T7	IO148RSB2
T8	IO145RSB2
T9	IO143RSB2
T10	GND
T11	IO129RSB2
T12	IO126RSB2
T13	IO125RSB2
T14	IO116RSB2
T15	GDC2/IO107RSB2
T16	TMS
T18	VJTAG
T19	GDB1/IO101RSB1
U1	IO160RSB2
U2	GEA1/IO166RSB3
U6	IO151RSB2
U14	IO121RSB2
U18	TRST
U19	GDA0/IO104RSB1
V1	IO159RSB2
V2	VCCIB3
V3	GEC2/IO162RSB2
V4	IO156RSB2
V5	IO153RSB2
V6	GND
V7	IO144RSB2
V8	IO141RSB2
V9	IO140RSB2

281-Pin CSP	
Pin Number	AGLP125 Function
V10	IO133RSB2
V11	IO127RSB2
V12	IO123RSB2
V13	IO120RSB2
V14	GND
V15	IO113RSB2
V16	GDA2/IO105RSB2
V17	TDI
V18	VCCIB2
V19	TDO
W1	GND
W2	FF/GEB2/IO163RSB 2
W3	IO155RSB2
W4	IO152RSB2
W5	IO150RSB2
W6	IO147RSB2
W7	IO142RSB2
W8	IO139RSB2
W9	IO136RSB2
W10	VCCIB2
W11	IO128RSB2
W12	IO124RSB2
W13	IO119RSB2
W14	IO115RSB2
W15	IO114RSB2
W16	IO110RSB2
W17	GDB2/IO106RSB2
W18	TCK
W19	GND

289-Pin CSP



Note: This is the bottom view of the package.

Note

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289-Pin CSP	
Pin Number	AGLP030 Function
A1	IO03RSB0
A2	NC
A3	NC
A4	GND
A5	IO10RSB0
A6	IO14RSB0
A7	IO16RSB0
A8	IO18RSB0
A9	GND
A10	IO23RSB0
A11	IO27RSB0
A12	NC
A13	NC
A14	GND
A15	NC
A16	NC
A17	IO30RSB0
B1	IO01RSB0
B2	GND
B3	NC
B4	NC
B5	IO07RSB0
B6	NC
B7	VCCIB0
B8	IO17RSB0
B9	IO19RSB0
B10	IO24RSB0
B11	IO28RSB0
B12	VCCIB0
B13	NC
B14	NC
B15	NC
B16	IO31RSB0
B17	GND
C1	NC
C2	IO00RSB0
C3	IO04RSB0

289-Pin CSP	
Pin Number	AGLP030 Function
C4	NC
C5	VCCIB0
C6	IO09RSB0
C7	IO13RSB0
C8	IO15RSB0
C9	IO21RSB0
C10	GND
C11	IO29RSB0
C12	NC
C13	NC
C14	NC
C15	GND
C16	IO34RSB0
C17	NC
D1	NC
D2	IO119RSB3
D3	GND
D4	IO02RSB0
D5	NC
D6	NC
D7	NC
D8	GND
D9	IO20RSB0
D10	IO25RSB0
D11	NC
D12	NC
D13	GND
D14	IO32RSB0
D15	IO35RSB0
D16	NC
D17	NC
E1	VCCIB3
E2	IO114RSB3
E3	IO115RSB3
E4	IO118RSB3
E5	IO05RSB0
E6	NC

289-Pin CSP	
Pin Number	AGLP030 Function
E7	IO06RSB0
E8	IO11RSB0
E9	IO22RSB0
E10	IO26RSB0
E11	VCCIB0
E12	NC
E13	IO33RSB0
E14	IO36RSB1
E15	IO38RSB1
E16	VCCIB1
E17	NC
F1	IO111RSB3
F2	NC
F3	IO116RSB3
F4	VCCIB3
F5	IO117RSB3
F6	NC
F7	NC
F8	IO08RSB0
F9	IO12RSB0
F10	NC
F11	NC
F12	NC
F13	NC
F14	GND
F15	NC
F16	IO37RSB1
F17	IO41RSB1
G1	IO110RSB3
G2	GND
G3	IO113RSB3
G4	NC
G5	NC
G6	NC
G7	GND
G8	GND
G9	VCC

289-Pin CSP		289-Pin CSP		289-Pin CSP	
Pin Number	AGLP030 Function	Pin Number	AGLP030 Function	Pin Number	AGLP030 Function
G10	GND	J13	IO43RSB1	L16	NC
G11	GND	J14	IO51RSB1	L17	NC
G12	IO40RSB1	J15	IO52RSB1	M1	NC
G13	NC	J16	GDC0/IO46RSB1	M2	VCCIB3
G14	IO39RSB1	J17	GDA0/IO47RSB1	M3	IO100RSB3
G15	IO44RSB1	K1	GND	M4	IO98RSB3
G16	NC	K2	GEB0/IO106RSB3	M5	IO93RSB3
G17	GND	K3	IO102RSB3	M6	IO97RSB3
H1	NC	K4	IO104RSB3	M7	NC
H2	GEC0/IO108RSB3	K5	IO99RSB3	M8	NC
H3	NC	K6	NC	M9	IO71RSB2
H4	IO112RSB3	K7	GND	M10	NC
H5	NC	K8	GND	M11	IO63RSB2
H6	IO109RSB3	K9	GND	M12	NC
H7	GND	K10	GND	M13	IO57RSB1
H8	GND	K11	GND	M14	NC
H9	GND	K12	NC	M15	NC
H10	GND	K13	NC	M16	NC
H11	GND	K14	NC	M17	VCCIB1
H12	NC	K15	IO53RSB1	N1	NC
H13	NC	K16	GND	N2	NC
H14	IO45RSB1	K17	IO49RSB1	N3	IO95RSB3
H15	VCCIB1	L1	IO103RSB3	N4	IO96RSB3
H16	GDB0/IO48RSB1	L2	IO101RSB3	N5	GND
H17	IO42RSB1	L3	NC	N6	NC
J1	NC	L4	GND	N7	IO85RSB2
J2	GEA0/IO107RSB3	L5	NC	N8	IO79RSB2
J3	VCCIB3	L6	NC	N9	IO77RSB2
J4	IO105RSB3	L7	GND	N10	VCCIB2
J5	NC	L8	GND	N11	NC
J6	NC	L9	VCC	N12	NC
J7	VCC	L10	GND	N13	IO59RSB2
J8	GND	L11	GND	N14	NC
J9	GND	L12	IO58RSB1	N15	GND
J10	GND	L13	IO54RSB1	N16	IO56RSB1
J11	VCC	L14	VCCIB1	N17	IO55RSB1
J12	IO50RSB1	L15	NC	P1	IO94RSB3

289-Pin CSP	
Pin Number	AGLP030 Function
P2	NC
P3	GND
P4	NC
P5	NC
P6	IO87RSB2
P7	IO80RSB2
P8	GND
P9	IO72RSB2
P10	IO67RSB2
P11	IO61RSB2
P12	NC
P13	VCCIB2
P14	NC
P15	IO60RSB2
P16	IO62RSB2
P17	VJTAG
R1	GND
R2	IO91RSB2
R3	NC
R4	NC
R5	NC
R6	VCCIB2
R7	IO83RSB2
R8	IO78RSB2
R9	IO74RSB2
R10	IO70RSB2
R11	GND
R12	NC
R13	NC
R14	NC
R15	NC
R16	TMS
R17	TRST
T1	IO92RSB3
T2	IO89RSB2
T3	NC
T4	GND

289-Pin CSP	
Pin Number	AGLP030 Function
T5	NC
T6	IO84RSB2
T7	IO81RSB2
T8	IO76RSB2
T9	VCCIB2
T10	IO69RSB2
T11	IO65RSB2
T12	IO64RSB2
T13	NC
T14	GND
T15	NC
T16	TDI
T17	TDO
U1	FF/IO90RSB2
U2	GND
U3	NC
U4	IO88RSB2
U5	IO86RSB2
U6	IO82RSB2
U7	GND
U8	IO75RSB2
U9	IO73RSB2
U10	IO68RSB2
U11	IO66RSB2
U12	GND
U13	NC
U14	NC
U15	NC
U16	TCK
U17	VPUMP

289-Pin CSP		289-Pin CSP		289-Pin CSP	
Pin Number	AGLP060 Function	Pin Number	AGLP060 Function	Pin Number	AGLP060 Function
A1	GAB1/IO03RSB0	C5	VCCIB0	E9	IO22RSB0
A2	NC	C6	IO09RSB0	E10	IO26RSB0
A3	NC	C7	IO13RSB0	E11	VCCIB0
A4	GND	C8	IO15RSB0	E12	NC
A5	IO10RSB0	C9	IO21RSB0	E13	GBB1/IO33RSB0
A6	IO14RSB0	C10	GND	E14	GBA2/IO36RSB1
A7	IO16RSB0	C11	IO29RSB0	E15	GBB2/IO38RSB1
A8	IO18RSB0	C12	NC	E16	VCCIB1
A9	GND	C13	NC	E17	IO44RSB1
A10	IO23RSB0	C14	NC	F1	GFC1/IO140RSB3
A11	IO27RSB0	C15	GND	F2	IO142RSB3
A12	NC	C16	GBA0/IO34RSB0	F3	IO149RSB3
A13	NC	C17	IO39RSB1	F4	VCCIB3
A14	GND	D1	IO150RSB3	F5	GAB2/IO154RSB3
A15	NC	D2	IO151RSB3	F6	IO153RSB3
A16	NC	D3	GND	F7	NC
A17	GBC0/IO30RSB0	D4	GAB0/IO02RSB0	F8	IO08RSB0
B1	GAA1/IO01RSB0	D5	NC	F9	IO12RSB0
B2	GND	D6	NC	F10	NC
B3	NC	D7	NC	F11	NC
B4	NC	D8	GND	F12	NC
B5	IO07RSB0	D9	IO20RSB0	F13	GBC2/IO40RSB1
B6	NC	D10	IO25RSB0	F14	GND
B7	VCCIB0	D11	NC	F15	IO43RSB1
B8	IO17RSB0	D12	NC	F16	IO46RSB1
B9	IO19RSB0	D13	GND	F17	IO45RSB1
B10	IO24RSB0	D14	GBB0/IO32RSB0	G1	GFC0/IO139RSB3
B11	IO28RSB0	D15	GBA1/IO35RSB0	G2	GND
B12	VCCIB0	D16	IO37RSB1	G3	IO144RSB3
B13	NC	D17	IO42RSB1	G4	IO145RSB3
B14	NC	E1	VCCIB3	G5	IO146RSB3
B15	NC	E2	IO147RSB3	G6	IO148RSB3
B16	GBC1/IO31RSB0	E3	GAC2/IO152RSB3	G7	GND
B17	GND	E4	GAA2/IO156RSB3	G8	GND
C1	IO155RSB3	E5	GAC1/IO05RSB0	G9	VCC
C2	GAA0/IO00RSB0	E6	NC	G10	GND
C3	GAC0/IO04RSB0	E7	IO06RSB0	G11	GND
C4	NC	E8	IO11RSB0	G12	IO48RSB1

289-Pin CSP		289-Pin CSP		289-Pin CSP	
Pin Number	AGLP060 Function	Pin Number	AGLP060 Function	Pin Number	AGLP060 Function
G13	IO41RSB1	J17	GCA1/IO56RSB1	M4	IO122RSB3
G14	IO47RSB1	K1	GND	M5	GEB0/IO113RSB3
G15	IO49RSB1	K2	GFA0/IO135RSB3	M6	GEB1/IO114RSB3
G16	IO50RSB1	K3	GFB2/IO133RSB3	M7	NC
G17	GND	K4	IO128RSB3	M8	NC
H1	VCOMPLF	K5	IO123RSB3	M9	IO90RSB2
H2	GFB0/IO137RSB3	K6	IO125RSB3	M10	NC
H3	NC	K7	GND	M11	IO83RSB2
H4	IO141RSB3	K8	GND	M12	NC
H5	IO143RSB3	K9	GND	M13	GDA1/IO76RSB1
H6	GFB1/IO138RSB3	K10	GND	M14	GDA0/IO77RSB1
H7	GND	K11	GND	M15	IO71RSB1
H8	GND	K12	IO64RSB1	M16	IO69RSB1
H9	GND	K13	IO61RSB1	M17	VCCIB1
H10	GND	K14	IO66RSB1	N1	IO119RSB3
H11	GND	K15	IO65RSB1	N2	IO120RSB3
H12	GCC1/IO52RSB1	K16	GND	N3	GEC0/IO115RSB3
H13	IO51RSB1	K17	GCC2/IO60RSB1	N4	GEA0/IO111RSB3
H14	GCA0/IO57RSB1	L1	GFA2/IO134RSB3	N5	GND
H15	VCCIB1	L2	GFC2/IO132RSB3	N6	NC
H16	GCA2/IO58RSB1	L3	IO127RSB3	N7	IO104RSB2
H17	GCC0/IO53RSB1	L4	GND	N8	IO98RSB2
J1	VCCPLF	L5	IO121RSB3	N9	IO96RSB2
J2	GFA1/IO136RSB3	L6	GEC1/IO116RSB3	N10	VCCIB2
J3	VCCIB3	L7	GND	N11	NC
J4	IO131RSB3	L8	GND	N12	NC
J5	IO130RSB3	L9	VCC	N13	GDB2/IO79RSB2
J6	IO129RSB3	L10	GND	N14	NC
J7	VCC	L11	GND	N15	GND
J8	GND	L12	GDC1/IO72RSB1	N16	GDB0/IO75RSB1
J9	GND	L13	GDB1/IO74RSB1	N17	GDC0/IO73RSB1
J10	GND	L14	VCCIB1	P1	IO118RSB3
J11	VCC	L15	IO70RSB1	P2	IO117RSB3
J12	GCB2/IO59RSB1	L16	IO68RSB1	P3	GND
J13	GCB1/IO54RSB1	L17	IO67RSB1	P4	NC
J14	IO62RSB1	M1	IO126RSB3	P5	NC
J15	IO63RSB1	M2	VCCIB3	P6	IO106RSB2
J16	GCB0/IO55RSB1	M3	IO124RSB3	P7	IO99RSB2

289-Pin CSP		289-Pin CSP	
Pin Number	AGLP060 Function	Pin Number	AGLP060 Function
P8	GND	T12	IO82RSB2
P9	IO91RSB2	T13	NC
P10	IO86RSB2	T14	GND
P11	IO81RSB2	T15	NC
P12	NC	T16	TDI
P13	VCCIB2	T17	TDO
P14	NC	U1	FF/GEB2/IO109RSB2
P15	GDA2/IO78RSB2	U2	GND
P16	GDC2/IO80RSB2	U3	NC
P17	VJTAG	U4	IO107RSB2
R1	GND	U5	IO105RSB2
R2	GEA2/IO110RSB2	U6	IO101RSB2
R3	NC	U7	GND
R4	NC	U8	IO94RSB2
R5	NC	U9	IO92RSB2
R6	VCCIB2	U10	IO87RSB2
R7	IO102RSB2	U11	IO85RSB2
R8	IO97RSB2	U12	GND
R9	IO93RSB2	U13	NC
R10	IO89RSB2	U14	NC
R11	GND	U15	NC
R12	NC	U16	TCK
R13	NC	U17	VPUMP
R14	NC		
R15	NC		
R16	TMS		
R17	TRST		
T1	GEA1/IO112RSB3		
T2	GEC2/IO108RSB2		
T3	NC		
T4	GND		
T5	NC		
T6	IO103RSB2		
T7	IO100RSB2		
T8	IO95RSB2		
T9	VCCIB2		
T10	IO88RSB2		
T11	IO84RSB2		

289-Pin CSP		289-Pin CSP		289-Pin CSP	
Pin Number	AGLP125 Function	Pin Number	AGLP125 Function	Pin Number	AGLP125 Function
A1	GAB1/IO03RSB0	C5	VCCIB0	E9	IO32RSB0
A2	IO11RSB0	C6	IO17RSB0	E10	IO36RSB0
A3	IO08RSB0	C7	IO23RSB0	E11	VCCIB0
A4	GND	C8	IO27RSB0	E12	IO56RSB0
A5	IO19RSB0	C9	IO33RSB0	E13	GBB1/IO60RSB0
A6	IO24RSB0	C10	GND	E14	GBA2/IO63RSB1
A7	IO26RSB0	C11	IO43RSB0	E15	GBB2/IO65RSB1
A8	IO30RSB0	C12	IO45RSB0	E16	VCCIB1
A9	GND	C13	IO50RSB0	E17	IO73RSB1
A10	IO35RSB0	C14	IO52RSB0	F1	GFC1/IO194RSB3
A11	IO38RSB0	C15	GND	F2	IO196RSB3
A12	IO40RSB0	C16	GBA0/IO61RSB0	F3	IO202RSB3
A13	IO42RSB0	C17	IO68RSB1	F4	VCCIB3
A14	GND	D1	IO204RSB3	F5	GAB2/IO209RSB3
A15	IO48RSB0	D2	IO205RSB3	F6	IO208RSB3
A16	IO54RSB0	D3	GND	F7	IO14RSB0
A17	GBC0/IO57RSB0	D4	GAB0/IO02RSB0	F8	IO20RSB0
B1	GAA1/IO01RSB0	D5	IO07RSB0	F9	IO25RSB0
B2	GND	D6	IO10RSB0	F10	IO29RSB0
B3	IO06RSB0	D7	IO18RSB0	F11	IO51RSB0
B4	IO13RSB0	D8	GND	F12	IO53RSB0
B5	IO15RSB0	D9	IO34RSB0	F13	GBC2/IO67RSB1
B6	IO21RSB0	D10	IO41RSB0	F14	GND
B7	VCCIB0	D11	IO47RSB0	F15	IO75RSB1
B8	IO28RSB0	D12	IO55RSB0	F16	IO71RSB1
B9	IO31RSB0	D13	GND	F17	IO77RSB1
B10	IO37RSB0	D14	GBB0/IO59RSB0	G1	GFC0/IO193RSB3
B11	IO39RSB0	D15	GBA1/IO62RSB0	G2	GND
B12	VCCIB0	D16	IO66RSB1	G3	IO198RSB3
B13	IO44RSB0	D17	IO70RSB1	G4	IO203RSB3
B14	IO46RSB0	E1	VCCIB3	G5	IO201RSB3
B15	IO49RSB0	E2	IO200RSB3	G6	IO206RSB3
B16	GBC1/IO58RSB0	E3	GAC2/IO207RSB3	G7	GND
B17	GND	E4	GAA2/IO211RSB3	G8	GND
C1	IO210RSB3	E5	GAC1/IO05RSB0	G9	VCC
C2	GAA0/IO00RSB0	E6	IO12RSB0	G10	GND
C3	GAC0/IO04RSB0	E7	IO16RSB0	G11	GND
C4	IO09RSB0	E8	IO22RSB0	G12	IO72RSB1

289-Pin CSP		289-Pin CSP		289-Pin CSP	
Pin Number	AGLP125 Function	Pin Number	AGLP125 Function	Pin Number	AGLP125 Function
G13	IO64RSB1	J17	GCA1/IO83RSB1	M4	IO172RSB3
G14	IO69RSB1	K1	GND	M5	GEB0/IO167RSB3
G15	IO78RSB1	K2	GFA0/IO189RSB3	M6	GEB1/IO168RSB3
G16	IO76RSB1	K3	GFB2/IO187RSB3	M7	IO159RSB2
G17	GND	K4	IO179RSB3	M8	IO161RSB2
H1	VCOMPLF	K5	IO175RSB3	M9	IO135RSB2
H2	GFB0/IO191RSB3	K6	IO177RSB3	M10	IO128RSB2
H3	IO195RSB3	K7	GND	M11	IO121RSB2
H4	IO197RSB3	K8	GND	M12	IO113RSB2
H5	IO199RSB3	K9	GND	M13	GDA1/IO103RSB1
H6	GFB1/IO192RSB3	K10	GND	M14	GDA0/IO104RSB1
H7	GND	K11	GND	M15	IO97RSB1
H8	GND	K12	IO88RSB1	M16	IO96RSB1
H9	GND	K13	IO94RSB1	M17	VCCIB1
H10	GND	K14	IO95RSB1	N1	IO180RSB3
H11	GND	K15	IO93RSB1	N2	IO178RSB3
H12	GCC1/IO79RSB1	K16	GND	N3	GEC0/IO169RSB3
H13	IO74RSB1	K17	GCC2/IO87RSB1	N4	GEO0/IO165RSB3
H14	GCA0/IO84RSB1	L1	GFA2/IO188RSB3	N5	GND
H15	VCCIB1	L2	GFC2/IO186RSB3	N6	IO156RSB2
H16	GCA2/IO85RSB1	L3	IO182RSB3	N7	IO148RSB2
H17	GCC0/IO80RSB1	L4	GND	N8	IO144RSB2
J1	VCCPLF	L5	IO173RSB3	N9	IO137RSB2
J2	GFA1/IO190RSB3	L6	GEC1/IO170RSB3	N10	VCCIB2
J3	VCCIB3	L7	GND	N11	IO119RSB2
J4	IO185RSB3	L8	GND	N12	IO111RSB2
J5	IO183RSB3	L9	VCC	N13	GDB2/IO106RSB2
J6	IO181RSB3	L10	GND	N14	IO109RSB2
J7	VCC	L11	GND	N15	GND
J8	GND	L12	GDC1/IO99RSB1	N16	GDB0/IO102RSB1
J9	GND	L13	GDB1/IO101RSB1	N17	GDC0/IO100RSB1
J10	GND	L14	VCCIB1	P1	IO174RSB3
J11	VCC	L15	IO98RSB1	P2	IO171RSB3
J12	GCB2/IO86RSB1	L16	IO92RSB1	P3	GND
J13	GCB1/IO81RSB1	L17	IO91RSB1	P4	IO160RSB2
J14	IO90RSB1	M1	IO184RSB3	P5	IO157RSB2
J15	IO89RSB1	M2	VCCIB3	P6	IO154RSB2
J16	GCB0/IO82RSB1	M3	IO176RSB3	P7	IO152RSB2

289-Pin CSP	
Pin Number	AGLP125 Function
P8	GND
P9	IO132RSB2
P10	IO125RSB2
P11	IO126RSB2
P12	IO112RSB2
P13	VCCIB2
P14	IO108RSB2
P15	GDA2/IO105RSB2
P16	GDC2/IO107RSB2
P17	VJTAG
R1	GND
R2	GEA2/IO164RSB2
R3	IO158RSB2
R4	IO155RSB2
R5	IO150RSB2
R6	VCCIB2
R7	IO145RSB2
R8	IO141RSB2
R9	IO134RSB2
R10	IO130RSB2
R11	GND
R12	IO118RSB2
R13	IO116RSB2
R14	IO114RSB2
R15	IO110RSB2
R16	TMS
R17	TRST
T1	GEA1/IO166RSB3
T2	GEC2/IO162RSB2
T3	IO153RSB2
T4	GND
T5	IO147RSB2
T6	IO143RSB2
T7	IO140RSB2
T8	IO139RSB2
T9	VCCIB2
T10	IO131RSB2
T11	IO127RSB2

289-Pin CSP	
Pin Number	AGLP125 Function
T12	IO124RSB2
T13	IO122RSB2
T14	GND
T15	IO115RSB2
T16	TDI
T17	TDO
U1	FF/GEB2/IO163RSB2
U2	GND
U3	IO151RSB2
U4	IO149RSB2
U5	IO146RSB2
U6	IO142RSB2
U7	GND
U8	IO138RSB2
U9	IO136RSB2
U10	IO133RSB2
U11	IO129RSB2
U12	GND
U13	IO123RSB2
U14	IO120RSB2
U15	IO117RSB2
U16	TCK
U17	VPUMP

4 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the IGLOO PLUS datasheet.

Revision	Changes	Page
Revision 11 (Jun 2009)	The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "IGLOO PLUS Device Status" table indicates the status for each device in the family.	N/A
	The "Reprogrammable Flash Technology" section was revised to add "250 MHz (1.5 V systems) and 160 MHz (1.2 V systems) System Performance."	I
	The "I/Os with Advanced I/O Standards" section was revised to add definitions for hot-swap and cold-sparing.	1-7
	Conditional statements regarding hot insertion were removed from the description of VI in Table 2-1 • Absolute Maximum Ratings, since all IGLOO PLUS devices are hot insertion enabled.	2-1
	Table 2-2 • Recommended Operating Conditions ^{1,2} was revised. 1.2 V DC wide range supply voltage and 3.3 V wide range supply voltage (SAR 26270) were added for VCCI. VJTAG DC Voltage was revised (SAR 24052). The value range for VPUMP programming voltage for operation was changed from "0 to 3.45" to "0 to 3.6" (SAR 25220).	2-2
	Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to TJ = 70°C, VCC = 1.425 V) and Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to TJ = 70°C, VCC = 1.14 V) were revised.	2-6, 2-7
	Table 2-8 • Power Supply State per Mode is new.	2-7
	The tables in the "Quiescent Supply Current" section were updated (SARs 24882 and 24112). Some of the table notes were changed or deleted.	2-7
VIH maximum values in tables were updated as needed to 3.6 V (SAR 20990 and SAR 79370).	N/A	

Revision	Changes	Page
Revision 11 (continued)	<p>The values in the following tables were updated. 3.3 V LVCMOS and 1.2 V LVCMOS wide range were added to the tables where applicable.</p> <p>Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings</p> <p>Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings¹</p> <p>Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings</p> <p>Table 2-22 • Summary of Maximum and Minimum DC Input Levels</p> <p>Table 2-23 • Summary of AC Measuring Points</p> <p>Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V</p> <p>Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V</p> <p>Table 2-28 • I/O Output Buffer Maximum Resistances 1</p>	<p>2-9</p> <p>2-9</p> <p>2-19</p> <p>2-20</p> <p>2-21</p> <p>2-22</p> <p>2-23</p> <p>2-24</p>
	<p>A table note was added to Table 2-16 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices and Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices stating the value for PDC4 is the minimum contribution of the PLL when operating at lowest frequency.</p>	<p>2-11, 2-12</p>
	<p>Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances was revised, including addition of 3.3 V and 1.2 V LVCMOS wide range. The notes defining R_{WEAK PULL-UP-MAX} and R_{WEAK PULLDOWN-MAX} were revised (SAR 21348).</p>	<p>2-25</p>
	<p>Table 2-30 • I/O Short Currents IOSH/IOSL was revised to include data for 3.3 V and 1.2 V LVCMOS wide range (SAR 79353 and SAR 79366).</p>	<p>2-25</p>
	<p>Table 2-31 • Duration of Short Circuit Event before Failure was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months (SAR 26259).</p>	<p>2-26</p>
	<p>The tables in the "Single-Ended I/O Characteristics" section were updated. Notes clarifying I_{IL} and I_{IH} were added.</p> <p>Tables for 3.3 V LVCMOS and 1.2 V LVCMOS wide range were added (SAR 79370, SAR 79353, and SAR 79366).</p> <p>Notes in the wide range tables state that the minimum drive strength for any LVCMOS 3.3 V (or LVCMOS 1.2 V) software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models (SAR 25700).</p>	<p>2-27</p>
	<p>The following sentence was deleted from the "2.5 V LVCMOS" section: It uses a 5 V–tolerant input buffer and push-pull output buffer (SAR 24916).</p>	<p>2-32</p>
	<p>The tables in the "Input Register" section, "Output Register" section, and "Output Enable Register" section were updated. The tables in the "VersaTile Characteristics" section were updated.</p>	<p>2-45 through 2-56</p>

Revision	Changes	Page
Revision 11 (continued)	The following tables were updated in the "Global Tree Timing Characteristics" section: Table 2-85 • AGLP060 Global Resource (1.5 V) Table 2-86 • AGLP125 Global Resource (1.5 V) Table 2-88 • AGLP060 Global Resource (1.2 V)	2-58
	Table 2-90 • IGLOO PLUS CCC/PLL Specification and Table 2-91 • IGLOO PLUS CCC/PLL Specification were revised (SAR 79388). VCO output jitter and maximum peak-to-peak jitter data were changed. Three notes were added to the table in connection with these changes.	2-61
	Figure 2-28 • Write Access after Write onto Same Address and Figure 2-29 • Write Access after Read onto Same Address were deleted.	N/A
	The tables in the "SRAM", "FIFO" and "Embedded FlashROM Characteristics" sections were updated.	2-68, 2-77
Revision 10 (Apr 2009) Product Brief v1.5 DC and Switching Characteristics Advance v0.5	The –F speed grade is no longer offered for IGLOO PLUS devices. References to it have been removed from the document. The speed grade column and note regarding –F speed grade were removed from "IGLOO PLUS Ordering Information". The "Speed Grade and Temperature Grade Matrix" section was removed.	III, IV
Revision 9 (Feb 2009) Product Brief v1.4	The "Advanced I/O" section was revised to add two bullets regarding support of wide range power supply voltage.	I
	The "I/Os with Advanced I/O Standards" section was revised to add 3.0 V wide range to the list of supported voltages. The "Wide Range I/O Support" section is new.	1-7
Revision 8 (Jan 2009) Packaging v1.5	The "201-Pin CSP" pin table was revised to add a note regarding pins G1 and H1.	3-8
Revision 7 (Dec 2008) Product Brief v1.3	A note was added to IGLOO PLUS Devices: "AGLP060 in CS201 does not support the PLL."	I
	Table 2 • IGLOO PLUS FPGAs Package Size Dimensions was updated to change the nominal size of VQ176 from 100 to 400 mm ² .	II
Revision 6 (Oct 2008) DC and Switching Characteristics Advance v0.4	Data was revised significantly in the following tables: Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade, Commercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade Commercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V Table 2-50 • 2.5 LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage Table 2-51 • 2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage	2-22, 2-33
Revision 5 (Aug 2008) Product Brief v1.2 Packaging v1.4	The VQ128 and VQ176 packages were added to Table 1 • IGLOO PLUS Product Family, the "I/Os Per Package 1" table, Table 2 • IGLOO PLUS FPGAs Package Size Dimensions, "IGLOO PLUS Ordering Information", and the "Temperature Grade Offerings" table.	I to IV
	The "128-Pin VQFP" package drawing and pin table are new.	3-2
	The "176-Pin VQFP" package drawing and pin table are new.	3-5

Revision	Changes	Page
Revision 4 (Jul 2008) Product Brief v1.1 DC and Switching Characteristics Advance v0.3	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2 V / 1.5 V to 1.2 V to 1.5 V.	N/A
Revision 3 (Jun 2008) DC and Switching Characteristics Advance v0.2	Tables have been updated to reflect default values in the software. The default I/O capacitance is 5 pF. Tables have been updated to include the LVCMOS 1.2 V I/O set.	N/A
	Table note 3 was updated in Table 2-2 • Recommended Operating Conditions ^{1,2} to add the sentence, "V _{CCI} should be at the same voltage within a given I/O bank." References to table notes 5, 6, 7, and 8 were added. Reference to table note 3 was removed from V _{PUMP} Operation and placed next to V _{CC} .	2-2
	Table 2-4 • Overshoot and Undershoot Limits 1 was revised to remove "as measured on quiet I/Os" from the title. Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was deleted.	2-3
	The table note for Table 2-9 • Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Flash*Freeze Mode* to remove the sentence stating that values do not include I/O static contribution.	2-7
	The table note for Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Sleep Mode* was updated to remove V _{JTAG} and V _{CCI} and the statement that values do not include I/O static contribution.	2-7
	The table note for Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Shutdown Mode was updated to remove the statement that values do not include I/O static contribution.	2-8
	Note 2 of Table 2-12 • Quiescent Supply Current (IDD), No IGLOO PLUS Flash*Freeze Mode 1 was updated to include V _{CCPLL} . Table note 4 was deleted.	2-8
	Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings and Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings ¹ were updated to remove static power. The table notes were updated to reflect that power was measured on V _{CCI} . Table note 2 was added to Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings .	2-9, 2-9
	Table 2-16 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices and Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices were updated to change the definition for P _{DC5} from bank static power to bank quiescent power. Table subtitles were added for Table 2-16 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices , Table 2-17 • Different Components Contributing to Dynamic Power Consumption in IGLOO PLUS Devices , and Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices .	2-11, 2-12
	The "Total Static Power Consumption—PSTAT" section was revised.	2-12
	Table 2-32 • Schmitt Trigger Input Hysteresis is new.	2-26
Packaging v1.3	The "281-Pin CSP" package drawing is new.	3-13
	The "281-Pin CSP" table for the AGLP125 device is new.	3-13

Revision	Changes	Page
Revision 3 (continued)	The "289-Pin CSP" package drawing was incorrect. The graphic was showing the CS281 mechanical drawing and not the CS289 mechanical drawing. This has now been corrected.	3-17
Revision 2 (Jun 2008) Packaging v1.2	The "289-Pin CSP" table for the AGLP030 device is new.	3-17
Revision 1 (Jun 2008) Packaging v1.1	The "289-Pin CSP" table for the AGLP060 device is new.	3-20
	The "289-Pin CSP" table for the AGLP125 device is new.	3-23

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "IGLOO PLUS Device" table on page II, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

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The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Unmarked (production)

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