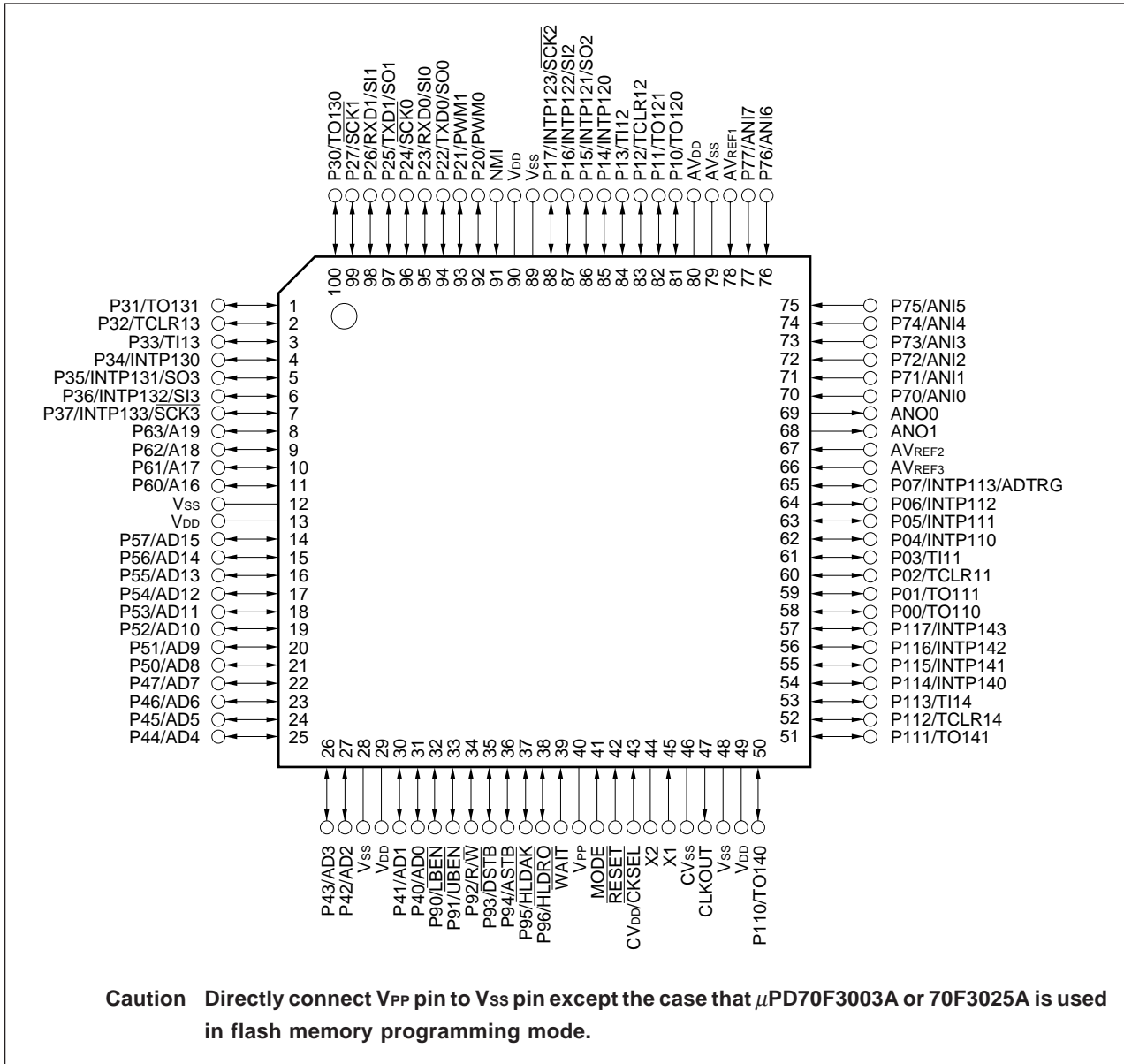


PIN CONFIGURATION (Top View)

- 100-Pin Plastic LQFP (fine pitch) (14 × 14 mm)

μPD70F3003AGC-xx-8EU

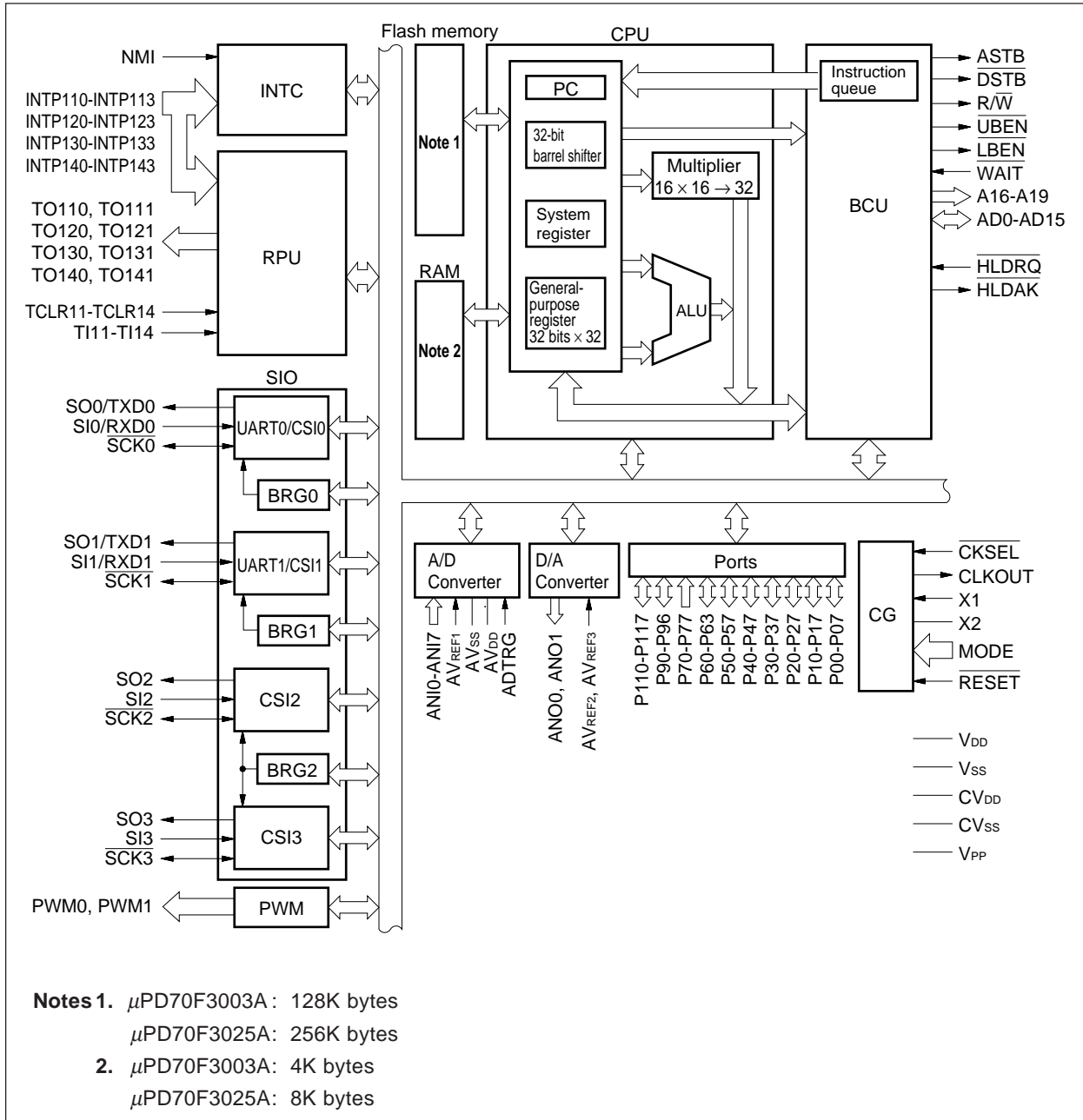
μPD70F3025AGC-xx-8EU



PIN NAMES

A16-A19	: Address Bus	P40-P47	: Port4
AD0-AD15	: Address/Data Bus	P50-P57	: Port5
ADTRG	: AD Trigger Input	P60-P63	: Port6
ANI0-ANI7	: Analog Input	P70-P77	: Port7
ANO0, ANO1	: Analog Output	P90-P96	: Port9
ASTB	: Address Strobe	P110-P117	: Port11
AV _{DD}	: Analog V _{DD}	PWM0, PWM1	: Pulse Width Modulation
AV _{REF1} -AV _{REF3}	: Analog Reference Voltage	RESET	: Reset
AV _{SS}	: Analog V _{SS}	R/W	: Read/Write Status
CV _{DD}	: Power Supply for Clock Generator	RXD0, PXD1	: Receive Data
CV _{SS}	: Ground for Clock Generator	SCK0-SCK3	: Serial Clock
CKSEL	: Clock Select	SI0-SI3	: Serial Input
CLKOUT	: Clock Output	SO0-SO3	: Serial Output
DSTB	: Data Strobe	TO110, TO111,	: Timer Output
HLD _{AK}	: Hold Acknowledge	TO120, TO121,	
HLDRQ	: Hold Request	TO130, TO131,	
INTP110-INTP113,	: Interrupt Request from Peripherals	TO140, TO141	
INTP120-INTP123,		TCLR11-TCLR14	: Timer Clear
INTP130-INTP133,		TI11-TI14	: Timer Input
INTP140-INTP143		TXD0, TXD1	: Transmit Data
L _{BEN}	: Lower Byte Enable	U _{BEN}	: Upper Byte Enable
MODE	: Mode	WAIT	: Wait
NMI	: Non-maskable Interrupt Request	X1, X2	: Crystal
P00-P07	: Port0	V _{DD}	: Power Supply
P10-P17	: Port1	V _{PP}	: Programming Power Supply
P20-P27	: Port2	V _{SS}	: Ground
P30-P37	: Port3		

INTERNAL BLOCK DIAGRAM



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1. DIFFERENCES AMONG PRODUCTS

Parameter			μPD703003	μPD703003A	μPD703004A	μPD703025A	μPD70F3003	μPD70F3003A	μPD70F3025A	
Internal ROM			Mask ROM				Flash memory			
			128K bytes		96K bytes	256K bytes	128K bytes		256K bytes	
Internal RAM			4K bytes			8K bytes	4K bytes		8K bytes	
Operation mode	Normal operation mode	Single chip mode	Provided							
		ROM-less mode	Provided	None			Provided	None		
	Flash memory programming mode		None				Provided			
V _{PP} pin			None				Provided			
CKC register value at reset			00H	MODE = 0: 03H MODE = 1: 00H			00H	MODE = 0: 03H MODE = 1: 00H		
Electrical specifications			Current consumption, etc. differs. (Refer to each product data sheets.)							
Others			Noise immunity and noise radiation differ because circuit scale and mask layout differ.							

2. PIN FUNCTIONS

2.1 Port Pins

(1/2)

Pin Name	I/O	Function	Shared with:
P00	I/O	Port 0 8-bit I/O port. Can be set in input or output mode in 1-bit units.	TO110
P01			TO111
P02			TCLR11
P03			TI11
P04			INTP110
P05			INTP111
P06			INTP112
P07			INTP113/ADTRG
P10	I/O	Port 1 8-bit I/O port. Can be set in input or output mode in 1-bit units.	TO120
P11			TO121
P12			TCLR12
P13			TI12
P14			INTP120
P15			INTP121/SO2
P16			INTP122/SI2
P17			INTP123/SCK2
P20	I/O	Port 2 8-bit I/O port. Can be set in input or output mode in 1-bit units.	PWM0
P21			PWM1
P22			TXD0/SO0
P23			RXD0/SI0
P24			SCK0
P25			TXD1/SO1
P26			RXD1/SI1
P27			SCK1
P30	I/O	Port 3 8-bit I/O port. Can be set in input or output mode in 1-bit units.	TO130
P31			TO131
P32			TCLR13
P33			TI13
P34			INTP130
P35			INTP131/SO3
P36			INTP132/SI3
P37			INTP133/SCK3
P40-P47	I/O	Port 4 8-bit I/O port. Can be set in input or output mode in 1-bit units.	AD0-AD7
P50-P57	I/O	Port 5 8-bit I/O port. Can be set in input or output mode in 1-bit units.	AD8-AD15

(2/2)

Pin Name	I/O	Function	Shared with:
P60-P63	I/O	Port 6 4-bit I/O port. Can be set in input or output mode in 1-bit units.	A16-A19
P70-P77	Input	Port 7 8-bit input port.	ANI0-ANI7
P90	I/O	Port 9 7-bit I/O port. Can be set in input or output mode in 1-bit units.	$\overline{\text{LBEN}}$
P91			$\overline{\text{UBEN}}$
P92			$\overline{\text{R/W}}$
P93			$\overline{\text{DSTB}}$
P94			$\overline{\text{ASTB}}$
P95			$\overline{\text{HLD\text{A}K}}$
P96			$\overline{\text{HLDRQ}}$
P110	I/O	Port 11 8-bit I/O port. Can be set in input or output mode in 1-bit units.	TO140
P111			TO141
P112			TCLR14
P113			TI14
P114			INTP140
P115			INTP141
P116			INTP142
P117			INTP143

2.2 Pins Other Than Port Pins

(1/2)

Pin Name	I/O	Function	Shared with:
TO110	Output	Pulse signal output of timer 11-14	P00
TO111			P01
TO120			P10
TO121			P11
TO130			P30
TO131			P31
TO140			P110
TO141			P111
TCLR11	Input	External clear signal of timer 11-14	P02
TCLR12			P12
TCLR13			P32
TCLR14			P112
TI11	Input	External count clock of timer 11-14	P03
TI12			P13
TI13			P33
TI14			P113
INTP110	Input	External maskable interrupt reuest input and external capture trigger input of timer 11	P04
INTP111			P05
INTP112			P06
INTP113			P07/ADTRG
INTP120	Input	External maskable interrupt reuest input and external capture trigger input of timer 12	P14
INTP121			P15/SO2
INTP122			P16/S12
INTP123			P17/ $\overline{\text{SCK2}}$
INTP130	Input	External maskable interrupt reuest input and external capture trigger input of timer 13	P34
INTP131			P35/SO3
INTP132			P36/SI3
INTP133			P37/ $\overline{\text{SCK3}}$
INTP140	Input	External maskable interrupt reuest input and external capture trigger input of timer 14	P114
INTP141			P115
INTP142			P116
INTP143			P117
SO0	Output	Serial transmit data output of CSI0-CSI3 (3 wire)	P22/TXD0
SO1			P25/TXD1
SO2			P15/INTP121
SO3			P35/INTP131
SI0	Input	Serial receive data output of CSI0-CSI3 (3 wire)	P23/RXD0
SI1			P26/RXD1
SI2			P16/INTP122
SI3			P36/INTP132

(2/2)

Pin Name	I/O	Function	Shared with:
$\overline{\text{SCK0}}$	I/O	Serial clock I/O of CSI0-CSI3 (3 wire)	P24
$\overline{\text{SCK1}}$			P27
$\overline{\text{SCK2}}$			P17/INTP123
$\overline{\text{SCK3}}$			P37/INTP133
TXD0	Output	Serial transmit data output of UART0-UART1	P22/SO0
TXD1			P25/SO1
RXD0	Input	Serial receive data input of UART0-UART1	P23/SI0
RXD1			P26/SI1
PWM0	Output	Pulse signal output of PWM	P20
PWM1			P21
AD0-AD7	I/O	16-bit multiplexed address/data bus when external memory is connected	P40-P47
AD8-AD15			P50-P57
A16-A19	Output	High-order address bus when external memory is connected	P60-P63
$\overline{\text{LBEN}}$	Output	Low-order byte enable signal output of external data bus	P90
$\overline{\text{UBEN}}$		High-order byte enable signal output of external data bus	P91
$\overline{\text{R/W}}$	Output	External read/write status output	P92
$\overline{\text{DSTB}}$		External data strobe signal output	P93
ASTB		External address strobe signal output	P94
$\overline{\text{HLDAK}}$	Output	Bus hold acknowledge output	P95
$\overline{\text{HLDRQ}}$	Input	Bus hold request input	P96
ANI0-ANI7	Input	Analog input to A/D converter	P70-P77
ANO0, ANO1	Output	Analog output of D/A converter	—
NMI	Input	Non-maskable interrupt request input	—
CLKOUT	Output	System clock output	—
$\overline{\text{CKSEL}}$	Input	Input specifying operation mode of clock generator	CV _{DD}
$\overline{\text{WAIT}}$	Input	Control signal input inserting wait state in bus cycle	—
MODE	Input	Operation mode specification	—
$\overline{\text{RESET}}$	Input	System reset input	—
X1	Input	System clock resonator connection. Input external clock to X1 to supply external clock.	—
X2	—		—
ADTRG	Input	A/D converter external trigger input	P07/INTP113
AV _{REF1}	Input	Reference voltage input for A/D converter	—
AV _{REF2}	Input	Reference voltage input for D/A converter	—
AV _{REF3}			—
AV _{DD}	—	Positive power supply for A/D converter	—
AV _{SS}	—	Ground potential for A/D converter	—
CV _{DD}	—	Positive power supply for internal clock generator	$\overline{\text{CKSEL}}$
CV _{SS}	—	Ground potential for internal clock generator	—
V _{DD}	—	Positive power supply	—
V _{SS}	—	Ground potential	—
V _{PP}	—	High voltage application pin when program is written/verified	—

2.3 I/O Circuits of Pins and Recommended Connections of Unused Pins

Table 2-1 shows the I/O circuit type of each pin, and the recommended connections of the unused pins. Figure 2-1 shows a partially simplified diagram of each circuit.

When connecting a pin to V_{DD} or V_{SS} via resistor, use of a resistor of 1 to 10 kΩ is recommended.

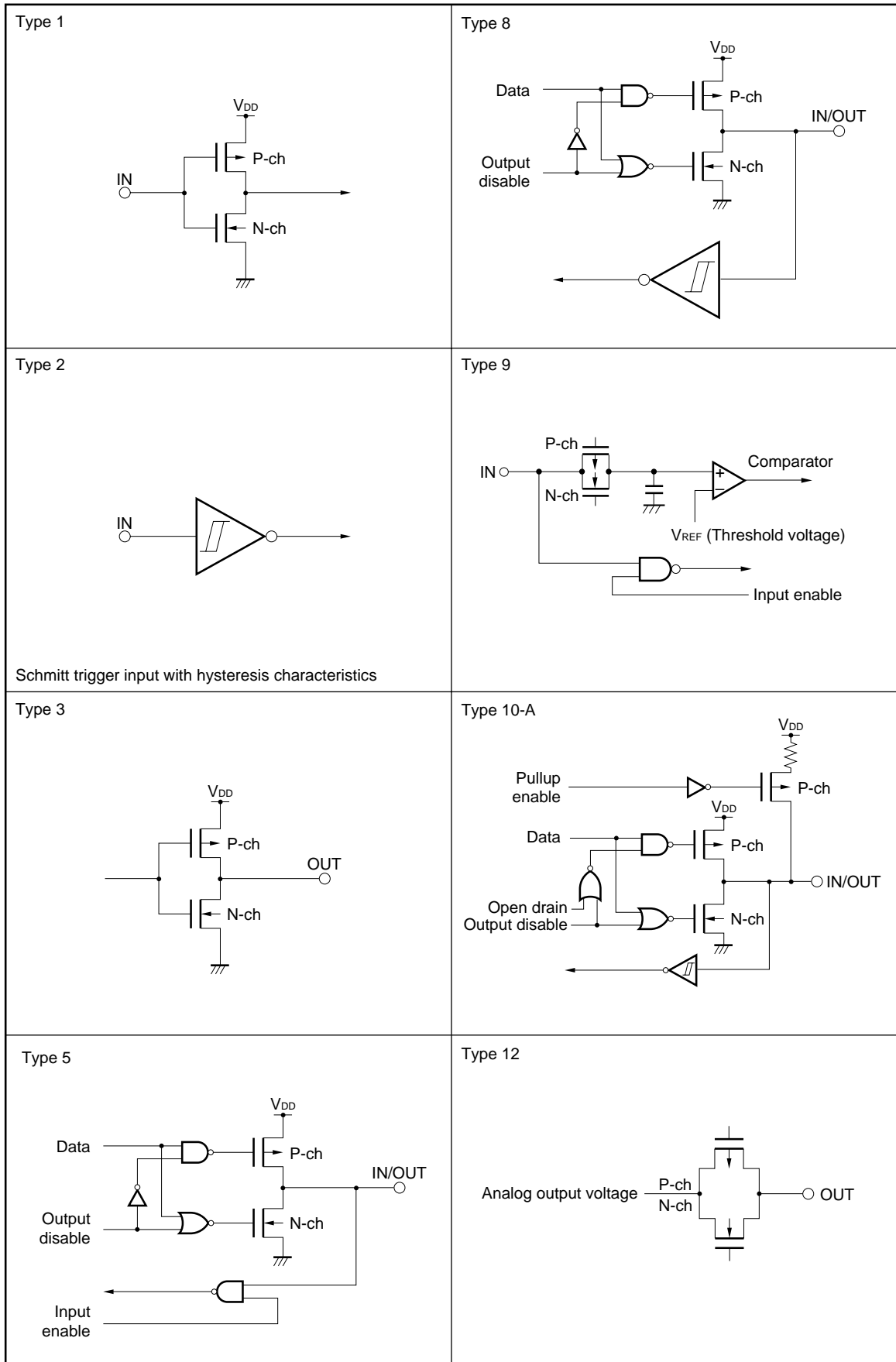
Table 2-1. I/O Circuit Types of Each Pin and Recommended Connections of Unused Pins (1/2)

Pin	I/O Circuit Type	Recommended Connections	
P00/TO110, P01/TO111	5	Input : Individually connect to V _{DD} or V _{SS} via resistor. Output : Leave unconnected.	
P02/TCLR11, P03/TI11, P04/INTP110-P07/INTP113/ADTRG	8		
P10-TO120, P11/TO121	5		
P12/TCLR12, P13/TI12 P14/INTP120 P15/INTP121/SO2 P16/INTP122/SI2 P17/INTP123/ $\overline{\text{SCK2}}$	8		
P20/PWM0, P21/PWM1 P22/TXD0/SO0	5		
P23/RXD0/SI0, P24/ $\overline{\text{SCK0}}$	8		
P25/TXD1/SO1	5		
P26/RXD1/SI1, P27/ $\overline{\text{SCK1}}$	8		
P30/TO130, P31/TO131	5		
P32/TCLR13, P33/TI13 P34/INTP130	8		
P35/INTP131/SO3 P36/INTP132/SI3 P37/INTP133/ $\overline{\text{SCK3}}$	10-A		
P40/AD0-P47/AD7 P50/AD8-P57/AD15 P60/A16-P63/A19	5		
P70/ANI0-P77/ANI7	9		Directly connect to V _{SS} .
P90/ $\overline{\text{LBEN}}$ P91/ $\overline{\text{UBEN}}$ P92/ $\overline{\text{R/W}}$ P93/ $\overline{\text{DSTB}}$ P94/ASTB P95/HLDAK P96/HLDRQ	5		Input: Individually connect to V _{DD} or V _{SS} via resistor. Output: Leave unconnected.
P110/TO140, P111/TO141	8		
P112/TCLR14, P113/TI14			
P114/INTP140-P117/INTP143			

Table 2-1. I/O Circuit Types of Each Pin and Recommended Connections of Unused Pins (2/2)

Pin	I/O Circuit Type	Recommended Connections
ANO0, ANO1	12	Leave unconnected.
NMI	2	Directly connect to V _{SS} .
CLKOUT	3	Leave unconnected.
$\overline{\text{WAIT}}$	1	Directly connect to V _{DD} .
MODE	2	—
$\overline{\text{RESET}}$		—
$\overline{\text{CV}}_{\text{DD}}/\overline{\text{CKSEL}}$		—
AV _{REF1} -AV _{REF3} , AV _{SS}	—	Directly connect to V _{SS} .
AV _{DD}	—	Directly connect to V _{DD} .
V _{PP}	—	Directly connect to V _{SS} .

Figure 2-1. I/O Circuits of Pins



3. ELECTRICAL SPECIFICATIONS

3.1 Normal Operation Mode

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Condition	Ratings	Unit	
Supply voltage	V _{DD}	V _{DD} pin	-0.5 to +7.0	V	
	CV _{DD}	CV _{DD} pin	-0.5 to V _{DD} + 0.3	V	
	CV _{SS}	CV _{SS} pin	-0.5 to +0.5	V	
	AV _{DD}	AV _{DD} pin	-0.5 to V _{DD} + 0.3	V	
	AV _{SS}	AV _{SS} pin	-0.5 to +0.5	V	
Input voltage	V _{I1}	Note , V _{DD} = 5.0 V ± 10 %	-0.5 to V _{DD} + 0.3	V	
	V _{I2}	V _{PP} pin in flash memory programming mode, V _{DD} = 5.0 V ± 10 %	-0.5 to +11.0	V	
Clock input voltage	V _K	X1 pin, V _{DD} = 5.0 V ± 10 %	-0.5 to V _{DD} + 1.0	V	
Output current, low	I _{CL}	1 pin	4.0	mA	
		Total of all pins	100	mA	
Output current, high	I _{CH}	1 pin	-4.0	mA	
		Total of all pins	-100	mA	
Output voltage	V _O	V _{DD} = 5.0 V ± 10 %	-0.5 to V _{DD} + 0.3	V	
Analog input voltage	V _{IAN}	P70/ANI0-P77/ANI7	AV _{DD} > V _{DD}	-0.5 to V _{DD} + 0.3	V
			V _{DD} ≥ AV _{DD}	-0.5 to AV _{DD} + 0.3	V
Analog reference input voltage	AV _{REF}	AV _{REF1} -AV _{REF3}	AV _{DD} > V _{DD}	-0.5 to V _{DD} + 0.3	V
			V _{DD} ≥ AV _{DD}	-0.5 to AV _{DD} + 0.3	V
Operating ambient temperature	T _A		-40 to +85	°C	
★ Storage temperature	T _{stg}		-40 to +125	°C	

Note Except X1, P70/AN0-P77/AN7, AV_{REF1}-AV_{REF3}

- Cautions**
1. Do not directly connect the output (or I/O) pins of two or more IC products, and do not directly connect them to V_{DD}, V_{CC}, or GND pin. Open-drain pins and open-collector pins may be directly connected to one another however. Moreover, an external circuit that is designed to prevent contention of output can be connected to pins that go into a high-impedance state.
 2. Should the absolute maximum rating of even one of the above parameters be exceeded even momentarily, the quality of the program may be degraded. The absolute maximum ratings are, therefore, the values exceeding which the product may be physically damaged. Use the product so that these values are never exceeded.
The normal operating ranges of ratings and conditions in which the quality of the product is guaranteed are specified in the following DC Characteristics and AC Characteristics.

Capacitance (TA = 25 °C, VDD = VSS = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C _i	fc = 1 MHz Pins other than tested pin: 0 V			15	pF
I/O capacitance	C _{io}				15	pF
Output capacitance	C _o				15	pF

Operating Conditions

Operation Mode	Internal Operating Clock Frequency (f)	Operating Temperature (TA)	Supply Voltage (VDD)
Direct mode	0 to 33 MHz ^{Note 1}	-40 to +85 °C	5.0 V ± 10 %
	5 to 33 MHz ^{Note 2}	-40 to +85 °C	5.0 V ± 10 %
★ PLL mode	2 to 33 MHz	-40 to +85 °C	5.0 V ± 10 %

Notes 1. When A/D converter not used.

2. When A/D converter used.

Remark The internal operating clock frequency range in the PLL mode means the range in which the functional operation is guaranteed, and the frequency in the PLL lock status is specified by tc_{yx}.

DC Characteristics (TA = -40 to +85 °C, VDD = 5.0 V ± 10 %, VSS = 0 V)

(1/2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage, high	V _{IH}	Except X1 and Note 1	2.2		V _{DD} + 0.3	V
		Note 1	0.8 V _{DD}		V _{DD} + 0.3	V
Input voltage, low	V _{IL}	Except X1 and Note 1	-0.5		+0.8	V
		Note 1	-0.5		0.2 V _{DD}	V
Clock input voltage, high	V _{XH}	X1	0.8 V _{DD}		V _{DD} + 0.5	V
Clock input voltage, low	V _{XL}	X1	-0.5		0.6	V
Schmitt trigger input threshold voltage	V _{T+}	Note 1 , rising		3.0		V
	V _{T-}	Note 1 , falling		2.0		V
Schmitt trigger input hysteresis width	V _{T+} - V _{T-}	Note 1	0.5			V
Output voltage, high	V _{OH}	I _{OH} = -2.5 mA	0.7 V _{DD}			V
		I _{OH} = -100 μA	V _{DD} - 0.4			V
Output voltage, low	V _{OL}	I _{OC} = 2.5 mA			0.45	V
Input leakage current, high	I _{LIH}	V _i = V _{DD}			10	μA
Input leakage current, low	I _{LIL}	V _i = 0 V			-10	μA
Output leakage current, high	I _{LOH}	V _o = V _{DD}			10	μA
Output leakage current, low	I _{LOL}	V _o = 0 V			-10	μA
Software pull-up resistor	R	P35/INTP131/SO3, P36/INTP132/SI3, P37/INTP133/SCK3	15	40	90	kΩ

(2/2)

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	
Supply current	μPD70F3003A	Operating	I _{DD1}	Direct mode ^{Note 2}		$2.2 \times \phi + 7.5$	$2.5 \times \phi + 22$	mA
				PLL mode		$2.3 \times \phi + 9.5$	$2.6 \times \phi + 25$	mA
		In HALT mode	I _{DD2}	Direct mode ^{Note 2}		$1.2 \times \phi + 7.5$	$1.3 \times \phi + 15$	mA
				PLL mode		$1.3 \times \phi + 9.5$	$1.4 \times \phi + 17$	mA
		In IDLE mode	I _{DD3}	Direct mode ^{Note 2}		$8 \times \phi + 300$	$10 \times \phi + 500$	μA
				PLL mode		$0.1 \times \phi + 2$	$0.2 \times \phi + 3$	mA
		In STOP mode	I _{DD4}	CESEL = 0, Note 3		2	50	μA
				CESEL = 0, Note 4		2	200	μA
	CESEL = 1, Note 3				30	200	μA	
	CESEL = 1, Note 4				30	500	μA	
	μPD70F3025A	Operating	I _{DD1}	Direct mode ^{Note 2}		$2.5 \times \phi + 8$	$2.8 \times \phi + 22.5$	mA
				PLL mode		$2.6 \times \phi + 10$	$2.9 \times \phi + 25.5$	mA
		In HALT mode	I _{DD2}	Direct mode ^{Note 2}		$1.3 \times \phi + 7.5$	$1.4 \times \phi + 15$	mA
				PLL mode		$1.3 \times \phi + 12.5$	$1.4 \times \phi + 20$	mA
		In IDLE mode	I _{DD3}	Direct mode ^{Note 2}		$8 \times \phi + 300$	$10 \times \phi + 500$	μA
				PLL mode		$0.1 \times \phi + 2$	$0.2 \times \phi + 3$	mA
In STOP mode		I _{DD4}	CESEL = 0, Note 3		2	50	μA	
			CESEL = 0, Note 4		2	200	μA	
	CESEL = 1, Note 3			60	300	μA		
	CESEL = 1, Note 4			60	500	μA		

Notes 1. P02/TCLR11, P03/TI11, P04/INTP110-P07/INTP113, P12/TCLR12, P13/TI12, P14/INTP120, P15/INTP121/SO2, P16/INTP122/SI2, P17/INTP123/SCK2, P23/RXD0/SI0, P24/SCK0, P26/RXD1/SI1, P27/SCK1, P32/TCLR32, P33/TI13, P34/INTP130, P35/INTP131/SO3, P36/INTP132/SI3, P37/INTP133/SCK3, P112/TCLR14, P113/TI14, P114/INTP140-P117/INTP143, RESET, NMI, MODE

- 2. When A/D converter used : $\phi = 5$ to 33 MHz
When A/D converter not used: $\phi = 0$ to 33 MHz
- 3. $-40\text{ °C} \leq T_A \leq +50\text{ °C}$
- 4. $50\text{ °C} < T_A \leq 85\text{ °C}$

Remarks 1. TYP. value is a value for your reference at $T_A = 25\text{ °C}$ and $V_{DD} = 5.0\text{ V}$. The supply current does not include AV_{REF1} - AV_{REF3} and the current running through the software pull-up resistor.

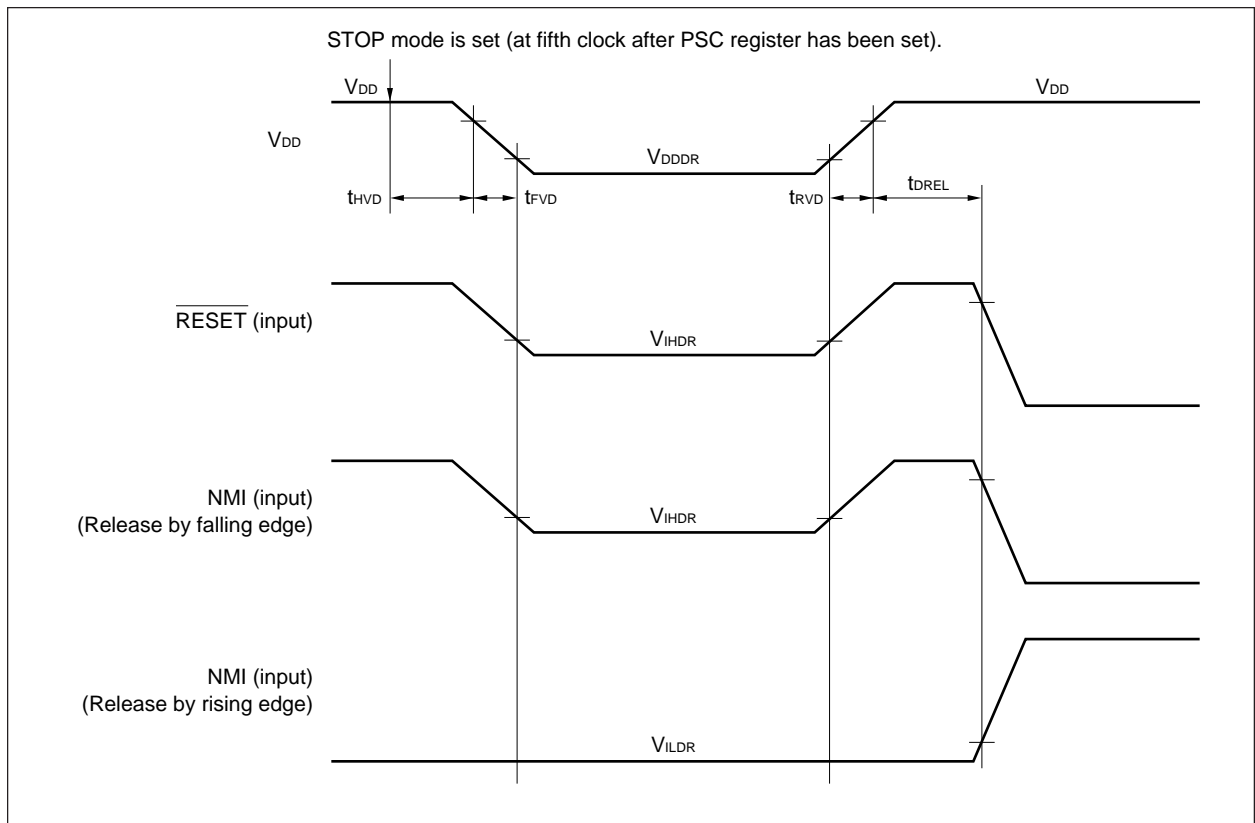
2. ϕ : Internal system clock frequency

Data Retention Characteristics (T_A = -40 to +85 °C)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Data hold voltage	V _{DDDR}	STOP mode	1.5		5.5	V
Data hold current	I _{DDDR}	V _{DD} = V _{DDDR}		0.2 V _{DDDR}	50	μA
			-40 °C ≤ T _A ≤ +50 °C		0.2 V _{DDDR}	50
					200	μA
Supply voltage rise time	t _{RVD}		200			μs
Supply voltage fall time	t _{FVD}		200			μs
Supply voltage hold time (vs. STOP mode setting)	t _{HVD}		0			ms
STOP mode release signal input time	t _{DREL}		0			ns
Data hold input voltage, high	V _{IHDR}	Note	0.9 V _{DDDR}		V _{DDDR}	V
Data hold input voltage, low	V _{ILDR}	Note	0		0.1 V _{DDDR}	V

Note P02/TCLR11, P03/TI11, P04/INTP110-P07/INTP113, P12/TCLR12, P13/TI12, P14/INTP120, P15/INTP121/SO2, P16/INTP122/SI2, P17/INTP123/SCK2, P23/RXD0/SI0, P24/SCK0, P26/RXD1/SI1, P27/SCK1, P32/TCLR32, P33/TI13, P34/INTP130, P35/INTP131/SO3, P36/INTP132/SI3, P37/INTP133/SCK3, P112/TCLR14, P113/TI14, P114/INTP140-P117/INTP143, RESET, NMI, MODE, X1

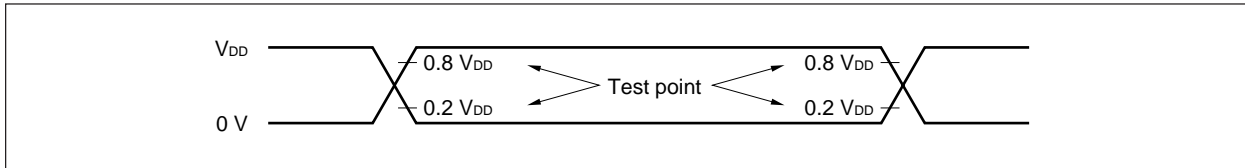
Remark TYP. value is a value for your reference at T_A = 25 °C and V_{DD} = 5.0 V.



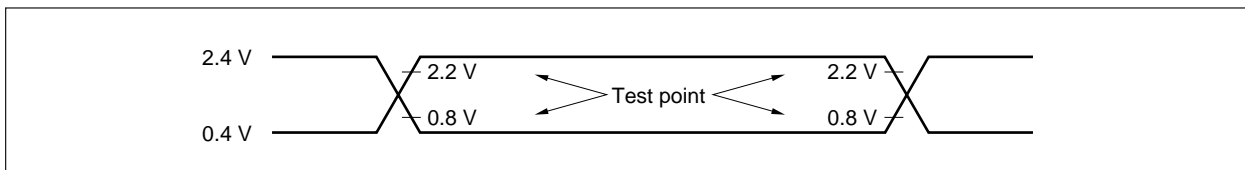
AC Characteristics ($T_A = -40$ to $+85$ °C, $V_{DD} = 5.0$ V \pm 10 %, $V_{SS} = 0$ V)

AC test input wave

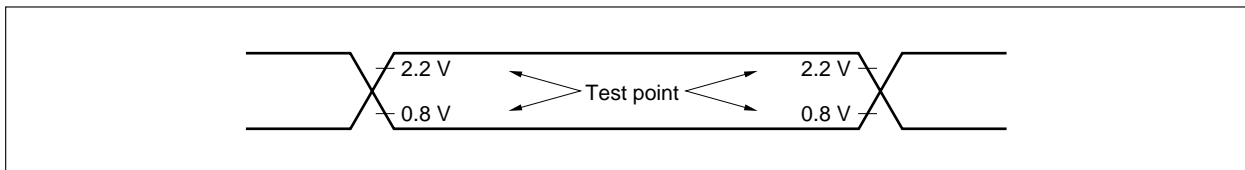
- (a) P02/TCLR11, P03/TI11, P04/INTP110-P07/INTP113, P12/TCLR12, P13/TI12, P14/INTP120, P15/INTP121/SO2, P16/INTP122/SI2, P17/INTP123/SCK2, P23/RXD0/SI0, P24/SCK0, P26/RXD1/SI1, P27/SCK1, P32/TCLR32, P33/TI13, P34/INTP130, P35/INTP131/SO3, P36/INTP132/SI3, P37/INTP133/SCK3, P112, TCLR14, P113/TI14, P114/INTP140-P117/INTP143, RESET, NMI, MODE, X1



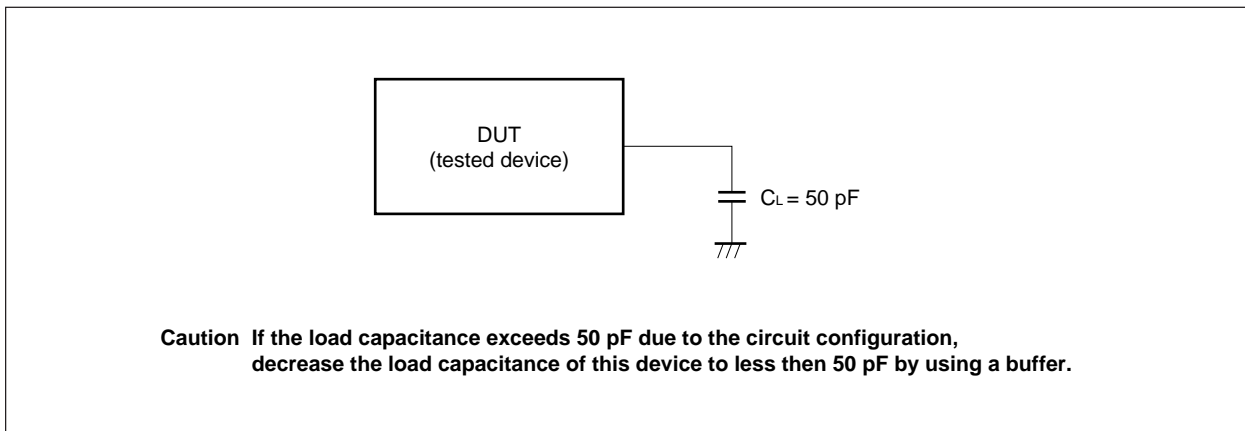
- (b) Other than (a)



AC test output test point



Load condition



[MEMO]

(1) Clock timing

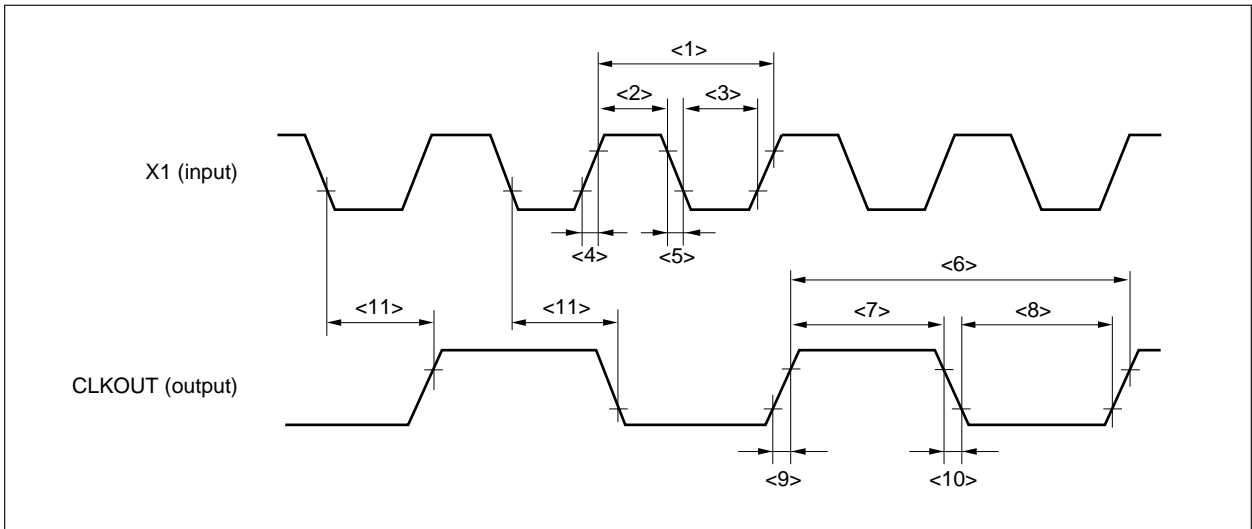
Parameter	Symbol		Condition	25 MHz Model		33 MHz Model		Unit
				MIN.	MAX.	MIN.	MAX.	
X1 input cycle	<1>	t _{CYX}	Direct mode	20	Note 1	15	Note 1	ns
			PLL mode (PLL lock status)	200	315	151	334	ns
X1 input width, high	<2>	t _{WXH}	Direct mode	7		6		ns
			PLL mode	80		60		ns
X1 input width, low	<3>	t _{WXL}	Direct mode	7		6		ns
			PLL mode	80		60		ns
X1 input rise time	<4>	t _{XR}	Direct mode		7		7	ns
			PLL mode		15		10	ns
X1 input fall time	<5>	t _{XF}	Direct mode		7		7	ns
			PLL mode		15		10	ns
CPU operating frequency	—	φ	Direct mode	Note 2	25	Note 2	33	MHz
			PLL mode	2	25	2	33	MHz
CLKOUT output cycle	<6>	t _{CYK}		40	Note 3	30	Note 3	ns
CLKOUT width, high	<7>	t _{WKH}		0.5 T – 5		0.5 T – 5		ns
CLKOUT width, low	<8>	t _{WKL}		0.5 T – 5		0.5 T – 5		ns
CLKOUT rise time	<9>	t _{XR}			5		5	ns
CLKOUT fall time	<10>	t _{XF}			5		5	ns
X1 ↓→ CLKOUT delay time	<11>	t _{DXK}	Direct mode	3	17	3	17	ns

★

- Notes**
1. When A/D converter used: 100 ns
When A/D converter not used: DC
 2. When A/D converter used: 5 MHz
When A/D converter not used: 0 MHz
 3. When A/D converter used: 200 ns
When A/D converter not used: DC

Remark T = t_{CYK}

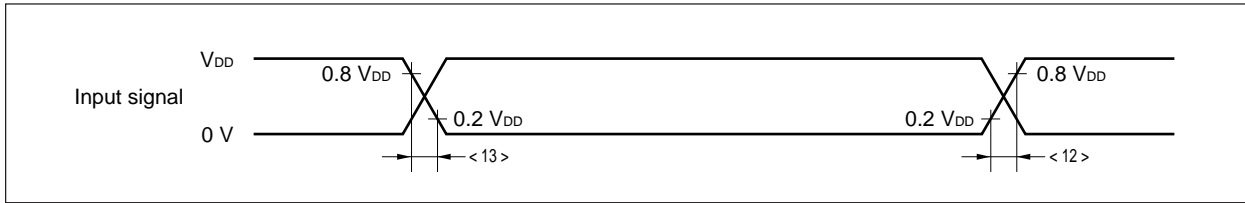
Parameter	Symbol		Condition	TYP.	Unit
Self oscillation frequency	—	φ _P	PLL mode	1	MHz



(2) Input wave

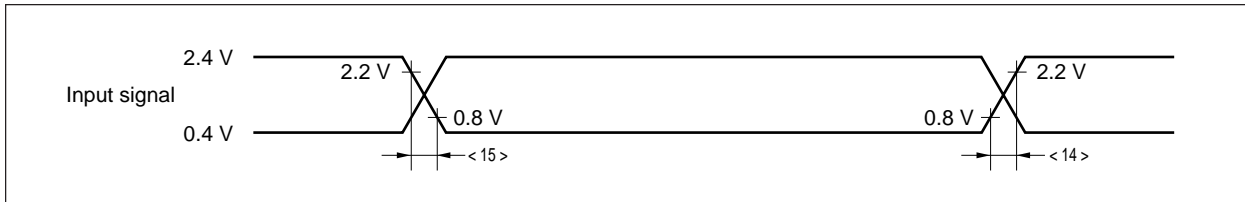
- (a) P02/TCLR11, P03/TI11, P04/INTP110-P07/INTP113, P12/TCLR12, P13/TI12, P14/INTP120, P15/INTP121/SO2, P16/INTP122/SI2, P17/INTP123/ $\overline{\text{SCK2}}$, P23/RXD0/SI0, P24/ $\overline{\text{SCK0}}$, P26/RXD1/SI1, P27/ $\overline{\text{SCK1}}$, P32/TCLR32, P33/TI13, P34/INTP130, P35/INTP131/SO3, P36/INTP132/SI3, P37/INTP133/ $\overline{\text{SCK3}}$, P112/TCLR14, P113/TI14, P114/INTP140-P117/INTP143, $\overline{\text{RESET}}$, NMI, MODE

Parameter	Symbol	Condition	25 MHz Model		33 MHz Model		Unit
			MIN.	MAX.	MIN.	MAX.	
Input rise time	<12> t_{IR2}			20		20	ns
Input fall time	<13> t_{IF2}			20		20	ns



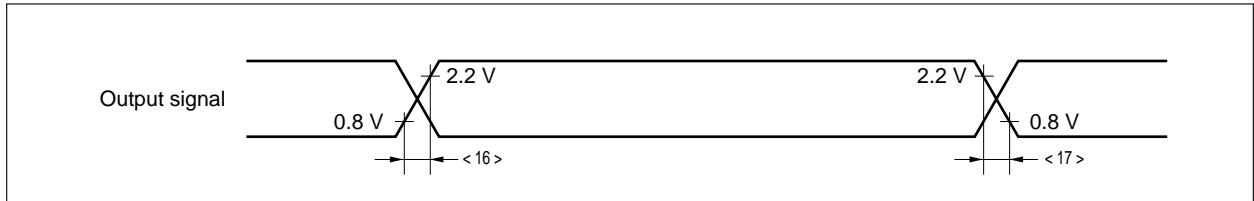
(b) Other than (a)

Parameter	Symbol	Condition	25 MHz Model		33 MHz Model		Unit
			MIN.	MAX.	MIN.	MAX.	
Input rise time	<14> t_{IR1}			10		10	ns
Input fall time	<15> t_{IF1}			10		10	ns



(3) Output wave (other than CLKOUT)

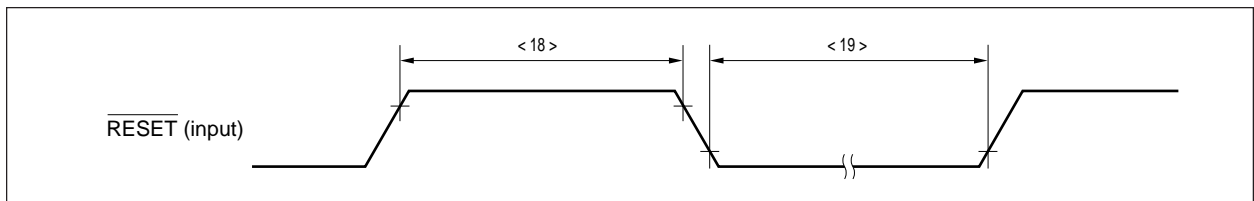
Parameter	Symbol	Condition	25 MHz Model		33 MHz Model		Unit
			MIN.	MAX.	MIN.	MAX.	
Output rise time	<16>	t _{OR}		10		10	ns
Output fall time	<17>	t _{OF}		10		10	ns



(4) Reset timing

Parameter	Symbol	Condition	25 MHz Model		33 MHz Model		Unit
			MIN.	MAX.	MIN.	MAX.	
RESET width, high	<18>	t _{WRSH}	500		500		ns
RESET width, low	<19>	On power application, or on releasing STOP mode	500 + T _{OST}		500 + T _{OST}		ns
		Except on power application, or except on releasing STOP mode	500		500		ns

Remark T_{OST}: oscillation stabilization time



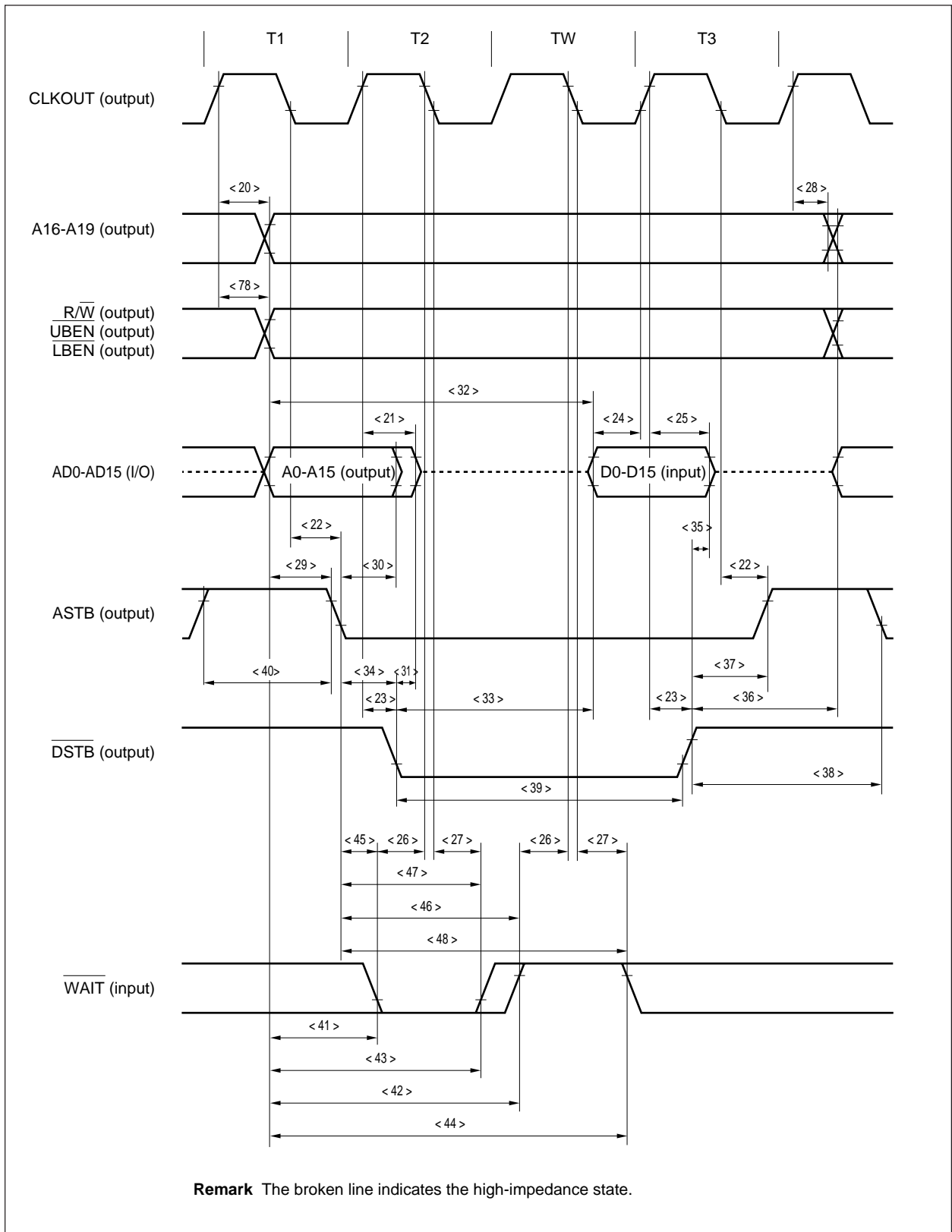
(5) Read timing (1/2)

Parameter	Symbol	Condition	25 MHz Model		33 MHz Model		Unit
			MIN.	MAX.	MIN.	MAX.	
CLKOUT ↑→ address delay time	<20>	t _{DKA}	3	20	3	20	ns
★ CLKOUT ↑→ R/W, \overline{UBEN} , \overline{LBEN} delay time	<78>	t _{DKA2}	-2	+13	-2	+13	ns
CLKOUT ↑→ address float delay time	<21>	t _{FKA}	3	15	3	15	ns
CLKOUT ↓→ ASTB delay time	<22>	t _{DKST}	3	15	3	15	ns
CLKOUT ↓→ \overline{DSTB} delay time	<23>	t _{DKD}	3	15	3	15	ns
Data input setup time (vs. CLKOUT ↑)	<24>	t _{SIDK}	5		5		ns
Data input hold time (vs. CLKOUT ↑)	<25>	t _{HKID}	5		5		ns
\overline{WAIT} setup time (vs. CLKOUT ↓)	<26>	t _{SWTK}	5		5		ns
\overline{WAIT} hold time (vs. CLKOUT ↓)	<27>	t _{HKWT}	5		5		ns
Address hold time (vs. CLKOUT ↑)	<28>	t _{HKA}	0		0		ns
★ Address setup time (vs. ASTB ↓)	<29>	t _{SAST}	-40 °C ≤ T _A ≤ +70 °C	0.5 T - 10	0.5 T - 10		ns
★			70 °C < T _A ≤ 85 °C	0.5 T - 12	0.5 T - 12		ns
Address hold time (vs. ASTB ↓)	<30>	t _{HSTA}	0.5 T - 10		0.5 T - 10		ns
\overline{DSTB} ↓→ address float delay time	<31>	t _{FDA}		0		0	ns
★ Data input setup time (vs. address)	<32>	t _{SAID}	-40 °C ≤ T _A ≤ +70 °C	(2 + n) T - 22	(2 + n) T - 22		ns
★			70 °C < T _A ≤ 85 °C	(2 + n) T - 25	(2 + n) T - 25		ns
★ Data input setup time (vs. \overline{DSTB} ↓)	<33>	t _{SDID}	-40 °C ≤ T _A ≤ +70 °C	(1 + n) T - 20	(1 + n) T - 20		ns
★			70 °C < T _A ≤ 85 °C	(1 + n) T - 24	(1 + n) T - 24		ns
ASTB ↓→ \overline{DSTB} ↓ delay time	<34>	t _{DSTD}	0.5 T - 10		0.5 T - 10		ns
Data input hold time (vs. \overline{DSTB} ↑)	<35>	t _{HDID}	0		0		ns
\overline{DSTB} ↑→ address output delay time	<36>	t _{DDA}	(1 + i) T		(1 + i) T		ns
\overline{DSTB} ↑→ ASTB ↑ delay time	<37>	t _{DDSTH}	0.5 T - 10		0.5 T - 10		ns
\overline{DSTB} ↑→ ASTB ↓ delay time	<38>	t _{DDSTL}	(1.5 + i) T - 10		(1.5 + i) T - 10		ns
★ \overline{DSTB} width, low	<39>	t _{WDL}	-40 °C ≤ T _A ≤ +70 °C	(1 + n) T - 10	(1 + n) T - 10		ns
★			70 °C < T _A ≤ 85 °C	(1 + n) T - 13	(1 + n) T - 13		ns
ASTB width, high	<40>	t _{WSTH}	T - 10		T - 10		ns
★ \overline{WAIT} setup time (vs. address)	<41>	t _{SAWT1}	n ≥ 1, -40 °C ≤ T _A ≤ +70 °C	1.5 T - 20	1.5 T - 20		ns
★			n ≥ 1, 70 °C < T _A ≤ 85 °C	1.5 T - 24	1.5 T - 24		ns
★	<42>	t _{SAWT2}	n ≥ 1, -40 °C ≤ T _A ≤ +70 °C	(1.5 + n) T - 20	(1.5 + n) T - 20		ns
★			n ≥ 1, 70 °C < T _A ≤ 85 °C	(1.5 + n) T - 24	(1.5 + n) T - 24		ns
\overline{WAIT} hold time (vs. address)	<43>	t _{HAWT1}	n ≥ 1	(0.5 + n) T	(0.5 + n) T		ns
★	<44>	t _{HAWT2}	n ≥ 1	(1.5 + n) T	(1.5 + n) T		ns
★ \overline{WAIT} setup time (vs. ASTB ↓)	<45>	t _{SSTWT1}	n ≥ 1, -40 °C ≤ T _A ≤ +70 °C	T - 18	T - 18		ns
★			n ≥ 1, 70 °C < T _A ≤ 85 °C	T - 20	T - 20		ns
★	<46>	t _{SSTWT2}	n ≥ 1	(1 + n) T - 15	(1 + n) T - 15		ns
\overline{WAIT} hold time (vs. ASTB ↓)	<47>	t _{HSTWT1}	n ≥ 1	nT	nT		ns
★	<48>	t _{HSTWT2}	n ≥ 1	(1 + n) T	(1 + n) T		ns

Remarks 1. T = t_{cyk}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.
3. i indicates the number of idle states (0 or 1) to be inserted in the read cycle.
4. Be sure to observe at least one of data input hold times t_{HKID} (<25>) and t_{HDID} (<35>).

(5) Read Timing (2/2): 1 wait



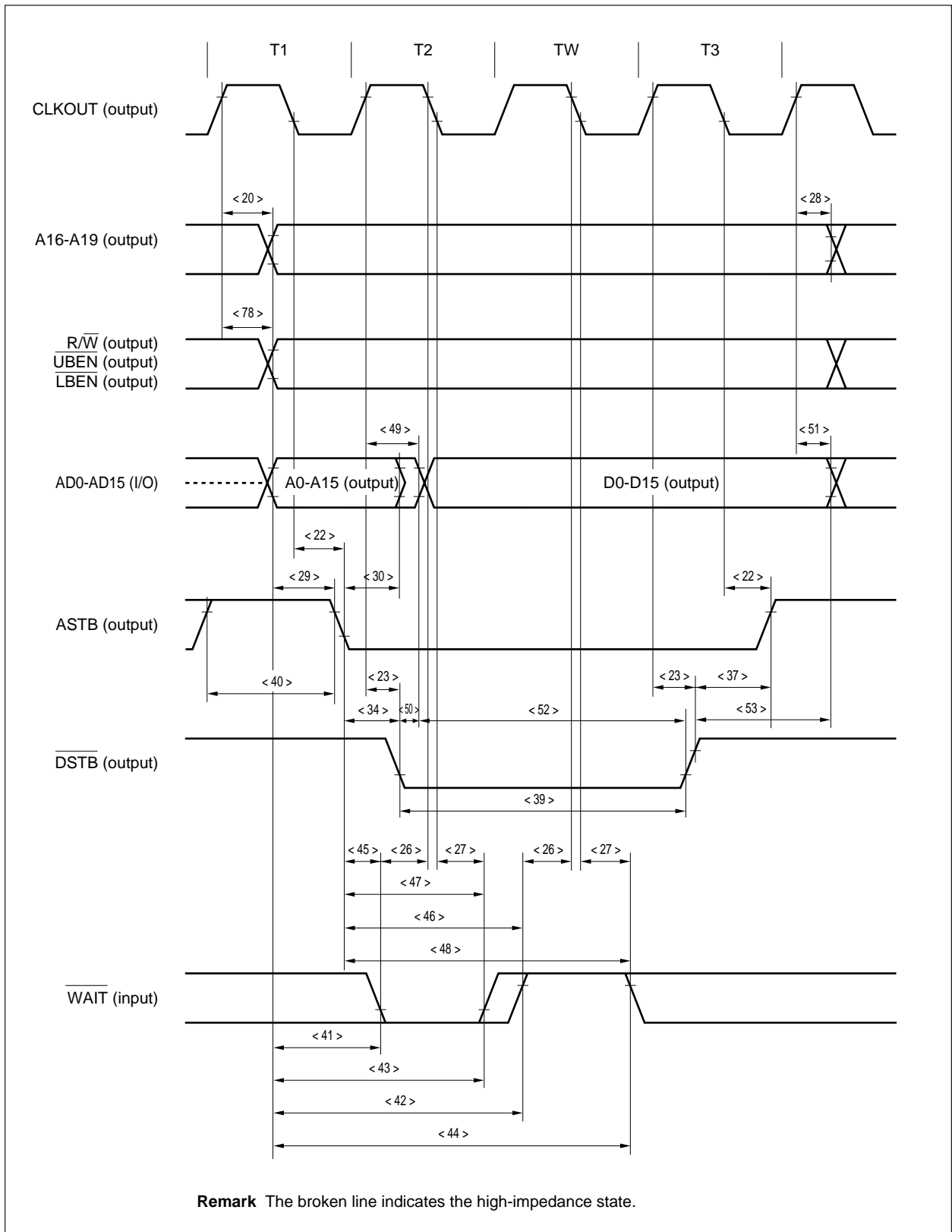
(6) Write timing (1/2)

Parameter	Symbol	Condition	25 MHz Model		33 MHz Model		Unit
			MIN.	MAX.	MIN.	MAX.	
CLKOUT ↑→ address delay time	<20>	t _{DKA}	3	20	3	20	ns
★ CLKOUT ↑→ R/W, \overline{UBEN} , \overline{LBEN} delay time	<78>	t _{DKA2}	-2	+13	-2	+13	ns
CLKOUT ↓→ ASTB delay time	<22>	t _{DKST}	3	15	3	15	ns
CLKOUT ↑→ \overline{DSTB} delay time	<23>	t _{DKD}	3	15	3	15	ns
\overline{WAIT} setup time (vs. CLKOUT ↓)	<26>	t _{SWTK}	5		5		ns
\overline{WAIT} hold time (vs. CLKOUT ↓)	<27>	t _{HKWT}	5		5		ns
Address hold time (vs. CLKOUT ↑)	<28>	t _{HKA}	0		0		ns
★ Address setup time (vs. ASTB ↓)	<29>	t _{SAST}	-40 °C ≤ T _A ≤ +70 °C	0.5 T - 10	0.5 T - 10		ns
★			70 °C < T _A ≤ 85 °C	0.5 T - 12	0.5 T - 12		ns
Address hold time (vs. ASTB ↓)	<30>	t _{HSTA}		0.5 T - 10	0.5 T - 10		ns
ASTB ↓→ \overline{DSTB} ↓ delay time	<34>	t _{DSTD}		0.5 T - 10	0.5 T - 10		ns
\overline{DSTB} ↑→ ASTB ↑ delay time	<37>	t _{DDSTH}		0.5 T - 10	0.5 T - 10		ns
★ \overline{DSTB} width, low	<39>	t _{WDL}	-40 °C ≤ T _A ≤ +70 °C	(1 + n) T - 10	(1 + n) T - 10		ns
★			70 °C < T _A ≤ 85 °C	(1 + n) T - 13	(1 + n) T - 13		ns
\overline{ASTB} width, high	<40>	t _{WSTH}		T - 10	T - 10		ns
★ \overline{WAIT} setup time (vs. address)	<41>	t _{SAWT1}	n ≥ 1, -40 °C ≤ T _A ≤ +70 °C	1.5 T - 20	1.5 T - 20		ns
★			n ≥ 1, 70 °C < T _A ≤ 85 °C	1.5 T - 24	1.5 T - 24		ns
★	<42>	t _{SAWT2}	n ≥ 1, -40 °C ≤ T _A ≤ +70 °C	(1.5 + n) T - 20	(1.5 + n) T - 20		ns
★			n ≥ 1, 70 °C < T _A ≤ 85 °C	(1.5 + n) T - 24	(1.5 + n) T - 24		ns
\overline{WAIT} hold time (vs. address)	<43>	t _{HAWT1}	n ≥ 1	(0.5 + n) T	(0.5 + n) T		ns
★	<44>	t _{HAWT2}	n ≥ 1	(1.5 + n) T	(1.5 + n) T		ns
★ \overline{WAIT} setup time (vs. ASTB ↓)	<45>	t _{SSTWT1}	n ≥ 1, -40 °C ≤ T _A ≤ +70 °C	T - 18	T - 18		ns
★			n ≥ 1, 70 °C < T _A ≤ 85 °C	T - 20	T - 20		ns
★	<46>	t _{SSTWT2}	n ≥ 1	(1 + n) T - 15	(1 + n) T - 15		ns
\overline{WAIT} hold time (vs. ASTB ↓)	<47>	t _{HSTWT1}	n ≥ 1	nT	nT		ns
★	<48>	t _{HSTWT2}	n ≥ 1	(1 + n) T	(1 + n) T		ns
★ CLKOUT ↑→ data output delay time	<49>	t _{DKOD}	-40 °C ≤ T _A ≤ +70 °C	20	20		ns
★			70 °C < T _A ≤ 85 °C	23	23		ns
\overline{DSTB} ↓→ data output delay time	<50>	t _{DDOD}		10	10		ns
Data output hold time (vs. CLKOUT ↑)	<51>	t _{HKOD}		0	0		ns
Data output setup time (vs. \overline{DSTB} ↑)	<52>	t _{SODD}		(1 + n) T - 15	(1 + n) T - 15		ns
Data output hold time (vs. \overline{DSTB} ↑)	<53>	t _{HDOD}		T - 10	T - 10		ns

Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.

(6) Write timing (2/2): 1 wait



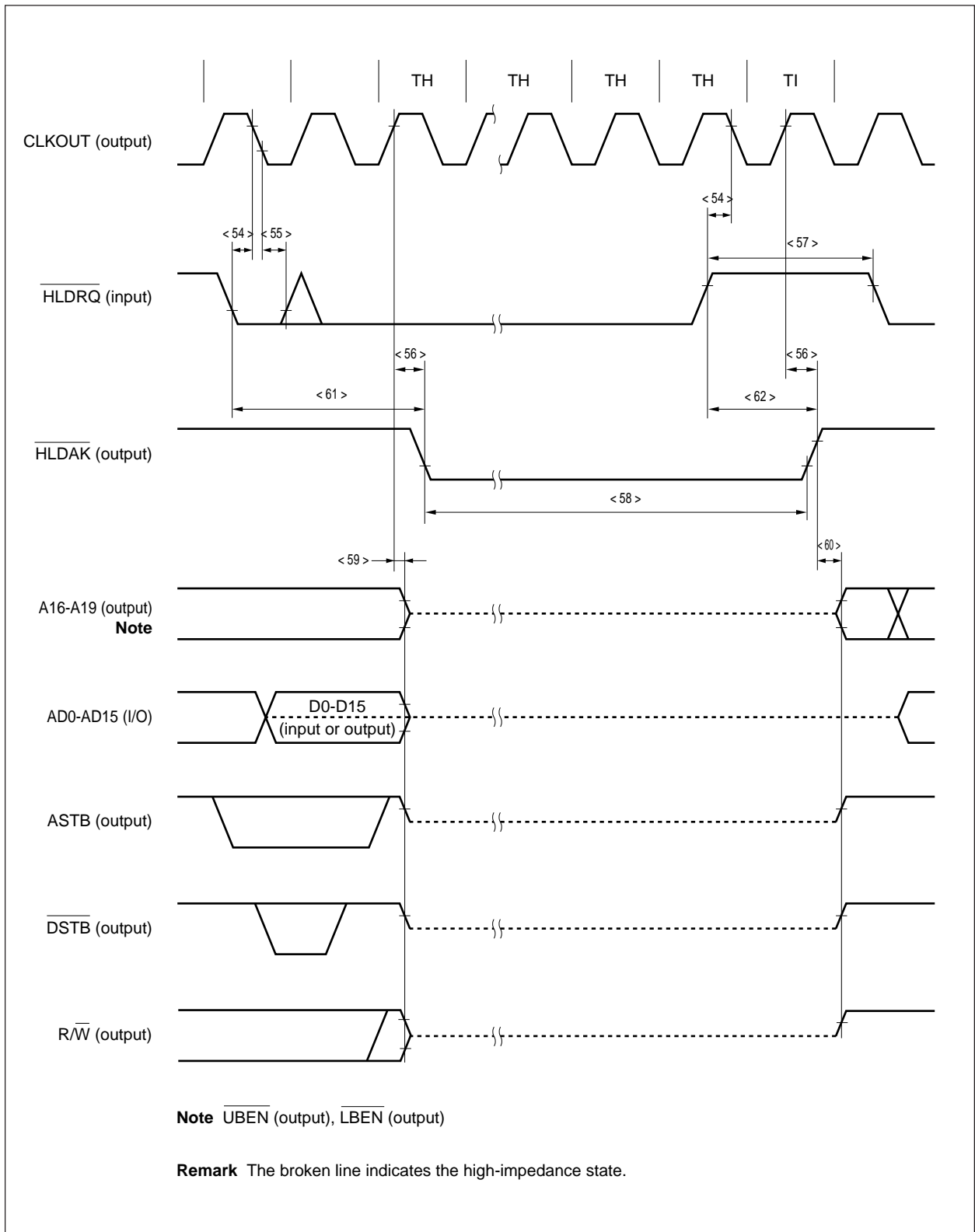
(7) Bus hold timing (1/2)

Parameter	Symbol		Condition	25 MHz Model		33 MHz Model		Unit
				MIN.	MAX.	MIN.	MAX.	
$\overline{\text{HLDRQ}}$ setup time (vs. CLKOUT ↓)	<54>	t _{SHOK}		5		5		ns
$\overline{\text{HLDRQ}}$ hold time (vs. CLKOUT ↓)	<55>	t _{HKHQ}		5		5		ns
CLKOUT ↑ → $\overline{\text{HLD\!A\!K}}$ delay time	<56>	t _{DKHA}			20		20	ns
$\overline{\text{HLDRQ}}$ width, high	<57>	t _{WHQH}		T + 10		T + 10		ns
★ $\overline{\text{HLD\!A\!K}}$ width, low	<58>	t _{WHAL}	-40 °C ≤ T _A ≤ +70 °C	T - 10		T - 10		ns
★			70 °C < T _A ≤ 85 °C	T - 12		T - 12		ns
CLKOUT ↑ → Bus float delay time	<59>	t _{DKF}			20		20	ns
$\overline{\text{HLD\!A\!K}}$ ↑ → bus output delay time	<60>	t _{DHAC}		-3		-3		ns
$\overline{\text{HLDRQ}}$ ↓ → $\overline{\text{HLD\!A\!K}}$ ↓ delay time	<61>	t _{DHQHA1}			(2n + 7.5) T + 20		(2n + 7.5) T + 20	ns
$\overline{\text{HLDRQ}}$ ↑ → $\overline{\text{HLD\!A\!K}}$ ↑ delay time	<62>	t _{DHQHA2}		0.5 T	1.5 T + 20	0.5 T	1.5 T + 20	ns

Remarks 1. T = t_{cyk}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.

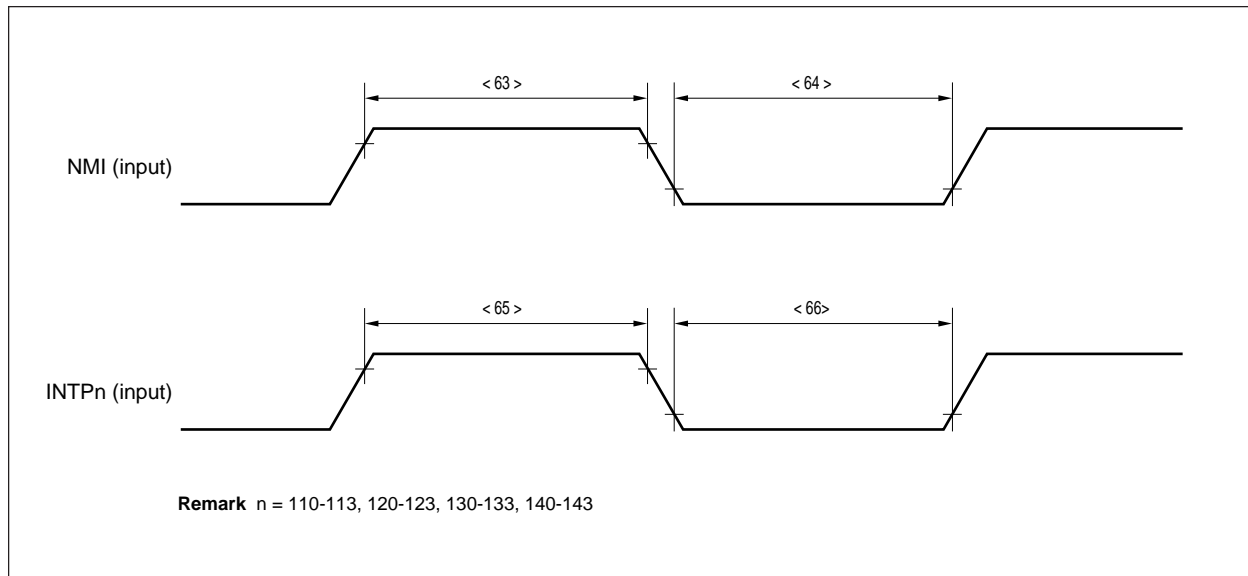
(7) Bus hold timing (2/2)



(8) Interrupt timing

Parameter	Symbol		Condition	25 MHz Model		33 MHz Model		Unit
				MIN.	MAX.	MIN.	MAX.	
NMI width, high	<63>	t _{WNH}		500		500		ns
NMI width, low	<64>	t _{WNL}		500		500		ns
INTPn width, high	<65>	t _{WITH}	n = 110-113, 120-123, 130-133, 140-143	3 T + 10		3 T + 10		ns
INTPn width, low	<66>	t _{WTL}	n = 110-113, 120-123, 130-133, 140-143	3 T + 10		3 T + 10		ns

Remark T = t_{cyk}



[MEMO]

(9) CSI timing (1/2)

(a) Master mode

(i) CSI0-CSI2 timing

Parameter	Symbol		Condition	25 MHz Model		33 MHz Model		Unit
				MIN.	MAX.	MIN.	MAX.	
\overline{SCKn} cycle	<67>	t_{CYSK1}	Output	160		120		ns
\overline{SCKn} width, high	<68>	t_{WSKH1}	Output	$0.5 t_{CYSK1} - 20$		$0.5 t_{CYSK1} - 20$		ns
\overline{SCKn} width, low	<69>	t_{WSKL1}	Output	$0.5 t_{CYSK1} - 20$		$0.5 t_{CYSK1} - 20$		ns
SIn setup time (vs. $\overline{SCKn} \uparrow$)	<70>	t_{SSISK1}		30		30		ns
SIn hold time (vs. $\overline{SCKn} \uparrow$)	<71>	t_{HSKSI1}		0		0		ns
SOn output delay time (vs. $\overline{SCKn} \downarrow$)	<72>	t_{DSKSO1}			18		18	ns
SOn output hold time (vs. $\overline{SCKn} \uparrow$)	<73>	t_{HSKSO1}		$0.5 t_{CYSK1} - 5$		$0.5 t_{CYSK1} - 5$		ns

Remark n = 0-2

(ii) CSI3 timing

Parameter	Symbol		Condition	25 MHz Model		33 MHz Model		Unit	
				MIN.	MAX.	MIN.	MAX.		
$\overline{SCK3}$ cycle	<67>	t_{CYSK3}	Output	$R_L = 1.5$ $k\Omega$ $C_L = 50$ pF	500		500		ns
$\overline{SCK3}$ width, high	<68>	t_{WSKH3}	Output		$0.5 t_{CYSK3} - 70$		$0.5 t_{CYSK3} - 70$		ns
$\overline{SCK3}$ width, low	<69>	t_{WSKL3}	Output		$0.5 t_{CYSK3} - 70$		$0.5 t_{CYSK3} - 70$		ns
SI3 setup time (vs. $\overline{SCK3} \uparrow$)	<70>	t_{SSISK3}		100		100		ns	
SI3 hold time (vs. $\overline{SCK3} \uparrow$)	<71>	t_{HSKSI3}		50		50		ns	
SO3 output delay time (vs. $\overline{SCK3} \downarrow$)	<72>	t_{DSKSO3}	$R_L = 1.5 K\Omega$ $C_L = 50 pF$		150		150	ns	
SO3 output hold time (vs. $\overline{SCK3} \uparrow$)	<73>	t_{HSKSO3}		$0.5 t_{CYSK3} - 5$		$0.5 t_{CYSK3} - 5$		ns	

Remark R_L and C_L are the load resistance and load capacitance respectively of the $\overline{SCK3}$ and SO3 output lines.

(b) Slave mode

(i) CSI0-CSI2 timing

Parameter	Symbol		Condition	25 MHz Model		33 MHz Model		Unit
				MIN.	MAX.	MIN.	MAX.	
\overline{SCKn} cycle	<67>	t_{CYSK2}	Input	160		120		ns
\overline{SCKn} width, high	<68>	t_{WSKH2}	Input	50		30		ns
\overline{SCKn} width, low	<69>	t_{WSKL2}	Input	50		30		ns
SIn setup time (vs. $\overline{SCKn} \uparrow$)	<70>	t_{SSISK2}		10		10		ns
SIn hold time (vs. $\overline{SCKn} \uparrow$)	<71>	t_{HSKSI2}		10		10		ns
SOn output delay time (vs. $\overline{SCKn} \downarrow$)	<72>	t_{DSKSO2}			30		30	ns
SOn output hold time (vs. $\overline{SCKn} \uparrow$)	<73>	t_{HSKSO2}		t_{WSKH2}		t_{WSKH2}		ns

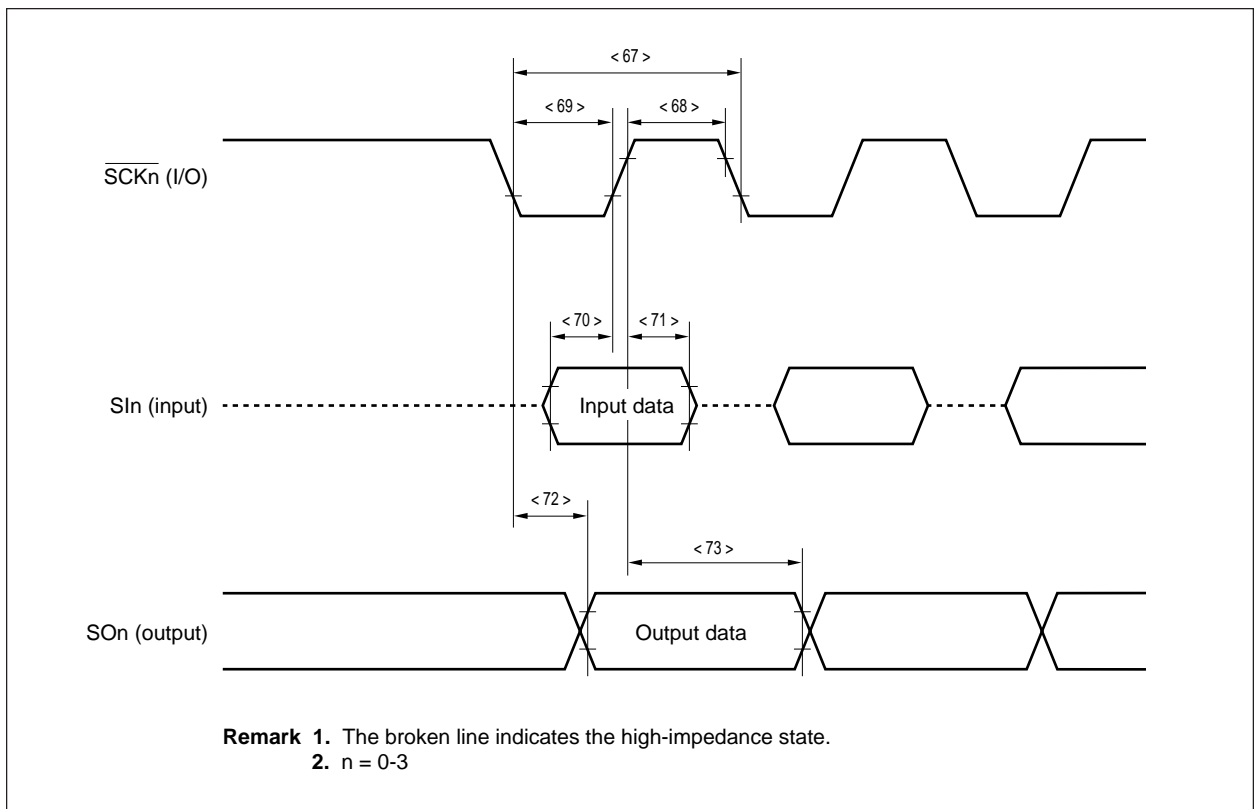
Remark n = 0-2

(9) CSI timing (2/2)

(ii) CSI3 timing

Parameter	Symbol	Condition	25 MHz Model		33 MHz Model		Unit	
			MIN.	MAX.	MIN.	MAX.		
$\overline{\text{SCK3}}$ cycle	<67>	t_{CYSK4}	Input	500		500		ns
$\overline{\text{SCK3}}$ width, high	<68>	t_{WSKH4}	Input	180		180		ns
$\overline{\text{SCK3}}$ width, low	<69>	t_{WSKL4}	Input	180		180		ns
SI3 setup time (vs. $\overline{\text{SCK3}} \uparrow$)	<70>	t_{SSISK4}		100		100		ns
SI3 hold time (vs. $\overline{\text{SCK3}} \uparrow$)	<71>	t_{HSKSI4}		50		50		ns
SO3 output delay time (vs. $\overline{\text{SCK3}} \downarrow$)	<72>	t_{DSKSO4}	$R_L = 1.5 \text{ k}\Omega$		150		150	ns
SO3 output hold time (vs. $\overline{\text{SCK3}} \uparrow$)	<73>	t_{HSKSO4}	$C_L = 50 \text{ pF}$	t_{WSKH4}		t_{WSKH4}		ns

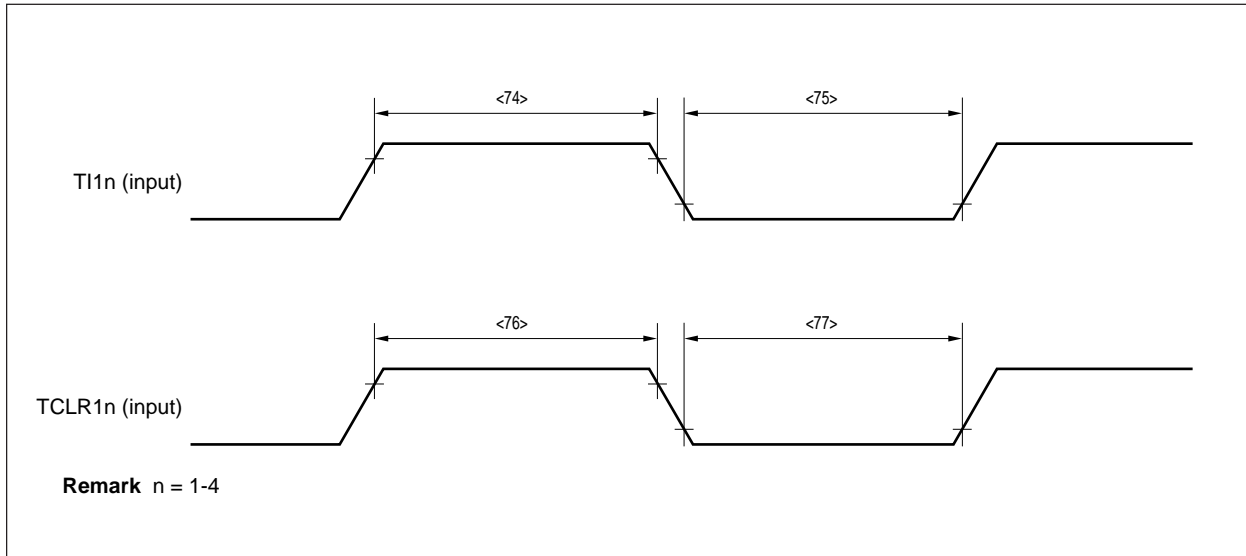
Remark R_L and C_L are the load resistance and load capacitance respectively of the SCK3 and SO3 output lines.



(10) RPU timing

Parameter	Symbol		Condition	25 MHz Model		33 MHz Model		Unit
				MIN.	MAX.	MIN.	MAX.	
Tl1n width, high	<74>	t _{WTIH}		3 T + 10		3 T + 10		ns
Tl1n width, low	<75>	t _{WTIL}		3 T + 10		3 T + 10		ns
TCLR1n width, high	<76>	t _{WTCH}		3 T + 10		3 T + 10		ns
TCLR1n width, low	<77>	t _{WTCL}		3 T + 10		3 T + 10		ns

Remark T = t_{cyk}



A/D Converter Characteristics (T_A = -40 to +85 °C, V_{DD} = AV_{DD} = 5 V ±10 %, V_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	25 MHz Model			33 MHz Model			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Resolution	—		10			10			bit
Overall error ^{Note 1}	—	4.5 V ≤ AV _{REF1} ≤ AV _{DD}			±0.4			±0.4	%FSR
	—	3.5 V ≤ AV _{REF1} ≤ AV _{DD}			±0.7			±0.7	%FSR
Quantize error	—				±1/2			±1/2	LSB
Conversion time	t _{CONV}	4.5 V ≤ AV _{REF1} ≤ AV _{DD}	48			60			t _{cyk}
		3.5 V ≤ AV _{REF1} ≤ AV _{DD}	48			60			t _{cyk}
Sampling time	t _{SAMP}	4.5 V ≤ AV _{REF1} ≤ AV _{DD}	8			10			t _{cyk}
		3.5 V ≤ AV _{REF1} ≤ AV _{DD}	8			10			t _{cyk}
Zero-scale error ^{Note 1}	—	4.5 V ≤ AV _{REF1} ≤ AV _{DD}		±1.5	±3.5		±1.5	±3.5	LSB
	—	3.5 V ≤ AV _{REF1} ≤ AV _{DD}		±1.5	±4.5		±1.5	±4.5	LSB
Full-scale error ^{Note 1}	—	4.5 V ≤ AV _{REF1} ≤ AV _{DD}		±1.5	±2.5		±1.5	±2.5	LSB
	—	3.5 V ≤ AV _{REF1} ≤ AV _{DD}		±1.5	±4.5		±1.5	±4.5	LSB
Non-linear error ^{Note 1}	—	4.5 V ≤ AV _{REF1} ≤ AV _{DD}		±1.5	±2.5		±1.5	±2.5	LSB
	—	3.5 V ≤ AV _{REF1} ≤ AV _{DD}		±1.5	±4.5		±1.5	±4.5	LSB
Analog input voltage ^{Note 2}	V _{IAN}		-0.3		AV _{DD} +0.3	-0.3		AV _{DD} +0.3	V
Reference voltage	AV _{REF1}		3.5		AV _{DD}	3.5		AV _{DD}	V
AV _{REF1} current	AI _{REF1}			1.2	3.0		1.2	3.0	mA
AV _{DD} supply current	AI _{DD}			2.3	6.0		2.3	6.0	mA

★

- Notes**
1. Except quantize error
 2. The conversion result is 000H when V_{IAN} = 0.
 Converted with 10-bit resolution when 0 < V_{IAN} < AV_{REF1}.
 The conversion result is 3FFH when AV_{REF1} ≤ V_{IAN} ≤ AV_{DD}.

D/A Converter Characteristics (T_A = -40 to + 85 °C, V_{DD} = AV_{DD} = 5 V ±10 %, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	25 MHz Model			33 MHz Model			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Resolution	—				8			8	bit
Overall error	—	Load conditions: 2 MΩ, 30 pF AV _{REF2} = V _{DD} AV _{REF3} = 0			0.8			0.8	%
	—	Load conditions: 2 MΩ, 30 pF AV _{REF2} = 0.75 V _{DD} AV _{REF3} = 0.25 V _{DD}			1.0			1.0	%
	—	Load conditions: 4 MΩ, 30 pF AV _{REF2} = V _{DD} AV _{REF3} = 0			0.6			0.6	%
	—	Load conditions: 4 MΩ, 30 pF AV _{REF2} = 0.75 V _{DD} AV _{REF3} = 0.25 V _{DD}			0.8			0.8	%
Settling time	—	Load conditions: 2 MΩ, 30 pF			10			10	μs
★ Output resistance	RO			8			8		kΩ
AV _{REF2} input voltage	AV _{REF2}		0.75 V _{DD}		V _{DD}	0.75 V _{DD}		V _{DD}	V
AV _{REF3} input voltage	AV _{REF3}		0		0.25 V _{DD}	0		0.25 V _{DD}	V
★ AV _{REF2} -AV _{REF3} resistance value	R _{AIREF}	DACS0, DACS1 = 55H	2	4		2	4		kΩ

3.2 Flash Memory Programming Mode

★ **Basic Characteristics** ($T_A = -40$ to $+85$ °C, $V_{DD} = 5$ V ± 10 %, $V_{SS} = 0$ V, $V_{PP} = 10.3$ V ± 0.3 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_x		10		33	MHz
Supply voltage	V_{DD}		4.5		5.5	V
	V_{PPL}	V_{PP} low level detection	-0.5		$0.2 V_{DD}$	V
	V_{PPM}	V_{PP} , V_{DD} level detection	$0.8 V_{DD}$		$1.2 V_{DD}$	V
	V_{PPH}	V_{PP} high voltage detection	10.0	10.3	10.6	V
V_{DD} supply current	I_{DO}				$3.0 \times \phi + 25$	mA
V_{PP} supply current	I_{PP}	$V_{PP} = 10.3$ V			200	mA
V_{PP} pull-down resistance value	R_{VPP}		5		15	kΩ
Transfer speed between programmer and device	–	CSI0	0.2		1	MHz
	–	UART0	4800		76800	bps
Number of rewrite	C_{WRT}				20	times
Write time	t_{WRT}	Note		200	500	μs
Erasure time	t_{ERASE}	μPD70F3003A		20	40	s
		μPD70F3025A		40	80	s

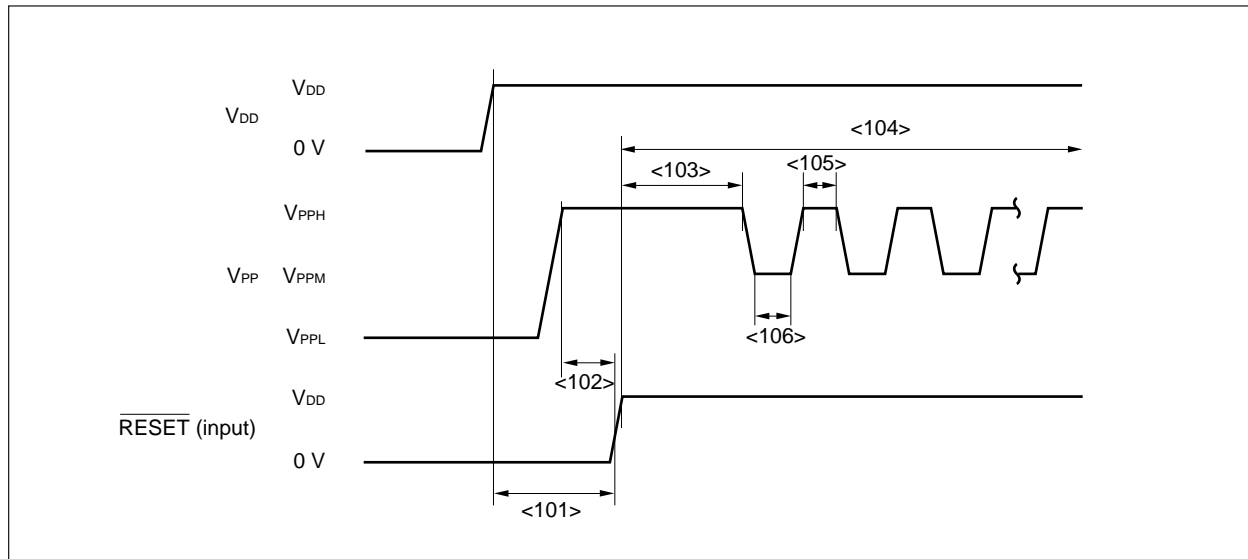
Note When retried 10 times with 50 μs write time

Remark φ: Internal system clock frequency

Serial Write Operation Characteristics

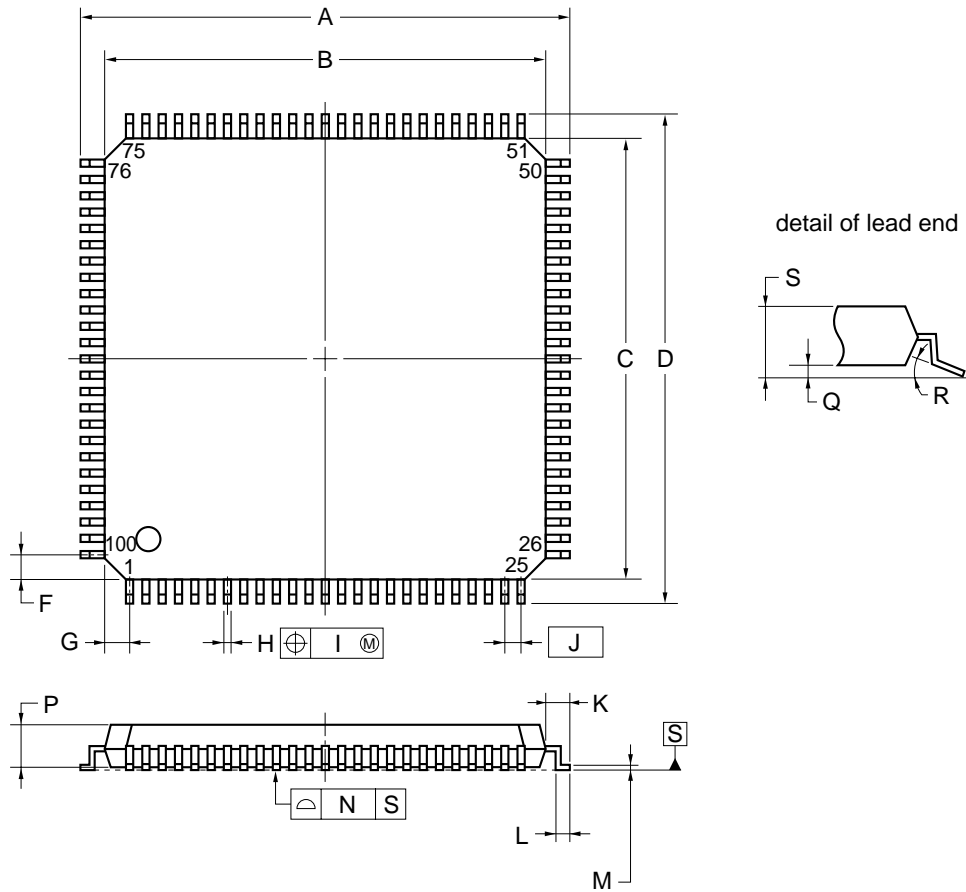
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$V_{DD} \uparrow \rightarrow \overline{\text{RESET}} \uparrow$ setup time	<101> t_{DRRR}		10			ms
$V_{PP} \uparrow \rightarrow \overline{\text{RESET}} \uparrow$ setup time	<102> t_{PSRR}		1.0			μs
$\overline{\text{RESET}} \uparrow \rightarrow V_{PP}$ count start time	<103> t_{RRCF}		$5T + 500$			ns
Count end time	<104> t_{COUNT}				10	ms
V_{PP} counter width, high	<105> t_{CH}		1.0			μs
V_{PP} counter width, low	<106> t_{CL}		1.0			μs

Remark T = t_{cyk}



★ 4. PACKAGE DRAWING

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



NOTE
 Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	16.00±0.20
B	14.00±0.20
C	14.00±0.20
D	16.00±0.20
F	1.00
G	1.00
H	0.22 ^{+0.05} _{-0.04}
I	0.08
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	0.17 ^{+0.03} _{-0.07}
N	0.08
P	1.40±0.05
Q	0.10±0.05
R	3° ^{+7°} _{-3°}
S	1.60 MAX.

S100GC-50-8EU-1

★ 5. RECOMMENDED SOLDERING CONDITIONS

Solder this product under the following recommended conditions.

For details of the recommended soldering conditions, refer to information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended, consult NEC.

Table 5-1. Soldering Conditions

μPD70F3003AGC-xx-8EU : 100-pin plastic LQFP (fine pitch) (14 × 14 mm)

μPD70F3025AGC-xx-8EU : 100-pin plastic LQFP (fine pitch) (14 × 14 mm)

Soldering Method	Soldering Condition	Symbol of Recommended Soldering Condition
Infrared reflow	Package peak temperature: 235 °C, Time: 30 seconds max. (210 °C min.), Number of times: 3 max., Number of days: 3 ^{Note} (after that, prebaking is necessary at 125 °C for 10 hours.)	IR35-103-3
VPS	Package peak temperature: 215 °C, Time: 40 seconds max. (200 °C min.), Number of times: 3 max., Number of days: 3 ^{Note} (after that, prebaking is necessary at 125 °C for 10 hours.)	VP15-103-3
Partial heating	Pin temperature: 300 °C max., Time: 3 seconds max. (per side of device)	—

Note The number of days for storage at 25 °C, 65% RH MAX after the dry pack has been opened.

Caution Do not use two or more soldering methods in combination (except partial heating method).

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Related document : μ PD703003 Data Sheet (U12261E)
 μ PD703003A, 703004A, 703025A Data Sheet (U13188E)
 μ PD70F3003 Data Sheet (U12036E)

Reference document: Concept of Electrical Characteristics - Microcomputers (IEI-601) (Japanese version)

The related documents referred to in this publication may include preliminary versions. However, preliminary versions are not marked as such.

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- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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[MEMO]

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