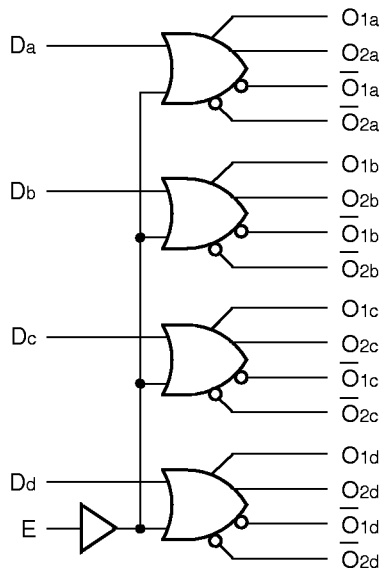


FEATURES

- Max. propagation delay of 800ps
- Enable to Output max. of 950ps
- IEE min. of -60mA
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- 50% faster than National 300K
- Function and pinout compatible with National and Signetics F100K
- ESD protection of 2000V
- Available in 24-pin CERDIP, 24-pin CERPAC and 28-pin PLCC packages

BLOCK DIAGRAM



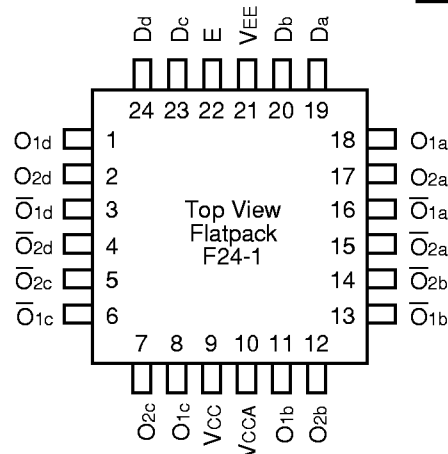
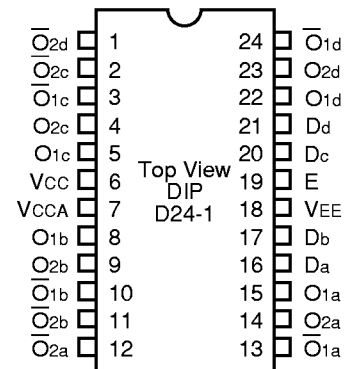
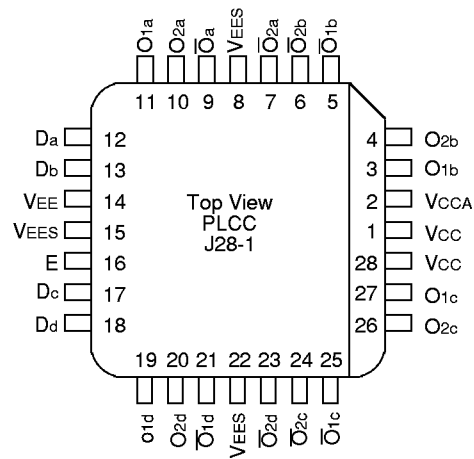
PIN NAMES

Pin	Function
Da – Dd	Data Inputs (n-1...5)
E	Enable Input
O _{na} – O _{nd}	Data Outputs
\overline{O}_{na} – \overline{O}_{nd}	Complementary Data Outputs
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

DESCRIPTION

The SY100S313 offers four drivers with two OR and two NOR outputs, designed for use in high-performance ECL systems. The four drivers are controlled by a common Enable signal which is buffered to minimize input loading. If the D inputs are not used, the Enable signal can be used to drive sixteen 50Ω lines. All inputs have 75KΩ pulldown resistors and all outputs are buffered.

PIN CONFIGURATIONS



LOGIC EQUATION

$$O = D + E$$

$$\overline{O} = \overline{D + E}$$

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{IH}	Input HIGH Current, All Inputs	—	—	200	μA	V _{IN} = V _{IH} (Max.)
I _{EE}	Power Supply Current	-60	-43	-20	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Output	200	900	200	900	200	900	ps	
t _{PLH} t _{PHL}	Propagation Delay Enable to Output	300	1100	300	1100	300	1100	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

CERPACK

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

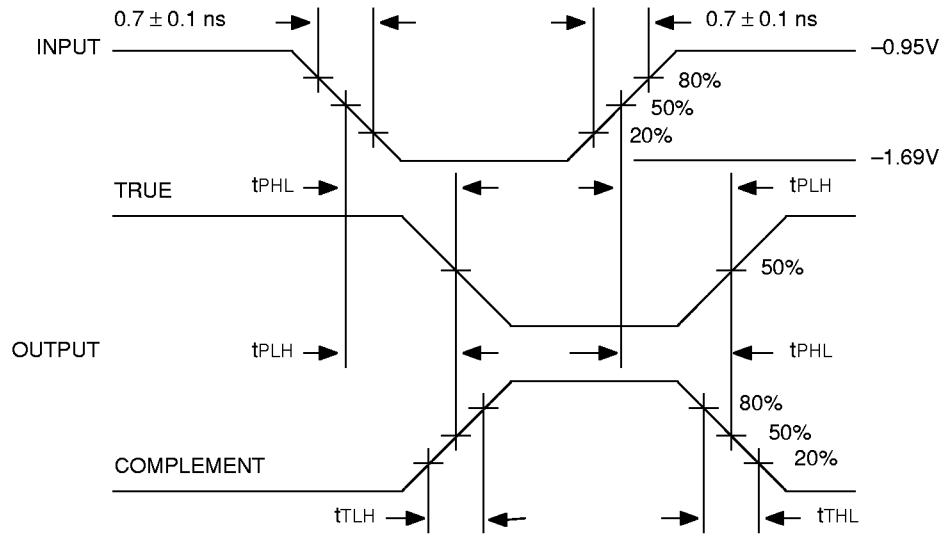
Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Output	200	850	200	850	200	850	ps	
t _{PLH} t _{PHL}	Propagation Delay Enable to Output	300	1000	300	1000	300	1000	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

PLCC

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Output	200	800	200	800	200	800	ps	
t _{PLH} t _{PHL}	Propagation Delay Enable to Output	300	950	300	950	300	950	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

TIMING DIAGRAM



Propagation Delay and Transition Times

NOTE:

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S313DC	D24-1	Commercial
SY100S313FC	F24-1	Commercial
SY100S313JC	J28-1	Commercial
SY100S313JCTR	J28-1	Commercial

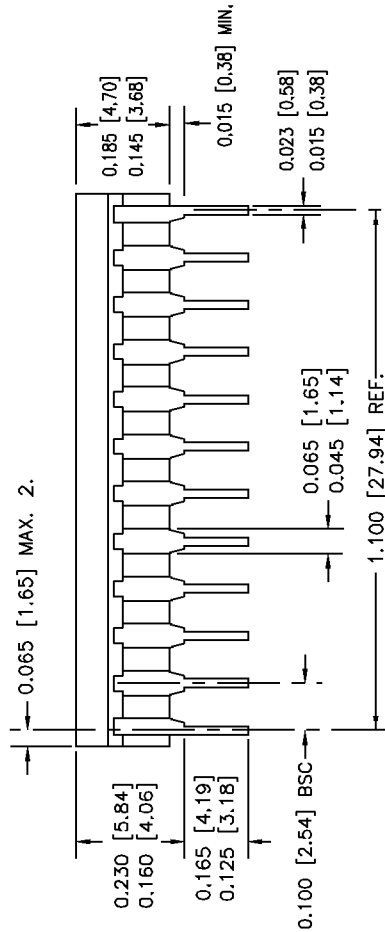
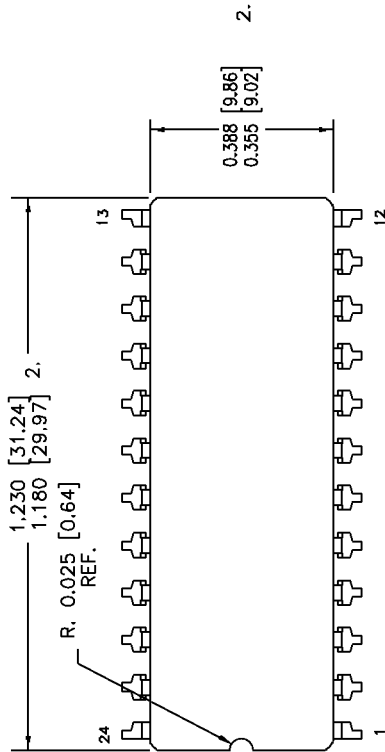
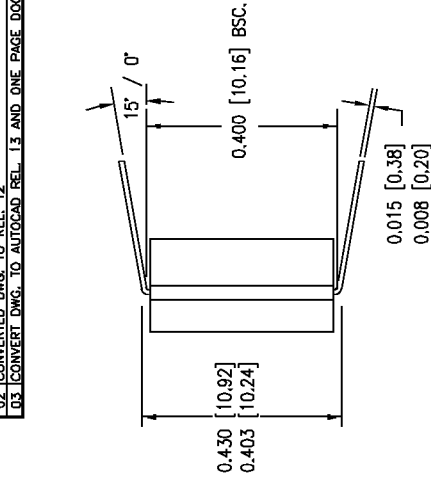
24 LEAD CERDIP (D24-1)

FILE/REV #: PD0003A03

PD/0003/ASCORP

PAGE 1 OF 1

REV.	REVISION DESCRIPTION	DATE
01	CONVERT DWG. TO DESIGNER VERSION 4.0 FORMAT.	12/30/93
02	CONVERTED DWG. TO REL. 12	03/15/96
03	CONVERT DWG. TO AUTOCAD REL. 1.3 AND ONE PAGE DOCUMENT.	02/18/98



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
- THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.



3250 SCOTT BOULEVARD
SANTA CLARA CA 95054
TEL: 408-980-9191
FAX: 408-567-7878

APPROVALS	DATE	APPROVALS	DATE	SIZE	24 LEAD CERDIP (400" WIDE) PACKAGE OUTLINE
ORIGINATOR: FERMIN G. LURRITA	02/23/98	QUALITY: MARSHALL WILDER		A	
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			
RELEASE DATE:					

SCALE	REVISION
N/A	03

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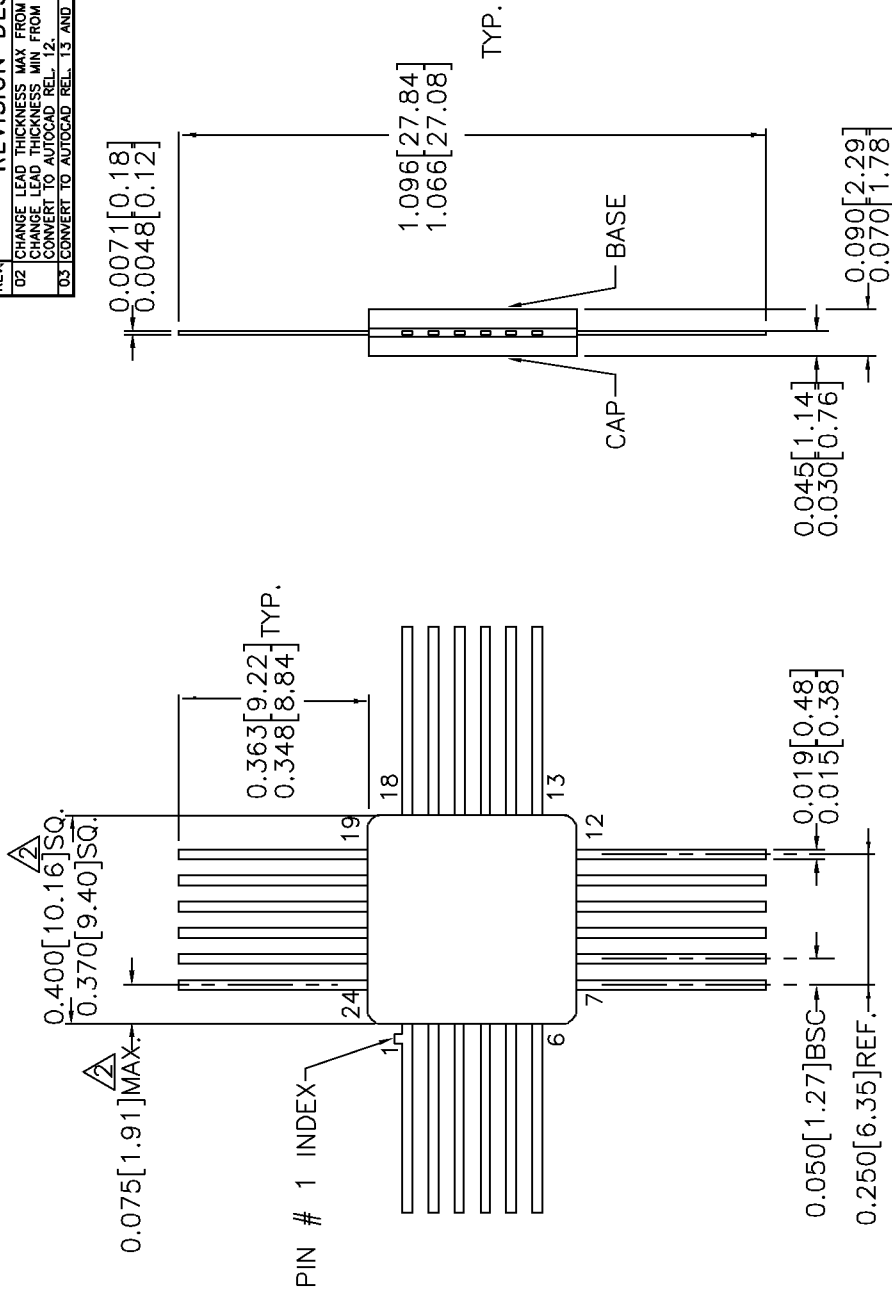
28 LEAD PLASTIC LEADED CHIP

FILE/REV #: PD/0006/ASCORP

PAGE 1 OF 1

REVISION DESCRIPTION

REV.	REVISION DESCRIPTION	DATE
02	CHANGE LEAD THICKNESS MAX FROM 0.006[0.15] TO 0.0071[0.18] CHANGE LEAD THICKNESS MIN FROM 0.004[0.10] TO 0.0048[0.12] CONVERT TO AUTOCAD REL. 12.	01/04/96
03	CONVERT TO AUTOCAD REL. 13 AND 1 PAGE DWG.	02/18/98



- NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
 - THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
 3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.



3250 SCOTT BOULEVARD
SANTA CLARA, CA 95054
TEL: 408-980-9191
FAX: 408-587-7878

APPROVALS	DATE	APPROVALS	DATE	SIZE	24 LEAD CERPACK
ORIGINATOR: FERNIN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A	PACKAGE OUTLINE
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFLIPPID			
RELEASE DATE:					

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SCALE: IN/A
REVISION: 03

28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)

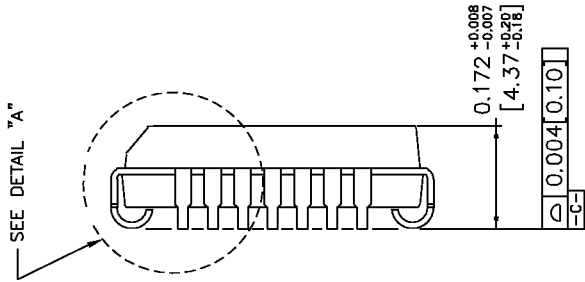
FILE/REV #: PD0008A03

PD/0008/ASCORP

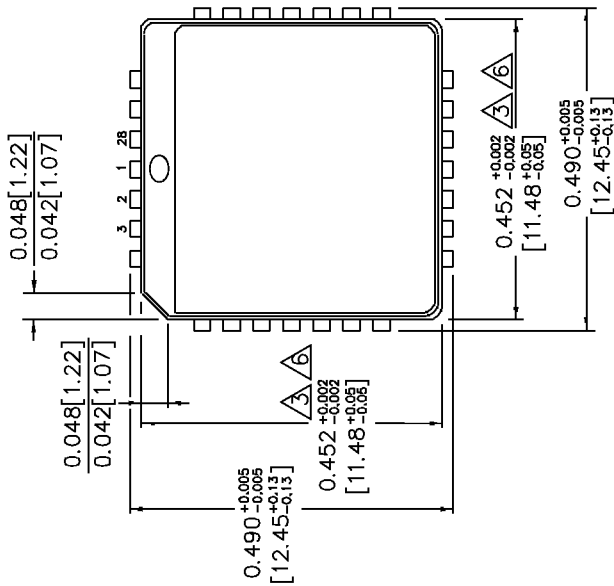
PAGE 1 OF 1

REV.	REVISION DESCRIPTION	DATE
01	CONVERT TO DESIGNER VERSION A.D. FORMAT AND COVER PAGE TO SPEC. CHANGE BODY WIDTH DIMENSION FROM 0.450[11.43] TO 0.443[11.25] TYP. GEOMETRICAL ERROR.	08/18/94
02	CONVERT DWG FROM DESIGNER TO AUTOCAD REL. 12. REFERENCE AMIKOR DWG. NO. 34653 REV. 00.	02/22/96
03	CONVERT DWG TO REL. 15 AND ONE PAGE DOCUMENT.	02/18/98

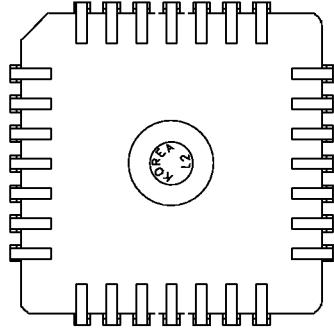
SIDE VIEW



TOP VIEW



BOTTOM VIEW



NOTES:

1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.



3250 SCOTT BOULEVARD
SANTA CLARA, CA. 95054
TEL: 408-960-9191
FAX: 408-367-7878

APPROVALS	DATE	APPROVALS	DATE	SIZE	28 LEAD PLCC	PACKAGE OUTLINE
ORIGINATOR: ERMIN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A		
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO				
RELEASE DATE:						

SCALE
N/A
REVISION
03

DETAIL "A"

