

# **SWITCHMODE™ Series NPN Silicon Power Darlington Transistors with Base-Emitter Speedup Diode**

The MJ10020 and MJ10021 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated SWITCHMODE applications such as:

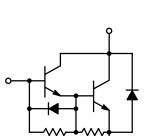
- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times

150 ns Inductive Fall Time at 25°C (Typ) 750 ns Inductive Storage Time at 25°C (Typ)

- Operating Temperature Range –65 to +200°C
- 100°C Performance Specified for:

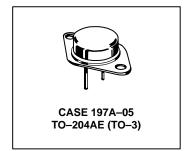
Reversed Biased SOA with Inductive Loads Switching Times with Inductive Loads Saturation Voltages

Leakage Currents



# MJ10020 MJ10021

60 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTORS
200 AND 250 VOLTS
250 WATTS



### **MAXIMUM RATINGS**

Rating	Symbol	MJ10020	MJ10021	Unit
Collector–Emitter Voltage	V <sub>CEO</sub>	200	250	Vdc
Collector–Emitter Voltage	V <sub>CEV</sub>	300	350	Vdc
Emitter Base Voltage	V <sub>EB</sub>	8.0		Vdc
Collector Current — Continuous — Peak (1)	I <sub>C</sub>	60 100		Adc
Base Current — Continuous — Peak (1)	I <sub>B</sub>	20 30		Adc
Total Power Dissipation @ $T_C = 25^{\circ}C$ @ $T_C = 100^{\circ}C$ Derate above $25^{\circ}C$	P <sub>D</sub>	250 143 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-65 to +200		°C

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{ heta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	TL	275	°C

1

<sup>(1)</sup> Pulse Test: Pulse Width = 5 ms, Duty Cycle  $\leq$  10%.

### **ELECTRICAL CHARACTERISTICS** (T<sub>C</sub> = 25°C unless otherwise noted)

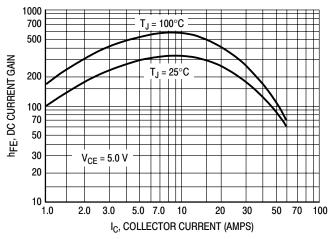
Characteristic			Symbol	Min	Тур	Max	Unit
OFF CHARACTERIST	rics						
Collector–Emitter Su: (I <sub>C</sub> = 100 mA, I <sub>B</sub> =	staining Voltage (Table 1) 0)	MJ10020 MJ10021	V <sub>CEO(sus)</sub>	200 250	_	_	Vdc
Collector Cutoff Current $(V_{CEV} = Rated \ Value, \ V_{BE(off)} = 1.5 \ Vdc)$ $(V_{CEV} = Rated \ Value, \ V_{BE(off)} = 1.5 \ Vdc, \ T_C = 150 ^{\circ}C)$			I <sub>CEV</sub>		_	0.25 5.0	mAdo
Collector Cutoff Curro (V <sub>CE</sub> = Rated V <sub>CE</sub> )	ent <sub>V</sub> , R <sub>BE</sub> = 50 Ω, T <sub>C</sub> = 100°C)		I <sub>CER</sub>	_	_	5.0	mAdd
Emitter Cutoff Current $(V_{EB} = 2.0 \text{ V}, I_{C} = 0)$			I <sub>EBO</sub>	_	_	175	mAdd
SECOND BREAKDOV	VN						
Second Breakdown (	Collector Current with base forward biased		I <sub>S/b</sub>		See Fig	gure 13	
Clamped Inductive S	OA with Base Reverse Biased		RBSOA		See Fig	gure 14	
ON CHARACTERISTI	CS (2)	•					1
DC Current Gain (I <sub>C</sub> = 15 Adc, V <sub>CE</sub> :	= 5.0 V)		h <sub>FE</sub>	75	_	1000	_
Collector–Emitter Saturation Voltage $ \begin{aligned} &(I_C=30 \text{ Adc}, I_B=1.2 \text{ Adc}) \\ &(I_C=60 \text{ Adc}, I_B=4.0 \text{ Adc}) \\ &(I_C=30 \text{ Adc}, I_B=1.2 \text{ Adc}, T_C=100^{\circ}\text{C}) \end{aligned} $		V <sub>CE(sat)</sub>		_ _ _	2.2 4.0 2.4	Vdc	
Base–Emitter Saturation Voltage ( $I_C$ = 30 Adc, $I_B$ = 1.2 Adc) ( $I_C$ = 30 Adc, $I_B$ = 1.2 Adc, $T_C$ = 100°C)		V <sub>BE(sat)</sub>			3.0 3.5	Vdc	
Diode Forward Voltage (I <sub>F</sub> = 30 Adc)			$V_{f}$	_	2.5	5.0	Vdc
OYNAMIC CHARACTI	ERISTICS						
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f <sub>test</sub> = 1.0 kHz)			$C_{ob}$	175	_	700	pF
SWITCHING CHARAC	CTERISTICS						
Resistive Load (Tab	le 1)					_	
Delay Time			t <sub>d</sub>	_	0.02	0.2	μs
Rise Time	$(V_{CC} = 175 \text{ Vdc}, I_{C} = 30 \text{ A},$	F 0	t <sub>r</sub>	_	0.30	1.0	μs
Storage Time	$I_{B1} = Adc, V_{BE(off)} = 5.0 \text{ V}, t_p = 25$ Duty Cycle $\leq 2.0\%$ ).	ο με	t <sub>s</sub>	_	1.0	3.5	μs
Fall Time	' ' ' '		t <sub>f</sub>	_	0.07	0.5	μs
Inductive Load, Cla	mped (Table 1)						
Storage Time	$I_{CM} = 30 \text{ A(pk)}, V_{CEM} = 200 \text{ V}, I_{B1} = 1.2 \text{ A}, V_{BE(off)} = 5 \text{ V}, T_{C} = 100^{\circ}\text{C})$		t <sub>sv</sub>	_	1.2	3.5	μs
Crossover Time			t <sub>c</sub>	_	0.45	2.0	μs
Storage Time		t <sub>sv</sub>	_	0.75	_	μs	
Crossover Time $(I_{CM} = 30 \text{ A(pk)}, V_{CEM} = 200 \text{ V, } I_{B1} = 1.2 \text{ A}, V_{BE(off)} = 5 \text{ V, } T_{C} = 25^{\circ}\text{C})$		t <sub>c</sub>	_	0.25	_	μs	
Fall Time			t <sub>fi</sub>	_	0.15	_	μs

<sup>(1)</sup> Pulse Test: PW = 300  $\mu$ s, Duty Cycle  $\leq$  2%.

### TYPICAL ELECTRICAL CHARACTERISTICS

4.5

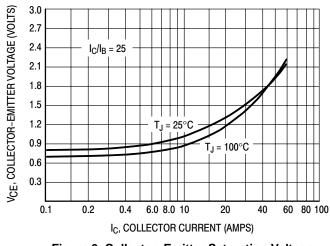
4.0



V<sub>CE</sub>, COLLECTOR-EMITTER VOLTAGE (VOLTS) 3.5 3.0 2.5 2.0 = 30 A1.5 = 10 A1.0 I<sub>C</sub> = 1.0 A 0.5 2.0 3.0 5.0 0.01 0.02 0.05 0.2 0.3 0.5 1.0 10 IR, BASE CURRENT (AMPS)

Figure 1. DC Current Gain

Figure 2. Collector Saturation Region



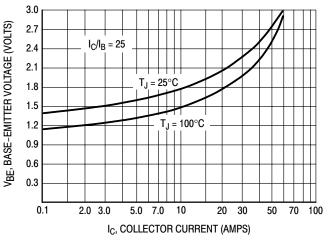
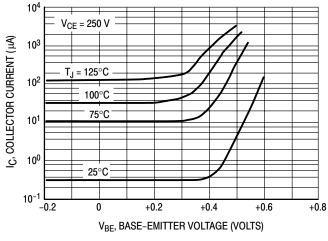


Figure 3. Collector-Emitter Saturation Voltage

Figure 4. Base-Emitter Voltage



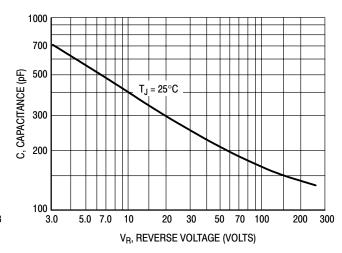


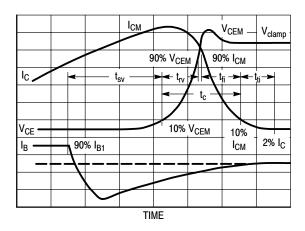
Figure 5. Collector Cutoff Region

Figure 6. Output Capacitance

**Table 1. Test Conditions for Dynamic Performance** 

	V. BROOM AND INDUCTIVE SWITCHING			DECICEIVE CMITCHING	
	V <sub>CEO(sus)</sub>	RBSOA AND INDUCTIVE SWITCHING		RESISTIVE SWITCHING	
INPUT	$ \begin{array}{c c} 20 \Omega \\ \hline 0 & 1 \end{array} $ $ \begin{array}{c c} 5 V \\ \hline 0 & 2 \end{array} $ PW Varied to Attain $ \begin{array}{c c} 1C = 100 \text{ mA} \end{array} $	INDUCTIVE TEST CIRCUIT  TUT  IN4937 OR  EQUIVALENT  Volump = VCC  RS = 0.1 \( \Omega)  VCC		TURN-ON TIME  O 1  I <sub>B1</sub> = 0 2  I <sub>B1</sub> adjusted to obtain the forced h <sub>FE</sub> desired  TURN-OFF TIME  Use inductive switching driver as the input to the resistive test circuit.	
CIRCUIT	$\begin{aligned} & L_{coil} = 10 \text{ mH, V}_{CC} = 10 \text{ V} \\ & R_{coil} = 0.7 \Omega \\ & V_{clamp} = V_{CEO(sus)} \end{aligned}$	$L_{coil}$ = 180 μH $R_{coil}$ = 0.05 $\Omega$ $V_{CC}$ = 20 V		$V_{CC}$ = 175 $V$ $R_L$ = 5.6 $\Omega$ Pulse Width = 25 $\mu$ s	
TEST CIRCUITS	lc	OUTPUT WAVEFORMS  t <sub>1</sub> Clamped  t V <sub>clamp</sub> t <sub>1</sub> TIME  t <sub>2</sub> t <sub>3</sub>	$\begin{aligned} &t_1 \text{ Adjusted to} \\ &\text{Obtain } l_C \\ &t_1 \approx \frac{L_{coil} \left(l_{CM}\right)}{V_{CC}} \\ &t_2 \approx \frac{L_{coil} \left(l_{CM}\right)}{V_{Clamp}} \\ &\text{Test Equipment} \\ &\text{Scope} - \text{Tektronix} \\ &475 \text{ or Equivalent} \end{aligned}$	RESISTIVE TEST CIRCUIT  TUT  RL  2  VCC  VCC	

<sup>\*</sup>Adjust –V such that  $V_{BE(off)}$  = 5 V except as required for RBSOA (Figure 14).





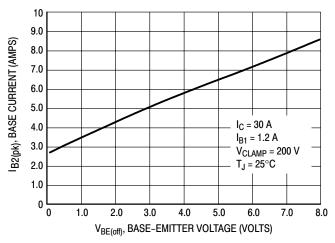


Figure 8. Typical Peak Reverse Base Current

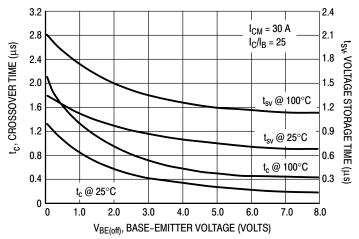


Figure 9. Typical Inductive Switching Times

### **SWITCHING TIMES NOTE**

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

 $t_{sv}$  = Voltage Storage Time, 90%  $I_{B1}$  to 10%  $V_{CEM}$ 

 $t_{rv}$  = Voltage Rise Time, 10–90%  $V_{CEM}$ 

 $t_{fi}$  = Current Fall Time, 90–10%  $I_{CM}$ 

 $t_{ti} = Current Tail, 10-2\% I_{CM}$ 

 $t_c$  = Crossover Time, 10%  $V_{CEM}$  to 10%  $I_{CM}$ 

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222A:

$$P_{SWT} = 1/2 V_{CC} I_{C} (t_{c}) f$$

In general,  $t_{rv} + t_{fi} \cong t_c$ . However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t<sub>c</sub> and t<sub>sv</sub>) which are guaranteed at 100°C.

### **RESISTIVE SWITCHING**

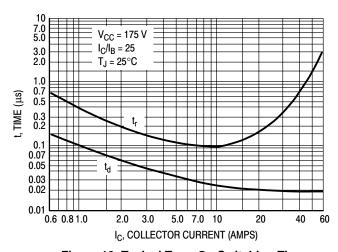


Figure 10. Typical Turn-On Switching Times

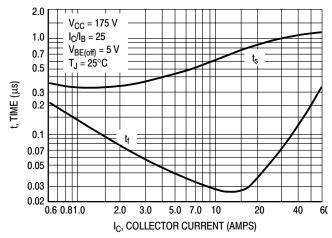


Figure 11. Typical Turn-Off Switching Times

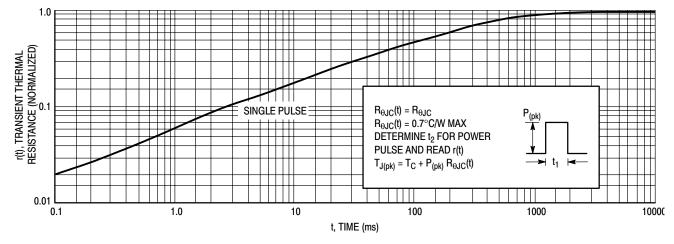


Figure 12. Thermal Response

The Safe Operating Area figures shown in Figures 13 and are specified for these devices under the test conditions shown.

# 100 $_{\odot}$ 100 $_{\odot}$

Figure 13. Maximum Forward Bias Safe Operating Area

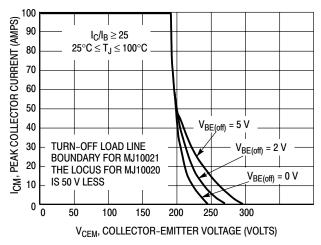


Figure 14. Maximum RBSOA, Reverse Bias Safe Operating Area

### SAFE OPERATING AREA INFORMATION

### **FORWARD BIAS**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on  $T_C = 25^{\circ}C$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C \ge 25^{\circ}C$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

 $T_{J(pk)}$  may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

### **REVERSE BIAS**

For Inductive loads, high voltage and high current must be sustained simultaneously during turn—off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage—current condition allowable during reverse biased turn—off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

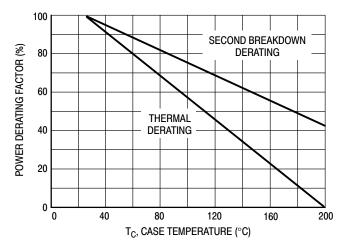
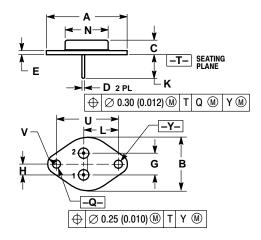


Figure 15. Power Derating

### PACKAGE DIMENSIONS

**CASE 197A-05** TO-204AE (TO-3) **ISSUE J** 



### NOTES

- DIMENSIONING AND TOLERANCING PER ANSI Y14 5M 1982
- 2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	1.530 REF		38.86 REF		
В	0.990	1.050	25.15	26.67	
C	0.250	0.335	6.35	8.51	
D	0.057	0.063	1.45	1.60	
Е	0.060	0.070	1.53	1.77	
G	0.430 BSC		10.92 BSC		
Н	0.215 BSC		5.46 BSC		
K	0.440	0.480	11.18	12.19	
L	0.665 BSC 16.89 BSC		BSC		
N	0.760	0.830	19.31	21.08	
Q	0.151	0.165	3.84	4.19	
U	1.187 BSC		30.15 BSC		
٧	0.131	0.188	3.33	4.77	

STYLE 1: PIN 1. BASE

2. EMITTER CASE: COLLECTOR

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