ANALOG DEVICES

16×16-Bit CMOS Multiplier/Accumulator

ADSP-1010B

FEATURES

- **Higher-Speed Version of ADSP-1010A**
- **16×16-Bit Parallel Multiplication/Accumulation**
- **45ns Multiply/Accumulate Time**
- **170mW Power Dissipation with 10MHz Clock**
- **Twos Complement or Unsigned Magnitude**
- **Preloadable Accumulation Registers**
- **Available in Hermetically Sealed 64-Pin Ceramic DIP, Hermetically Sealed 68-Pin Grid Array or 68-Lead PLCC**
- **Available Specified to MIL-STD-883, Class B**
- **Pin-Compatible with ADSP-1010, ADSP-1010A, TDC1010J1, TMC2010J3 and TMC2110J3**

APPLICATIONS

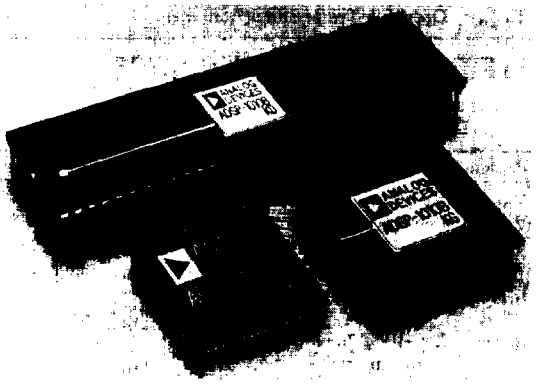
- **Digital Signal Processing**
  - **Digital Filtering**
  - **Fourier Transformations**
  - **Correlations**
- **Image Processing**
- **Telecommunications**

GENERAL DESCRIPTION

The ADSP-1010B is a high speed, low power 16×16-bit parallel multiplier/accumulator fabricated in 1.0 micron CMOS. The ADSP-1010B is a pin-for-pin replacement for Analog Devices' ADSP-1010 and ADSP-1010A and is also pin-for-pin compatible with TRW's TDC1010J1, TMC2010J3, and TMC2110J3. The ADSP-1010B consumes the same power as the ADSP-1010A at the rated maximum clock rate of the ADSP-1010A.

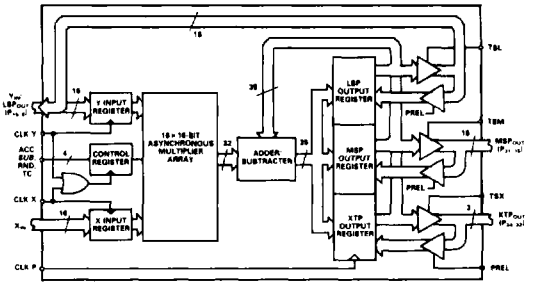
The ADSP-1010B has two 16-bit input ports, a 16-bit most significant product (MSP) port, a 16-bit least significant product (LSP) port and a 3-bit extended product (XTP) port. The LSP output port is a bidirectional port shared with the Y input port. Inputs can be represented in either twos complement or unsigned magnitude formats. The ADSP-1010B produces a 32-bit product whose MSP can be rounded with a control which causes a 1 to be added to the most significant bit (MSB) of the LSP. After multiplying, the ADSP-1010B can latch its product directly into the output register or update the output registers with its previous contents added to or subtracted from the product. The output registers can also be initialized prior to multiplication/accumulation with data preloaded from the output ports.

All input pins are ESD protected. The input and output registers are all D-type positive-edge-triggered flip-flops. The input



registers are controlled by independent clock lines. A third clock line controls the product registers. Each of the three product registers has its own three-state output control. Three-state outputs and independently clocked inputs allow the ADSP-1010B to be connected directly to a single 16-bit bus.

The ADSP-1010B is available for both commercial and MIL temperature ranges. MIL-grade parts are available processed fully to MIL-STD-883, Class B. Additionally, the ADSP-1010B is available in either a 64-pin hermetically sealed ceramic DIP, a space-saving, hermetically sealed 68-pin grid array or a 68-lead PLCC.



Functional Block Diagram

SPECIFICATIONS[1]

RECOMMENDED OPERATING CONDITIONS

		ADSP-1010B J and K Grades		ADSP-1010B S and T Grades[2]		
Parameter		**Min**	**Max**	**Min**	**Max**	**Unit**
V_{DD}	Supply Voltage	4.75	5.25	4.5	5.5	V
T_{AMB}	Operating Temperature (Ambient)	0	+70	−55	+125	°C

ELECTRICAL CHARACTERISTICS

			ADSP-1010B J and K Grades		ADSP-1010B S and T Grades[2]		
Parameter		**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
V_{IH}	High-Level Input Voltage	@ V_{DD} = max	2.0		2.0		V
V_{IL}	Low-Level Input Voltage	@ V_{DD} = min		0.8		0.8	V
V_{OH}	High-Level Output Voltage	@ V_{DD} = min & I_{OH} = −1.0mA	2.4		2.4		V
V_{OL}	Low-Level Output Voltage	@ V_{DD} = min & I_{OL} = 4.0mA		0.4		0.4	V
I_{IH}	High-Level Input Current, All Inputs	@ V_{DD} = max & V_{IN} = 5.0V		10		10	μA
I_{IL}	Low-Level Input Current, All Inputs	@ V_{DD} = max & V_{IN} = 0V		10		10	μA
I_{OZ}	Three-State Leakage Current	@ V_{DD} = max; High Z; V_{IN} = 0V or max		50		50	μA
I_{DD}	Supply Current	@ max Clock Rate; V_{IN} = 0 to 3V		110[3]		125	mA
I_{DD}	Supply Current Quiescent	All V_{IN} = 2.4V		35		40	mA

SWITCHING CHARACTERISTICS[4]

		ADSP-1010B J Grade 0 to +70°C		K Grade 0 to +70°C		S Grade[2] −55°C to +125°C		T Grade[2] −55°C to +125°C		
Parameter		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{MAC}	Multiply/Accumulate Time		55		45		65		55	ns
t_D	Output Delay		25		25		30		30	ns
t_{ENA}	Three-State Enable Delay		25		25		30		30	ns
t_{DIS}	Three-State Disable Delay		25		25		30		30	ns
t_{PW}	Clock Pulse Width	15		15		15		15		ns
t_S	Input Setup Time	15		15		20		20		ns
t_H	Input Hold Time	3		3		3		3		ns

NOTES

[1]All min and max specifications are over power supply and temperature range indicated.

[2]S and T grade parts are available processed and tested in accordance with MIL-STD-883, Class B. The processing and test methods used for S/883B and T/883B versions of the ADSP-1010B can be found in Analog Devices' Military Databook.

[3]Guaranteed but not tested.

[4]Input levels are GND and 3.0V. Rise times are 5ns. Input timing reference levels and output reference levels are 1.5V, except for t_{ENA} and t_{DIS} which are indicated in Figure 2.

Specifications subject to change without notice.

ORDERING INFORMATION

Part Number	Temperature Range	Package	Package Outline	Part Number	Temperature Range	Package	Package Outline
ADSP-1010BJP	0 to +70°C	68-Lead PLCC	P-68	ADSP-1010BTD	−55°C to +125°C	64-Pin Ceramic DIP	D-64A
ADSP-1010BKP	0 to +70°C	68-Lead PLCC	P-68	ADSP-1010BSD/883B	−55°C to +125°C	64-Pin Ceramic DIP	D-64A
ADSP-1010BJD	0 to +70°C	64-Pin Ceramic DIP	D-64A	ADSP-1010BTD/883B	−55°C to +125°C	64-Pin Ceramic DIP	D-64A
ADSP-1010BKD	0 to +70°C	64-Pin Ceramic DIP	D-64A	ADSP-1010BSG	−55°C to +125°C	68-Pin Grid Array	G-68A
ADSP-1010BJG	0 to +70°C	68-Pin Grid Array	G-68A	ADSP-1010BTG	−55°C to +125°C	68-Pin Grid Array	G-68A
ADSP-1010BKG	0 to +70°C	68-Pin Grid Array	G-68A	ADSP-1010BSG/883B	−55°C to +125°C	68-Pin Grid Array	G-68A
ADSP-1010BSD	−55°C to +125°C	64-Pin Ceramic DIP	D-64A	ADSP-1010BTG/883B	−55°C to +125°C	68-Pin Grid Array	G-68-A

Contact DSP Marketing in Norwood concerning the availability of other package types.

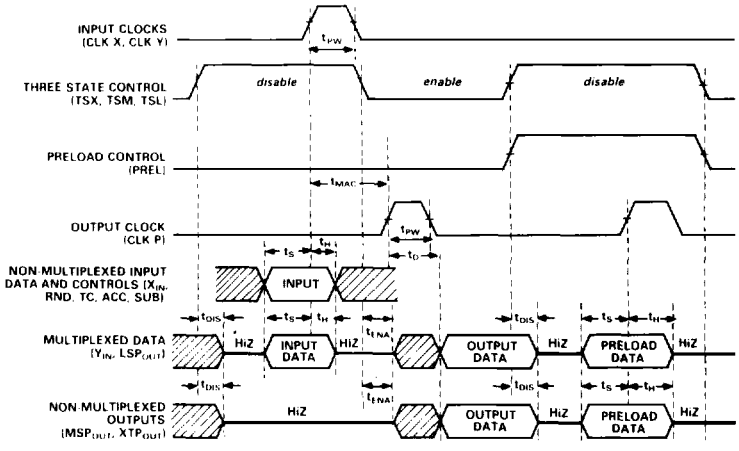


Figure 1. ADSP-1010B Timing Diagram

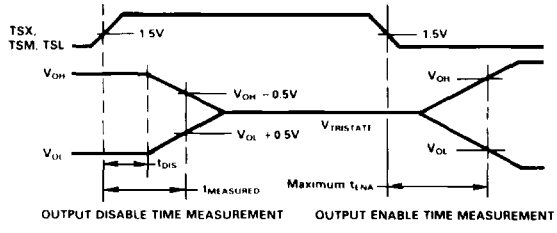


Figure 2. Three-State Disable and Enable

Output disable time, t_{DIS}, is measured from the time the output enable control signal reaches 1.5V to the time when all outputs have ceased driving. This is calculated by measuring the time, $t_{measured}$, from the same starting point to when the output voltages have changed by 0.5V toward +1.5V. From the tester capacitive loading, C_L, and the measured current i_L, the decay time, t_{DECAY}, can be approximated to first order by:

$$t_{DECAY} = \frac{C_L \cdot 0.5V}{i_L}$$

from which

$$t_{DIS} = t_{measured} - t_{DECAY}$$

is calculated. Disable times are longest at the highest specified temperature.

The maximum output enable time, maximum t_{ENA}, is also measured from output enable control signal at 1.5V to the time when all outputs have reached TTL input levels (V_{OH} or V_{OL}). This could also be considered as "data valid." Maximum enable times are longest at the highest specified temperature.

METHOD OF OPERATION

The X and Y input registers are positive-edge triggered D-type flip-flops. Input data is loaded to the X and Y registers with the rising edges of CLK X and CLK Y, respectively. The X and Y input data can be represented in either twos complement or unsigned magnitude formats. (Mixed-mode is not supported.)

TC, RND, ACC and SUB are registered input controls. Note that these four controls are latched by the rising edge of the logical OR of CLK X and CLK Y. Be sure that CLK X and CLK Y are both LO (logic 0) before attempting to clock in these controls.

When the registered twos complement control, TC, is HI (logic 1), the inputs are interpreted as twos complement numbers. (See Table I for the ADSP-1010B's data formats.) When TC is LO, the inputs are interpreted as unsigned magnitude numbers. In both cases, outputs will be in the same format as inputs. No shifting is performed in the ADSP-1010B, so all multiplications, including (twos complement) negative full scale multiplied by negative full scale, yield valid results.

When the registered RND control is HI, the MSP will be rounded by adding a binary 1 (with carry) to the most significant bit (MSB) of the LSP, consistently rounding toward positive infinity at midscale. Truncating the MSP (RND LO) introduces a large-sample statistical bias into the MSP of $-(2^{16}-1)/2$ times the LSB of the LSP, while rounding (RND HI) reduces the bias to +1/2 times the LSB of the LSP.

Registered ACC and SUB controls determine whether the product will be latched directly into the output registers or whether they will be updated with the previous contents of the output registers added to or subtracted from the product. If ACC is LO, the product will overwrite the previous contents of the output registers. Holding ACC low at the beginning of a summation avoids the need for a separate operation to clear the output registers. If ACC is HI and SUB is LO, the previous contents of the output registers will be added to the product and stored in the output registers. If ACC is HI and SUB is HI, the previous contents of the output registers will be subtracted from the product and stored in the output registers. (Table II displays these conditions in a truth table.)

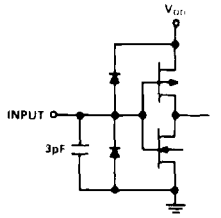


Figure 3. Equivalent Input Circuits

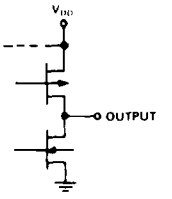


Figure 4. Equivalent Output Circuits

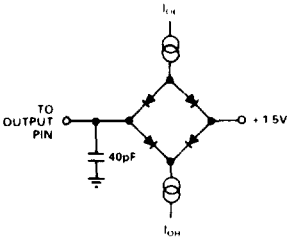


Figure 5. Normal Load for ac Measurements

The accumulation register is partitioned into three words: a 16-bit LSP, a 16-bit MSP and a 3-bit XTP. The 3-bit extension register makes possible summing at least eight large products without overflow. In twos complement mode, the MSB of the XTP will be the product sign bit. Sign bits, or zeros in the case of unsigned magnitude, are extended from the MSB of the product to the MSB of the XTP in the adder/subtracter. (Data preloaded to the accumulation registers will not be sign-extended until it is added to or subtracted from a product.)

The rising edge of CLK P latches the LSP, MSP and XTP into the accumulation registers. Each of these registers has its own three-state control. A HI on the asynchronous TSL, TSM or TSX line disables the corresponding LSP, MSP or XTP output driver to a high impedance state. Conversely, a LO on TSL, TSM or TSX enables the corresponding output driver, driving the output bus.

The asynchronous preload control, PREL, can be used to initialize the output registers. In conjunction with TSL, TSM and TSX, PREL can be used to preload either one, two or all three of the output registers simultaneously. If PREL is HI while either TSL, TSM or TSX is also HI, then the data at the output ports is loaded into the respective output registers on the rising edge of CLK P. (See Table III for a truth table of these conditions.)

X & Y INPUT DATA FORMATS							OUTPUT DATA FORMATS																
							XTP			MSP						LSP							
15	14	13	.....	2	1	0	34	33	32	31	30	29	.....	18	17	16	15	14	13	.....	2	1	0
INTEGER TWOS COMPLEMENT (TC = 1)																							
sign (-2^{15})	2^{14}	2^{13}	.....	2^2	2^1	2^0	-2^{34}	2^{33}	2^{32}	2^{31}	2^{30}	2^{29}	.....	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	.....	2^2	2^1	2^0
FRACTIONAL TWOS COMPLEMENT (TC = 1)																							
sign (-2^0)	2^{-1}	2^{-2}	.....	2^{-13}	2^{-14}	2^{-15}	-2^4	2^3	2^2	2^1	2^0	2^{-1}	.....	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	.....	2^{-28}	2^{-29}	2^{-30}
UNSIGNED MAGNITUDE (INTEGER) (TC = 0)																							
2^{15}	2^{14}	2^{13}	.....	2^2	2^1	2^0	2^{34}	2^{33}	2^{32}	2^{31}	2^{30}	2^{29}	.....	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	.....	2^2	2^1	2^0

Table I. Data Formats

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . −0.3V to 7V
Input Voltage . . . . . −0.3 to V_{DD}
Output Voltage . . . . . −0.3 to V_{DD}
Operating Temperature Range ($T_{AMBIENT}$) . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (10sec) . . . . . +300°C

ESD SENSITIVITY

THE ADSP-1010B features proprietary input protection circuitry to dissipate high energy discharges (Human Body Model). Per Method 3015 of MIL-STD-883, the ADSP-1010B has been classified as a Class 1 device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual*.

ACC	SUB	Function
1	1	$Accumulator_t = X_t \bullet Y_t - Accumulator_{t-1}$
1	0	$Accumulator_t = X_t \bullet Y_t + Accumulator_{t-1}$
0	X	$Accumulator_t = X_t \bullet Y_t$

Table II. Function Truth Table

PREL	TSX	TSM	TSL	XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Z
0	0	1	0	Q	Z	Q
0	0	1	1	Q	Z	Z
0	1	0	0	Z	Q	Q
0	1	0	1	Z	Q	Z
0	1	1	0	Z	Z	Q
0	1	1	1	Z	Z	Z
1	0	0	0	Z	Z	Z
1	0	0	1	Z	Z	Preload
1	0	1	0	Z	Preload	Z
1	0	1	1	Z	Preload	Preload
1	1	0	0	Preload	Z	Z
1	1	0	1	Preload	Z	Preload
1	1	1	0	Preload	Preload	Z
1	1	1	1	Preload	Preload	Preload

NOTE:
Z = Output buffers at high impedance (output disabled)
Q = Output buffers at low impedance. Contents of output register will be transferred to output pins.
Preload = Output buffers at high impedance.
Preload data supplied externally at output pins will be loaded into the output register at the rising edge of CLK P.

Table III. Preload Truth Table

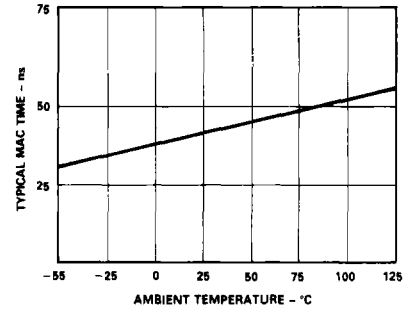


Figure 6. Approx. Multiply Time vs. Temperature

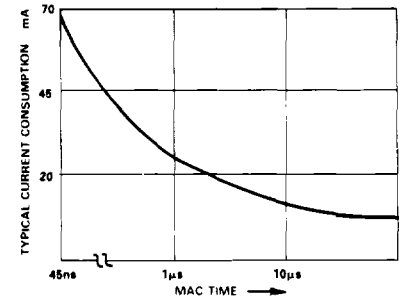


Figure 7. Typical I_{DD} vs. Frequency of Operation

5

PIN CONFIGURATION

PIN NO.	PACKAGE DIP	PIN-GRID	PLCC	PIN NO.	PACKAGE DIP	PIN-GRID	PLCC
1	X6	Y1, P1	X6	35	P26	P32	P25
2	X5	Y2, P2	X7	36	P27	P33	P24
3	X4	Y3, P3	X8	37	P28	P34	P23
4	X3	Y4, P4	X9	38	P29	CLK P	P22
5	X2	Y5, P5	X10	39	P30	TSM	P21
6	X1	Y6, P6	X11	40	P31	PREL	P20
7	X0	Y7, P7	X12	41	P32	TSX	P19
8	Y0, P0	GND	X13	42	P33	TC	P18
9	Y1, P1	Y8, P8	X14	43	P34	V_{DD}	P17
10	Y2, P2	Y9, P9	X15	44	CLK P	CLK Y	P16
11	Y3, P3	Y10, P10	TSL	45	TSM	CLK X	Y15, P15
12	Y4, P4	Y11, P11	RND	46	PREL	ACC	Y14, P14
13	Y5, P5	Y12, P12	SUB	47	TSX	SUB	Y13, P13
14	Y6, P6	Y13, P13	ACC	48	TC	RND	Y12, P12
15	Y7, P7	Y14, P14	CLK X	49	V_{DD}	TSL	Y11, P11
16	GND	Y15, P15	CLK Y	50	CLK Y	X15	Y10, P10
17	Y8, P8	N/C	V_{DD}	51	CLK X	N/C	Y9, P9
18	Y9, P9	P16	V_{DD}	52	ACC	X14	Y8, P8
19	Y10, P10	P17	V_{DD}	53	SUB	X13	GND
20	Y11, P11	P18	V_{DD}	54	RND	X12	GND
21	Y12, P12	P19	TC	55	TSL	X11	Y7, P7
22	Y13, P13	P20	TSX	56	X15	X10	Y6, P6
23	Y14, P14	P21	PREL	57	X14	X9	Y5, P5
24	Y15, P15	P22	TSM	58	X13	X8	Y4, P4
25	P16	P23	CLK P	59	X12	X7	Y3, P3
26	P17	P24	P34	60	X11	X6	Y2, P2
27	P18	P25	P33	61	X10	X5	Y1, P1
28	P19	P26	P32	62	X9	X4	Y0, P0
29	P20	P27	P31	63	X8	X3	X0
30	P21	P28	P30	64	X7	X2	X1
31	P22	P29	P29	65		X1	X2
32	P23	P30	P28	66		X0	X3
33	P24	P31	P27	67		Y0, P0	X4
34	P25	N/C	P28	68		N/C	X5