ALPHA SEMICONDUCTOR
Excellence in Analog Power Products

AS OP-05

Instrumentation Operational Amplifier

FEATURES

- High gain ..... 300,000 Min.
- Low drift vs. temperature ..... 0.5 μV/°C
- High CMMR ..... 114 dB Min.
- Low bias current ..... ±2nA Max.
- Low noise ..... 0.5μV Max., 0.1 < f < 10Hz
- High R_{in} ..... 30 MΩMin
- Fits in 725, 108A, 741 sockets

APPLICATIONS

- Sample & Hold Amplifiers
- Integrators
- Medical Instrumentation
- Instrumentation Amplifiers & Buffers
- Strain Gauge & Thermocouple

PRODUCT DESCRIPTION

The ALPHA Semiconductor AS OP-05 is an internally compensated Operational Amplifier. The OP-05 is well defined for instrumentation and low signal level applications where precision and stability over time and temperature are needed. The AS OP-05 offers a low input offset voltage and bias current including very high levels of gain, input impedance, CMRR, and PSRR.

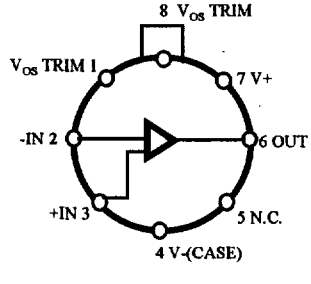
The AS OP-05 is also an excellent choice for applications which are looking for low noise, low power, and low cost. The AS OP-05 is available in TO-99 and 8-pin plastic SOIC packages. The operating temperatures are 0°C to 70°C and -55°C to +125°C.

ORDERING INFORMATION

TA=25°C V_{os} Max (mV)	TO-99 8-PIN	PLASTIC DIP 8-PIN	PLASTIC SOIC 8-PIN	OPER. TEMP. RANGE
0.15	OP-05AJ			MIL
0.5	OP-05J			MIL
0.5	OP-05EJ	OP-05EP	OP-05ES	COM.
1.3	OP-05CJ	OP-05CP	OP-05CS	COM.

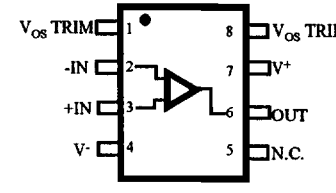
PIN CONFIGURATION

TO-99



Bottom View

8-Pin Surface Mount
8-Pin MINI-DIP



Top View

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±22V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
J Packages ..... -65 to +150°C
P Packages ..... -65 to +125°C
Operating Temperature Range
OP-05A, OP-05 ..... -55 to +125°C
OP-05E, OP-05C ..... 0 to +70°C
Dice Junction Temperature(Tj) ..... -65 to +150°C
Lead Temperature (Soldering, 60 Sec.) ..... 300°C

NOTES:
1. See table for maximum ambient temperature rating and derating factor.
2. Absolute maximum ratings apply to both DICE and packaged parts unless otherwise noted.
3. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99(J)	80°C	7.1 mW/°C
9-Pin Plastic DIP (P)	36°C	5.6 mW/°C

ELECTRICAL CHARACTERISTICS at V_S=±15V, Ta=25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05A			OP-05			UNITS
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	V_{os}			0.07	0.15		0.2	0.5	mV
Long Term Input offset Voltage Stability	V_{OS}/Time	(Note 1)		0.2	1.0		0.2	1.0	$\mu V/M_o$
Input Offset Current	I_{os}			0.7	2.0		1.0	2.8	nA
Input Bias Current	I_B			±0.7	±2.0		±1.0	±3.0	nA
Input Noise Voltage (Note 2)	e_{nrm}	0.1Hz to 10Hz		0.35	0.6		0.35	0.6	μV_{p-p}
Input Noise Voltage Density (Note 2)	e_n	f_o=10Hz		10.3	18.0		10.3	18.0	nV/√Hz
Input Noise Voltage Density (Note 2)	e_n	f_o=100Hz		10.0	13.0		10.0	13.0	nV/√Hz
Input Noise Voltage Density (Note 2)	e_n	f_o=1000Hz		9.6	11.0		9.6	11.0	nV/√Hz
Input Noise Current (Note 2)	i_{np-p}	0.1 Hz to 10Hz		14	30		14	30	pA_{p-p}
Input Noise Current Density (Note 2)	i_n	f_o=10Hz		0.32	0.80		0.32	0.80	nV/√Hz
Input Noise Current Density (Note 2)	i_n	f_o=100 Hz		0.14	0.23		0.14	0.23	nV/√Hz
Input Noise Current Density (Note 2)	i_n	f_o=1000Hz		0.12	0.17		0.12	0.17	nV/√Hz
Input Resistance-Differential-Mode	R_{in}	(Note 3)	30	80		20	60		MΩ
Input Resistance-Common Mode	R_{inCM}			200			200		GΩ
Input Voltage Range	IVR		±13.5	±14.0		±13.5	±14.0		V
Common-Mode Rejection Ratio	CMRR	V_{CM}=±13.5	114	126		114	126		dB
Power Supply Rejection Ratio	PSRR	$V_{S=}$±3V to ±18		4	10		4	10	μV/V
Large Signal Voltage Gain	AV_O	R_l>2kΩ V_o=±10V	300	500		200	500		V/mV
Large Signal Voltage Gain	AV_O	R_l>500Ω V_o=±0.5 V_e=±3V (Note 3)	150	500		150	500		V/mV
Output Voltage Swing	V_o	R_l >10kΩ	±12.5	±13.0		±12.5	±13.0		V
Output Voltage Swing	V_o	R_l>2kΩ	±12.0	±12.8		±12.0	±12.8		V
Output Voltage Swing	V_o	R_l>1kΩ	±10.5	±12.0		±10.5	±12.0		V
Slew Rate (Note 2)	SR	R_l >2kΩ	0.1	0.3		0.1	0.3		V/μs
Closed-Loop Bandwidth (Note 2)	BW	A_{vcl}=+1.0	0.4	0.6		0.4	0.6		MHz
Open Loop Output Resistance	R_o	V_o=0, Io=0		60			60		Ω
Power Consumption	P_d	No Load		90	120		90	120	mW
Power Consumption	P_d	V_e=±3V, No load		4	6		4	6	mW
Offset Adjustment Range		R_p=20kΩ		4			4		mV

ELECTRICAL CHARACTERISTICS at V_s=±15V, Ta=25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05E			OP-05C			UNITS
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	V_{os}			0.2	0.5		0.3	1.3	mV
Long Term Input offset Voltage Stability	V_{OS}/Time	(Note 1)		0.3	1.5		0.4	2.0	µV/M$_o$
Input Offset Current	I_{os}			1.2	3.8		1.8	6.0	nA
Input Bias Current	I_B			±1.2	±4.0		±1.8	±7.0	nA
Input Noise Voltage (Note 2)	e_{npp}	0.1Hz to 10Hz		0.35	0.6		0.38	0.65	μV_{p-p}
Input Noise Voltage Density (Note 2)	e_n	f_o=10Hz		10.3	18.0		10.5	20.0	nV/√Hz
Input Noise Voltage Density (Note 2)	e_n	f_o=100Hz		10.0	13.0		10.2	13.5	nV/√Hz
Input Noise Voltage Density (Note 2)	e_n	f_o=1000Hz		9.6	11.0		9.8	11.5	nV/√Hz
Input Noise Current (Note 2)	i_{npp}	0.1 Hz to 10Hz		14	30		15	35	pA_{p-p}
Input Noise Current Density (Note 2)	i_n	f_o=10Hz		0.32	0.80		0.35	0.90	nV/√Hz
Input Noise Current Density (Note 2)	i_n	f_o=100 Hz		0.14	0.23		0.15	0.27	nV/√Hz
Input Noise Current Density (Note 2)	i_n	f_o=1000Hz		0.12	0.17		0.13	0.18	nV/√Hz
Input Resistance-Differential-Mode	R_{in}	(Note 3)	15	50		8	33		MΩ
Input Resistance-Common Mode	R_{inCM}			160			120		GΩ
Input Voltage Range	IVR		±13.5	±14.0		±13.0	±14.0		V
Common-Mode Rejection Ratio	CMRR	V_{CM}=±13.5	110	123		100	32		dB
Power Supply Rejection Ratio	PSRR	V_S=±3V to ±18		5	20		7	120	µV/V
Large Signal Voltage Gain	AV_O	R_L>2kΩ V_o=±10V	200	500		120	400		V/mV
Large Signal Voltage Gain	AV_O	R_L>500Ω V_o=±0.5 V_e=±3V (Note 3)	150	500		100	400		V/mV
Output Voltage Swing	V_o	R_L >10kΩ	±12.0	±13.0		±12.0	±13.0		V
Output Voltage Swing	V_o	R_L>2kΩ	±12.0	±12,8		±11.5	±12.8		V
Output Voltage Swing	V_o	R_L>1kΩ	±10.5	±12.0			±12.0		V
Slew Rate (Note 2)	SR	R_L >2kΩ	0.1	0.3		0.1	0.3		V/µs
Closed-Loop Bandwidth (Note 2)	BW	A_{VCL}=+1.0	0.4	0.6		0.4	0.6		MHz
Open Loop Output Resistance	R_o	V_o=0, Io=0		60			60		Ω
Power Consumption	P_d	No Load		90	120		95	150	mW
Power Consumption	P_d	V_e=±3V, No load		4	6		4	8	mW
Offset Adjustment Range		R_p=20kΩ		4			4		mV

ELECTRICAL CHARACTERISTICS at V_s=±15V, -55°C≤Ta≤+125°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05A Min.	OP-05A Typ.	OP-05A Max.	OP-05 Min.	OP-05 Typ.	OP-05 Max.	UNITS
Input Offset Voltage	V_{os}			0.10	0.24		0.3	0.7	µV
Average Input Offset Voltage Drift Without External Trim	TCV_{os}	(Note 2)		0.3	0.9		0.7	2.0	µV/°C
With External Trim	TCV_{os}	R_p=20kΩ (Note 3)		0.2	0.5		0.3	1.0	µV/°C
Input Offset Current	I_{os}			1.0	4.0		1.8	5.6	nA
Average Input Offset Current Drift	TCI_{os}	Note 2		5	25		8	50	pA/°C
Input Bias Current	I_B			±1	±4		±2	±6	nA
Average Input Bias Current Drift	TCI_B	Note 2		8	25		13	50	pA/°C
Input Voltage Range	IVR		±13.0	±13.5		±13.0	±13.5		V
Common Mode Rejection Ratio	CMRR	V_{CM} ±13.0 V	110	123		110	123		dB
Power Supply Rejection Ratio	PSRR	V_s=±3V to ±18V		5	20		5	20	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L>2kΩ, V_O= ±10V	200	400		150	400		V/mV
Output Voltage Swing	V_O	R_L>2kΩ	±12.0	±12.6		±12.0	±12.6		V

ELECTRICAL CHARACTERISTICS at V_s=±15V, 0°C≤Ta≤+70°C, unless otherwise noted.

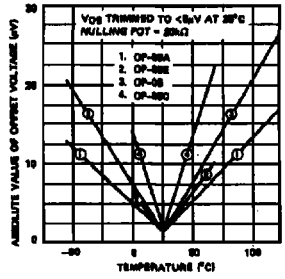
PARAMETER	SYMBOL	CONDITIONS	OP-05E Min.	OP-05E Typ.	OP-05E Max.	OP-05C Min.	OP-05C Typ.	OP-05C Max.	UNITS
Input Offset Voltage	V_{os}			0.25	0.6		0.35	1.6	µV
Average Input Offset Voltage Ddift Without External Trim	TCV_{os}	(Note 2)		0.7	2.0		1.3	4.5	µV/°C
With External Trim	TCV_{os}	R_p=20kΩ (Note 3)		0.2	0.6		0.4	1.5	µV/°C
Input Offset Current	I_{os}			1.4	5.3		2.0	8.0	nA
Average Input Offset Current Drift	TCI_{os}	Note 2		8	35		12	50	pA/°C
Input Bias Current	I_B			±1.5	±5.5		±2.2	±9.0	nA
Average Input Bias Current Drift	TCI_B	Note 2		13	35		18	50	pA/°C
Input Voltage Range	IVR		±13.0	±13.5		±13.0	±13.5		V
Common Mode Rejection Ratio	CMRR	V_{CM} ±13.0 V	107	123		97	120		dB
Power Supply Rejection Ratio	PSRR	V_s=±3V to ±18V		7	32		10	51	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L>2kΩ, V_O= ±10V	180	450		100	400		V/mV
Output Voltage Swing	V_O	R_L>2kΩ	±12.0	±12.6		±11.0	±12.6		V

Notes:

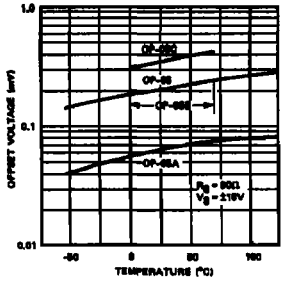
1. Long-term input offset voltage stability refers to the averaged trend line of V_{os} vs. time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in Vos during the first 30 operating days are typically 2.5µV.
2. Sample tested.
3. Guaranteed by design.

TYPICAL CHARACTERISTICS

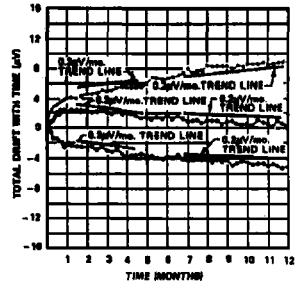
TRIMMED OFFSET VOLTAGE vs TEMPERATURE



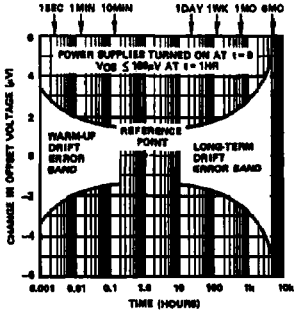
UNTRIMMED OFFSET VOLTAGE vs TEMPERATURE



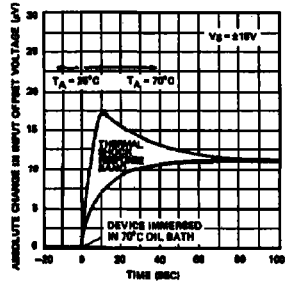
TYPICAL OFFSET VOLTAGE STABILITY vs TIME



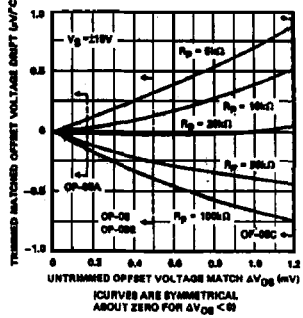
OFFSET VOLTAGE DRIFT WITH TIME



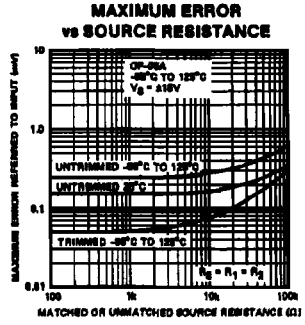
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



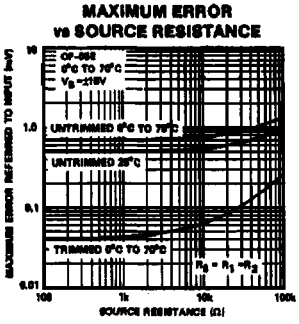
TRIMMED OFFSET VOLTAGE DRIFT



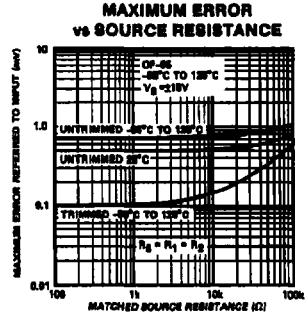
MAXIMUM ERROR vs SOURCE RESISTANCE



MAXIMUM ERROR vs SOURCE RESISTANCE

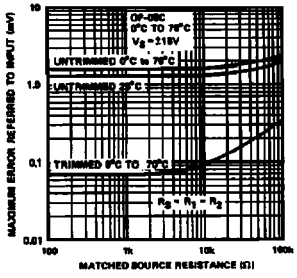


MAXIMUM ERROR vs SOURCE RESISTANCE

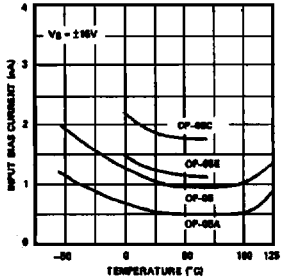


TYPICAL CHARACTERISTICS (continued)

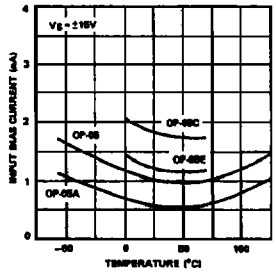
MAXIMUM ERROR vs SOURCE RESISTANCE



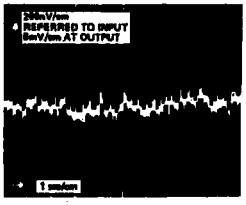
INPUT BIAS CURRENT vs TEMPERATURE



INPUT OFFSET CURRENT vs TEMPERATURE

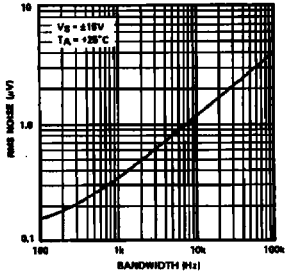


OP-05 LOW FREQUENCY NOISE

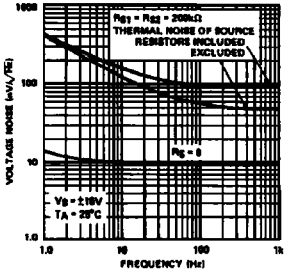


(SEE NOISE TEST CIRCUIT)

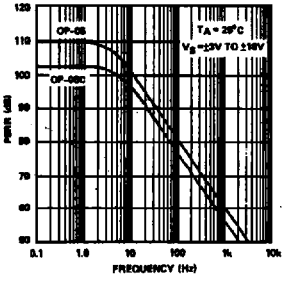
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



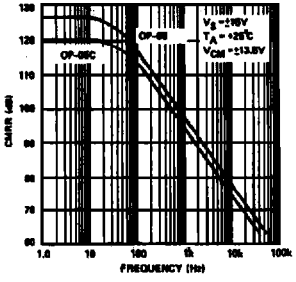
VOLTAGE NOISE DENSITY vs FREQUENCY



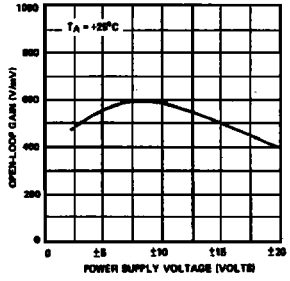
PSRR vs FREQUENCY



CMRR vs FREQUENCY

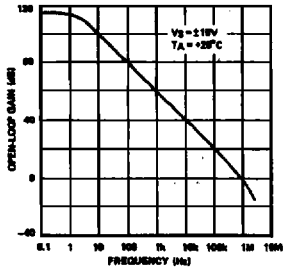


OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE

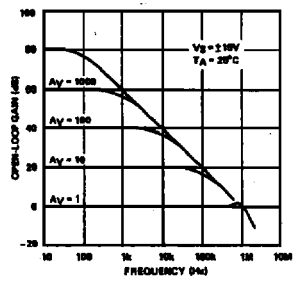


TYPICAL CHARACTERISTICS (continued)

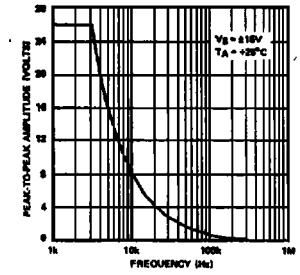
OPEN-LOOP GAIN vs FREQUENCY



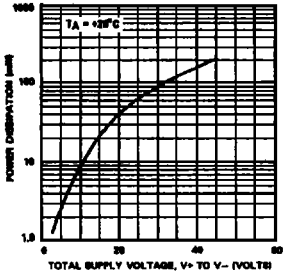
CLOSED-LOOP GAIN vs FREQUENCY



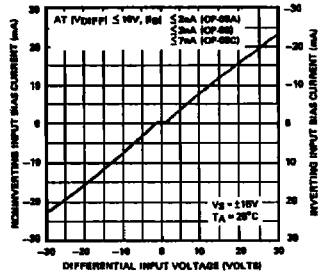
MAXIMUM OUTPUT SWING vs FREQUENCY



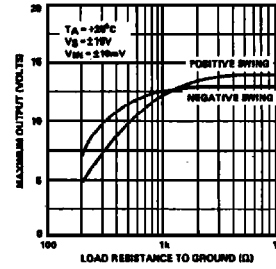
POWER CONSUMPTION vs POWER SUPPLY



INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE

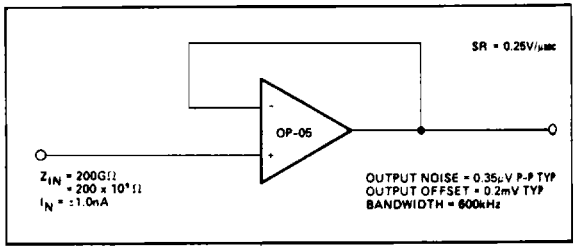


APPLICATION HINTS

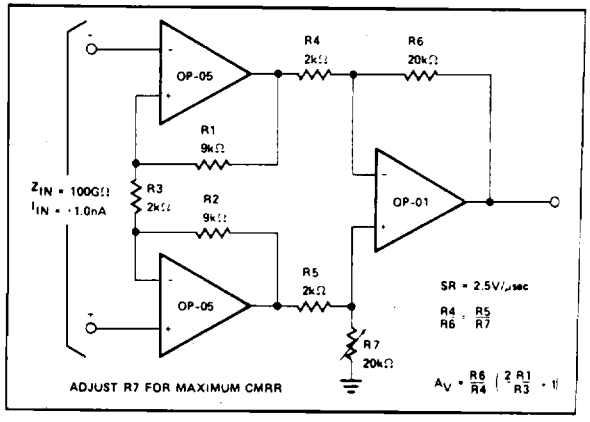
OP-05 series devices can be fitted directly to 725 and 108/108A Series sockets with or without removal of external compensation components. Additionally, the OP-05 may be fitted to unnulled 741 series. However, if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP-05 operation. The OP-05 provides stable operation with load capacitance of up to 500pF and ±10V swings; larger capacitances should be decoupled with a 50Ω resistor.

Offset stability can be degraded by stray thermoelectric voltages arising from dissimilar metals at the contacts to the input terminals. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

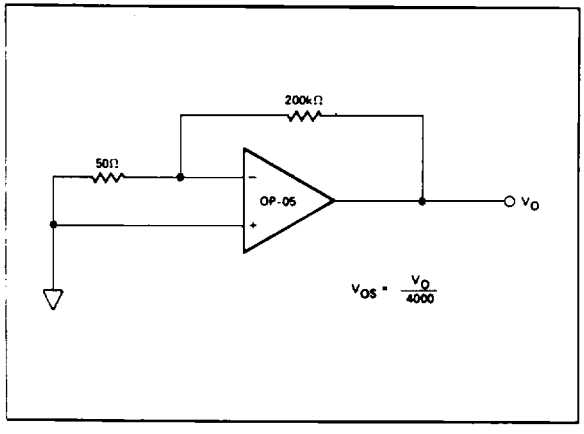
STABLE, HIGH-IMPEDANCE BUFFER



HIGH IMPEDANCE, HIGH COMMON-MODE REJECTION INSTRUMENTATION AMPLIFIER



TYPICAL OFFSET VOLTAGE TEST CIRCUIT



TYPICAL LOW-FREQUENCY NOISE TEST CIRCUIT*