STATIC RAM 64K × 32 2M BIT

Type name	Max. Access time (ns)	Load memory	Outward dimensions W × H × D (mm)	Data sheet page
MH6432NZ-15	15	M5M5258BJ × 8	92.71 × 17.6 × 8.9	3/8
MH6432NZ-20	20			
MH6432NZ-25	25			
MH6432NZ-35	35			
MH6432NZ-20L	20			
MH6432NZ-25L	25			
MH6432NZ-35L	35			
COMMON DATA				4/8

MH6432NZ-15,-20,-25,-35, -20L,-25L,-35L

2097152-BIT(65536-WORD BY 32-BIT)CMOS STATIC RAM

DESCRIPTION

The MH6432NZ is a 2097152 bits CMOS static RAM module organized as 65536 words by 32-bits. It consists of eight industry standard 64K × 4 static RAMs.

The stand-by current is low enough for a battery back-up application. It is mounted a soj package on a 64-pin Zig-Zag in line package.

FEATURES

Type name	Access time (max)	Power dissipation	
		Active (typ)	Stand by (typ)
MH6432NZ-15	15ns	2400mW	40mW
MH6432NZ-20	20ns		
MH6432NZ-25	25ns		
MH6432NZ-35	35ns		
MH6432NZ-20L	20ns		400μW
MH6432NZ-25L	25ns		
MH6432NZ-35L	35ns		

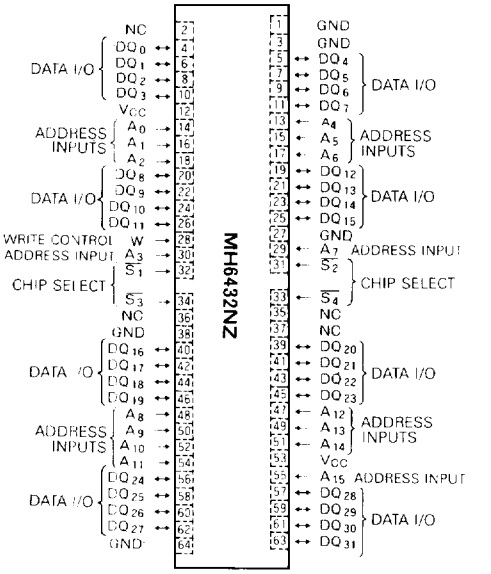
- Single +5V Power Supply
- No Clocks, No Refresh
- Directly TTL Compatible: All Inputs and Outputs
- Simple Memory Expantion by $\overline{S}$
- Common Data I/O
- Power down by $\overline{S}$
- Solder dipping lead

APPLICATION

High-speed memory systems

PIN CONFIGRATION (TOP VIEW)

(Both side)



Outline 64N5

NC: NO CONNECTION

2097152-BIT
MH6432NZ (65536-WORD BY 32-BIT)CMOS STATIC RAM

FUNCTION

A write operation is executed during the $\overline{S}$ low and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the DQ terminal is maintained in the high impedance state.

In a read operation, after setting $\overline{W}$ to high, and $\overline{S}$ to low if the address signals are stable, the data is available at the DQ terminal.

When $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other devices.

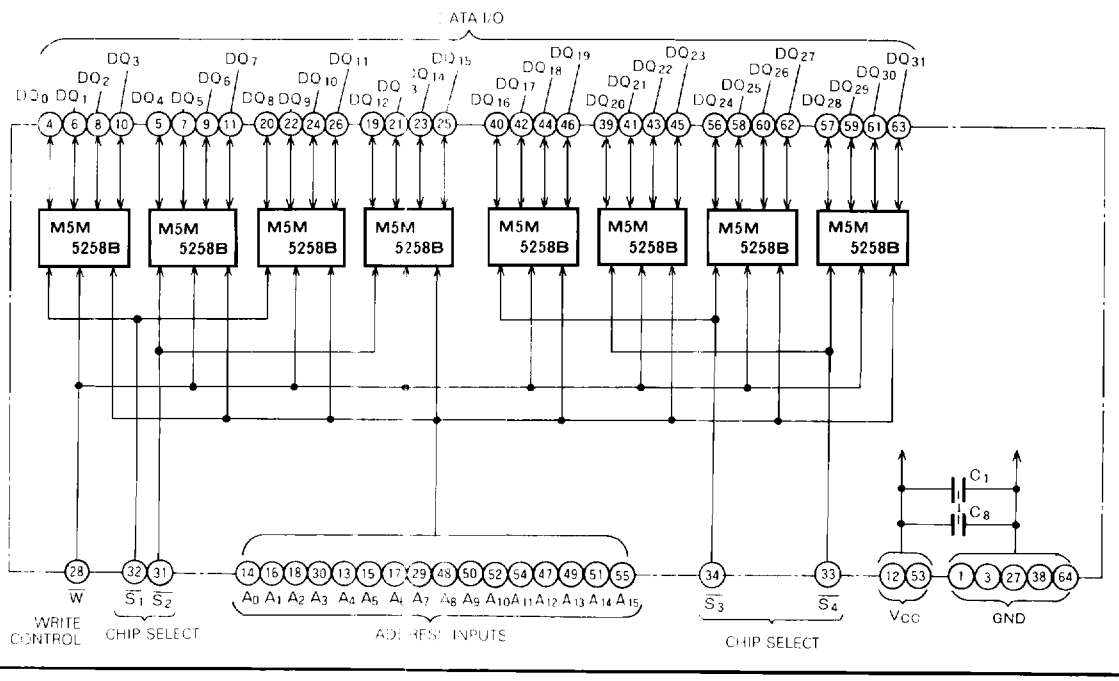
Single $\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

MODE SELECTION

$\overline{S}$	$\overline{W}$	Mode	Data I/O	I_{CC}
H	X	Non selection	High-impedance	Stand-by
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

H : V_{IH} L : V_{IL} X : V_{IL} or V_{IH}

BLOCK DIAGRAM



2097152-BIT
MH6432NZ (65536-WORD BY 32-BIT)CMOS STATIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−3.5*~7	V
V_I	Input voltage		−3.5*~7	V
V_O	Output voltage		−3.5*~7	V
Pd	Maximum power dissipation		8	W
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		−40~125	°C

* : Pulse width≦20ns, In case of DC: −0.5V

DC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage			2.4		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			−0.5*		0.6	V
V_{OH}	High-level output voltage	I_{OH}=−4mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL}=8mA				0.4	V
I_I	Input current	V_I=0~V_{CC}				16	μA
I_{OZ}	Off-state output current	$V_I(\overline{S})=V_{IH}$, V_O=0~V_{CC}				10	μA
I_{CC1}	Supply current from V_{CC}	$V_I(\overline{S})=V_{IL}$, Output open	AC (15ns cycle)			1040	mA
			AC (20, 25ns cycle)			960	
			DC		560	680	
I_{CC2}	Stand-by current	$V_I(\overline{S})=V_{IH}$	AC (15ns cycle)			400	mA
			AC (20, 25ns cycle)			320	
			Other $V_I \geqq V_{IH}$ or $\leqq V_{IL}$			240	
I_{CC3}	Stand-by current	$V_I(\overline{S})=V_{CC}-0.2V$, Other $V_I \leqq 0.2V$ or $V_I \geqq V_{CC}-0.2V$	-15, -20, -25, -35		8	80	mA
			-20L, -25L, -35L		80	800	μA

Note 1: Current flow into an IC is positive, out is negative
* −3.0V in case of AC (Pulse width ≦ 20ns)

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			60	pF
C_O	Output capacitance	V_O=GND, V_O=25mVrms, f=1MHz			20	pF

2097152-BIT
MH6432NZ (65536-WORD BY 32-BIT)CMOS STATIC RAM

AC ELECTRICAL CHARACTERISTICS (T_a=0~70℃, V_{CC}=5V ± 10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ..... V_{IH}=3V, V_{IL}=0V
Input rise and fall time 3ns
Input timing reference level
..... V_{IH}=2.4V, V_{IL}=0.6V
Output timing reference level
..... V_{OH}=2.0V, V_{OL}=0.8V
Output loads ..... Fig. 1, Fig. 2

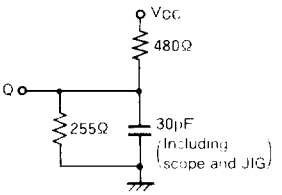


Fig. 1 Output load

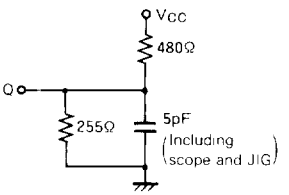


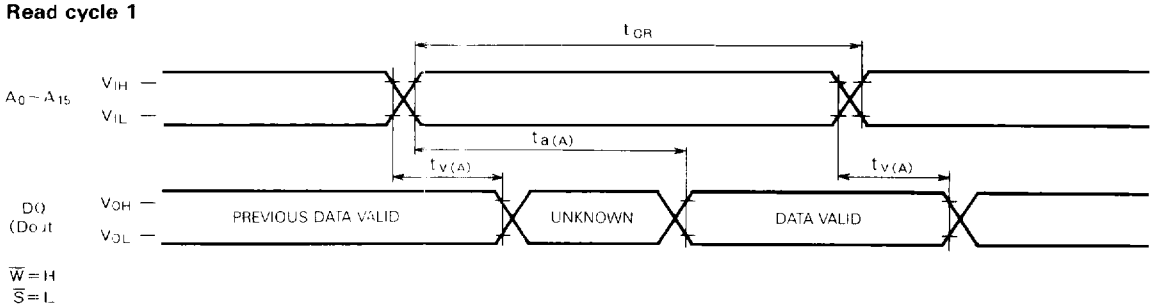
Fig. 2 Output load for ten, tdis

(2) READ CYCLE

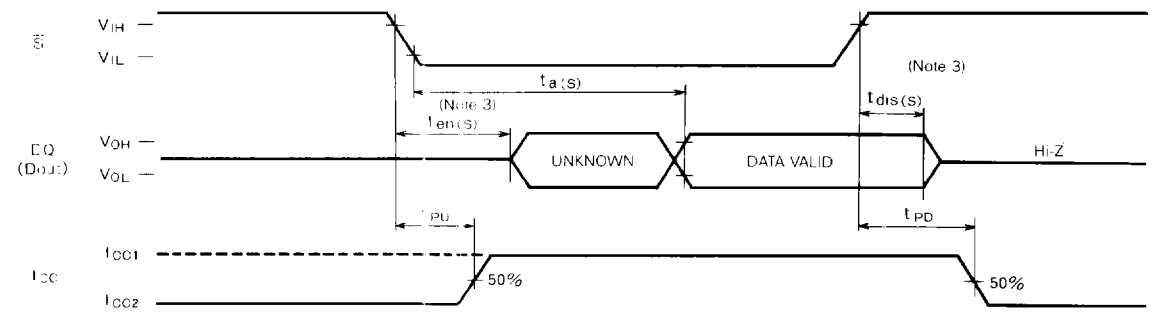
Symbol	Parameter	Limits												Unit
		MH6432NZ-15			MH6432NZ-20, -20L			MH6432NZ-25, -25L			MH6432NZ-35, -35L			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	15			20			25			35			ns
$t_{a(A)}$	Address access time			15			20			25			35	ns
$t_{a(S)}$	Chip select access time			15			20			25			35	ns
$t_{v(A)}$	Data valid time after address	3			3			5			5			ns
$t_{en(S)}$	Chip selection to output active	3			3			5			5			ns
$t_{dis(S)}$	Output disable time from CS	0		7	0		8	0		10	0		10	ns
t_{PU}	Power-up time after chip selection	0			0			0			0			ns
t_{PD}	Power down time after chip deselection			15			20			25			35	ns

(3) TIMING DIAGRAMS FOR READ CYCLE

Read cycle 1



Read cycle 2(Note 2)



Note 2. Address valid prior to or coincident with $\overline{S}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.

MITSUBISHI ELECTRIC

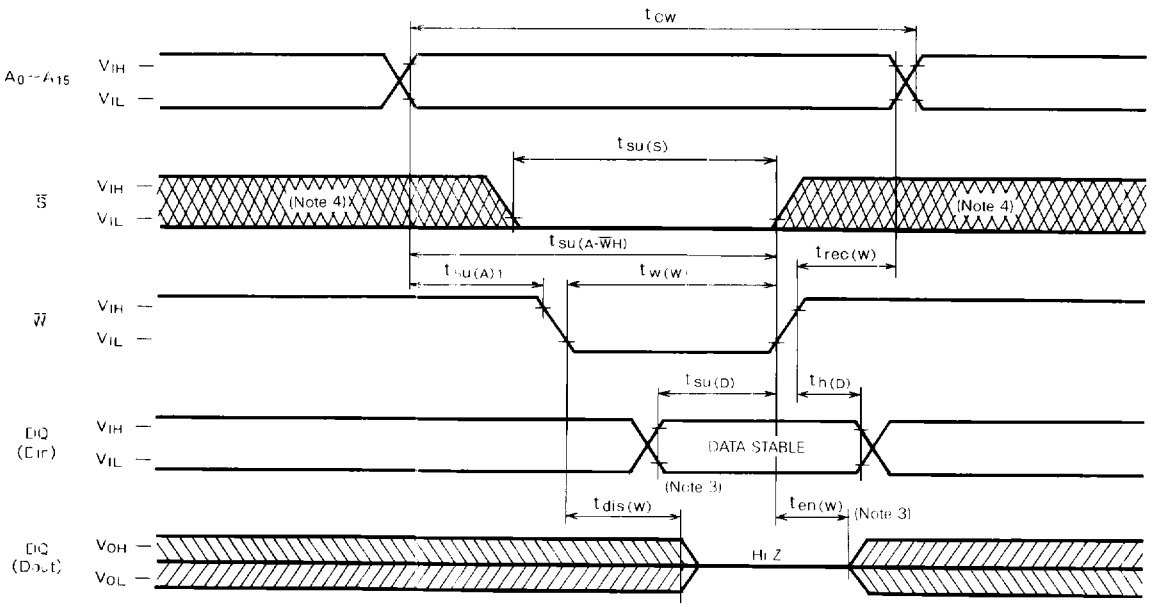
2097152-BIT
MH6432NZ (65536-WORD BY 32-BIT)CMOS STATIC RAM

(4) WRITE CYCLE

Symbol	Parameter	Limits												Unit
		MH6432NZ-15			MH6432NZ-20, -20L			MH6432NZ-25, -25L			MH6432NZ-35, -35L			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	15			20			25			35			ns
$t_{su(S)}$	Chip select setup time	12			15			20			30			ns
$t_{su(A)1}$	Address setup time (W)	0			0			0			0			ns
$t_{su(A)2}$	Address setup time (S)	0			0			0			0			ns
$t_{w(W)}$	Write pulse width	12			15			20			25			ns
$t_{rec(W)}$	Write recovery time	0			0			0			0			ns
$t_{su(D)}$	Data setup time	7			8			10			15			ns
$t_{h(D)}$	Data hold time	0			0			0			0			ns
$t_{dis(W)}$	Output disable time from W	0		7	0		8	0		10	0		10	ns
$t_{en(W)}$	Output enable time from W	0			0			0			0			ns
$t_{su(A-\overline{W}H)}$	Address to $\overline{W}$ high	12			15			20			30			ns

(5) TIMING DIAGRAMS FOR WRITE CYCLE

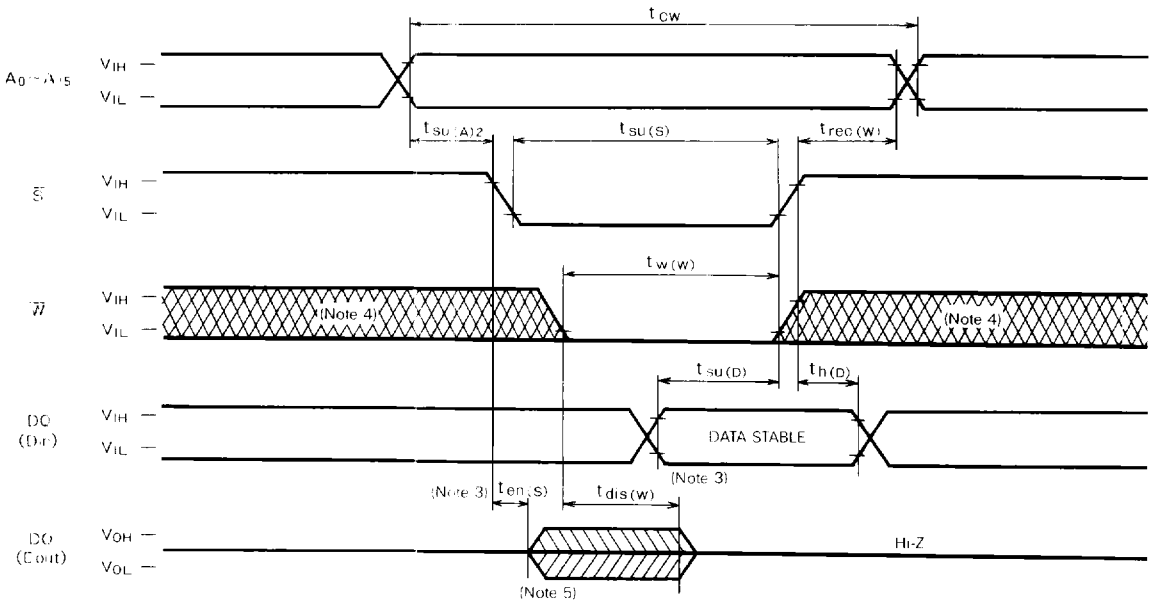
Write cycle 1 ($\overline{W}$ control mode)



MITSUBISHI ELECTRIC

2097152-BIT
MH6432NZ (65536-WORD BY 32-BIT)CMOS STATIC RAM

Write cycle 2 ($\overline{S}$ control mode)



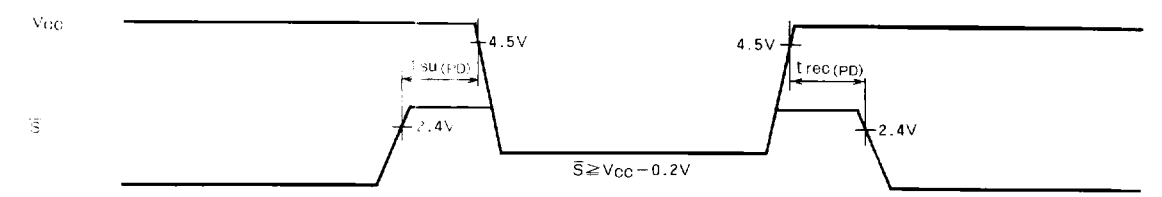
Note 4. Hatching indicates the state is don't care.
5. When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.

POWER DOWN CHARACTERISTICS (Ta=0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S})}$	Chip select input voltage	$V_{I(\overline{S})} \geq V_{CC}-0.2V$		$V_{CC}-0.2$			V
$t_{su(PD)}$	Power down setup time	$V_I \geq V_{CC}-0.2V$ or $0V \leq V_I \leq 0.2V$		0			ns
$t_{rec(PD)}$	Power down recovery time		-20L	20			ns
			-25L	25			
			-35L	35			
$I_{CC(PD)}$	Power down supply current	$V_{CC}=3.0V$				400	μA
		$V_{CC}=5.5V$				800	

Note 6. This is only MH6432NZ-20L, -25L, -35L.

TIMING WAVEFORM FOR POWER DOWN



MITSUBISHI ELECTRIC