

1M x 4 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 1,048,576 x 4 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage (+5.0V or +3.3V), access time(-5, -6, -7 or -8), power consumption (Normal or Low power), and package type (SOJ, DIP, ZIP or TSOP-II) are optional features of this family. All of this family have CAS-before-RAS refresh, RAS-only refresh and Hidden refresh capabilities. Furthermore, self-refresh operation is available in 3.3V Low power version.

This 1Mx4 Fast Page Mode DRAM Family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memory for main frames and mini computers, personal computer and high performance microprocessor systems.

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FEATURES

• Part Identification

- KM44C1000C/CL(5V)
- KM44V1000C/CL(3.3V)

• Active Power Dissipation

Unit : mW

Speed	3.3V	5V
-5	-	470
-6	220	415
-7	200	360
-8	180	-

• Refresh cycles

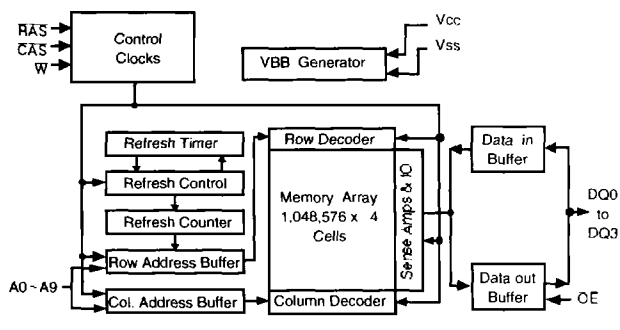
	V _{cc}	Refresh cycle	Refresh time	
			Normal	L
C1000C	5V	1K	16ms	128ms
V1000C	3.3V			

• Performance range:

Speed	t _{RAC}	t _{CAC}	t _{RC}	t _{PC}	Remark
-5	50ns	13ns	90ns	35ns	5V
-6	60ns	15ns	110ns	40ns	5V/3.3V
-7	70ns	20ns	130ns	45ns	5V/3.3V
-8	80ns	20ns	150ns	50ns	3.3V

- Fast Page Mode operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- Self-refresh capability (3.3V, L-ver only)
- Fast parallel test mode capability
- TTL(5V)/LVTTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V $\pm$ 10% power supply(5V product)
- Single +3.3V $\pm$ 0.3V power supply(3.3V product)

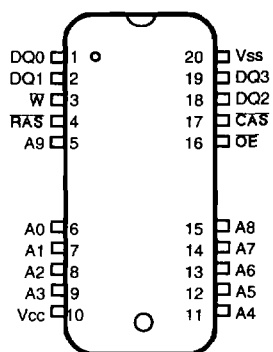
FUNCTIONAL BLOCK DIAGRAM



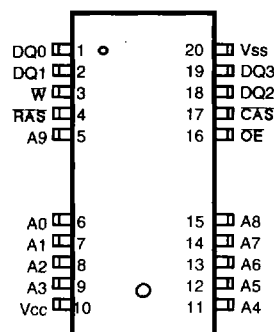
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PIN CONFIGURATION (Top Views)

• KM44C/V1000CJ



• KM44C/V1000CT



Pin Name	Pin Function
A0 - A9	Address Inputs
DQ0 -3	Data In/Out
Vss	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe
W	Read/Write Input
OE	Data Outputs Enable
Vcc	Power(+5.0V)
	Power(+3.3V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage temperature	T _{stg}	-55 to +150	-55 to +150	°C
Power dissipation	P _D	600	600	mW
Short circuit output current	I _{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply voltage	V _{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	0	0	0	V
Input high voltage	V _{IH}	2.0	-	V _{CC} +0.3 ^{*1}	2.4	-	V _{CC} +1.0 ^{*1}	V
Input low voltage	V _{IL}	-0.3 ^{*2}	-	0.8	-1.0 ^{*2}	-	0.8	V

*1 : V_{CC}+1.3V/15ns(3.3V), V_{CC}+2.0V/20ns(5V), Pulse width is measured at V_{CC}

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at V_{SS}

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input leakage current (Any input 0≤V _{IN} ≤V _{CC} +0.3V, all other pins not under test=0 volts.)	I _{IL} (L)	-5	5	μA
	Output leakage current (Data out is disabled, 0V≤V _{OUT} ≤V _{CC})	I _{OL} (L)	-5	5	μA
	Output high voltage level(I _{OH} =-2mA)	V _{OH}	2.4	-	V
	Output low voltage level(I _{OL} =2mA)	V _{OL}	-	0.4	V
5V	Input leakage current (Any input 0≤V _{IN} ≤V _{CC} +0.5V all other pins not under test=0 volts.)	I _{IL} (L)	-5	5	μA
	Output leakage current (Data out is disabled, 0V≤V _{OUT} ≤V _{CC})	I _{OL} (L)	-5	5	μA
	Output high voltage level(I _{OH} =-5mA)	V _{OH}	2.4	-	V
	Output low voltage level(I _{OL} =4.2mA)	V _{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM44V1000C	KM44C1000C	
I _{CC1}	Don't care	-5	-	85	mA
		-6	60	75	mA
		-7	55	65	mA
		-8	50	-	mA
I _{CC2}	Don't care	Don't care	1	2	mA
I _{CC3}	Don't care	-5	-	85	mA
		-6	60	75	mA
		-7	55	65	mA
		-8	50	-	mA
I _{CC4}	Don't care	-5	-	65	mA
		-6	45	55	mA
		-7	40	45	mA
		-8	35	-	mA
I _{CC5}	Normal L	Don't care	0.5	1	mA
			100	200	μA
I _{CC6}	Don't care	-5	-	85	mA
		-6	60	75	mA
		-7	55	65	mA
		-8	50	-	mA
I _{CC7}	L	Don't care	200	300	μA
I _{CCS}	L	Don't care	150	-	μA

I_{CC1} *: Operating current ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min.)I_{CC2} : Standby current ($\overline{RAS}=\overline{CAS}=W=V_{IH}$)I_{CC3} *: $\overline{RAS}$ -only refresh current ($\overline{CAS}=V_{IH}$, $\overline{RAS}$, Address cycling @t_{RC}=min.)I_{CC4} *: Fast Page Mode current ($\overline{RAS}=V_{IL}$, $\overline{CAS}$, Address cycling @t_{PC}=min.)I_{CC5} : Standby current ($\overline{RAS}=\overline{CAS}=W=V_{CC}-0.2V$)I_{CC6} *: $\overline{CAS}$ -before- $\overline{RAS}$ refresh current ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min.)I_{CC7} : Battery back-up current, Average power supply current, Battery back-up modeInput high voltage(V_{IH})= $V_{CC}-0.2V$, Input low voltage(V_{IL})=0.2V, $\overline{CAS}=0.2V$ DQ0-3 = Don't care, t_{RC}= 125μs(L-ver) , t_{RAS}=t_{RASmin}~300 nsI_{CCS} : Self refresh current $\overline{RAS}=\overline{CAS}=V_{IL}$, $\overline{W}=\overline{OE}=A0 \sim A9=V_{CC}-0.2V$ or 0.2V,DQ0 ~ DQ3= $V_{CC}-0.2V$, 0.2V or OPEN

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3} and I_{CC6}, address can be changed maximum once while $\overline{RAS}=V_{IL}$. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time t_{PC}.

CAPACITANCE($T_A=25^{\circ}\text{C}$, $V_{CC}=5\text{V}$ or 3.3V , $f=1\text{MHz}$)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A9]	C_{IN1}	-	5	pF
Input capacitance [$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{W}}$, $\overline{\text{OE}}$]	C_{IN2}	-	7	pF
Output capacitance [DQ0 - DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, See note 1,2)

 Test condition(5V device) : $V_{CC}=5.0\text{V} \pm 10\%$, $V_{IH}/V_{IL}=2.4/0.8\text{V}$, $V_{OH}/V_{OL}=2.4/0.4\text{V}$

 Test condition(3.3V device) : $V_{CC}=3.3\text{V} \pm 0.3\text{V}$, $V_{IH}/V_{IL}=2.0/0.8\text{V}$, $V_{OH}/V_{OL}=2.0/0.8\text{V}$

Parameter	Symbol	- 5 ^{*1}		- 6		- 7		- 8 ^{*2}		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t _{RWC}	133		155		185		205		ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}		50		60		70		80	ns	3,4,10
Access time from $\overline{\text{CAS}}$	t _{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t _{AA}		25		30		35		40	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	t _{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t _{OFF}	0	13	0	15	0	20	0	20	ns	6
Transition time (rise and fall)	t _T	3	50	3	50	3	50	3	50	ns	2
$\overline{\text{RAS}}$ precharge time	t _{RP}	30		40		50		60		ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{\text{RAS}}$ hold time	t _{RS}	13		15		20		20		ns	
$\overline{\text{CAS}}$ hold time	t _{CS}	50		60		70		80		ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	13	10K	15	10K	20	10K	20	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	20	37	20	45	20	50	20	60	ns	4
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	15	25	15	30	15	35	15	40	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	5		5		5		5		ns	
Row address set-up time	t _{ASR}	0		0		0		0		ns	
Row address hold time	t _{BAH}	10		10		10		10		ns	
Column address set-up time	t _{ASC}	0		0		0		0		ns	
Column address hold time	t _{CAH}	10		10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	t _{AR}	40		45		55		60		ns	15
Column address to $\overline{\text{RAS}}$ lead time	t _{BAL}	25		30		35		40		ns	
Read command set-up time	t _{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	t _{RBH}	0		0		0		0		ns	
Write command hold time	t _{WCH}	10		10		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	t _{WCR}	40		45		55		60		ns	15
Write command pulse width	t _{WP}	10		10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	15		15		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	t _{CWL}	13		15		20		20		ns	

Note) *1 : 5V only, *2 : 3.3V only

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, See note 2)

Parameter	Symbol	- 5 ^{*1}		- 6		- 7		- 8 ^{*2}		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	t _{DS}	0		0		0		0		ns	9
Data hold time	t _{DH}	10		10		15		15		ns	9
Data hold time referenced to $\overline{\text{RAS}}$	t _{DHR}	40		45		55		60		ns	15
Refresh period(Normal)	t _{REF}		16		16		16		16	ms	
Refresh period(L-ver)	t _{REF}		128		128		128	0	128	ms	
Write command set-up time	t _{WCS}	0		0		0		50		ns	7
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	t _{CWD}	36		40		50		110		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	t _{RWD}	73		85		100		70		ns	7
Column address to $\overline{\text{W}}$ delay time	t _{AWD}	48		55		65		75		ns	7
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	t _{CPWD}	53		60		70		10		ns	
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	t _{CSR}	10		10		10		15		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	t _{CHR}	10		10		15		5		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	t _{RPC}	5		5		5		30		ns	
$\overline{\text{CAS}}$ precharge time($\overline{\text{C}}$ -B-R counter test cycle)	t _{CPT}	20		20		25				ns	
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}		30		35		40	50	45	ns	3
Fast Page mode cycle time	t _{PC}	35		40		45		105		ns	
Fast Page mode read-modify-write cycle time	t _{PRWC}	76		85		100		10		ns	
$\overline{\text{CAS}}$ precharge time (Fast page cycle)	t _{CP}	10		10		10		80		ns	
$\overline{\text{RAS}}$ pulse width (Fast page cycle)	t _{RASP}	50	200K	60	200K	70	200K	45	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t _{RHCP}	30		35		40				ns	
$\overline{\text{OE}}$ access time	t _{OEa}		13		15		20	20	20	ns	
$\overline{\text{OE}}$ to data delay	t _{OE_D}	13		15		20		0		ns	
Out put buffer turn off delay time from $\overline{\text{OE}}$	t _{OEZ}	0	13	0	15	0	20	20	20	ns	6
$\overline{\text{OE}}$ command hold time	t _{OE_H}	13		15		20		10		ns	
Write command set-up time(Test mode in)	t _{WTS}	10		10		10		10		ns	
Write command hold time(Test mode in)	t _{WTH}	10		10		10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time($\overline{\text{C}}$ -B-R refresh)	t _{WRP}	10		10		10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time($\overline{\text{C}}$ -B-R refresh)	t _{WRH}	10		10		10		100		ns	
$\overline{\text{RAS}}$ pulse width($\overline{\text{C}}$ -B-R self refresh)	t _{RASS}	100		100		100		150		us	14
$\overline{\text{RAS}}$ precharge time ($\overline{\text{C}}$ -B-R self refresh)	t _{RPS}	90		110		130		-50		ns	14
$\overline{\text{CAS}}$ hold time ($\overline{\text{C}}$ -B-R self refresh)	t _{CHS}	-50		-50		-50				ns	14

Note) *1 : 5V only, *2 : 3.3V only

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5 ^{*1}		-6		-7		-8 ^{*2}		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from RAS	tRAC		55		65		75		85	ns	3,4,10
Access time from CAS	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,10
RAS pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
CAS pulse width	tCAS	18	10K	20	10K	25	10K	25	10K	ns	
RAS hold time	tRSH	18		20		25		25		ns	
CAS hold time	tCSH	55		65		75		85		ns	
Column address to RAS lead time	tRAL	30		35		40		45		ns	
CAS to W delay time	tCWD	41		45		55		55		ns	7
RAS to W delay time	tRWD	78		90		105		115		ns	7
Column address to W delay time	tAWD	53		60		70		75		ns	7
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
RAS pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	85	200K	ns	
Access time form CAS precharge	tCPA		35		40		45		50	ns	3
OE access time	tOEA		20		20		25		25	ns	
OE to data delay	tOED	18		20		25		25		ns	
OE command hold time	tOEH	18		20		25		25		ns	

Note) *1 : 5V only, *2 : 3.3V only

NOTES

1. An initial pause of 200 μ s is required after power up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V device)/1 TTL(3.3V device) loads and 100pF.
4. Operation within the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RCD}(\text{max})$ is specified as a reference point only. If $t_{RCD}(\text{max})$ is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol} .
7. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{RWD} \geq t_{RWD}(\text{min})$ and $t_{AWD} \geq t_{AWD}(\text{min})$, then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RAD}(\text{max})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled by t_{AA} .
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. $t_{OFF}(\text{max})$ and $t_{OEZ}(\text{max})$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. For all of the refresh modes except for distributed $\overline{CAS}$ -Before- $\overline{RAS}$ refresh, 1024cycles of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.(3.3V L-ver.)
15. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\text{max})$.