512K x 36 and 1M x 18 PIPELINE 'NO WAIT' STATE BUS SRAM

PRELIMINARY INFORMATION
SEPTEMBER 2002

FEATURES

- 100 percent bus utilization
- No wait cycles between Read and Write
- Internal self-timed write cycle
- Individual Byte Write Control
- Single R/W (Read/Write) control pin
- Clock controlled, registered address, data and control
- Interleaved or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining for TQFP
- Power Down mode
- Common data inputs and data outputs
- $\overline{CKE}$ pin to enable clock and suspend operation
- JEDEC 100-pin TQFP, 119 PBGA package
- V_{DD} +2.5V power supply (± 5%)
- V_{DDQ}: 2.5V I/O Supply Voltage
- Industrial temperature available

DESCRIPTION

The 18 Meg 'NVP' product family feature high-speed, low-power synchronous static RAMs designed to provide a burstable, high-performance, 'no wait' state, device for network and communications customers. They are organized as 524, 288 words by 36 bits and 1M words by 18 bits, fabricated with *ISSI*'s advanced CMOS technology.

Incorporating a 'no wait' state feature, wait cycles are eliminated when the bus switches from read to write, or write to read. This device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit.

All synchronous inputs pass through registers are controlled by a positive-edge-triggered single clock input. Operations may be suspended and all synchronous inputs ignored when Clock Enable, $\overline{CKE}$ is HIGH. In this state the internal device will hold their previous values.

All Read, Write and Deselect cycles are initiated by the ADV input. When the ADV is HIGH the internal burst counter is incremented. New external addresses can be loaded when ADV is LOW.

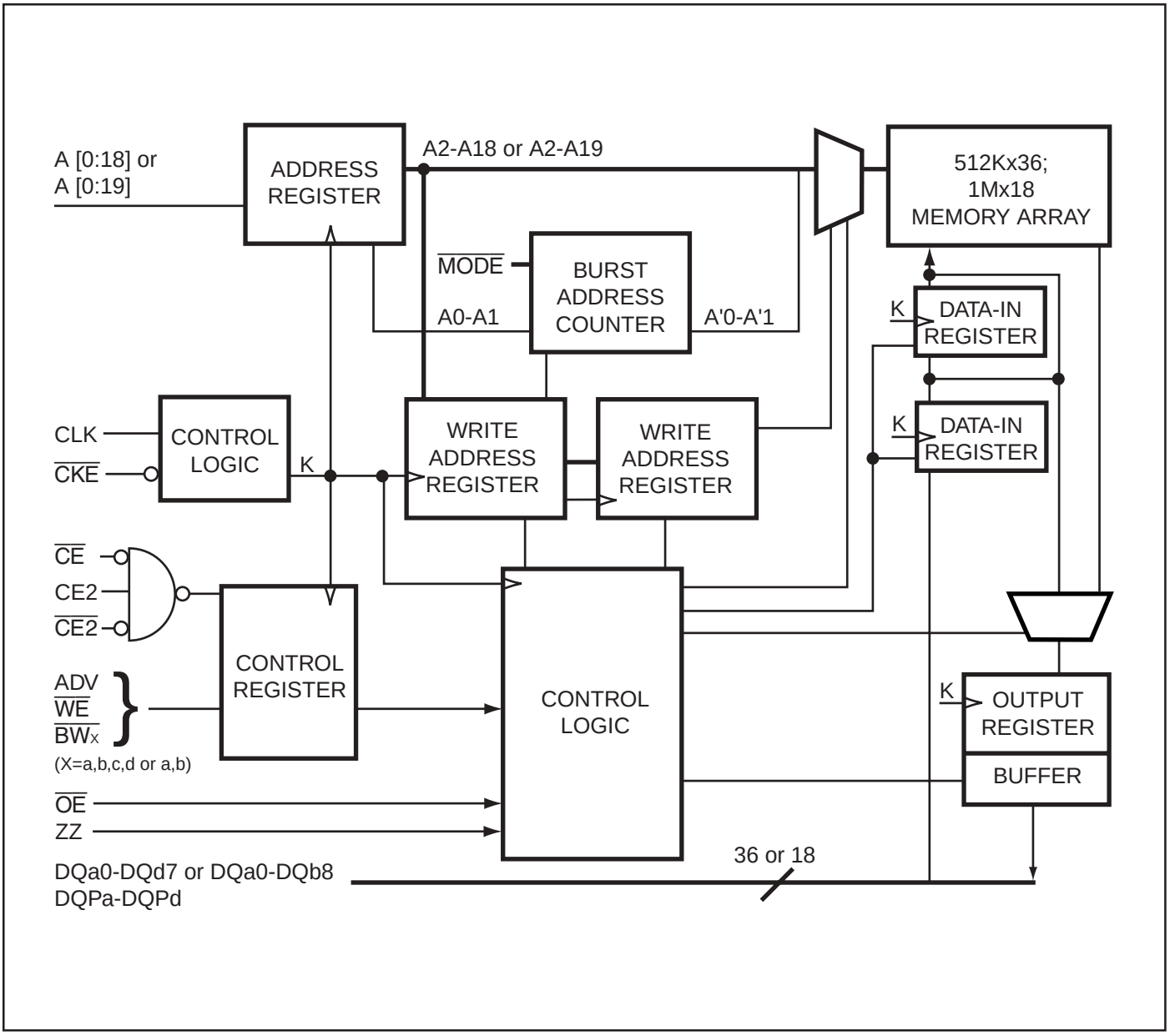
Write cycles are internally self-timed and are initiated by the rising edge of the clock inputs and when $\overline{WE}$ is LOW. Separate byte enables allow individual bytes to be written.

A burst mode pin (MODE) defines the order of the burst sequence. When tied HIGH, the interleaved burst sequence is selected. When tied LOW, the linear burst sequence is selected.

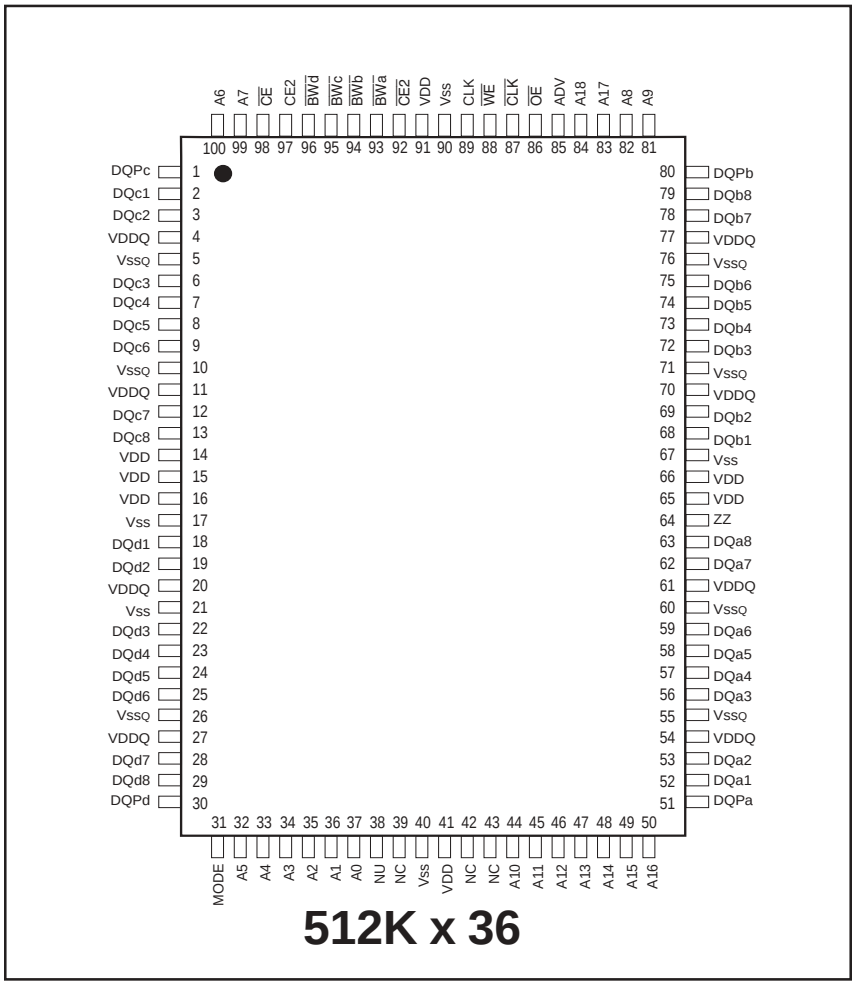
FAST ACCESS TIME

Symbol	Parameter	-133	-166	Units
t_{KQ}	Clock Access Time	4.2	3.6	ns
t_{KC}	Cycle Time	7.5	6	ns
	Frequency	133	166	MHz

BLOCK DIAGRAM



PIN CONFIGURATION
100-Pin TQFP

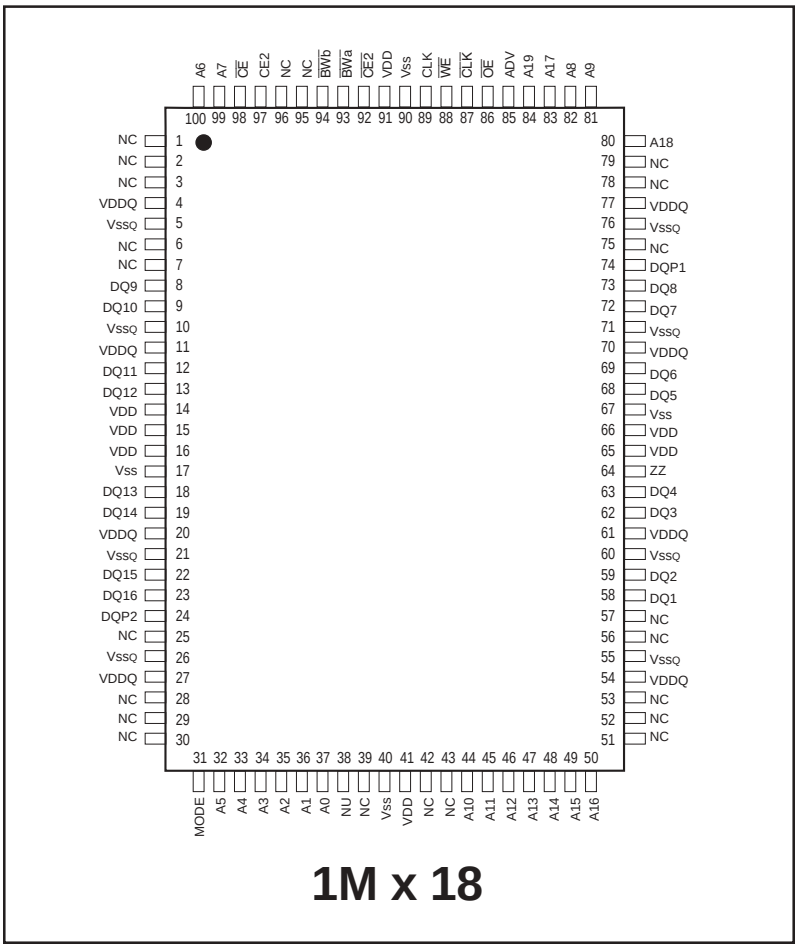


PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A18	Synchronous Address Inputs
CLK	Synchronous Clock
ADV	Synchronous Burst Address Advance
$\overline{BWa}$-$\overline{BWd}$	Synchronous Byte Write Enable
$\overline{WE}$	Write Enable
VSS	Ground for Core
NU	Not usable
NC	Not Connected

$\overline{CKE}$	Clock Enable
$\overline{CE}$, $\overline{CE2}$, CE2	Synchronous Chip Enable
$\overline{OE}$	Output Enable
DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
VDD	+2.5V Power Supply
VSSQ	Ground for output Buffer
VDDQ	Isolated Output Buffer Supply:2.5V
ZZ	Snooze Enable
DQPa-DQPd	Parity Data I/O

PIN CONFIGURATION
100-Pin TQFP



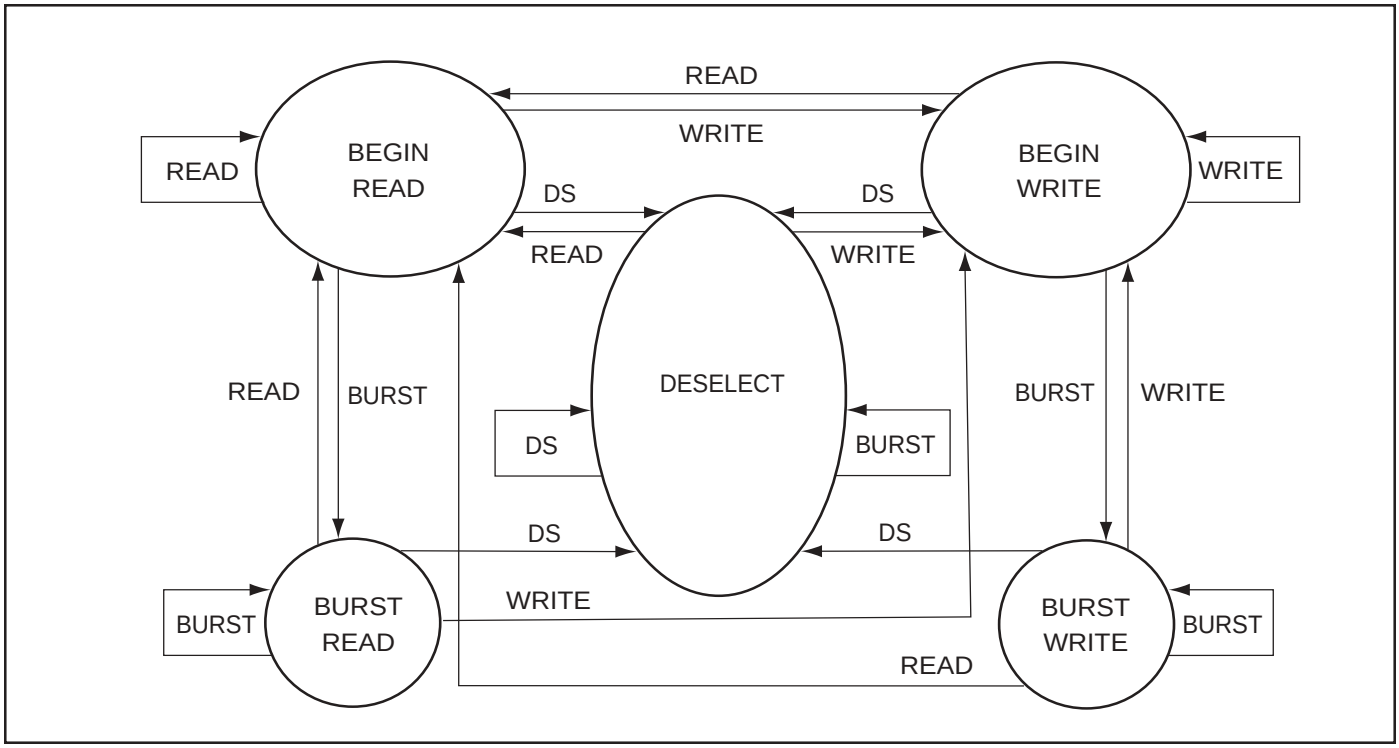
1M x 18

PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A19	Synchronous Address Inputs
CLK	Synchronous Clock
ADV	Synchronous Burst Address Advance
$\overline{BWa}$-$\overline{BWb}$	Synchronous Byte Write Enable
$\overline{WE}$	Write Enable
$\overline{CKE}$	Clock Enable
Vss	Ground for Core
NU	Not usable
NC	Not Connected

$\overline{CE}$, CE2, $\overline{CE2}$	Synchronous Chip Enable
$\overline{OE}$	Output Enable
DQ1-DQ16	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
V_{DD}	+2.5V Power Supply
V_{SSQ}	Ground for output Buffer
V_{DDQ}	Isolated Output Buffer Supply: +2.5V
ZZ	Snooze Enable
DQP1-DQP2	Parity Data I/O DQP1 is parity for DQ1-8; DQP2 is parity for DQ9-16

STATE DIAGRAM



SYNCHRONOUS TRUTH TABLE(1)

Operation	Address Used	$\overline{CE}1$	CE2	$\overline{CE}2$	ADV	$\overline{WE}$	$\overline{BW}x$	$\overline{OE}$	$\overline{CKE}$	CLK
Not Selected	N/A	H	X	X	L	X	X	X	L	↑
Not Selected	N/A	X	L	X	L	X	X	X	L	↑
Not Selected	N/A	X	X	H	L	X	X	X	L	↑
Not Selected Continue	N/A	X	X	X	H	X	X	X	L	↑
Begin Burst Read	External Address	L	H	L	L	H	X	L	L	↑
Continue Burst Read	Next Address	X	X	X	H	X	X	L	L	↑
NOP/Dummy Read	External Address	L	H	L	L	H	X	H	L	↑
Dummy Read	Next Address	X	X	X	H	X	X	H	L	↑
Begin Burst Write	External Address	L	H	L	L	L	L	X	L	↑
Continue Burst Write	Next Address	X	X	X	H	X	L	X	L	↑
NOP/Write Abort	N/A	L	H	L	L	L	H	X	L	↑
Write Abort	Next Address	X	X	X	H	X	H	X	L	↑
Ignore Clock	Current Address	X	X	X	X	X	X	X	H	↑

Notes:
1. "X" means don't care.
2. The rising edge of clock is symbolized by ↑
3. A continue deselect cycle can only be entered if a deselect cycle is executed first.
4. $\overline{WE}$ = L means Write operation in Write Truth Table.
   $\overline{WE}$ = H means Read operation in Write Truth Table.
5. Operation finally depends on status of asynchronous pins (ZZ and $\overline{OE}$).

ASYNCHRONOUS TRUTH TABLE(1)

Operation	ZZ	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes:

1. X means "Don't Care".
2. For write cycles following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
3. Sleep Mode means power Sleep Mode where stand-by current does not depend on cycle time.
4. Deselected means power Sleep Mode where stand-by current depends on cycle time.

WRITE TRUTH TABLE (x18)

Operation	$\overline{WE}$	$\overline{BW}$a	$\overline{BW}$b
READ	H	X	X
WRITE BYTE a	L	L	H
WRITE BYTE b	L	H	L
WRITE ALL BYTEs	L	L	L
WRITE ABORT/NOP	L	H	H

Notes:

1. X means "Don't Care".
2. All inputs in this table must beet setup and hold time around the rising edge of CLK.

WRITE TRUTH TABLE (x36)

Operation	$\overline{WE}$	$\overline{BW}$a	$\overline{BW}$b	$\overline{BW}$c	$\overline{BW}$d
READ	H	X	X	X	X
WRITE BYTE a	L	L	H	H	H
WRITE BYTE b	L	H	L	H	H
WRITE BYTE c	L	H	H	L	H
WRITE BYTE d	L	H	H	H	L
WRITE ALL BYTEs	L	L	L	L	L
WRITE ABORT/NOP	L	H	H	H	H

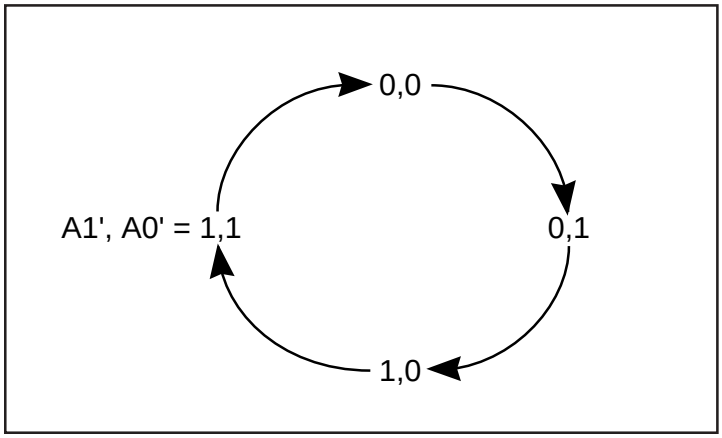
Notes:

1. X means "Don't Care".
2. All inputs in this table must beet setup and hold time around the rising edge of CLK.

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{DD})

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = GND)



ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
P_D	Power Dissipation	1.6	W
V_{IN}, V_{OUT}	Voltage Relative to GND for I/O Pins	–0.5 to V_{DDQ} + 0.3	V
V_{IN}	Voltage Relative to GND for for Address and Control Inputs	–0.3 to 3.6	V

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuity to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	2.5V ± 5%	3.3V ± 5%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	2.5V Min.	2.5V Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –1.0 mA (2.5V) I_{OH} = –100 µA (2.5V)	2.0 V_{DD} -0.2	— —	V
V_{OL}	Output LOW Voltage	I_{OL} = 1.0 mA (2.5V) I_{OL} = 100 µA (2.5V)	— —	0.4 0.2	V
V_{IH}	Input HIGH Voltage		1.7	V_{DD}+ 0.3	V
V_{IHI}	Input HIGH Voltage for Mode pin		V_{DD} -0.3	V_{DD}+ 0.3	V
V_{ILI}	Input HIGH Voltage for Mode pin and NU Pins		-0.3	0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.7	V
I_{LI}	Input Leakage Current	V_{IN} = 0 to V_{DD}(1)	–1	1	µA
I_{NU}	Input Current (NU Pin)	V_{IN} = 0V to 0.3V	-1	1	µA
I_{LO}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{DDQ}, $\overline{OE}$ = V_I	–1	1	µA

POWER SUPPLY CHARACTERISTICS(1) (Over Operating Range)

Symbol	Parameter	Test Conditions	-133 MAX x18	-133 MAX 36	-166 MAX x18	-166 MAX x32/36	Unit
I_{CC}	AC Operating Supply Current	Device Selected, $\overline{OE}$ = V_{IH}, ZZ ≤ V_{IL}, All Inputs ≤ 0.2V OR ≥ V_{DD} – 0.2V, Cycle Time ≥ t_{KC} min.	370	400	410	440	mA
I_{SB}	Standby Current TTL Input	Device Deselected, V_{CC} = Max., All Inputs ≤ 0.2V OR ≥ V_{DD}– 0.2V, ZZ ≤ V_{IL}, f = Max.	160	160	210	210	mA
I_{SBI}	Standby Current CMOS Input	all inputs = V_{DD} - 0.2 or 0.2V CLOOK = V_{SS}	10	10	10	10	mA

Note:
1. NU pin must be Low or not Connected

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = GND	7	pF
C_{IN}	Input Capacitance for Mode, ZZ, NU pin	V_{IN} = GND	10	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$= GND	9	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

2.5V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 2.5V
Input Rise and Fall Times	1V/ ns
Input and Output Timing and Reference Level	1.25V
Output Load	See Figures 3 and 4

2.5V I/O OUTPUT LOAD EQUIVALENT

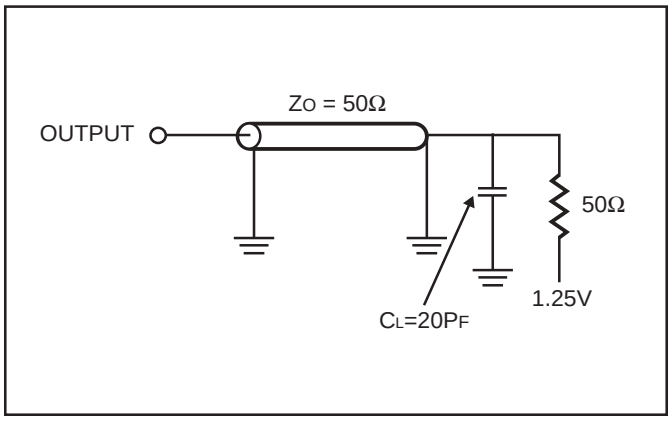


Figure 3

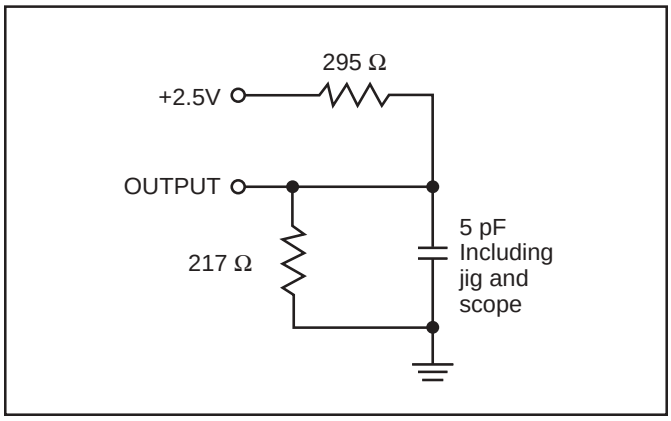


Figure 4

READ/WRITE CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

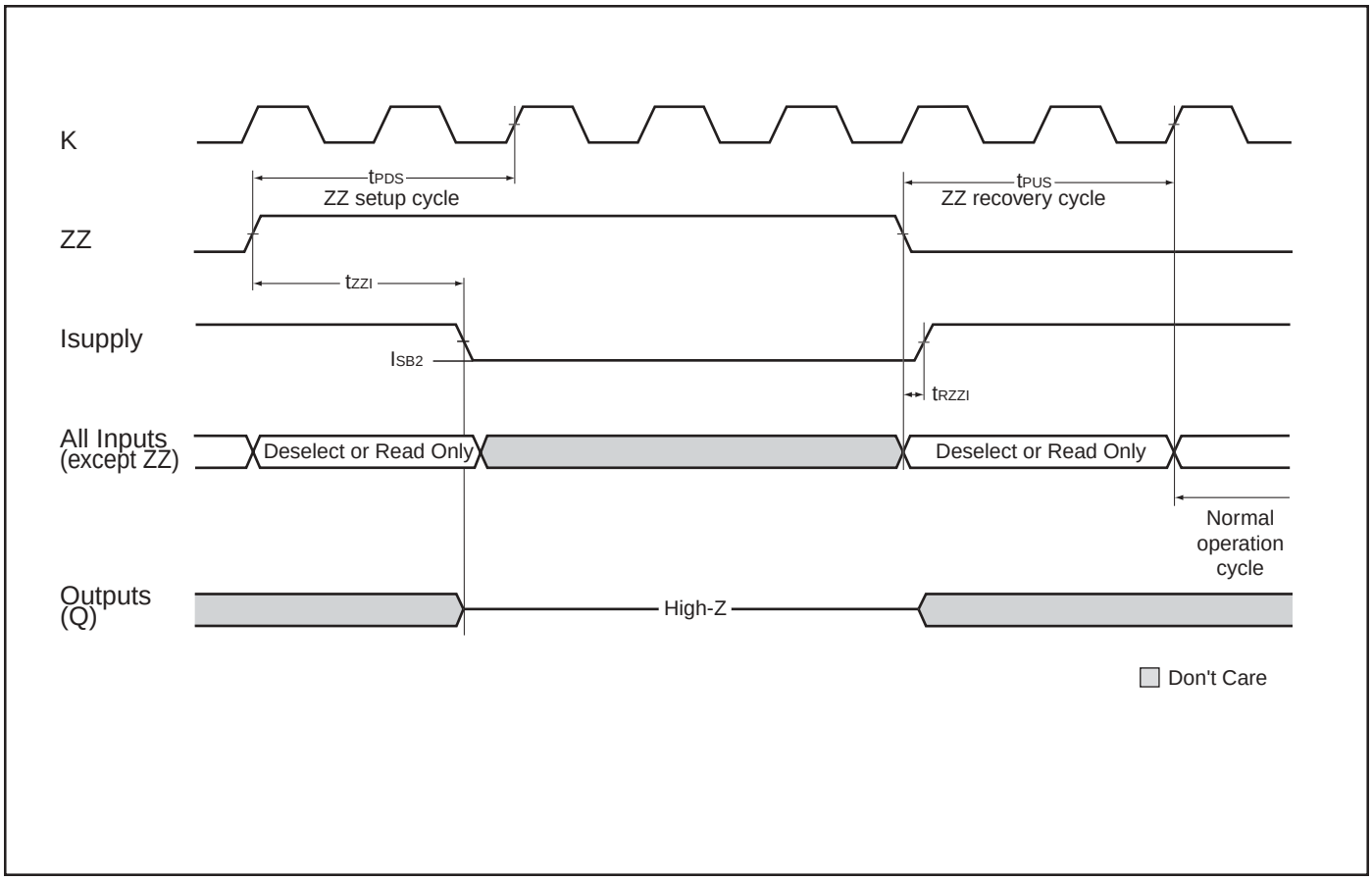
Symbol	Parameter	-133 Min.	-133 Max.	-166 Min.	-166 Max.	Unit
fmax	Clock Frequency	—	133	—	166	MHz
t_{KC}	Cycle Time	7.5	—	6	—	ns
t_{KH}	Clock High Time	3	—	2.2	—	ns
t_{KL}	Clock Low Time	3	—	2.2	—	ns
t_{KQ}	Clock Access Time	—	4.2	—	3.6	ns
t_{KQX}[2]	Clock High to Output Invalid	1.5	—	1.5	—	ns
t_{KQLZ}[2,3]	Clock High to Output Low-Z	0	—	0	—	ns
t_{KQHZ}[2,3]	Clock High to Output High-Z	—	3.5	—	3.5	ns
t_{OEQ}	Output Enable to Output Valid	—	4.2	—	3.8	ns
t_{OELZ}[2,3]	Output Enable to Output Low-Z	1.5	—	1.5	—	ns
t_{OEHZ}[2,3]	Output Disable to Output High-Z	1.5	4.2	1.5	3.8	ns
t_{AS}	Address Setup Time	2	—	1.5	—	ns
t_{WS}	Read/Write Setup Time	2	—	1.5	—	ns
t_{CES}	Chip Enable Setup Time	2	—	1.5	—	ns
t_{SE}	Clock Enable Setup Time	2	—	1.5	—	ns
t_{AVS}	Address Advance Setup Time	2	—	1.5	—	ns
t_{DS}	Data Setup Time	1.7	—	1.5	—	ns
t_{AH}	Address Hold Time	0.5	—	0.5	—	ns
t_{HE}	Clock EnableHold Time	0.5	—	0.5	—	ns
t_{WH}	Write Hold Time	0.5	—	0.5	—	ns
t_{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	ns
t_{ADVH}	Address Advance Hold Time	0.5	—	0.5	—	ns
t_{DH}	Data Hold Time	0.5	—	0.5	—	ns
t_{PDS}	ZZ High to Power Down	—	2	—	2	cyc
t_{PUS}	ZZ Low to Power Down	—	2	—	2	cyc

Notes:
1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.

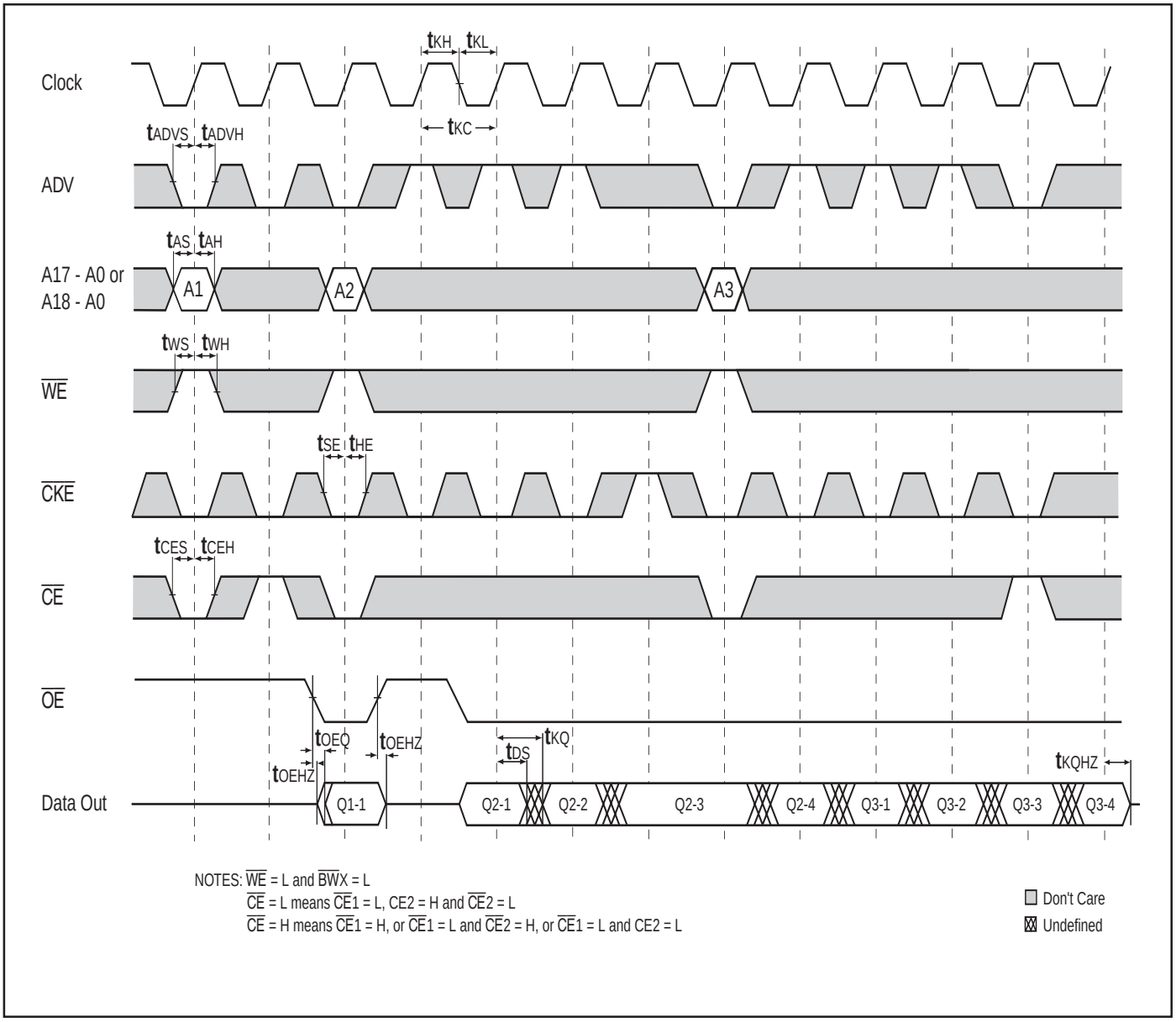
SLEEP MODE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Max.	Unit
I_{SB2}	Current during SLEEP MODE	ZZ ≥ V_{IH}		20	mA
t_{PDS}	ZZ active to input ignored		2		cycle
t_{PUS}	ZZ inactive to input sampled		2		cycle
t_{ZZI}	ZZ active to SLEEP current		2		cycle
t_{RZZI}	ZZ inactive to exit SLEEP current		0		ns

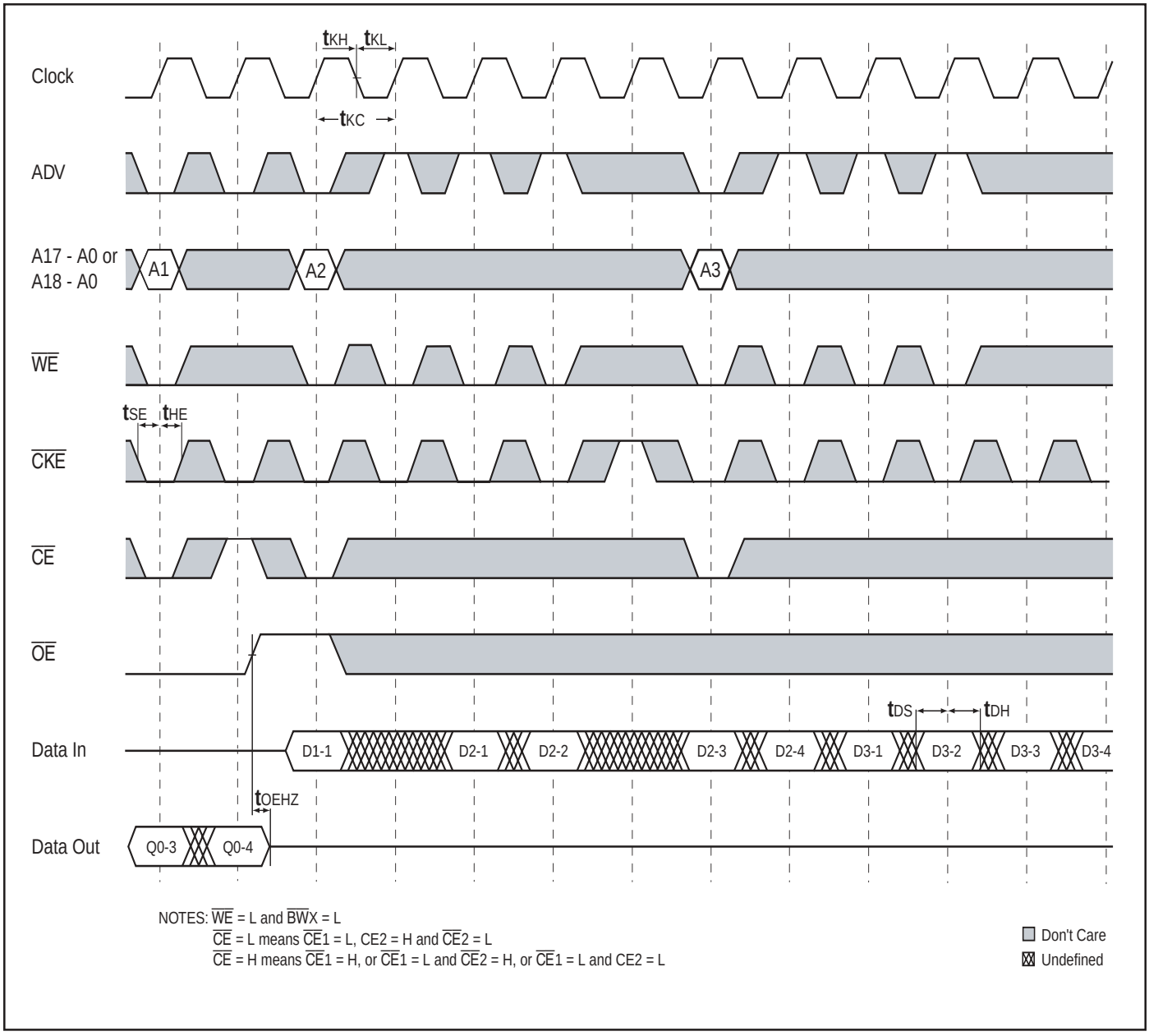
SLEEP MODE TIMING



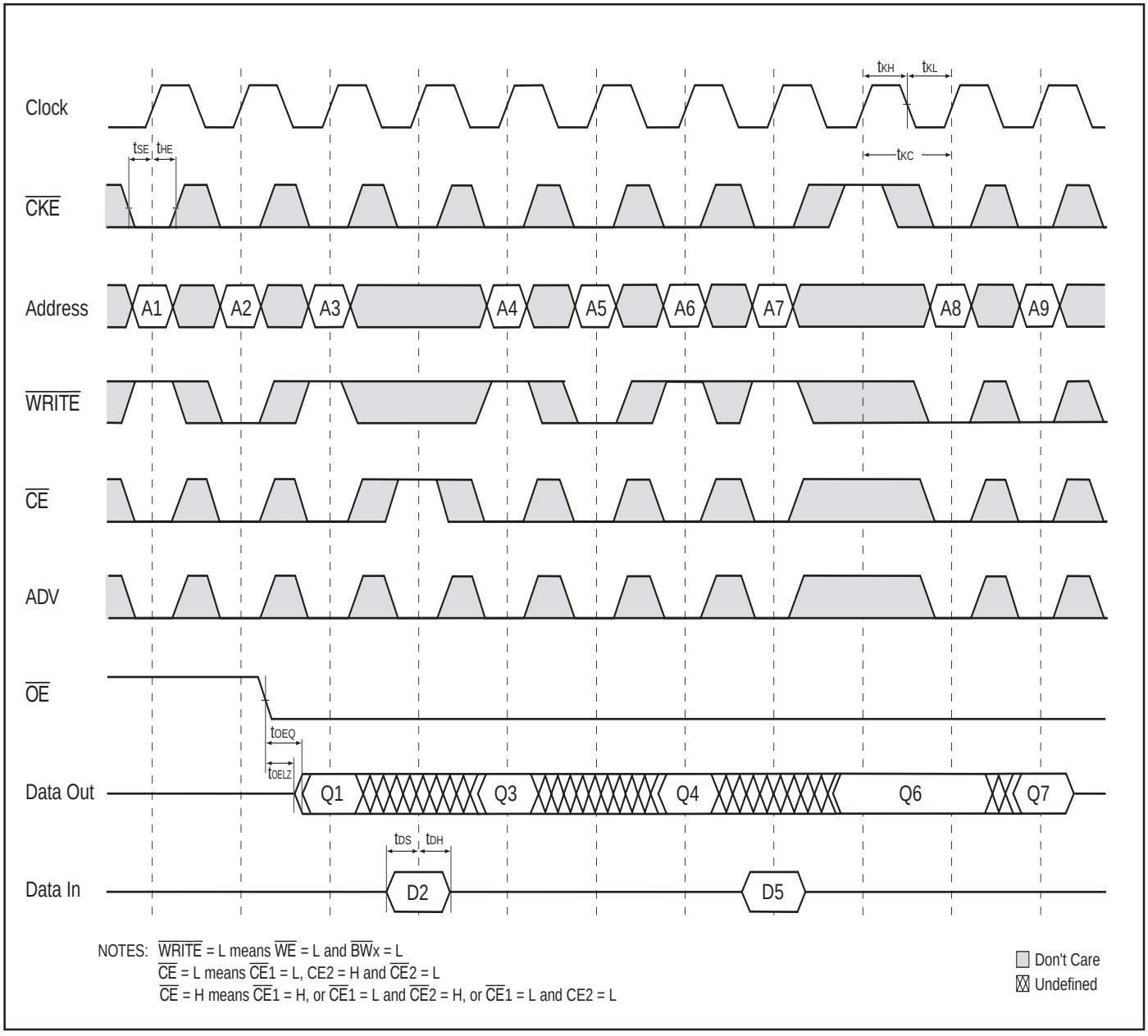
READ CYCLE TIMING



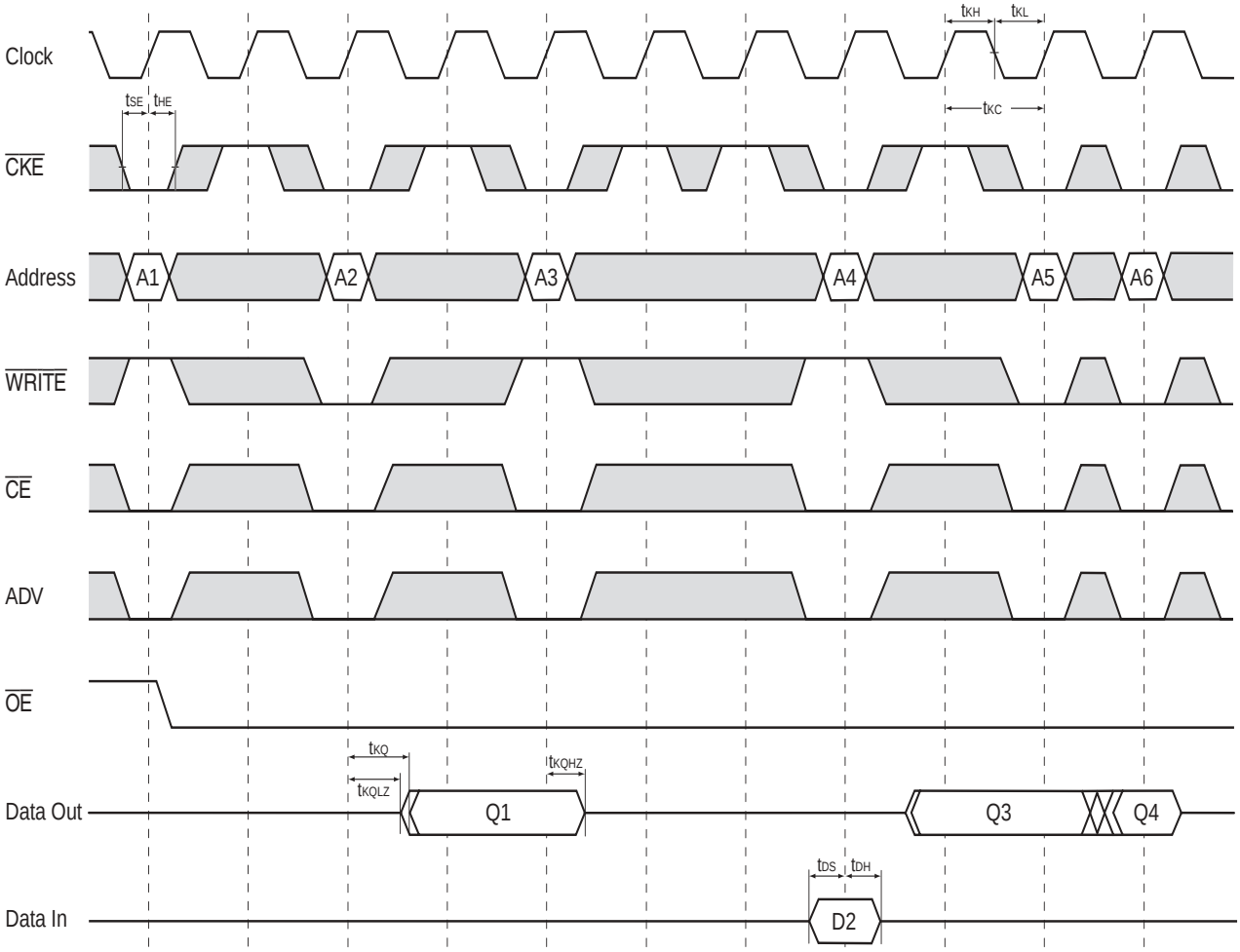
WRITE CYCLE TIMING



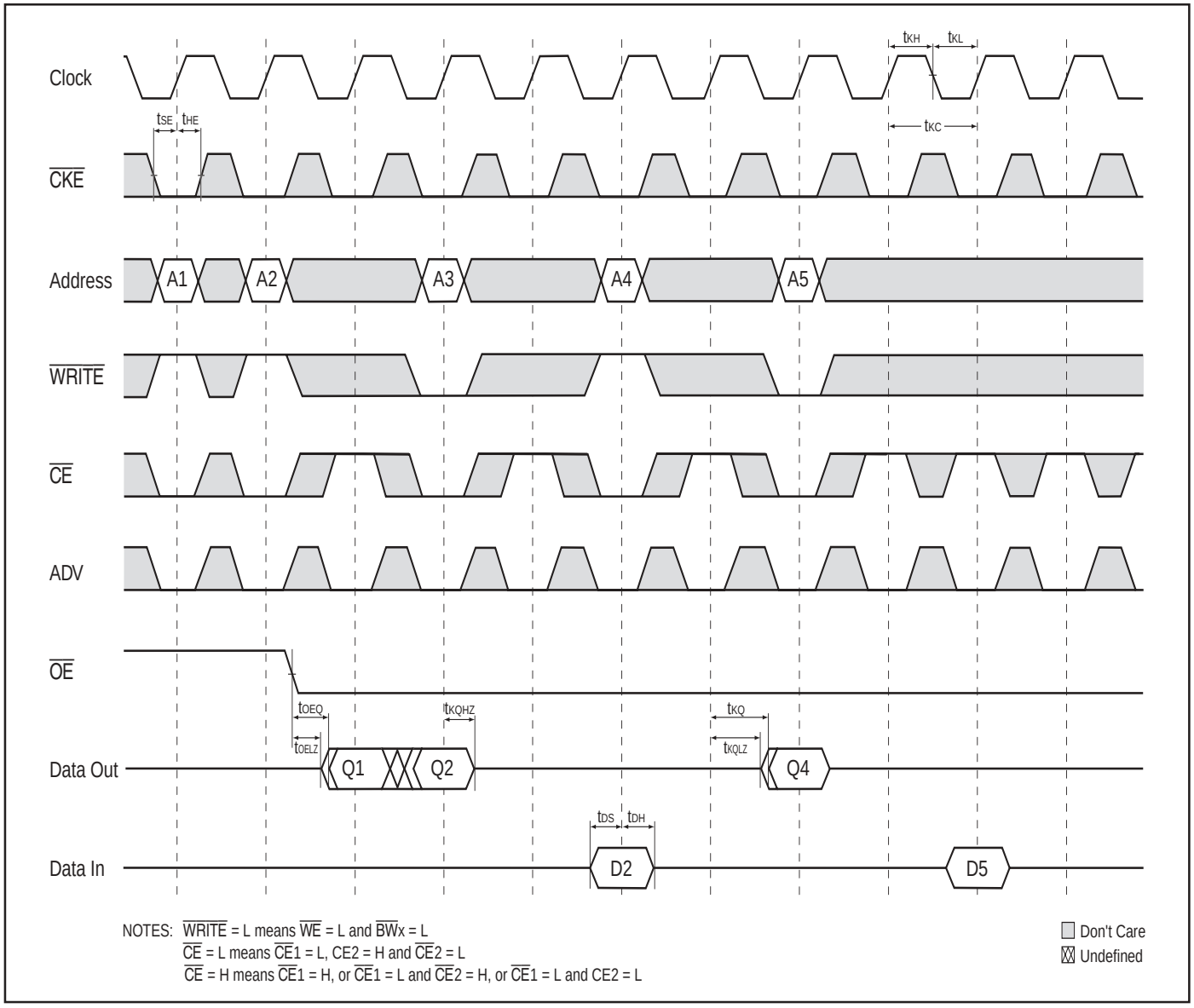
SINGLE READ/WRITE CYCLE TIMING



$\overline{CKE}$ OPERATION TIMING



$\overline{CE}$ OPERATION TIMING



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Frequency	Order Part Number	Package
512Kx36		
166	IS61NVP51236-166TQ	TQFP
133	IS61NVP51236-133TQ	TQFP
1Mx18		
166	IS61NVP10018-166TQ	TQFP
133	IS61NVP10018-133TQ	TQFP

Industrial Range: –40°C to +85°C

Frequency	Order Part Number	Package
512Kx36		
166	IS61NVP51236-166TQI	TQFP
133	IS61NVP51236-133TQI	TQFP
1Mx18		
166	IS61NVP10018-166TQI	TQFP
133	IS61NVP10018-133TQI	TQFP