Product Specification Sheet

AT&T Microelectronics

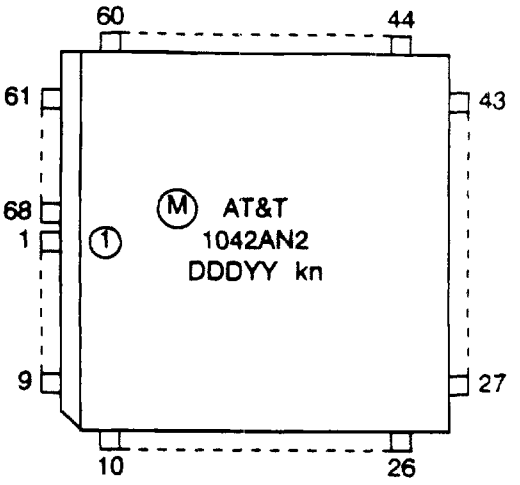
Initial Use

5ESS/5E

1042AN2
Quad Z-Line Controller

Description

The 1042AN2 Quad Z-Line Controller (QZLC) is used on the Z-interface pack of the ISLU2 to control four Z-line interface circuits. The QZLC provides an interface between a 4 Mbits/s serial bitstream that is divided into thirty-two 16-bit timeslots and the four Z-line interface circuits. Each line circuit contains a codec (T-7548 or equivalent) that connects to the QZLC via independent 512 kHz serial channels called subscriber line datalinks (SLDs). All line circuit control registers are accessible on the QZLC device by system software.



Package Outline
68-pin chip carrier (0.050" pitch)
Dimensions per 105709265

Characteristics

Absolute Maximum Ratings	
Power Supply Voltage	$V_{DD} - V_{SS} = 7.0$ V
Input Voltage	V_{SS} to V_{DD} (for $V_{DD} - V_{SS} > 6.1$ V)
Storage Temperature	−40 °C to +125 °C
Recommended Maximum Operating Conditions	
Power Supply Voltage	$V_{DD} - V_{SS} = 5.5$ V
Input Voltage	(V_{SS} − 0.3 V) to (V_{DD} + 0.3 V)
Operating Temperature	0 °C to 85 °C
ESD Failure Threshold	
Human Body Model	>500 V all pins, >1000 V cor. pins
Charged Device Model	>500 V all pins, >1000 V cor. pins
General Characteristics	
I/O Levels	TTL and/or CMOS compatible
Technology	0.9 μm CMOS custom logic
Power Supply	5 V ± 10%
Package	Plastic chip carrier

For additional information, contact your AT&T Account Manager or the following:

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PS91-001CMOS-07

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Pin Identification

Pkg Pin	Type	Signal Name	Pkg Pin	Type	Signal Name
1	IN-TTL	SYNC0	35	VSS	VSS.M1
2	IN-TTL	CLK0	36	OUT-TS	SDATEN7
3	IN-TTL	DIN0	37	OUT-TS	SDATEN6
4	IN-TTL	SEL0	38	OUT-TS	SDATEN5
5	IN-TTL-PU	HLCTS	39	OUT-TS	SDATEN4
6	IN-TTL-PU	HLREG	40	OUT-TS	SDATEN3
7	VSS	VSS.M1	41	OUT-TS	SDATEN2
8	IN-TTL-PU	SELBASS	42	OUT-TS	SDATEN1
9	VDD	VDD.M1	43	OUT-TS	SDATEN0
10	OUT-TS	RLY0	44	VSS	VSS.M1
11	OUT-TS	RLY1	45	I/O-PU	SLD3_
12	IN-TTL-PU	TEST	46	I/O-OD	SCAN_
13	IN-TTL-PU	DISELC	47	IN-TTL-PU	DTEST
14	I/O-PU	SLD0_	48	IN-TTL-PU	CTEST
15	IN-TTL-PU	TESTRTB	49	I/O-PU	VERS3_
16	IN-TTL-PU	MCTSB	50	VDD	VDD.M1
17	IN-TTL-PU	BATTFD	51	IN-TTL-PU	GIDBTSTB
18	IN-TTL-PU	TESTADB	52	IN-TTL-PU	GIDBMONB
19	IN-TTL	MN5DET	53	OUT-TS	SCL
20	VSS	VSS.M1	54	IN-TTL-PU	INITB
21	OUT-OD	CK12K	55	OUT-TS	SDIR
22	OUT-OD	CK16K	56	I/O-PU	SLD1_
23	OUT-TS	CONCK	57	IN-TTL-PU	AMUSEL
24	OUT-TS	SDATEN8B	58	IN-TTL-PU	VERS0
25	I/O-PU	SLD2_	59	I/O-PU	VERS1_
26	VDD	VDD.M1	60	IN-TTL	RESET
27	I/O-TS	SDATA_7	61	OUT-TS	DOUT1
28	I/O-TS	SDATA_6	62	OUT-TS	DOUT0
29	I/O-TS	SDATA_5	63	VSS	VSS.M1
30	I/O-TS	SDATA_4	64	I/O-PU	VERS2_
31	I/O-TS	SDATA_3	65	IN-TTL	SYNC1
32	I/O-TS	SDATA_2	66	IN-TTL	CLK1
33	I/O-TS	SDATA_1	67	IN-TTL	DIN1
34	I/O-TS	SDATA_0	68	IN-TTL	SEL1

Terminology

IN — Input pin	SCH — Schmitt Trigger Input
OUT — Output pin	OPEN — Unused in this application
I/O — Bidirectional pin	PU — Pull-up resistor on pin
VDD — Power pin (5 V nominal)	PD — Pull-down resistor on pin
VSS — Ground pin	TS — 3-state output
TTL — Logic levels (0.4 V and 2.4 V nominal)	OD — Open-drain output
MOS — Logic levels (0.5 V and 4.5 V nominal)	