DENSE-PAC MICROSYSTEMS

128 Megabit FLASH EEPROM

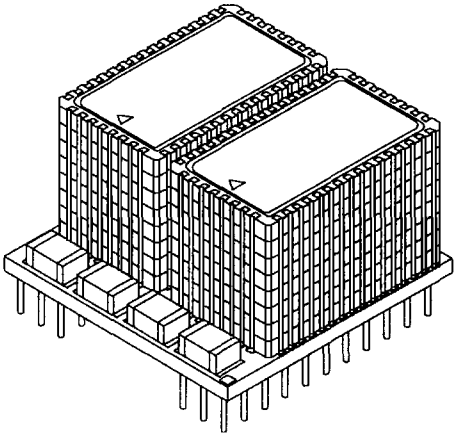
DPZ8MX16NV3

DESCRIPTION:

The DPZ8MX16NV3 "VERSA-STACK" module is a revolutionary new memory subsystem using Dense-Pac Microsystems' ceramic Stackable Leadless Chip Carriers (SLCC) mounted on a co-fired ceramic substrate. It offers 128 Megabits of FLASH EEPROM in a single package envelope of 1.090" x 1.090" x .776".

The DPZ8MX16NV3 is built with two stacks of 8 SLCC packages each containing a 1 Meg x 8 FLASH memory devices. Each SLCC is hermetically sealed making the module suitable for commercial, industrial and military applications.

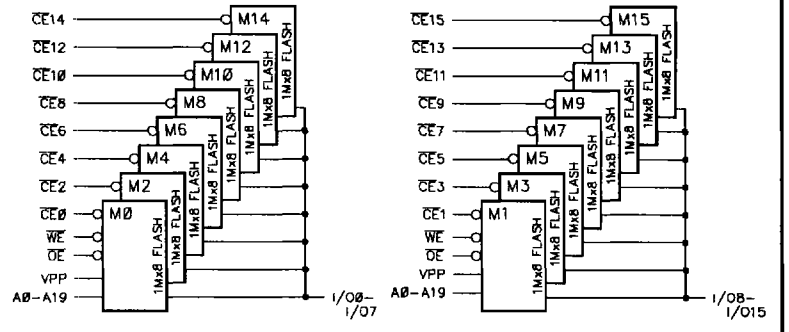
By using SLCCs, the "Versa-Stack" family of modules offers a higher board density of memory than available with conventional through-hole, surface mount, module or hybrid techniques.



FEATURES:

- Organization: 8Meg x 16, 16 Meg x 8
- Fast Access Times:
  90, 100, 120, 150ns (max.)
- High-Density Symmetrically Blocked Architecture
  - Sixteen 64 Kbyte Blocks Per Device
- Extended Cycling Capability
  - 10K Block Erase Cycles
- Automated Byte Write and Block Erase
  - Command User Interface
  - Status Register
- SRAM-Compatible Write Interface
- Hardware Data Protection Feature
  - Erase / Write Lockout during Power Transitions
- 66 - Pin PGA "VERSA-STACK" Package

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES	
A0 - A19	Address Inputs
I/O0 - I/O15	Data Input/Output
$\overline{CE0}$ - $\overline{CE15}$	Chip Enables
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{PP}	Programming Voltage (+12.0V)
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

PIN-OUT DIAGRAM

(TOP VIEW)

1	$\overline{CE2}$	12	N.C.	23	$\overline{CE0}$	34	$\overline{CE3}$	45	VDD	56	$\overline{CE1}$
2	$\overline{CE6}$	13	N.C.	24	$\overline{CE4}$	35	$\overline{CE7}$	46	N.C.	57	$\overline{CE5}$
3	$\overline{CE10}$	14	VSS	25	$\overline{CE8}$	36	$\overline{CE11}$	47	N.C.	58	$\overline{CE9}$
4	A13	15	$\overline{CE14}$	26	$\overline{CE12}$	37	A6	48	$\overline{CE15}$	59	$\overline{CE13}$
5	A14	16	A10	27	$\overline{OE}$	38	A7	49	A3	60	A0
6	A15	17	A11	28	VPP	39	A17	50	A4	61	A1
7	A16	18	A12	29	$\overline{WE}$	40	A8	51	A5	62	A2
8	A18	19	VDD	30	I/O7	41	A9	52	N.C.	63	I/O15
9	I/O0	20	N.C.	31	I/O6	42	I/O8	53	N.C.	64	I/O14
10	I/O1	21	A19	32	I/O5	43	I/O9	54	VSS	65	I/O13
11	I/O2	22	I/O3	33	I/O4	44	I/O10	55	I/O11	66	I/O12

PRODUCT OVERVIEW

The DPZ8MX16NV3 is a high-performance 128 Megabit memory organized as 16 -1 Mbyte (1,048,576 bytes) of 8 bits each. Sixteen 64 Kbyte (65,536 byte) blocks are included in each of the sixteen 1 Meg x 8 devices on the module. A memory map is shown in this specification. A block erase operation erases one of the sixteen blocks of memory in typically 1.6 seconds, independent of the remaining blocks. Each block can be independently erased and written 10,000 cycles. Erase Suspend mode allows system software to suspend block erase to read data or execute code from any other block of each device.

The Command User Interface serves as the interface between the microprocessor or microcontroller and the internal operation of the fuse devices.

Byte Write and Block Erase Automation allow byte write and block erase operations to be executed using a two-write command sequence to the Command User Interface. The internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for byte write and block erase operations, including verifications, thereby unburdening the microprocessor or microcontroller. Writing of memory data is performed in byte increments typically within 9µs, an 80% improvement over current flash memory products.

The Status Register indicates the status of the WSM and when the WSM successfully completes the desired byte write or block erase operation.

Maximum access time is 150ns (t_{ACC}) over the military temperature range (-55°C to +125°C) and over V_{DD} supply voltage range 4.5V to 5.5V.

When the $\overline{CE}$ pin is at V_{DD}, the I_{CC} CMOS Standby mode is enabled.

PRINCIPLES OF OPERATION

The device includes on-chip write automation to manage write and erase functions. The Write State Machine allows for: 100% TTL-level control inputs, fixed power supplies during block erasure and byte write, and minimal processor overhead with RAM-like interface timings.

After initial device power-up, or after return from deep powerdown mode (see Table 1), the module functions as a read-only memory. Manipulation of external memory-control pins allow array read, standby and output disable operations. Both Status Register and device identifier can also be accessed through the Command User Interface when $V_{PP} = V_{PPL}$.

This same subset of operations is also available when high voltage is applied to the V_{PP} pin. In addition, high voltage on V_{PP} enable successful block erasure and byte writing of the device. All functions associated with altering memory contents (byte write, block erase, status and device identifier) are accessed via the Command User Interface and verified through the Status Register.

Commands are written using standard microprocessor write timings. Command User Interface contents serve as input to the WSM, which controls the block erase and byte write circuitry. Write cycles also internally latch addresses and data needed for byte write or block erase operations. With the appropriate command written to the register, standard microprocessor read timings output array data, access the device identifier codes, or output byte write and block erase status for verification.

Interface software to initiate and poll progress of internal byte write and block erase can be stored in any of the module blocks. This code is copied to, and executed from, system RAM during actual flash memory update. After successful completion of byte write and/or block erase, code/data reads from the module are again possible via the Read Array command. Erase suspend/resume capability allows system software to suspend block erase to read data and execute code from any other block.

COMMAND USER INTERFACE AND WRITE AUTOMATION

An on-chip state machine controls block erase and byte write, freeing the system processor for other tasks. After receiving the Erase Setup and Erase Confirm commands, the state machine controls block pre-conditioning and erase, returning progress via the status Register. Byte write is similarly controlled, after destination address and expected data are supplied. The program and erase algorithms are regulated by the state machine, including pulse repetition where required and internal verification and margining of data.

DATA PROTECTION

Depending on the application, the system designer may choose to make the V_{PP} power supply switchable (available only when memory byte writes/block erases are required) or hardwired to V_{PPH}. When $V_{PP} = V_{PPL}$, memory contents cannot be altered. The module Command User Interface architecture provides protection from unwanted byte write or block erase operations even when high voltage is applied to V_{PP}. Additionally, all functions are disabled whenever V_{DD} is below the write lockout voltage V_{LKO}. The module accommodates either design practice and encourage optimization of the processor-memory interface.

The two-step byte write/block erase Command User Interface write sequence provides additional software write protection.

MEMORY MAP *

FFFFF	64 Kbyte Block
F0000	
EFFFF	64 Kbyte Block
E0000	
DFFFF	64 Kbyte Block
D0000	
CFFFF	64 Kbyte Block
C0000	
BFFFF	64 Kbyte Block
B0000	
AFFFF	64 Kbyte Block
A0000	
9FFFF	64 Kbyte Block
90000	
8FFFF	64 Kbyte Block
80000	
7FFFF	64 Kbyte Block
70000	
6FFFF	64 Kbyte Block
60000	
5FFFF	64 Kbyte Block
50000	
4FFFF	64 Kbyte Block
40000	
3FFFF	64 Kbyte Block
30000	
2FFFF	64 Kbyte Block
20000	
1FFFF	64 Kbyte Block
10000	
0FFFF	64 Kbyte Block
00000	

* Per 1 Meg x 8 Device.

BUS OPERATION

Flash memory reads, erases and writes in-system via the local CPU. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

READ

The module has three read modes. The memory can be read from any of its blocks, and information can be read from the device identifier or Status Register. V_{PP} can be at either V_{PPL} or V_{PPH}.

The first task is to write the appropriate read mode command to the Command User Interface (array, device identifier, or Status Register). The module automatically resets to Read Array mode upon initial device powerup. The module has four control pins, two of which must be logically active to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the device selection control, and when active enables the selected memory device. Output Enable ($\overline{OE}$) is the data input/output (I/O0 - I/O7, I/O8 - I/O15) direction control, and when active derives data from the selected memory onto the I/O bus. The AC Waveform for Read Operations illustrates read bus cycle waveforms.

OUTPUT DISABLE

With $\overline{OE}$ at a logic-high level (V_{IH}), the device outputs are disabled. Output pins (I/O0 - I/O7, I/O8 - I/O15) are placed in a high-impedance state.

STANDBY

$\overline{CE}$ at a logic-high level (V_{IH}) places the module in standby mode. Standby operation disables much of the modules circuitry and substantially reduces device power consumption. The outputs (I/O0 - I/O7, I/O8 - I/O15) are placed in a high- impedance state independent of the status of $\overline{OE}$. If each device is deselected during block erase or byte write, the device will continue functioning and consuming normal active power until the operation completes.

DEVICE IDENTIFIER OPERATION

The device identifier operation outputs the manufacturer code, 89H, and the device code, A2H, for each device. The system CPU can then automatically match the device with its proper block erase and byte write algorithms.

The manufacture and device codes are read via the Command User Interface. Following a write of 90H to the Command User Interface, a read from address location 00000H outputs the manufacturer code (89H). A read from address location 00001H outputs the device code (A2H). It is not necessary to have high voltage applied to V_{PP} to read the device identifier from the Command User Interface.

WRITE

Writes to the Command User Interface enable reading of device data and device identifier. They also control inspection and clearing of the Status Register. Additionally, when $V_{PP} = V_{PPH}$, the Command User Interface controls block erasure and byte write. The contents of the interface register serve as input to the internal write state machine.

The Command User Interface itself does not occupy an addressable memory location. The interface register is a latch used to store the command and address and data information needed to execute the command. Erase Setup and Erase Confirm commands require both appropriate command data and an address within the block to be erased. The Byte Write Setup command requires both appropriate command data and the address of the location to be written.

The Command User Interface is written by bringing $\overline{WE}$ to a logic-low level (V_{IL}) while $\overline{CE}$ is low. Addresses and data are latched on the rising edge of $\overline{WE}$. Standard microprocessor write timing are used.

Refer to AC Write Characteristics and the AC Waveforms for Write Operations, for specific timing parameters.

Table 1: BUS OPERATION

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	V_{PP}	I/O0-I/O7, I/O8-I/O15
Read [1, 2]	V_{IL}	V_{IL}	V_{IH}	X	X	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	HIGH-Z
Standby	V_{IH}	X	X	X	X	HIGH-Z
Device Identifier (Mfg.)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	89H
Device Identifier (Device)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	A2H
Write [3, 4]	V_{IL}	V_{IH}	V_{IL}	X	X	D_{IN}

NOTES:

1. Refer to DC Characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPH} for V_{PP}. See DC Characteristics for $V_{PPL} = V_{PPL}$ voltages.
3. Command writes involving block erase or byte write are only successfully executed when $V_{PP} = V_{PPH}$.
4. Refer to Command Definitions for valid D_{IN} during a write operation.

COMMAND DEFINITIONS

When V_{PPL} is applied to the V_{PP} pin, read operations from the Status Register, device identifier, or array blocks are enabled. Placing V_{PPH} on V_{PP} enables successful byte write and block erase operations as well.

Device operations are selected by writing specific commands into the Command User Interface. Table 2 defines the device.

READ ARRAY COMMAND

Upon initial device powerup the module defaults to Read Array mode. This operation is also initiated by writing FFH into the Command User Interface. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the Command User Interface contents are altered. Once the internal Write State Machine has started a block erase or byte write operation, the device will not recognize the Read Array command, until the WSM has completed it s operation. The Read Array command is functional when $V_{PP} = V_{PPL}$ or V_{PPH}.

DEVICE IDENTIFIER COMMAND

Each device contains a device identifier operation, initiated by writing 90H into the Command User Interface. Following the command write, a read cycle form address 00000H retrieves the manufacturer code of 89H. A read cycle form address 000001H returns, the device code of A2H. To terminate the operation, it is necessary to write another valid command into the register. Like the Read Array command, the device identifier command is functional when $V_{PP} = V_{PPL}$ or V_{PPH}.

READ STATUS REGISTER COMMAND

The module contains a Status Register which may be read to determine when a byte write or block erase operation is complete, and whether that operation completed successfully. The Status Register may be read at any time by writing the Read Status Register command (70H) to the Command User Interface. After writing this command, all subsequent read operations output data from the Status Register, until another valid command is written to the Command User Interface. The contents of the Status Register are latched on the falling edge of $\overline{OE}$ or $\overline{CE}$, whichever occurs last in the read cycle. $\overline{OE}$ or $\overline{CE}$ must be toggled to V_{IH} before further reads to update the Status Register latch. The Read Status Register command functions when $V_{PP} = V_{PPL}$ or V_{PPH}.

CLEAR STATUS REGISTER COMMAND

The Erase Status and Byte Write Status bits are set to "1"s by the Write State Machine and can only be reset by the Clear Status Register Command. These bits indicate various failure conditions (see Table 3). By allowing system software to control the resetting of these bits, several operations may be performed (such as cumulatively writing several bytes or erasing multiple blocks in sequence). The Status Register may then be polled to determine if an error occurred during that sequence. This adds flexibility to the way the device may be used.

Additionally, the V_{PP} Status bit (SR.3) **MUST** be reset by system software before further byte writes or block erase are attempted. To clear the Status Register, the Clear Status Register command (50H) is written to the Command User Interface. The Clear Status Register command is functional when $V_{PP} = V_{PPL}$ or V_{PPH}.

ERASE SETUP / ERASE CONFIRM COMMANDS

Erase is executed one block at a time, initiated a two-cycle command sequence. An Erase Setup command (20H) is first written to the Command User Interface, followed by the Erase Confirm command (D0H). These commands require both appropriate sequencing and an address within the block to be erased to FFH. Block preconditioning, erase and verify are all handled internally by the Write State Machine, invisible to the system. After the two-command erase sequence is written to it,

Table 2: COMMAND DEFINITION

Command	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
		Operation	Address	Data [1]	Operation	Address	Data [1]
Read Array/Reset	1	Write	X	FFH	-	-	-
device Identifier	3	Write	X	90H	Read	DA	DID
Read Status Register	2	Write	X	70H	Read	X	SRD
Clear Status Register	1	Write	X	50H	-	-	-
Erase Setup/Erase Confirm	2	Write	BA	20H	Write	BA	D0H
Erase Suspend/Erase Resume	2	Write	X	B0H	Write	X	D0H
Byte Write Setup/Write	2	Write	WA	40H	Write	WA	WD
Alternate Byte Write Setup/Write	2	Write	WA	10H	Write	WA	WD

BA = Address within the block being erased.
DA = Device Address: 00H for manufacturer code, 01H for device code.
DID = Data read from device identifiers.
SRD = Data read from Status Register (see Table 3).
WA = Address of memory location to be written.
WD = Data to be written at location WA. Data is latched on the rising edge of $\overline{WE}$.

NOTES:

1. Bus operations are defined in Table 2.
2. Following the device identifier command, two read operations access manufacturer and device codes.
3. Either 40H or 10H are recognized by WSM as the Byte Write Setup command.
4. Commands other than those shown above are reserved by Intel for future device implementations and should not be used.

the device automatically outputs Status Register data when read (see Figure 3; Block Erase Flowchart). The CPU can detect the completion of the erase event by analyzing the WSM Status bit of the Status Register.

When erase is completed, the Erase Status bit should be checked. If erase error is detected, the Status Register should be cleared. The Command Status Register should be cleared. The command User Interface remains in Read Status mode until further commands are issued to it.

This two-step sequence of set-up followed by execution ensures that memory contents are not accidentally erase. Also, reliable block erasure can only occur when $V_{PP} = V_{PPH}$. In the absence of this high voltage, memory contents are protected against erasure. If block erase is attempted while $V_{PP} = V_{PPL}$, the V_{PP} Status bit will be set to "1". Erase attempts while $V_{PPL} < V_{PP} < V_{PPH}$ produce spurious results and should not be attempted.

ERASE SUSPEND / ERASE RESUME COMMANDS

The Erase Suspend command allows block erase interruption in order to read data from another block of memory. Once the erase process starts, writing the Erase Suspend command (B0H) to the Command User Interface requests that the WSM suspend the erase sequence at a predetermined point in the erase algorithm. The module continues to output Status Register data when read, after the Erase Suspend command is written to it. Polling the WSM status and Erase Suspend status bits will determine when the erase operation has been suspended (both will be set to "1").

At this point, a Read Array command can be written to the command User Interface to read data from blocks other that that which is suspended. The only other valid commands at this time are Read Status Register (70H) and Erase Resume (D0H), at which time the WSM will continue with the erase process. The Erase Suspend status and WSM status bits of the Status Register will be automatically cleared. After the Erase Resume command is written to it, the module automatically outputs Status Register data when read (see Figure 4; Erase Suspend/Resume Flowchart). V_{PP} must remain at V_{PPH} while the module is in Erase Suspend.

BYTE WRITE SETUP / WRITE COMMANDS

Byte write is executed by a two-command sequence. The Byte Write Setup command (40H) is written to the Command User Interface, followed by a second write specifying the address and data (latched on the rising edge of $\overline{WE}$) to be written. The WSM then takes over, controlling the byte write and write verify algorithms internally. After the two-command byte write sequence is written to it, the module automatically outputs Status Register data when read (see Figure 2; Automatic Byte Write Flowchart). The CPU can detect the completion of the byte write event by analyzing the WSM status bit of the Status Register. Only the Read Status Register command is valid while byte write is active.

When byte write is complete, the Byte Write status bit should be checked. If byte write error is detected the Status Register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The Command User Interface remains in Read Status Register mode until further commands are issued to it. If byte write is attempted while $V_{PP} = V_{PPL}$, the V_{PP} Status bit will be set to "1". Byte write attempts whole $V_{PPL} < V_{PP} < V_{PPH}$ produce spurious results and should not be attempted.

AUTOMATED BYTE WRITE

The module integrates programming algorithm on-chip, using the Command User Interface, Status Register and Write State Machine (WSM). On-chip integration dramatically simplifies system software and provides processor interface timings to the Command User Interface and Status Register. WSM operation, internal verify and V_{PP} high voltage presence are monitored and reported via the appropriate Status Register bits. Figure 2 shows a system software flowchart for device byte write. The entire sequence is performed with V_{PP} at V_{PPH}. Byte write abort occurs when V_{PP} drops to V_{PPL}. Although the WSM is halted, byte data is partially written at the location where byte write was aborted. Block erasure, or a repeat of byte write, is required to initialize this data to a known value.

Table 3: STATUS REGISTER DEFINITIONS

WSMS	ESS	ES	BWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

SR.7	WRITE STATE MACHINE STATUS	1 = Ready 0 = Busy
SR.6	ERASE SUSPEND STATUS	1 = Erase Suspended 0 = Erase in Progress/Completed
SR.5	ERASE STATUS	1 = Error in Block Erase 0 = Successful Block Erase
SR.4	BYTE WRITE STATUS	1 = Error in Byte Write 0 = Successful Byte Write
SR.3	V_{PP} STATUS	1 = V_{PP} Low Detect; Operation Abort 0 = V_{PP} O.K.
SR.2 SR.1 SR.0	RESERVED FOR FUTURE ENHANCEMENTS	These bits are reserved for future use and should be masked out when polling the Status Register

NOTES:
The write State Machine Status bit must first be checked to determine byte write or block erase completion, before the Byte Write or Erase Status bit are checked for success.
If the Byte Write AND Erase Status bits are set to "1"s during a block erase attempt, an improper command sequence was entered. Attempt the operation again.
The V_{PP} Status bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates the V_{PP} level only after the byte write or block erase command sequences have been switched on. The V_{PP} Status bit is not guaranteed to report accurate feedback between V_{PPL} and V_{PPH}.

AUTOMATED BLOCK ERASE

The Erase algorithm implemented internally, including all preconditioning of block data, WSM operation, erase success and V_{PP} high voltage presence are monitored and reported through the Status Register. Additionally, if a command other than Erase Confirm is written to the device following Erase Setup, both the Erase Status and Byte Write Status bits will be set to "1"s. When issuing the Erase Setup and Erase Confirm commands, they should be written to an address within the address range of the block to be erased. Figure 3 shows a system software flowchart for block erase.

Erase typically takes 1.6 seconds per block. The Erase Suspend/Erase Resume command sequence allows suspension of this erase operation to read data from a block other that that in which erase is being performed. A system software flowchart is shown in Figure 4.

The entire sequence is performed with V_{PP} at V_{PPH}. Abort occurs when V_{PP} falls to V_{PPL} while erase is in progress. Block data is partially erased by this operation, and a repeat of erase is required to obtain a fully erased block.

POWER SUPPLY DECOUPLING

Flash memory power switching characteristics require careful device decoupling. System designers are interested in 3 supply current issues; standby current levels (I_{SB}), active current level (I_{CC}) and transient peaks produced by falling and rising edges of $\overline{CE}$. Transient current magnitudes depend on the device outputs capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 µF ceramic capacitor connected between each V_{DD} and V_{SS}, and between its V_{PP} and VSS. These high frequency, low inherent-inductance capacitors should be placed as close as possible to package leads. Additionally, a 4.7 mF electrolytic capacitor should be placed at the arrays power supply connection between V_{DD} and V_{SS}. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

V_{PP} TRACE ON PRINTED CIRCUIT BOARDS

Writing flash memories, while they reside in the target system, requires that the printed circuit board designer pay attention to the V_{PP} power supply trace. The V_{PP} pin supplies the memory cell current for writing and erasing. Use similar trace widths and layout considerations given to the V_{SS} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

V_{DD}, V_{PP}, AND THE COMMAND / STATUS REGISTERS

Byte write and block erase completion are not guaranteed if V_{PP} drops below V_{PPH}. If the V_{PP} Status bit of the Status Register (SR.3) is set to "1", a Clear Status Register command MUST be issued before further byte write/block erase attempts are allowed by the WSM. Otherwise, the Byte Write (SR.4) or Erase (SR.5) Status bits of the Status Register will be set to "1"s if an error is detected. Data will be partially altered and the command sequence must be repeated after normal operation is restored. Device poweroff will clear the Status Register to initial value 10000 for the upper 5 bits.

The Command User Interface latches commands as issued by system software and is not altered by V_{PP} or $\overline{CE}$ transitions or WSM actions. Its state upon powerup or after V_{DD} transitions below V_{LKO}, is Read Array Mode.

After byte write or block erase is complete, even after V_{PP} transitions down to V_{PPL}, the Command User Interface must be reset to Read Array mode via the Read Array command if access to the memory array is desired.

POWER UP / DOWN PROTECTION

The module is designed to offer protection against accidental block erase or byte writing during power transitions. Upon power-up, the module is indifferent as to which power supply, V_{PP} or V_{DD}, powers up first. Power supply sequencing is not required. Internal circuitry in the module ensures that the Command User Interface is reset to the Read Array mode on power up.

A system designer must guard against spurious writes for V_{DD} voltages above V_{LKO} when V_{PP} is active. Since both $\overline{WE}$ and $\overline{CE}$ must be low for a command write, driving either to V_{IH} will inhibit writes. The Command User Interface architecture provides an added level of protection since alteration of memory contents only occurs after successful completion of the two-step command sequences.

POWER DISSIPATION

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash nonvolatility increases usable battery life, because the module does not consume any power to retain code or data when the system is off.

RECOMMENDED OPERATING RANGE [2]						
Symbol	Characteristic		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
V_{PP}	Programming Voltage		11.4	12.0	12.6	V
V_{IL}	Input LOW Voltage		-0.5[3]		0.8	V
V_{IH}	Input HIGH Voltage		2.0		V_{DD}+0.5	V
T_A	Operating Temperature	C	0	+25	+70	°C
		I	-40	+25	+85	
		M/B	-55	+25	+125	
V_{ID}	A9 I.D. Input/Output		11.5		13.0	V

ABSOLUTE MAXIMUM RATINGS [7]			
Symbol	Parameter	Value	Unit
T_{STC}	Storage Temperature	-65 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{OP}	Operating Temperature	-55 to +125	°C
I_{OUT}	Output Short Circuit Current	100 [6]	mA
$V_{I/O}$	Input/Output Voltage [2]	-0.5 to +7.0 [3]	V
V_{PP}	V_{PP} Supply Voltage [2] During Erase/Program	-2.0 to +14.0 [4]	V
V_{DD}	Supply Voltage [2]	-2.0 to +7.0 [4]	V

CAPACITANCE [7]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	165	pF	V_{IN} [3] = 0V
C_{CE}	Chip Enable	15		
C_{WE}	Write Enable	165		
C_{OE}	Output Enable	165		
$C_{I/O}$	Data Input/Output	85		

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Condition	Min.	Max.	Unit
V_{OH}	HIGH Voltage	I_{OH} = -2.5mA	2.4		V
V_{OL}	LOW Voltage	I_{OL} = 5.8mA		0.45	V

DC OPERATING CHARACTERISTICS: Over operating ranges						
Symbol	Characteristics	Test Conditions		Limits Min.	Limits Max.	Unit
I_{IN}	Input Leakage Current	V_{DD} = V_{DD} max., V_{IN} = V_{DD} or V_{SS}		-16	+16	µA
I_{OUT}	Output Leakage Current	V_{DD} = V_{DD} max., V_{OUT} = V_{DD} or V_{SS}		-80	+80	µA
I_{CCS}	V_{DD} Standby Current	V_{DD} = V_{DD} max., $\overline{CE}$ = V_{IH}			32	mA
		V_{DD} = V_{DD} max., $\overline{CE}$ = V_{DD} ± 0.2V			2400	µA
I_{CCR}	V_{DD} Read Current	V_{DD} = V_{DD} max., $\overline{CE}$ = V_{IL}, f = 8MHz, I_{OUT} - 0mA TTL Inputs	x8		80	mA
			x16		130	
I_{CCW}	V_{DD} Byte Write Current	Byte Write in Progress	x8		60	mA
			x16		90	
I_{CCE}	V_{DD} Block Erase Current	Block Erase in Progress	x8		60	mA
			x16		90	
I_{CCES}	V_{DD} Erase Suspend Current	Block Erase in Suspend, $\overline{CE}$ = V_{IH}			50	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} \leq V_{DD}$		-240	+240	µA
I_{PPR}	V_{PP} Read Current	$V_{PP} > V_{DD}$			3200	µA
I_{PPW}	V_{PP} Byte Write Current	V_{PP} = V_{PPH}, Byte Write in Progress	x8		35	mA
			x16		65	
I_{PPE}	V_{PP} Block Erase Current	V_{PP} = V_{PPH}, Block Erasure in Progress	x8		35	mA
			x16		65	
I_{PPES}	V_{PP} Erase Suspend Current	V_{PP} = V_{PPH}, Block Erasure Suspended			3200	µA
V_{PPL}	V_{PP} During Normal Operations			0	6.5	V
V_{PPH}	V_{PP} Erase/Write Operations			11.4	12.6	V
I_{LKO}	V_{DD} Erase/Write Lock Voltage			2.0		V

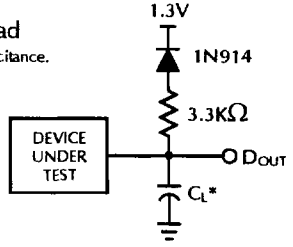
BLOCK ERASE AND BYTE WRITE PERFORMANCE			
Parameter	Min.	Max.	Unit
Block Erase Time		10	sec
Block Write Time		2.1	sec

OUTPUT LOAD		
Load	C_L	Parameters Measured
1	100 pF	except t_{DF}, t_{LZ} and t_{OLZ}
2	30pF	t_{DF}, t_{LZ} and t_{OLZ}

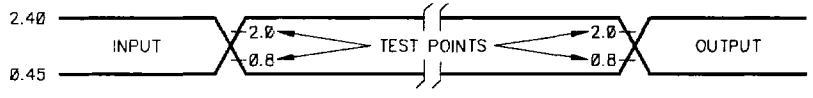
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Timing Reference Levels During Verify	0.8V and +2.4V

Figure 1. Output Load

* Including Probe and Jig Capacitance.



AC INPUT OUTPUT REFERENCE WAVEFORM

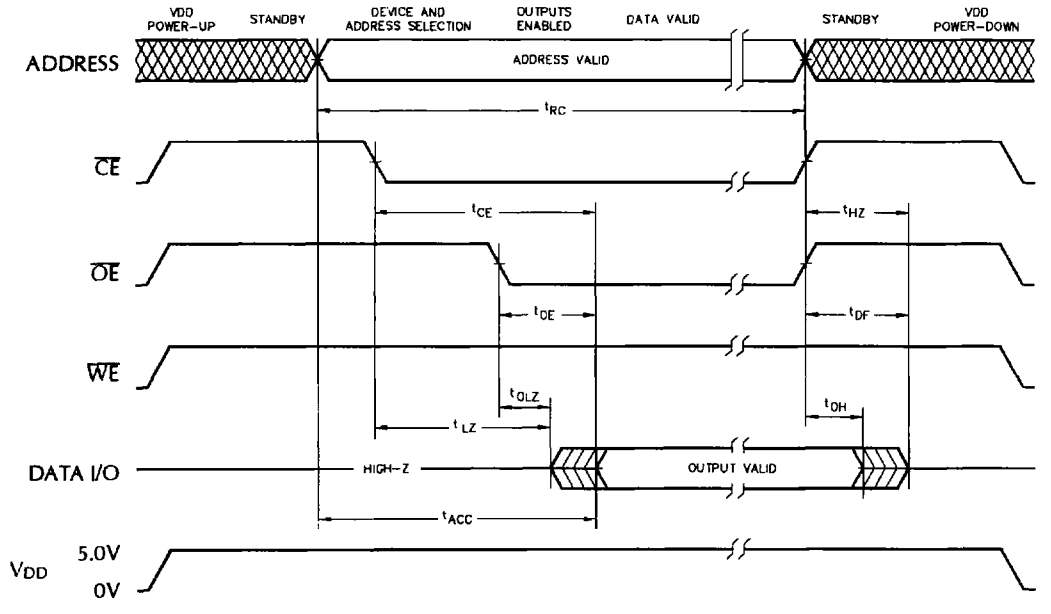


AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for Logic "1" and V_{OL} (0.45 V_{TTL}) for a Logic "0". Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to ()%) < 10ns.

AC Operating Conditions and Characteristics - Read Cycle: Over operating ranges

No.	Symbol	Parameter	90ns		100ns		120ns		150ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	90		100		120		150		ns
2	t_{ACC}	Address Access Time		90		100		120		150	ns
3	t_{CE}	Chip Enable Access Time		90		100		120		150	ns
4	t_{OE}	Output Enable Access Time		45		60		60		70	ns
5	t_{LZ}	Chip Enable to Output in LOW-Z [7,8]	0		0		0		0		ns
6	t_{HZ}	$\overline{CE}$ High to Output HIGH-Z		55		55		55		55	ns
7	t_{OLZ}	Output Enable to Output in LOW-Z [7,8]	0		0		0		0		ns
8	t_{DF}	Output Disable to Output in HIGH-Z [7,8]		30		30		30		30	ns
9	t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Change (whichever occurs first)	0		0		0		0		ns

READ CYCLE



NOTES:

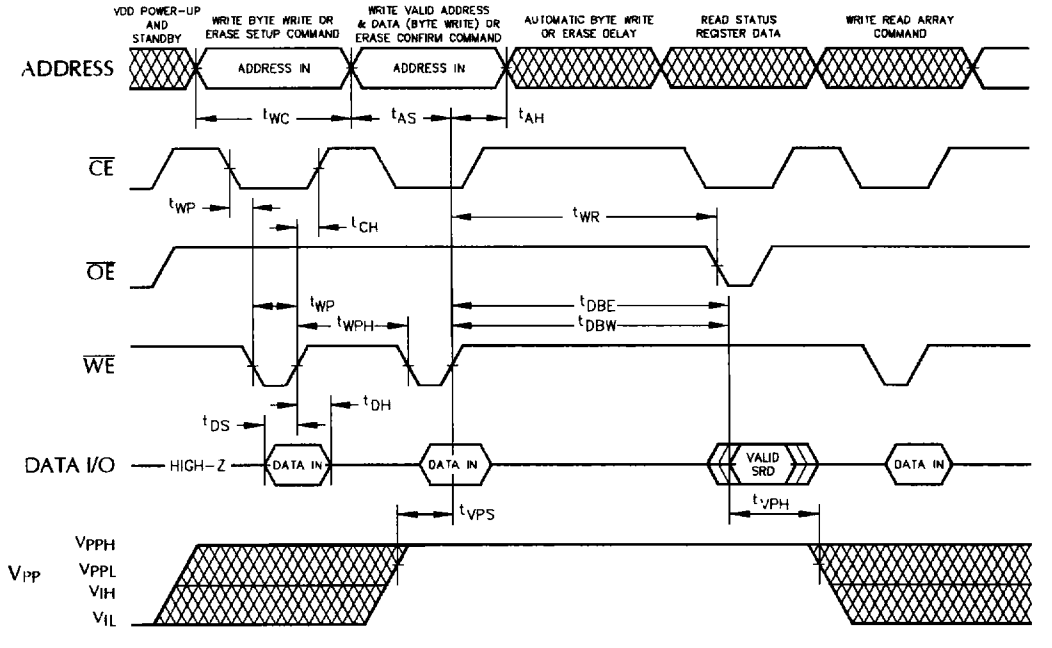
1. Each SLCC contains one FLASH memory device enabled by separate chip enables. Typically this module would be used as a x16 device with $\overline{CE}0$ and $\overline{CE}1$ tied together. When writing commands to the Command Register under these conditions, the command shown in the Command Definition Table should be duplicated to each byte (I/O0 - I/O7, I/O8 - I/O15) of the module. If the command to be written is 40H like that for Setup Program/Program, 4040H would be written to the module followed by the 16 bit data. A single device can be programmed or erased by writing the appropriate command to the device the operation is to be performed on while 00H is written to the other devices that are enabled at the same time.
   Care must be taken when doing Program Verify on a single device. Make certain that no other devices are driving the data bus of the devices that are not being verified but are enabled along with the device that is being verified. Any device that is enabled during Program Verify will be driving the data bus with the data that is programmed at that address.
2. All voltages are with respect to V_{SS}.
3. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
4. Maximum DC voltage on V_{PP} or A9 may over shoot to +14.0V for periods less than 20ns.
5. Output shorted for no more than 1 second. No more than one output shorted at a time.
6. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
7. This parameter is guaranteed and not 100% tested.
8. Transition is measured at the point of ±500mV from steady state voltage.
9. Chip Enable Controlled Writes: Write operations are driven by the valid combination of Chip Enable and Write Enable. In systems where Chip Enable defines the write pulse width *(within a longer Write Enable timing waveform)* all Set-up, Hold, and inactive Write Enable times should be measured relative to the Chip Enable waveform.

WAVEFORM KEY

AC Operating Conditions and Characteristics - Write Cycle: Over operating ranges											
No.	Symbol	Parameter	90ns		100ns		120ns		150ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t_{WC}	Write Cycle Time *	90		100		120		150		ns
11	t_{CS}	Chip Enable Setup to Write Enable Going Low	20		20		20		20		ns
12	t_{WP}	Write Pulse Width [9]	40		40		40		40		ns
13	t_{VPS}	V_{PP} Setup to Write Enable High	100		100		100		100		ns
14	t_{AS}	Address Setup Time to Write Enable High	40		40		40		40		ns
15	t_{DS}	Data Setup Time to Write Enable High	40		40		40		40		ns
16	t_{DH}	Data Hold Time from Write Enable High	5		5		5		5		ns
17	t_{AH}	Address Hold Time from Write Enable High	5		5		5		5		ns
18	t_{CH}	Chip Enable Hold from Write Enable High	10		10		10		10		ns
19	t_{WPH}	Write Pulse Width HIGH [9]	30		30		30		30		ns
20	t_{DBW}	Duration of Byte Write Operation *	6	32	6	32	6	32	6	32	µs
21	t_{DBE}	Duration of Block Erase Operation *†	0.3	10.0	0.3	10.0	0.3	10.0	0.3	10.0	sec
22	t_{WR}	Write Recovery Time before Read *‡	0		0		0		0		µs
23	t_{VPH}	V_{PP} Hold from Valid SDR *	0		0		0		0		ns

* Valid for both Write and Alternate $\overline{CE}$-Controlled Writes.
† The typical byte write time should be approximately 9µs with V_{PP} = 12.0V and T_A = 25°C.
‡ The typical block erase time should be approximately 1.6 seconds with V_{PP} = 12.0V and T_A = 25°C.

WRITE CYCLE



AC Operating Conditions and Characteristics Alternate $\overline{CE}$-Controlled Writes: Over operating ranges											
No.	Symbol	Parameter	90ns		100ns		120ns		150ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
24	t_{WS}	Write Enable Setup to Chip Enable Going Low	0		0		0		0		µs
25	t_{CP}	Chip Enable Pulse Width [9]	50		50		50		50		ns
26	t_{VPS}	V_{PP} Setup to Chip Enable High	100		100		100		100		ns
27	t_{AS}	Address Setup Time to Chip Enable High	40		40		40		40		ns
28	t_{DS}	Data Setup Time to Chip Enable High	40		40		40		40		ns
29	t_{DH}	Data Hold Time from Chip Enable High	5		5		5		5		ns
30	t_{AH}	Address Hold Time from Chip Enable High	5		5		5		5		ns
31	t_{WH}	Write Enable Hold from Chip Enable High	0		0		0		0		ns
32	t_{EPH}	Chip Enable Pulse Width HIGH [9]	25		25		25		25		ns

ALTERNATE WRITE CYCLE

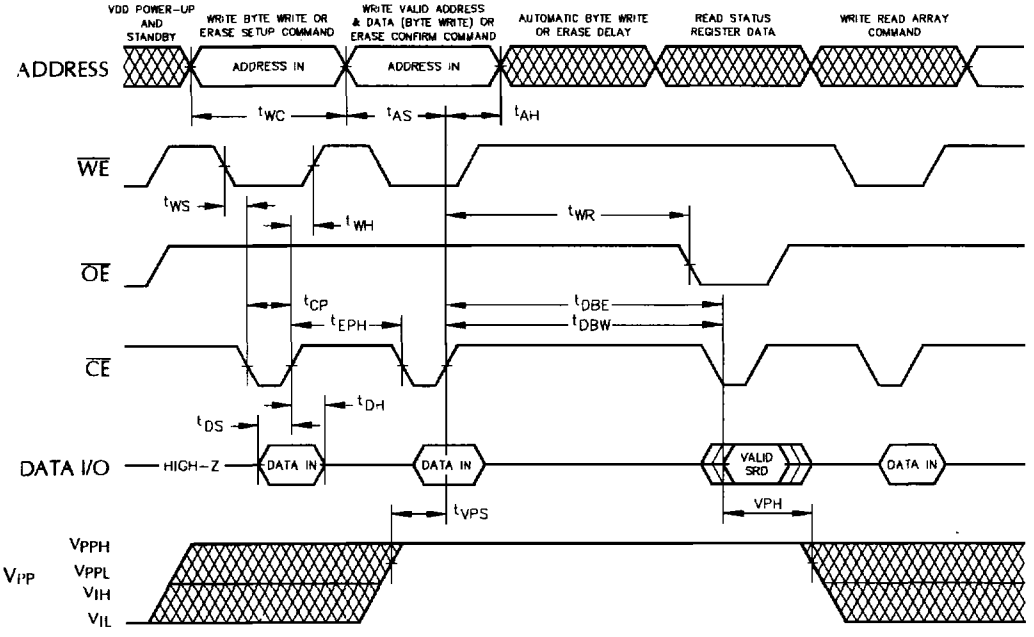
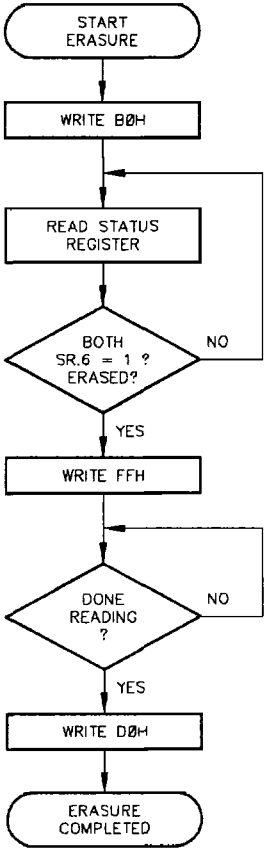
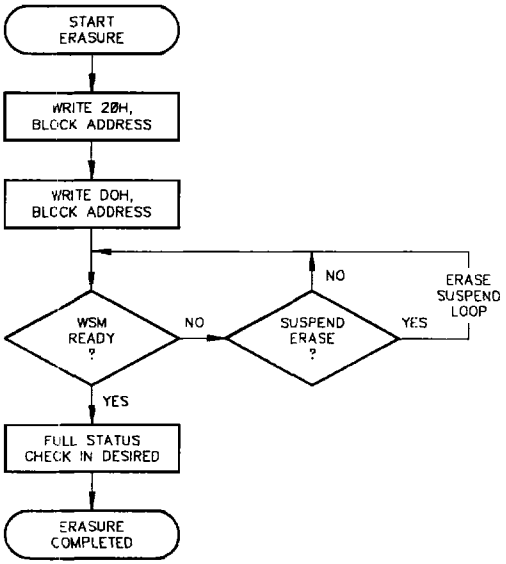


FIGURE 4: ERASE SUSPEND/RESUME FLOWCHART



Bus Operations	Command	Comments
Write	Erase Suspend	Data = B0H
Write	Read Status Register	Data = =70H
Standby/Read		Check SR.7 1 = Ready 0 = Busy Toggle $\overline{OE}$ or $\overline{CE}$ to update Status Register
Standby		Check SR.6 1 = Suspended
Write	Read Array	Date = FFH
Read		Read array data from block other than that being erased.
Write	Erase Resume	Data = D0H

FIGURE 3: AUTOMATIC BLOCK ERASE FLOWCHART

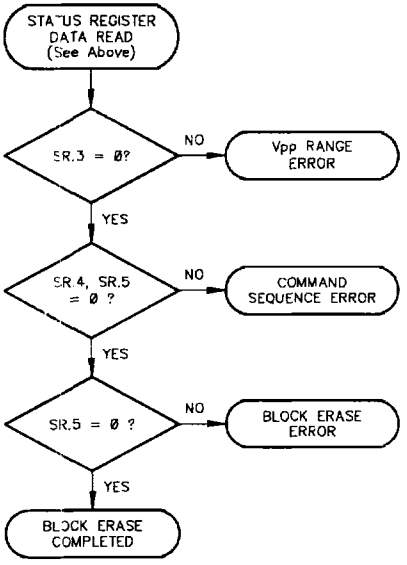


Bus Operations	Command	Comments
Write	Erase Setup	Data = 20H Address = Within block to be erased
Write	Erase	Data = =D0H Address = Within block to be erased
Standby/Read		Read Status Register Check SR.7 1 = Ready 0 = Busy Toggle $\overline{OE}$ or $\overline{CE}$ to update Status Register

Repeat for subsequence bytes.

Full status check can be done after each block or after a sequence of blocks.

Write FFH after the last block erase operation to reset the device to Read Array Mode.



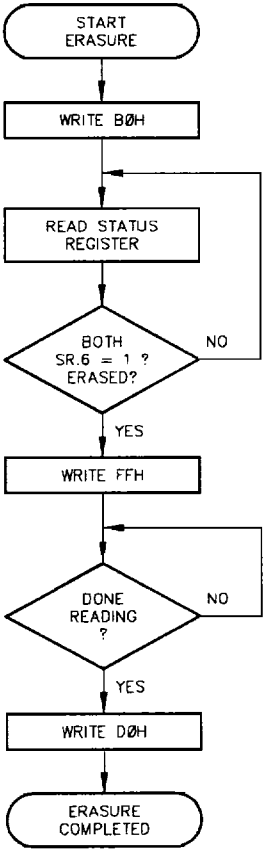
Bus Operations	Command	Comments
Optional Read		CPU may already have read Status Register data in WSM Read polling above.
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4,SRE.5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error

SR.3 MUST be cleared, if set during a Block Erase attempt, before further attempts are allowed by the Write State Machine.

SR.4 is only cleared by the Clear Status Register Command, in case where multiple block are erased before full status is checked.

If error is detected, clear the Status Register before attempting retry or other error recovery.

FIGURE 4: ERASE SUSPEND/RESUME FLOWCHART



Bus Operations	Command	Comments
Write	Erase Suspend	Data = B0H
Write	Read Status Register	Data= =70H
Standby/Read		Check SR.7 1 = Ready 0 = Busy Toggle $\overline{OE}$ or $\overline{CE}$ to update Status Register
Standby		Check SR.6 1 = Suspended
Write	Read Array	Date = FFH
Read		Read array data from block other than that being erased.
Write	Erase Resume	Data = D0H

ORDERING INFORMATION

DP Z 8M X 16 N V3 – XX X

PREFIX | TYPE | MEMORY DEPTH | DESIG | MEMORY WIDTH | DESIG | PACKAGE | SPEED | GRADE

C	COMMERCIAL	0°C to +70°C
I	INDUSTRIAL	–40°C to +85°C
M	MILITARY	–55°C to +125°C
B	MIL–PROCESSED	–55°C to +125°C

90	90ns
10	100ns
12	120ns
15	150ns

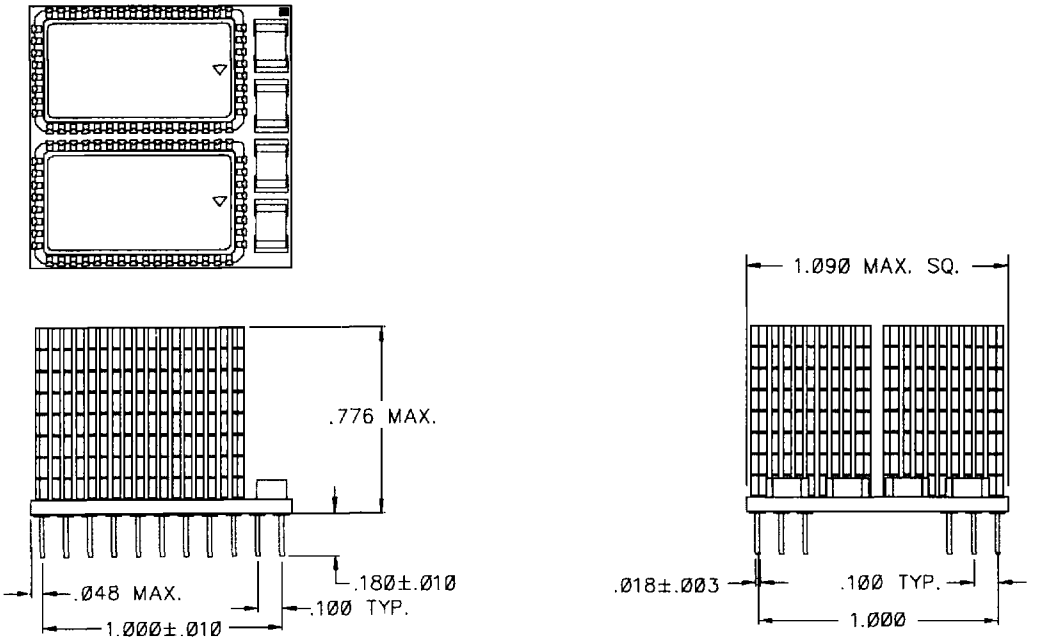
66 PIN GRID ARRAY / VERSA–STACK

8 MEGABIT BASED DEVICE

MODULE WITHOUT LOGIC SUPPORT

FLASH EEPROM

MECHANICAL DRAWING



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