TONE SQUELCH

S-7119 Series

The S-7119 Series is a CMOS LSI developed for telecommunication control devices using the CTCSS method. It servers as an encoder and a decoder of the setting tone. The tone output of 38 waves ranges from 67Hz to 250.3Hz. The tone can be set by transmitting the data in parallel to each program pin or by transmitting the data in serial to a built-in shift register. Also, two kinds of oscillation frequencies are available and can be used depending upon the frequency band width of a communication device. The S-7119 Series features low current consumption because of its CMOS configuration. A 28-pin small outline package enables customers to make portable communication systems.

■ Features

- Encoding and decoding function using the CTCSS method
- Switched-capacitor filter technology
- High-precision, high-stability tone output
- Tone output of 38 waves ranging from 67 Hz to 250.3 Hz
- A built-in tone signal eliminating filter
- 3.579545 MHz or 4.194304 MHz quartz crystal is usable
- Parallel or serial input is available for setting and controlling tone (the serial input unit is made up of 2-stage latch circuit)
- Low current consumption
  - Operating mode: 3 mA typ. (V_{DD} = 5 V)
  - Standby mode: 0.1 mA max. (V_{DD} = 5 V)
- 28-pin small outline package

■ Applications

- Portable communication devices
- Car telephones
- Professional communication systems
- Home automation devices
- Home security devices

■ Block Diagram

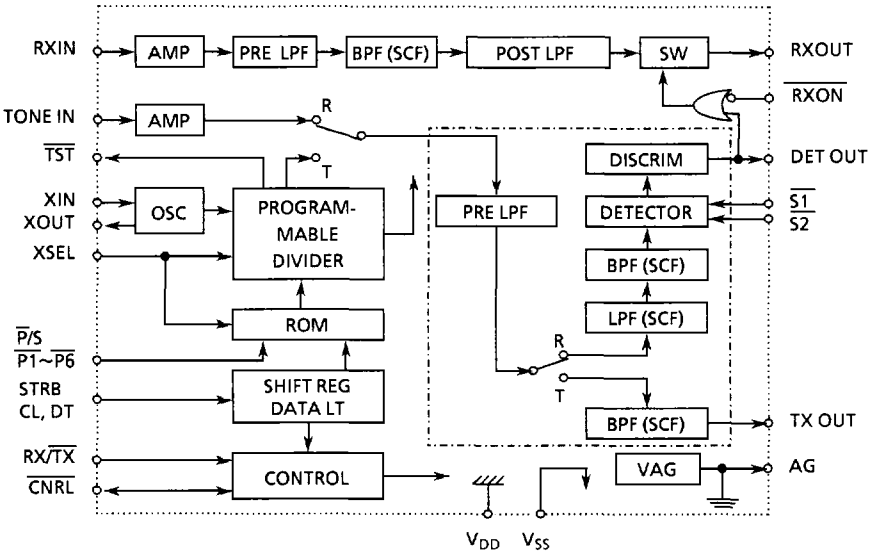


Figure 1

■ Pin Arrangement

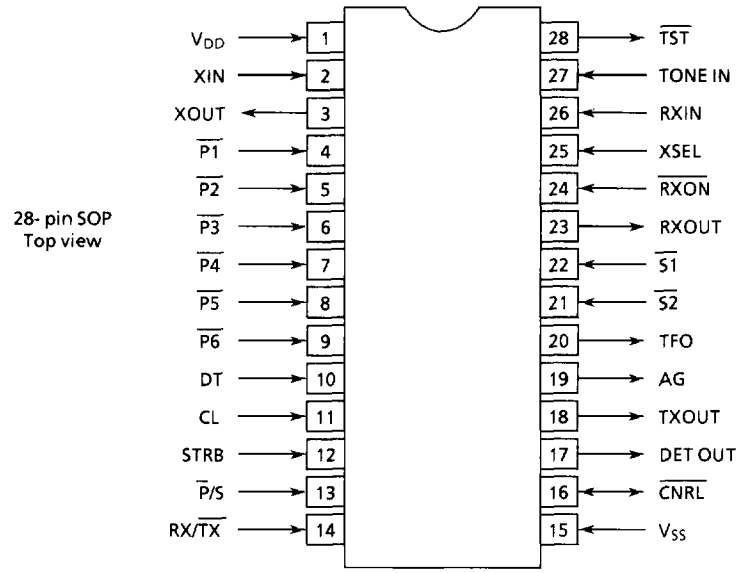


Figure 2

■ Terminal Description

Table 1

Terminal No.	Symbol	Description
1	V_{DD}	• Positive power supply terminal
2	XIN	• In- and output terminal for connecting X'tal
3	XOUT	• A X'tal of 3.579545MHz when XSEL terminal = L or a X'tal of 4.194304MHz when XSEL terminal = H is connected
4 to 9	$\overline{P1}$ to $\overline{P6}$	• Input terminal which sets tone frequency (with a built-in pull-up resistance) • A tone set by $\overline{P1}$ to $\overline{P6}$ is valid when $\overline{P/S}$ terminal is at L level
10	DT	• Input terminal which controls serial input (CMOS input)
11	CL	• DT terminal: Serial data input
12	STRB	• CL terminal: Data is written to the shift register on the rising edge of this terminal (Schmitt trigger input) • STRB terminal: The content of the shift register is latched to the data latch when this terminal is high and the content of the data latch is held when low
13	$\overline{P/S}$	• Input terminal which selects parallel input mode and serial input mode (CMOS input) • Parallel input ($\overline{CNRL}$, RX/$\overline{TX}$, and $\overline{P1}$ to $\overline{P6}$ are valid) mode when $\overline{P/S}$ is at L level; serial input (data latch is valid) mode when P/S is at H level
14	RX/$\overline{TX}$	• Input terminal which selects decode or encode of the setting tone (with a built-in pull-up resistor) • Encode mode of the setting tone when RX/$\overline{TX}$ is at L level • Decode mode of the setting tone when RX/$\overline{TX}$ is OPEN or at H level, and when $\overline{CNRL}$ terminal is at L level
15	V_{SS}	• Negative power supply terminal (usually connected to GND)
16	$\overline{CNRL}$	• Input terminal which controls operation mode when P/S is at L level (with a built-in pull-up resistor) • Serves as an output terminal when $\overline{P/S}$ is at H level, and outputs L when standby mode is selected (CMOS output)
17	DET OUT	• Output terminal which indicates the setting tone detection (CMOS output) • Becomes H when the setting tone is detected in the decode mode; is set at L in other modes
18	TXOUT	• Tone signal output terminal (CMOS output) • Outputs a transmission tone signal in encode mode; is set as AG potential in decode mode, and becomes high impedance in standby mode
19	AG	• GND terminal for analog circuit Usually generates (1/2)V_{DD}
20	TFO	• Output terminal for tests

Table 1

Terminal No.	Symbol	Description
21	$\overline{S2}$	• Input terminal which adjusts tone detection level for tone decoding (with a built-in pull-up resistor)
22	$\overline{S1}$	• $\overline{S1}$ and $\overline{S2}$ can change the minimum detect sensitivity level of the tone (see Table 6&7)
23	RXOUT	• Voice signal output terminal (tone elimination signal) • A voice signal which is entered from the RXIN terminal and out of which tone is eliminated is transmitted from this terminal when DET OUT output is high or $\overline{RXON}$ input is low ; otherwise the terminal is set at AG potential level
24	$\overline{RXON}$	• Input terminal which forces voice output (with a built-in pull-up resistor) • When $\overline{RXON}$ is at L level: the same as when DET OUT output is at H level; when $\overline{RXON}$ is OPEN or at H level, the mode is at normal level
25	XSEL	• Input terminal which selects X'tal frequency (CMOS input) • X'tal of 3.579545MHz when XSEL = L; X'tal of 4.194304MHz when XSEL = H
26	RXIN	• Analog signal (voice + tone) input terminal • Voice receiving input which is connected internally to BPF etc . to limit the signal within the voice band region
27	TONE IN	• Analog signal (voice + tone) input terminal • Tone detection input which is connected internally to LPF which passes only tone
28	$\overline{TST}$	• Output terminal for tests (Pchannel open drain output)

■ Absolute Maximum Ratings

Table 2

Ta = 25°C, V_{SS} = 0V

Parameter	Symbol	Ratings		Unit
		Min.	Max.	
Power supply voltage	V_{DD}	− 0.3	+ 6.0	V
Input voltage	V_{IN}	− 0.3	V_{DD} + 0.3	V
Output voltage	V_{OUT}	− 0.3	V_{DD} + 0.3	V
Operating ambient temperature	T_{opr}	− 30	+ 70	°C
Storage temperature	T_{stg}	− 40	+ 125	°C

■ Electrical Characteristics

** Measuring conditions

Measurement method of TXOUT, RXOUT output impedance (Ro)

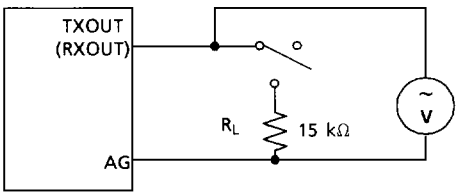


Figure 3

The following equation is obtained from Vo when load resistance (R_L) is ∞ and from Vo' when R_L is 15kΩ, :

$$V_O \cdot \frac{R_L}{R_O + R_L} = V_O'$$

$$\therefore R_O V_O' = (V_O - V_O')R_L \qquad \therefore \boxed{R_O = \frac{V_O - V_O'}{V_O'} R_L}$$

1. S-7119BF

Table 3

Unless otherwise specified, X'tal = 3.579545MHz or 4.194304MHz, $C_G = C_D = 30pF$, $V_{DD} = 5V$, $V_{SS} = 0V$, Ta = 25°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Op. power supply voltage	V_{DD}	Ta = − 30°C to + 70°C	4.5	5.0	5.5	V
Op.current consumption	I_{DDO}		−	3	8	mA
Standby current	I_{SD}	Standby mode	−	−	0.1	mA
RXIN-RXOUT frequency char.	f	RXIN = 500Hz, − 12dBm standard	−	Fig. 7	−	−
RXOUT high-wave distortion rate	D_{IS1}		−	2*	5	%
RXIN input resistance	R_{IN1}		−	1	−	MΩ
RXOUT output resistance**	R_{OUT1}	RXIN = 1kHz, − 18dBm input	−	0.8	3.2	kΩ
Maximum tone sensitive frequency deviation	$\left\|\frac{\Delta f}{f}\right\|$ max		−	−	0.5	%
Minimum tone insensitive frequency deviation	$\left\|\frac{\Delta f}{f}\right\|$ min		3.0	−	−	%
TONE IN input resistance	R_{IN2}		−	1	−	MΩ
TXOUT output resistance**	R_{OUT2}		−	0.5	2.0	kΩ
Tone detection response time	t_{ON}	162.2Hz, − 18dBm input ($\overline{S1} = \overline{S2} = L$)	−	−	200	ms
High-level input voltage	V_{IH}		$0.8 \times V_{DD}$	−	V_{DD}	V
Low-level input voltage	V_{IL}		0	−	$0.2 \times V_{DD}$	V
TXOUT transmission tone frequency deviation	$\frac{\Delta fT}{fT}$		− 0.16	−	+ 0.16	%
TXOUT transmission tone output level	V_{TX}		− 7.5	− 4.3	− 1.0	dBm
TXOUT harmonic distortion rate	D_{IS2}	Transmission tone distortion rate	−	2	5	%
TXOUT transmission tone output level deviation	dV_{TX}	Output level ratio between tone frequencies	− 0.2	−	0.2	dB
CL input hysteresis width	V_{HYS}		0.5	−	−	V
Pull-up resistance input current 1	I_{UP1}	$V_{IL} = 0V$	− 10	− 3	−	μA
Pull-up resistance input current 2	I_{UP2}	$V_{IH} = 4.5V$	−	− 10	−	μA
Input leakage current	I_{LI}	$V_{IL} = 0V$ or $V_{IH} = V_{DD}$	− 1	−	1	μA
DETOUT high level output current	I_{OH}	$V_{OH} = 4.5V$	−	− 0.3	− 0.1	mA
DETOUT low level output current	I_{OL}	$V_{OL} = 0.5V$	0.1	0.3	−	mA
$\overline{CNRL}$ high level output current	I_{OH}	$\overline{P/S} = H$, $V_{OH} = 4.5V$	−	− 0.3	− 0.1	mA
$\overline{CNRL}$ low level output current	I_{OL}	$\overline{P/S} = H$, $V_{OL} = 0.5V$	0.1	0.3	−	mA

*Excluding the clock from SCF.

Note) 0dBm = 0.775Vrms

2. S-7119CF

Table 4

Unless otherwise specified, X'tal = 3.579545MHz or 4.194304MHz, $C_G = C_D = 30pF$, $V_{DD} = 3V$, $V_{SS} = 0V$, Ta = 25°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Op. power supply voltage	V_{DD}	Ta = − 30°C to + 70°C	2.7	−	5.5	V
Op.current consumption	I_{DDO}		−	0.7	2	mA
Standby current	I_{SD}	Standby mode	−	−	0.1	mA
RXIN-RXOUT frequency char.	f	RXIN = 500Hz, − 12dBm standard	−	Fig. 7	−	−
RXOUT high-wave distortion rate	D_{IS1}		−	2*	5	%
RXIN input resistance	R_{IN1}		−	1	−	MΩ
RXOUT output resistance**	R_{OUT1}	RXIN = 1kHz, − 18dBm input	−	1.0	4.0	kΩ
Maximum tone sensitive frequency deviation	$\left\|\frac{\Delta f}{f}\right\|$ max		−	−	0.5	%
Minimum tone insensitive frequency deviation	$\left\|\frac{\Delta f}{f}\right\|$ min		3.0	−	−	%
TONE IN input resistance	R_{IN2}		−	1	−	MΩ
TXOUT output resistance**	R_{OUT2}		−	1.5	10	kΩ
Tone detection response time	t_{ON}	162.2Hz, − 18dBm input ($\overline{S1} = \overline{S2} = L$)	−	−	200	ms

*Excluding the clock from SCF.

Note) 0dBm = 0.775Vrms

Table 4

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
High-level input voltage	V_{IH}		$0.8 \times V_{DD}$	—	V_{DD}	V
Low-level input voltage	V_{IL}		0	—	$0.2 \times V_{DD}$	V
TXOUT transmission tone frequency deviation	$\frac{\Delta fT}{fT}$		−0.16	—	+0.16	%
TXOUT transmission tone output level	V_{TX}		−11.8	−8.6	−5.4	dBm
TXOUT harmonic distortion rate	D_{IS2}	Transmission tone distortion rate	—	2	5	%
TXOUT transmission tone output level deviation	dV_{TX}	Output level ratio between tone frequencies	−0.2	—	0.2	dB
CL input hysteresis width	V_{HYS}		0.3	—	—	V
Pull-up resistance input current 1	I_{UP1}	V_{IL} = 0V	−10	−1.5	—	μA
Pull-up resistance input current 2	I_{UP2}	V_{IH} = 2.5V	—	−10	—	μA
Input leakage current	I_{LI}	V_{IL} = 0V or V_{IH} = V_{DD}	−1	—	1	μA
DETOUT high level output current	I_{OH}	V_{OH} = 2.5V	—	−0.3	−0.1	mA
DETOUT low level output current	I_{OL}	V_{OL} = 0.5V	0.1	0.3	—	mA
$\overline{CNRL}$ high level output current	I_{OH}	$\overline{P/S}$ = H, V_{OH} = 2.5V	—	−0.3	−0.1	mA
$\overline{CNRL}$ low level output current	I_{OL}	$\overline{P/S}$ = H, V_{OL} = 0.5V	0.1	0.3	—	mA

■ Example of Peripheral Circuit

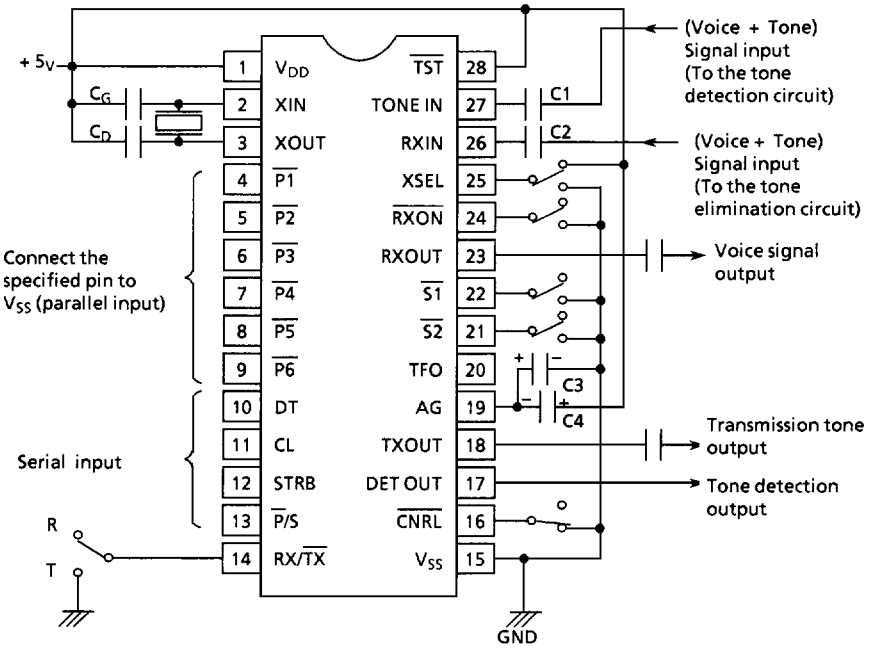
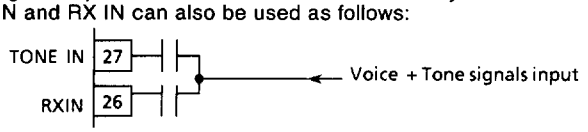


Figure 4

Notes:

1. X'tal: 3.579545MHz (when XSEL is 0V), CI ≤ 100Ω, 4.194304MHz (when XSEL is V_{DD})
2. $C_G = C_D$ = 20 to 50pF, C1 = C2 = 0.1μF, C3 = 3.3μF(2.0μF min.),C4 = 3.3μF (2.0μF min.)
3. When serial input is not used, connect pins of 10 to 13 to GND.
4. See Table 4 as to the operation mode by RX/$\overline{TX}$, $\overline{CNRL}$ terminals.
5. $\overline{S1}$ and $\overline{S2}$ are tone detection level adjustment inputs.
6. Voice signal output can be turned ON from outside by $\overline{RXON}$ terminal.
7. TONE IN and RX IN can also be used as follows:



■ Operation

1. Operation modes

Table 5

$\overline{CNRL}$, RX/$\overline{TX}$, $\overline{P}$/S, $\overline{RXON}$ inputs provide the following functions:

No.	$\overline{CNRL}$	RX/$\overline{TX}$	$\overline{P}$/S	$\overline{RXON}$	RXOUT	TXOUT	Operation mode
1	H or OPEN	H or OPEN	–	H or OPEN	AG	High impedance	Standby mode
2	–	L	–	↑	AG	Transmission tone output	Encode mode
3	L	H or OPEN	–	↑	AG or voice output	AG	Decode mode
4	–	–	L	–			Parallel input mode
5	–	–	H	–			Serial input mode
6	–	–	–	L	Voice output		Voice compulsion output mode

Note) – means "don't care."

2. Description of operations

(1) Standby mode

In the standby mode, the oscillator turns off, and the analog circuit as well as the divider also turn off. This reduces current consumption (RXOUT is at AG potential, TXOUT is at high-impedance and DETOUT is at V_{SS} potential). The standby mode also appears if the setting code of the tone frequency is not one of the values shown on Table 8.

(2) Encode mode

The encode mode is selected when RX/$\overline{TX}$ is set L level.
Pulses generated from the programmable divider according to the tone setting code pass through LPF and trasmitted from TXOUT as sine-wave tone signal.

(3) Decode mode

Tone signal is separated from signal input from TONE IN terminal through LPF and BPF for filtering the tone, and is sent to the tone detection circuit.

When the setting tone frequency is detected, DETOUT output will go H level and the voice signal will be output from RXOUT terminal (in the signal input from RXIN terminal, the tone is eliminated) (RXOUT is at AG potential unless the output is voice signal).

In case that the valid tone is successively detected over the setting number of times in the tone detection circuit, DETOUT goes H level. Tone termination is detected in case that tone is not detected over the setting number of times, and DETOUT goes L level. The minimum sensitive detection level of tone signal from TONE IN terminal can be changed by $\overline{S1}$ and $\overline{S2}$ terminals as shown on Table 6 and 7.

Table 6 Minimum tone detection sensitive levels for S-7119BF(V_{DD} = 5 V)

$\overline{S1}$ input	$\overline{S2}$ input	Minimum tone detection sensitive levels (TONE IN terminal)
H or OPEN	H or OPEN	-28dBm max.
L	H or OPEN	-33dBm max.
H or OPEN	L	-22dBm max.
L	L	-37dBm max.

Note) 0dBm = 0.755Vrms

Table 7 Minimum tone detection sensitive levels for S-7119CF(V_{DD} = 3 V)

$\overline{S1}$ input	$\overline{S2}$ input	Minimum tone detection sensitive levels (TONE IN terminal)
H or OPEN	H or OPEN	-27dBm max.
L	H or OPEN	-32dBm max.
H or OPEN	L	-21dBm max.
L	L	-36dBm max.

Note) 0dBm = 0.755Vrms

(4) Parallel input mode:

When $\overline{P}$/S is at L level, the parallel input mode is selected. $\overline{CNRL}$ and RX/$\overline{TX}$ terminals for controlling encode/decode become valid, and $\overline{P1}$ to $\overline{P6}$ terminals for setting the tone frequency become valid (see Tables 5 and 8). If any unspecified code is input from $\overline{P1}$ to $\overline{P6}$, the standby mode is selected.

(5) Serial input mode:

When $\overline{P}$/S is at H level, serial input mode is selected. Input from ($\overline{CNRL}$), (RX/$\overline{TX}$), $\overline{P1}$ to $\overline{P6}$ terminals becomes invalid and the content of the data latch (see Figure 5) becomes valid. Shift register reads and shifts DT data at the rise of CL signal. The data is latched in data latch when STRB input is at H level (see Figure 6). Shift register and data latch consist of 8 bits. The first 2 bits are for the operation mode control and successive 6 bits are for the tone setting (standby mode is selected when the received code is not one of the codes shown in Table 8).

In case that the the standby mode is selected by control bit or by tone setting bit when $\overline{P}$/S is at H level, L level is output from $\overline{CNRL}$ terminal ($\overline{CNRL}$ terminal is H level output in cases other than the standby mode). When the control bit is 00, RX/$\overline{TX}$ terminal input mode is entered and switching of decoder/encoder can be selected from RX/$\overline{TX}$ terminal (When $\overline{P}$/S = H, B8 = B7 = 0, decode mode is entered in case RX/$\overline{TX}$ = H or OPEN. The encode mode is selected in case RX/$\overline{TX}$ = L).

(6) Voice compulsion output mode:

When $\overline{RXON}$ becomes L level, voice signal will be output from RXOUT terminal irrespective of operation modes.

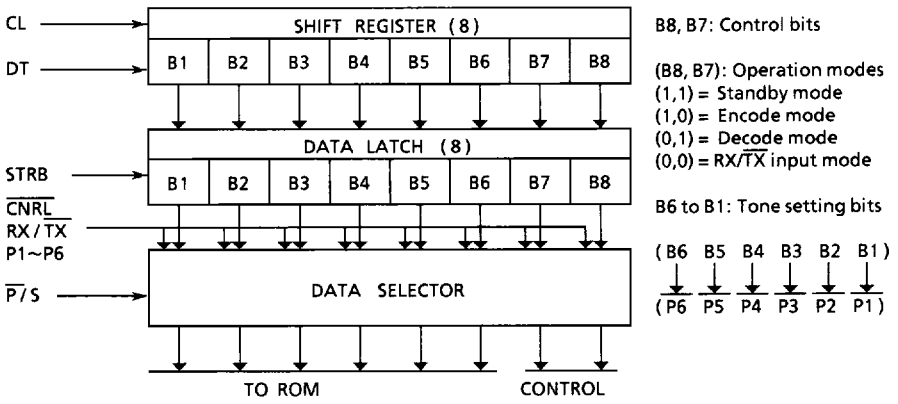
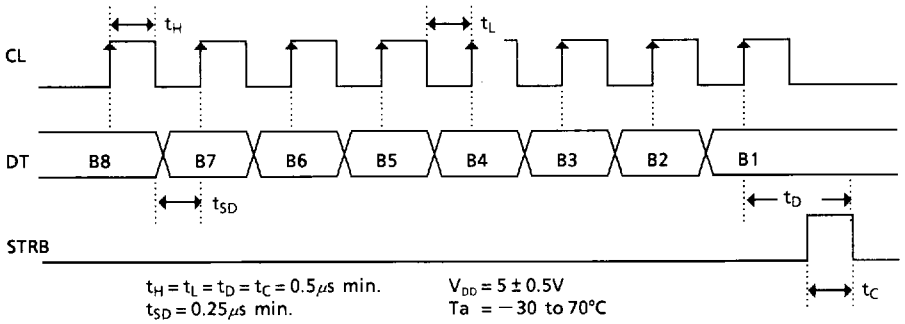


Figure 5 Serial input part block diagram



CL	↑	SHIFT
CL	↓	NO CHANGE
STRB	H	SHIFT REG → DATA LT
STRB	L	LATCHED

Figure 6 Serial input timing chart

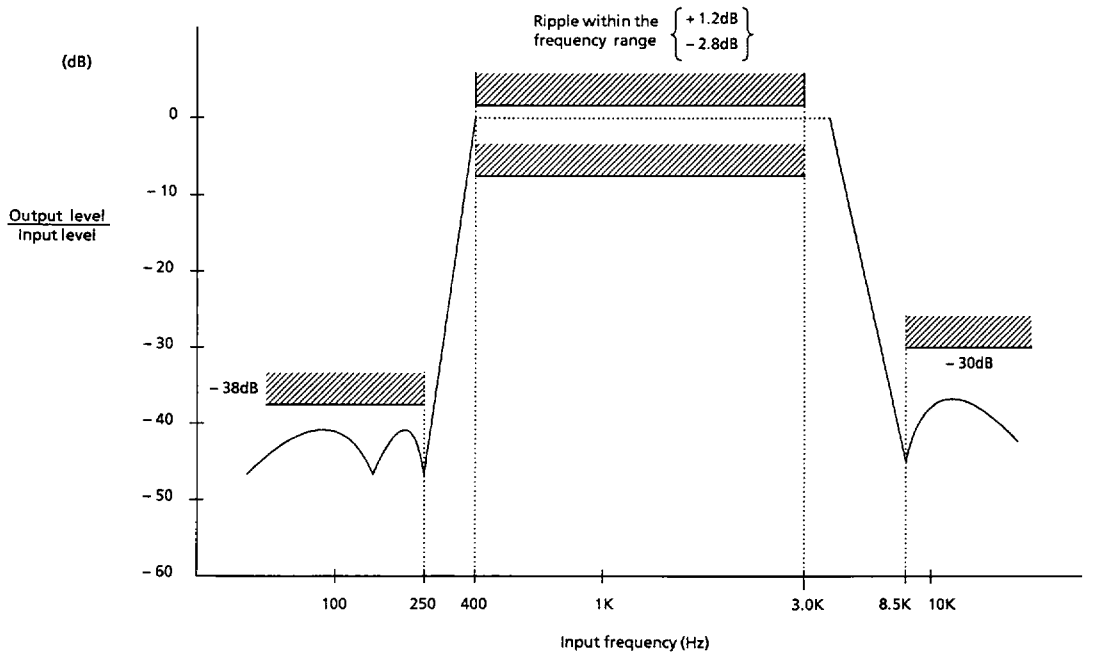


Figure 7 Frequency characteristics of RXIN-RXOUT

Table 8 Tone frequency code

Setting frequency	Decimal number	$\overline{P1}$	$\overline{P2}$	$\overline{P3}$	$\overline{P4}$	$\overline{P5}$	$\overline{P6}$	Setting frequency	Decimal number	$\overline{P1}$	$\overline{P2}$	$\overline{P3}$	$\overline{P4}$	$\overline{P5}$	$\overline{P6}$
67.0Hz	1	0	1	1	1	1	1	123.0Hz	13	0	1	0	0	1	1
	34	1	0	1	1	1	0	127.3	14	1	0	0	0	1	1
71.9	2	1	0	1	1	1	1	131.8	15	0	0	0	0	1	1
	35	0	0	1	1	1	0	136.5	16	1	1	1	1	0	1
74.4	36	1	1	0	1	1	0	141.3	17	0	1	1	1	0	1
77.0	3	0	0	1	1	1	1	146.2	18	1	0	1	1	0	1
	37	0	1	0	1	1	0	151.4	19	0	0	1	1	0	1
79.7	38	1	0	0	1	1	0	156.7	20	1	1	0	1	0	1
82.5	4	1	1	0	1	1	1	162.2	21	0	1	0	1	0	1
	39	0	0	0	1	1	0	167.9	22	1	0	0	1	0	1
85.4	40	1	1	1	0	1	0	173.8	23	0	0	0	1	0	1
88.5	5	0	1	0	1	1	1	179.9	24	1	1	1	0	0	1
	41	0	1	1	0	1	0	186.2	25	0	1	1	0	0	1
91.5	42	1	0	1	0	1	0	192.8	26	1	0	1	0	0	1
94.8	6	1	0	0	1	1	1	203.5	27	0	0	1	0	0	1
97.4	43	0	0	1	0	1	0	210.7	28	1	1	0	0	0	1
100.0	7	0	0	0	1	1	1	218.1	29	0	1	0	0	0	1
103.5	8	1	1	1	0	1	1	225.7	30	1	0	0	0	0	1
107.2	9	0	1	1	0	1	1	233.6	31	0	0	0	0	0	1
110.9	10	1	0	1	0	1	1	241.8	32	1	1	1	1	1	0
114.8	11	0	0	1	0	1	1	250.3	33	0	1	1	1	1	0
118.8	12	1	1	0	0	1	1								

Notes) 1. 0 is V_{SS} level, 1 is V_{DD} (or Open) level.
2. The decimal number is a decimal number when input data is set to a binary code of negative logic (set V_{SS} level to 1).
3. The serial input data is input in serial in the order of $\overline{P6}$ to $\overline{P1}$ from the DT terminal following control bits (2 bits) according to this code table (0 is V_{SS} level, and 1 is V_{DD} level).

■ Dimensions

1. S-7119BF(28-pin SOP)

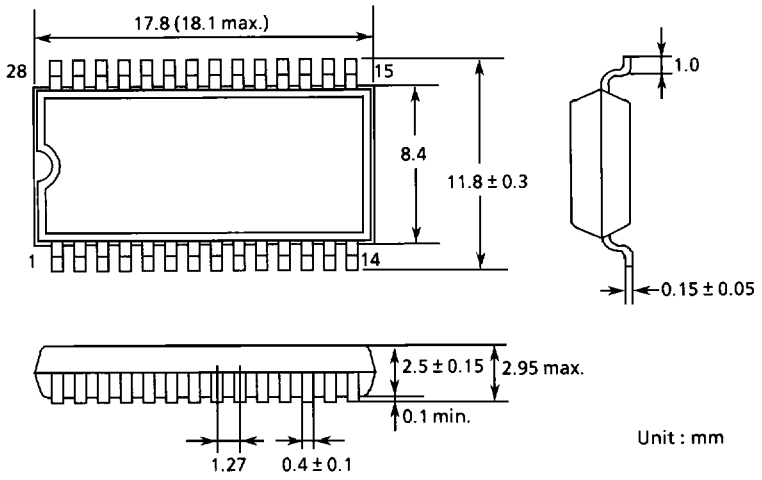


Figure7

2. S-7119CF(28-pin SOP)

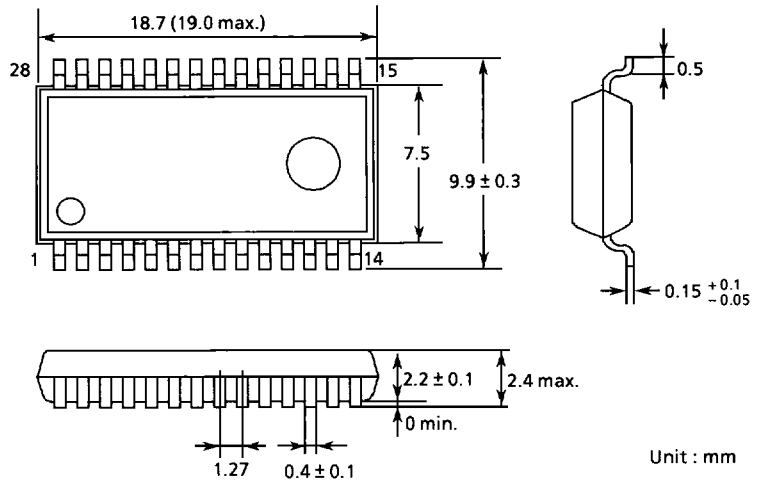


Figure8