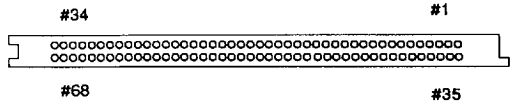
DESCRIPTION

The HYCFL001 is the Flash memory card consisting of two 5V-only 4Mbit (512Kx8) Flash memory chips in a metal plate housing. The Hyundai Flash memory card is optimized for the application of data and file storage in the portable PC and various electronic equipment market segments in which low power consumption, enhanced ruggedness, compact size and high reliability are required. The Hyundai Flash memory card complies with the 68 pin PCMCIA/JEIDA international standards to provide system functionality and compatibility. The Hyundai Flash memory card can be read and written in either x8 or x16 mode which allows for flexible integration into various application systems. The HYCFL001 has a separate 16Kbit EEPROM for attribute memory space in which OEMs can write the Card Information Structure (CIS) at their site. The Hyundai Flash memory card replicates the functions of magnetic disk based storage systems on the PCMCIA software platforms supplied by various PCMCIA software vendors including SystemSoft Corporation, Phoenix Technologies and Award Software.

FEATURES

- **Low power Dissipation (x8 mode)**
  - Max. 225mW for Read
  - Max. 325mW for Erase/Write
- **PCMCIA/JEIDA 68-pin Standard**
  - Selectable x8/x16
- **Single Power Supply of 5.0V± 5%**
  - for Read, Write and Erase
- **High Performance**
  - Max. 150ns Read Speed
- **High Write/Erase Endurance**
  - Min. 100,000 cycles
- **Write Protect Switch**
- **Seperate Attribute Memory**
  - 2 Kbyte EEPROM
- **Automatic Write and Erase Operation**
  - Typ. 1.5s 64KB Sector Erase
  - Typ. 16us Previously Erased Byte Write
- **Sector Erase Suspend/Resume**

PIN CONNECTION



PIN DESCRIPTION

$\overline{CD1}/\overline{CD2}$	Card Detect
$\overline{CE1}/\overline{CE2}$	Card Enable
$\overline{REG}$	Attribute Memory Select
A0-A25	Address Input
D0-D15	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
WP	Write Protect
$\overline{BVD1}/\overline{BVD2}$	Battery Voltage Detect
Vcc1/Vcc2	Power
Vss	Ground
NC	No Connection

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PIN NAME

PIN#	SIGNAL	I/O	FUNCTION	PIN#	SIGNAL	I/O	FUNCTION
1	Vss		Ground	35	Vss		Ground
2	D3	I/O	Data Bit 3	36	$\overline{CD1}$	O	Card Detect
3	D4	I/O	Data Bit 4	37	D11	I/O	Data Bit 11
4	D5	I/O	Data Bit 5	38	D12	I/O	Data Bit 12
5	D6	I/O	Data Bit 6	39	D13	I/O	Data Bit 13
6	D7	I/O	Data Bit 7	40	D14	I/O	Data Bit 14
7	$\overline{CE1}$	I	Card Enable	41	D15	I/O	Data Bit 15
8	A10	I	Address Bit 10	42	$\overline{CE2}$	I	Card Enable 2
9	$\overline{OE}$	I	Output Enable	43	NC		No Connect
10	A11	I	Address Bit 11	44	NC		No Connect
11	A9	I	Address Bit 9	45	NC		No Connect
12	A8	I	Address Bit 8	46	A17	I	Address Bit 17
13	A13	I	Address Bit 13	47	A18	I	Address Bit 18
14	A14	I	Address Bit 14	48	A19	I	Address Bit 19
15	$\overline{WE}$	I	Write Enable	49	NC		No Connect
16	NC		No Connect	50	NC		No Connect
17	Vcc1		Power Supply	51	Vcc2		Power Supply
18	NC		No Connect	52	NC		No Connect
19	A16	I	Address Bit 16	53	NC		No Connect
20	A15	I	Address Bit 15	54	NC		No Connect
21	A12	I	Address Bit 12	55	NC		No Connect
22	A7	I	Address Bit 7	56	NC		No Connect
23	A6	I	Address Bit 6	57	NC		No Connect
24	A5	I	Address Bit 5	58	NC		No Connect
25	A4	I	Address Bit 4	59	NC		No Connect
26	A3	I	Address Bit 3	60	NC		No Connect
27	A2	I	Address Bit 2	61	$\overline{REG}$	I	Register Select
28	A1	I	Address Bit 1	62	$\overline{BVD2}$	O	Battery Vltg Detect 2
29	A0	I	Address Bit 0	63	$\overline{BVD1}$	O	Battery Vltg Detect 1
30	D0	I/O	Data Bit 0	64	D8	I/O	Data Bit 8
31	D1	I/O	Data Bit 1	65	D9	I/O	Data Bit 9
32	D2	I/O	Data Bit 2	66	D10	I/O	Data Bit 10
33	WP	O	Write Protect	67	$\overline{CD2}$	O	Card Detect
34	Vss		Ground	68	Vss		Ground

NOTES :
I= Input to card, O= Output from card
I/O= Bi-directional
NC= No connect

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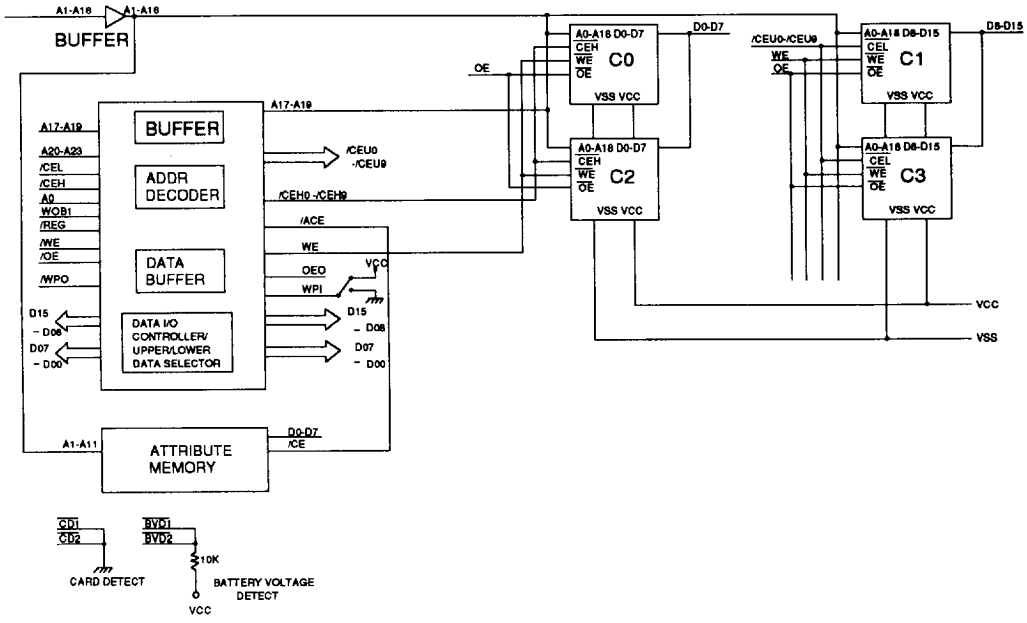
BLOCK DIAGRAM



NOTE :
1. 1MB card : C0+ C1
2. 2MB card : C0+ C1+ C2+ C3

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TRUTH TABLE : Common Memory

MODE	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	$\overline{OE}$	$\overline{WE}$	A0	D0-D7	D8-D15	NOTE
Standby	X	H	H	X	X	X	High-Z	High-Z	
READ									
x8 Read	H	H	L	L	H	L	Even Byte Data Out	High-Z	1
x8 Read	H	H	L	L	H	H	Odd Byte Data Out	High-Z	2
x8 Read	H	L	H	L	H	X	High-Z	Odd Byte Data Out	3
x16 Read	H	L	L	L	H	X	Even Byte Data Out	Odd Byte Data Out	
Output Disable	H	X	X	H	H	X	High-Z	High-Z	
WRITE									
x8 Write	H	H	L	H	L	L	Even Byte Data In	High-Z	1,4
x8 Write	H	H	L	H	L	H	Odd Byte Data In	High-Z	2,4
x8 Write	H	L	H	H	L	X	High-Z	Odd Byte Data In	3,4
x16 Write	H	L	L	H	L	X	Even Byte Data In	Odd Byte Data In	5
Output Disable	H	X	X	H	L	X	High-Z	High-Z	

NOTE :
1. Outputs or inputs the even(low) byte on D0-D7.
2. Outputs or inputs the odd(high) byte on D0-D7.
3. Outputs or inputs the odd(high) byte on D8-D15.
4. Refer to Table 1,2
5. Refer to Table 3

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TRUTH TABLE : Attribute Memory

MODE	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	$\overline{OE}$	$\overline{WE}$	A0	D0-D7	D8-D15	NOTE
Standby	X	H	H	X	X	X	High-Z	High-Z	
READ									
x8 Read	L	H	L	L	H	L	Even Byte Data Out	High-Z	
x8 Read	L	H	L	L	H	H	Not Valid	High-Z	1
x8 Read	L	L	H	L	H	X	High-Z	Not Valid	1
x16 Read	L	L	L	L	H	X	Even Byte Data Out	Not Valid	1
Output Disable	L	X	X	H	H	X	High-Z	High-Z	
WRITE									
x8 Write	L	H	L	H	L	L	Even Byte Data In	High-Z	
x8 Write	L	H	L	H	L	H	High-Z	High-Z	
x8 Write	L	L	H	H	L	X	High-Z	High-Z	
x16 Write	L	L	L	H	L	X	Even Byte Data In	High-Z	
Output Disable	L	X	X	H	L	X	High-Z	High-Z	

NOTE :
1. Only even(low) byte data is valid during Attribute Memory Read Operation.

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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 55	C
TSTG	Storage Temperature	- 20 to 65	C
VIN	Input Voltage on Any Pin Relative to Vss	-2.0 to 7.0	V
VOUT	Output Voltage on Any Pin Relative to Vss	-2.0 to 7.0	V
VCC	Voltage on Vcc Relative to Vss	- 0.5 to 6.0	V
IOS	Short Circuit Output Current	40	mA

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

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DC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	MAX.	UNIT	NOTE
I_{LI}	Input Leakage Current	V_{CC}= V_{CC}+ 1.0 $V_{SS} \leq V_{IN} \leq V_{CC}$		-300 -20	20	µA	
I_{LO}	Output Leakage Current	V_{CC}= V_{CC}+ 1.0 $V_{SS} \leq V_{OUT} \leq V_{CC}$			20	µA	
I_{CC1}	V_{CC} Supply Current, Read		x8		45	mA	1
			x16		90		
I_{CC2}	V_{CC} Supply Current, Erase/Write		x8		65	mA	1
			x16		130		
I_{CC3}	V_{CC} Supply Current, CMOS Standby		1MB		0.7	mA	
V_{OL}	Output Low Voltage	I_{OL}= 3.2mA			0.4	V	
V_{OH}	Output High Voltage	I_{OH}= 2.0mA		3.8	V_{CC}	V	
V_{LKO}	Low V_{CC} Lock-Out Voltage			3.2	4.2	V	

NOTE :
1. One Flash device active for x8, two Flash devices active for x16, all the others are in standby.

CAPACITANCE

(TA= 25C, V_{CC}= 5V± 5%, V_{SS}= 0V, f= 1MHz, unless otherwise noted)

SYMBOL	PARAMETER	MAX.	UNIT
C_{IN1}	Input Capacitance (All pin except A1-A9)	31	pF
C_{IN2}	Input Capacitance (A1-A9)	45	pF
C_{OUT}	Output Capacitance	31	pF
CD	Data Input/Output Capacitance (D0-D15)	31	pF

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AC CHARACTERISTICS

(TA= 0C to 55C, Vcc= 5V ± 5%, Vss= 0, unless otherwise noted)

#	SYMBOL	PARAMETER	HYCFL001 -150 MIN.	HYCFL001 -150 MAX.	UNIT	NOTE
	READ OPERATION					
1	tRC	Random Read Cycle Time	150		ns	
2	tAA	Address Access Time		150	ns	
3	tCE	Chip Enable Access Time		150	ns	
4	tOE	Output Enable to Output Valid		75	ns	
5	tCLZ	Chip Enable to Low-Z Output	5		ns	
6	tOLZ	Output Enable Low-Z Output	5		ns	
7	tCDF	Chip Disable to High-Z Output		75	ns	
8	tODF	Output Disable to High-Z Output		75	ns	
9	tOH	Output Hold From Address Change	5		ns	
	WRITE/ERASE OPERATIONS					
10	tWC	Write Cycle Time	150		ns	
11	tAS	Address Set-Up Time	20		ns	
12	tAH	Address Hold Time	55		ns	
13	tDS	Data Set-Up Time	50		ns	
14	tDH	Data Hold Time	20		ns	
15	tWR	Write Recovery Time Before Read	6		ns	
16	tCS	Chip Enable Set-Up Time	0		ns	
17	tCH	Chip Enable Hold Time	20		ns	
18	tWP	Write Pulse Width	45		ns	

	WRITE/ERASE OPERATIONS : $\overline{CE}$ Controlled					
10-1	tWC	Write Cycle Time	150		ns	
11-1	tAS	Address Set-Up Time	20		ns	
12-1	tAH	Address Hold Time	55		ns	
13-1	tDS	Data Set-Up Time	50		ns	
14-1	tDH	Data Hold Time	20		ns	
15-1	tOE	Output Enable Hold Time	20		ns	
16-1	tWS	Write Enable Set-Up Time Before $\overline{CE}$	0		ns	
17-1	tWH	Write Enable Hold Time	0		ns	
18-1	tCP	Chip Enable Pulse Width	65		ns	

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Table 1. Command Sequence : Even Byte

Command Sequence	Bus Cycle Req'd	1st Write Cycle		2nd Write Cycle		3rd Write Cycle		4th Read/Write Cycle		5th Write Cycle		6th Write Cycle	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Reset/Read	4	AAAAH	AAH	5554H	55H	AAAAH	F0H	RA	RD				
Autoselect	4	AAAAH	AAH	5554H	55H	AAAAH	90H	00H/02H	01H/A4H				
Byte Write	4	AAAAH	AAH	5554H	55H	AAAAH	A0H	PA	PD				
Segment Erase	6	AAAAH	AAH	5554H	55H	AAAAH	80H	AAAAH	AAH	5554H	55H	AAAAH	10H
Sector Erase	6	AAAAH	AAH	5554H	55H	AAAAH	80H	AAAAH	AAH	5554H	55H	SA	30H
Sector Erase Suspend		Add = X, Data = B0H											
Sector Erase Resume		Add = X, Data = 30H											

MEMORY CARD OPERATIONS

HYCFL001 is organized as an array of 512Kbit x 8 Flash memory devices. Each device has eight 64Kbyte sectors. Each device defines a logical address segment size.

Byte-wide erase operations could be executed in 4 ways :
- in increments of the segment size
- in increments of the sectors in individual segments
- all eight sectors in parallel within individual segments
- setected sectors of eight sectors within individual segments

When an additional Icc current is supplied to the device, multiple segments can be erased simultaneously. Once a memory sector or segment is erased, any address location within the sector or segment can be programmed. Programming operations can only convert data bit "1" to data bit "0". The only way to convert data bit "0" to data bit "1" is to erase the whole 64Kbyte sector or 512Kbyte segment. The erase operation can be performed only in the sector unit in Flash Memory.

HYCFL001 contains two seperate memory spaces, common memory space and attribute memory space. The data in the common memory space can be altered in a similar way as an individual Flash device. On-Card address and data buffers activate the appropriate Flash device in Flash memory array. Each device internally latches the address and data during write operation. See Truth Table : Common Memory.

Attribute memory space can be activated with $\overline{REG}$ pin driven low. The Card Information Structure (CIS) is stored in attribute memory and CIS describes the card's capability and specification. Hyundai Flash Card has seperate 16Kbit EEPROM for attriute memory. CIS is stored in attribute memory space and starts from address 00000H. Only D0-D7 are active during attribute memory access and D8-D15 are ignored. Odd order bytes output invalid data. See Truth Table : Attribute Memory.

Word-Wide Operations

HYCFL001 can be operated either in byte-wide or word-wide mode. In word-wide mode the Low byte (D0-D7) is activated when $\overline{CE1}$ is low and A0 is low. The high byte (D8-D15) is activated when $\overline{CE2}$ is low and A0 is Don't Care.

Byte-Wide Operations

Byte-wide data is available for read and write on D0-D7 when $\overline{CE1}$ is low and $\overline{CE2}$ is high. Even and odd bytes are stored in separate memory segments, C0 and C1. Even bytes are accessed when A0 is low and odd bytes are accessed when A0 is high. In byte-wide mode Erase operation performs the data multiplexing on D0-D7 by changing the state of A0. Each memory sector or segment pair is addressed seperately for Erase operations.

Card Detection

Each $\overline{CD}$ pin should be read by the host system to see if the memory card is inserted correctly. $\overline{CD1}$ and $\overline{CD2}$

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Table 2. Command Sequence : Odd Byte

Command Sequence	Bus Cycle Req'd	1st Write Cycle		2nd Write Cycle		3rd Write Cycle		4th Read/Write Cycle		5th Write Cycle		6th Write Cycle	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Reset/Read	4	AAABH	AAH	5555H	55H	AAABH	F0H	RA	RD				
Autoselect	4	AAABH	AAH	5555H	55H	AAABH	90H	00H/02H	01H/A4H				
Byte Write	4	AAABH	AAH	5555H	55H	AAABH	A0H	PA	PD				
Segment Erase	6	AAABH	AAH	5555H	55H	AAABH	80H	AAABH	AAH	5555H	55H	AAABH	10H
Sector Erase	6	AAABH	AAH	5555H	55H	AAABH	80H	AAABH	AAH	5555H	55H	SA	30H
Sector Erase Suspend		Add = X, Data = B0H											
Sector Erase Resume		Add = X, Data = 30H											

are internally tied to ground. If both bits are not detected, the system should indicate that the card must be re-inserted.

Write Protection

The Hyundai Flash memory card incorporates three types of protection for accidental data write. The first type is provided by the PCMCIA/JEIDA socket itself. In order to protect the card by appropriate power supply sequencing during hot insertion and removal, the power supply pin and control pin have specific pin lengths. The second type of protection is provided by the mechanical write protect switch. When this switch is activated, $\overline{WE}$ is forced high and Flash Command Register cannot receive any write commands. The third type is achieved when V_{CC1} and V_{CC2} are below V_{LKO}(Lock Out Voltage). Each Flash memory device will reset the command register to read mode when input voltage is below V_{LKO}.

MEMORY CARD BUS OPERATIONS

Read Enable

Memory card has two $\overline{CE}$(Card Enable) pins. Both $\overline{CE}$ pins must be active low in word-wide read access. In case of byte-wide access one $\overline{CE}$ pin is activated. $\overline{CE}$ pins control the selection between high and low byte memory segments and gates the power. $\overline{OE}$(Output Enable) controls the gating of data accessed from memory segment outputs. The Flash memory device automatically powers up at the read/reset state. In this case, command sequence is not needed to read data. Standard microprocessor read cycles retrieve array data. This default value ensures no memory content is altered during power transition. See AC Characteristics and Timing diagrams.

Output Disable

Data outputs from the card are disabled when $\overline{OE}$ is at a logic level high. In this condition, outputs are in the high-impedance state.

Standby Operations

Byte-wide read accesses activate half of the read/write output buffer(x16). In addition, only one memory segment is active between high and low order banks. Activating half of the output buffer is controlled by appropriate combinations of two $\overline{CE}$. $\overline{CE}$ pin controls the power to the high and low order banks of the memory. Outputs of the memory bank which is not selected are in the high impedance state. Individual memory segment is activated by address decoders. The other memory segments are in standby condition. Active memory segments keep drawing power until current write or erase operations are completed if the card is deselected during these operations.

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Table 3. Command Sequence : Word

Command Sequence	Bus Cycle Req'd	1st Write Cycle		2nd Write Cycle		3rd Write Cycle		4th Read/Write Cycle		5th Write Cycle		6th Write Cycle	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Reset/Read	4	AAAAH	AAAA	5554H	5555	AAAAH	F0F0	RA	RW				
Autoselect	4	AAAAH	AAAA	5554H	5555	AAAAH	9090	00H/02H	0101/A4A4				
Word Write	4	AAAAH	AAAA	5554H	5555	AAAAH	A0A0	PA	PW				
Segment Erase	6	AAAAH	AAAA	5554H	5555	AAAAH	8080	AAAAH	AAAA	5554H	5555	AAAAH	1010
Sector Erase	6	AAAAH	AAAA	5554H	5555	AAAAH	8080	AAAAH	AAAA	5554H	5555	SA	3030
Sector Erase Suspend		Add = X, Data = B0H											
Sector Erase Resume		Add = X, Data = 30H											

Autoselect Operation

Host system or external card reader/writer can read manufacturer and device ID codes from the card. Codes are available by writing 90H command to the command register of the memory segment. See Tables 1 and 2. Reading from address 00000H in any memory segment provides manufacturer ID while from 00002H provides device ID. Autoselect operation can be completed only after writing read/reset command sequences to the register.

Write Operation

Write and erase operations can be performed when V_{CC1} and V_{CC2} are above 4.75V. This activates state machines of addressed memory segments. Command register is a latch which saves addresses, commands and data informations used by state machine and memory array. When $\overline{WE}$ and $\overline{CE}$ are at low, and $\overline{OE}$ is at high, the command register is enabled for write operations. The falling edge of $\overline{WE}$ latches address information and the rising edge of $\overline{WE}$ latches data/command information. Write or erase operation is performed by writing appropriate data patterns to the command registers of accessed Flash memory sectors or segments. See Table 1, 2 and 3.

WORD-WIDE PROGRAMMING AND ERASING

Word-Wide Programming

See Table 3. Word write command is A0A0H. Each byte is independently programmed.

Word-Wide Erasing

Word-Wide erasing of memory segment pairs is similar to the word-wide programming. Erase word command is six bus cycle command sequence. Each byte is independently erased and verified. Each Flash memory device in the card is erased at different speeds. Therefore each device(byte) should be verified independently.

CARD INFORMATION STRUCTURE

Hyundai Flash memory card contains seperate 2Kbyte EEPROM for Card Information Structure(CIS). 2Kbyte can be used for attribute memory space of memory card. This allows all of the Flash memory in the card to be used for the common memory space.

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Table 4. Memory Sector Address Table for Memory Segment C0

	A18	A17	A16	Address Range
SA0	0	0	0	00000H-0FFFFH
SA1	0	0	1	10000H-1FFFFH
SA2	0	1	0	20000H-2FFFFH
SA3	0	1	1	30000H-3FFFFH
SA4	1	0	0	40000H-4FFFFH
SA5	1	0	1	50000H-5FFFFH
SA6	1	1	0	60000H-6FFFFH
SA7	1	1	1	70000H-7FFFFH

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Table 5. HYCFL001 CIS (TUPLE) DATA

ADDRESS	VALUE	DESCRIPTION	REMARK	ADDRES	VALUE	DESCRIPTION	REMARK
00H	01H	CISTPL_DEVICE		54H	6FH	o	
02H	03H	TPL_LINK		56H	6EH	n	
04H	53H	FLASH 150ns		58H	69H	i	
06H	0DH	1MB	CARD SIZE	5AH	63H	c	
08H	FFH	END OF DEVICE		5CH	73H	s	
0AH	17H	CISTPL_DEVICE_A	ATTRIBUTE MEMORY	5EH	20H	SPACE	
0CH	04H	TPL_LINK		60H	43H	C	
0EH	47H	EEPROM		62H	6FH	o	
10H	22H	150ns	SPEED	64H	2EH	.	
12H	39H	16Kb (2K X 8)	SIZE	66H	2CH	,	
14H	FFH	END OF DEVICE		68H	4CH	L	
16H	18H	CISTPL_JEDEC_C	FLASH DEVICE	6AH	74H	t	
18H	03H	TPL_LINK		6CH	64H	d	
1AH	04H	FUJITSU-ID		6EH	2EH	.	
1CH	A4H	MBM29F040A-ID		70H	00H	END TXT	
1EH	FFH	END OF DEVICE		72H	31H	1	
20H	1EH	CISTPL DEVICEGEO		74H	40H	M	
22H	06H	TPL_LINK		76H	42H	B	
24H	02H	DGTPL_BUS	BUS WIDTH= 2BYTE	78H	20H	SPACE	
26H	11H	DGTPL_EBS	64K ERASE SIZE	7AH	46H	F	
28H	01H	DGTPL_RBS	1 BYTE READ SIZE	7CH	4CH	L	
2AH	01H	DGTPL_WBS	1 BYTE WRITE SIZE	7EH	41H	A	
2CH	01H	DGTPL_PART	PARTITION= 1	80H	53H	S	
2EH	01H	DGTPL_HWIL	NO INTERLEAVE	82H	48H	H	
30H	15H	CISTPL VERS 1		84H	20H	SPACE	
32H	37H	TPL_LINK		86H	43H	C	
34H	04H	TPLLVI MAJOR		88H	41H	A	
36H	00H	TPLLVI MINOR		8AH	52H	R	
38H	48H	H		8CH	44H	D	
3AH	79H	y		8EH	20H	SPACE	
3CH	75H	u		90H	48H	H	
3EH	6EH	n		92H	59H	Y	
40H	64H	d		94H	43H	C	
42H	61H	a		96H	46H	F	
44H	69H	i		98H	4CH	L	
46H	20H	SPACE		9AH	30H	0	
48H	45H	E		9CH	30H	0	
4AH	6CH	l		9EH	31H	1	
4CH	65H	e		A0H	00H	END TXT	
4EH	63H	c		A2H	FFH	END OF LIST	
50H	74H	t		A4H			
52H	72H	r		A6H			
				A8H			

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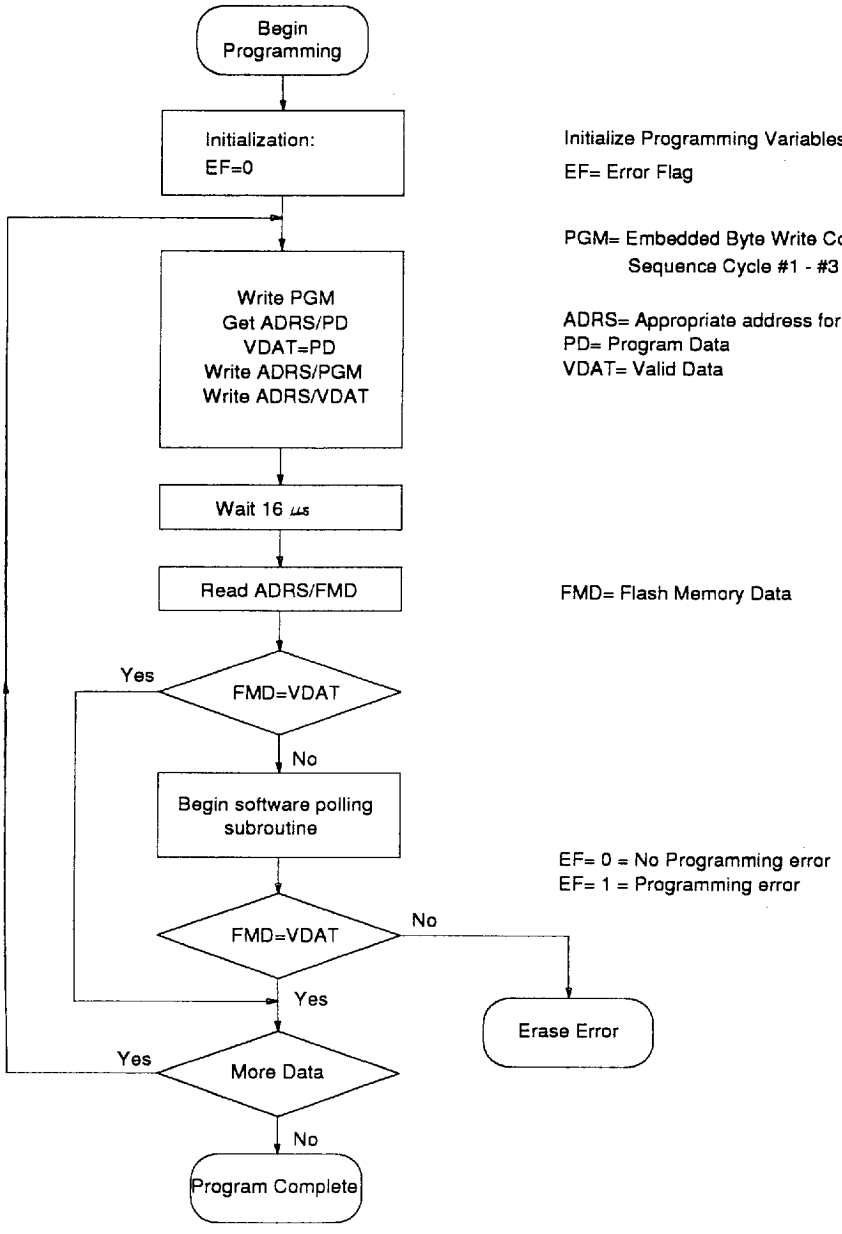

Figure 1. Byte-Wide Programming Flow Chart

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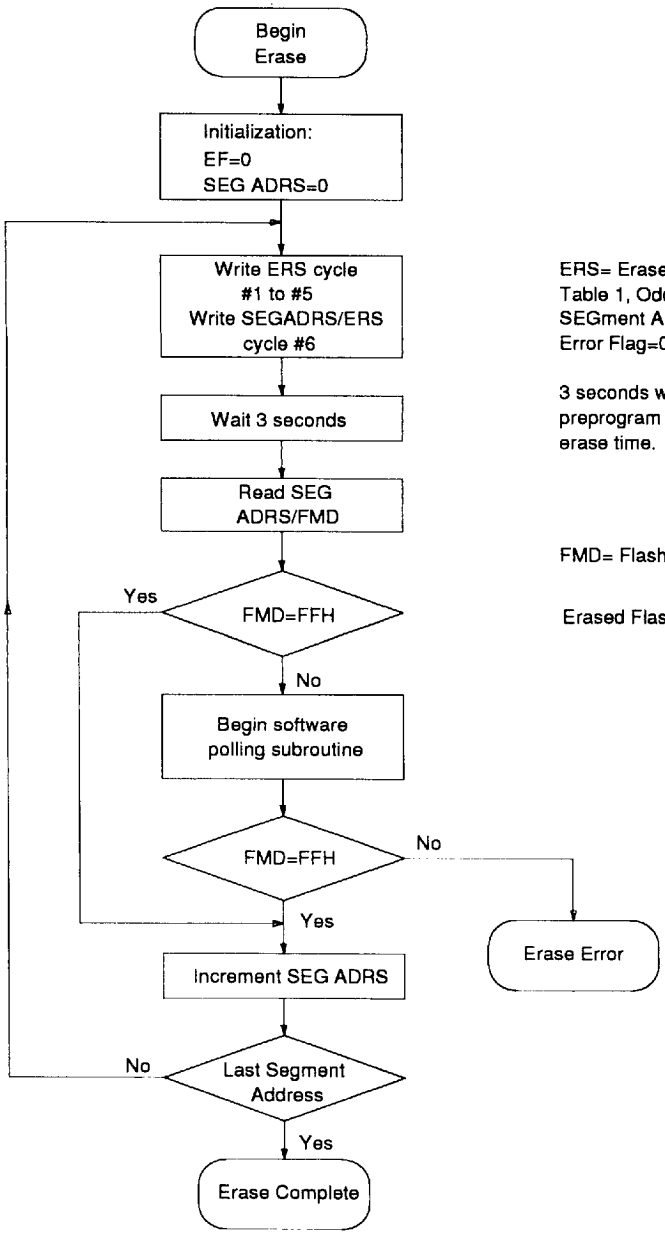

Figure 2. Byte-Wide Erasure Flow Chart

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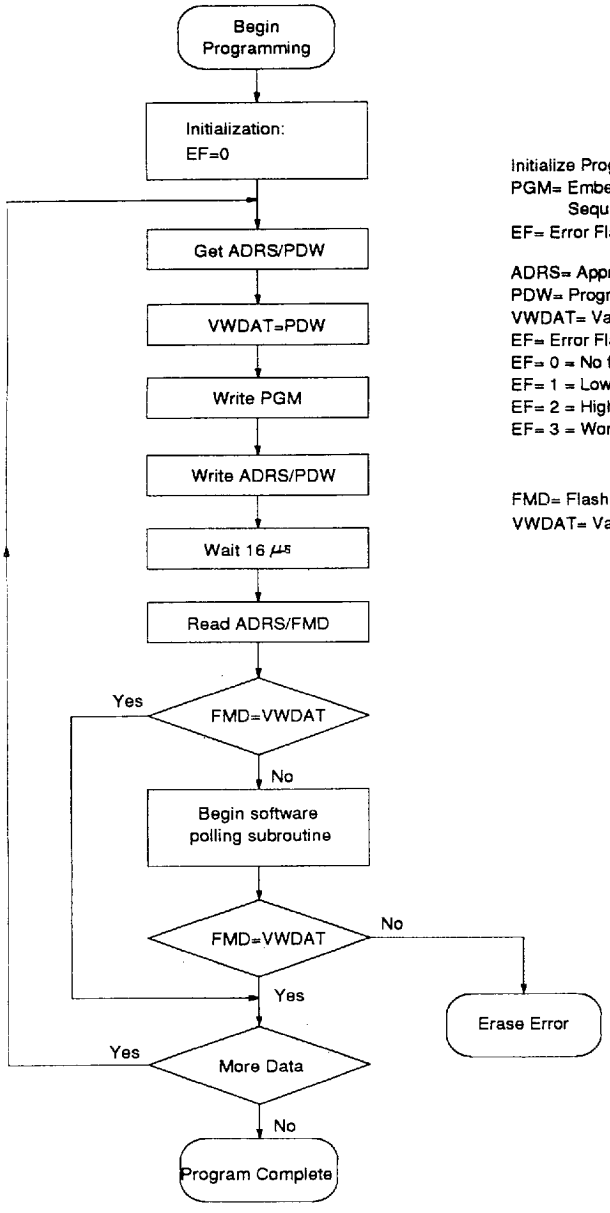

Initialize Programming Variables:
PGM= Embedded Word Write Command
Sequence Cycle #1 - #3 (Table 3)
EF= Error Flag

ADRS= Appropriate address for Memory Segment (Cycle #4)
PDW= Program Data Word
VWDAT= Valid Word Data
EF= Error Flag
EF= 0 = No failure
EF= 1 = Low byte program error
EF= 2 = High byte program error
EF= 3 = Word-wide program error

FMD= Flash Memory Data
VWDAT= Valid Word Data

Figure 3. Word-Wide Programming Flow Chart

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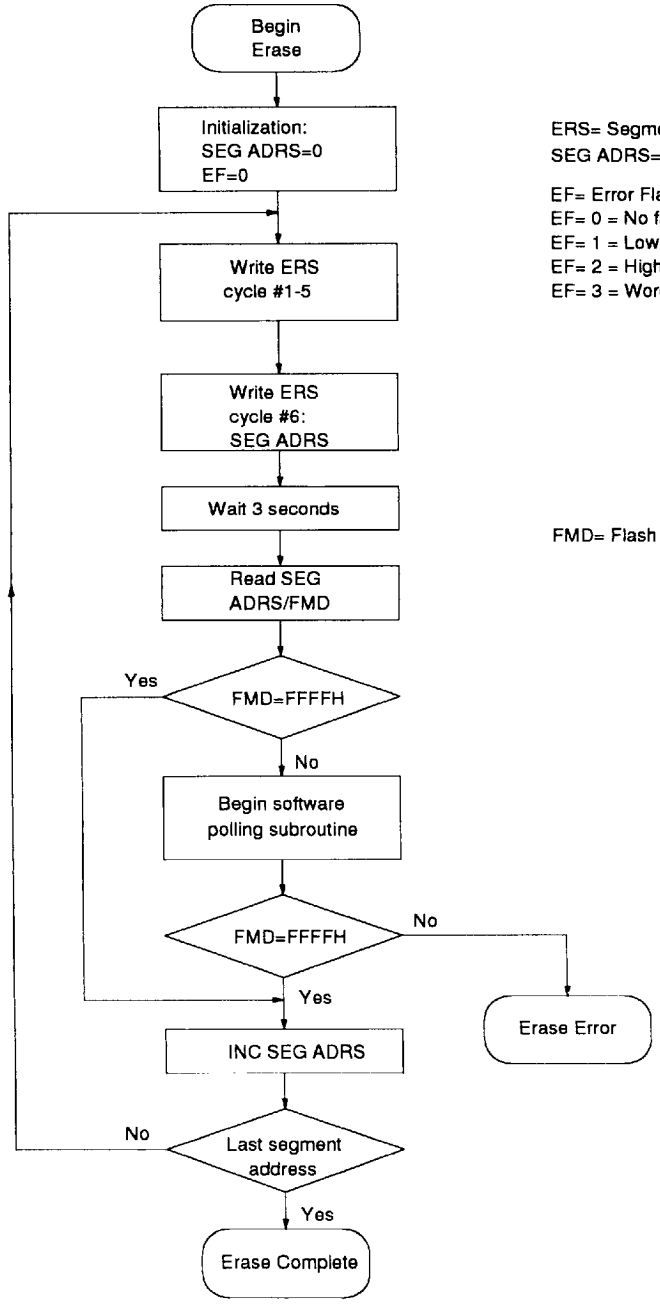

Figure 4. Word-Wide Erasure Flow Chart

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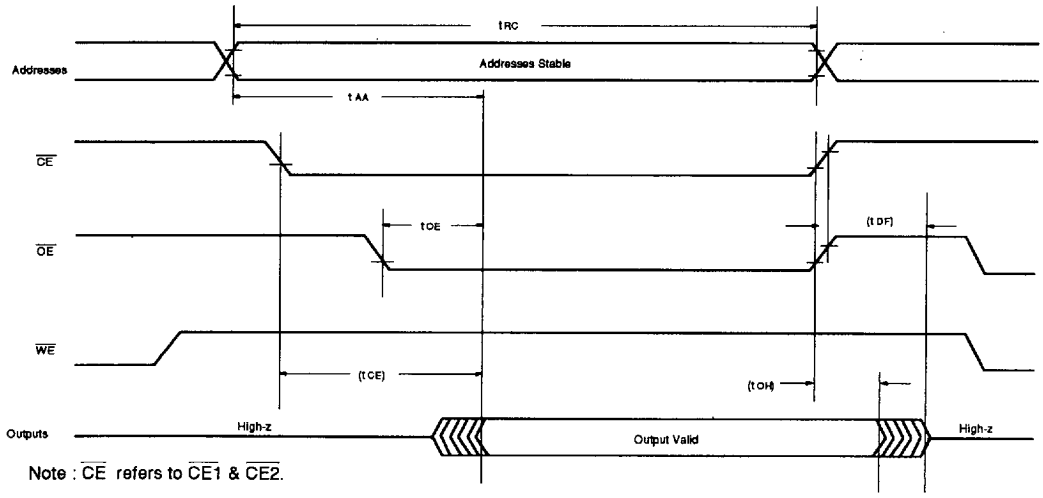

Figure 5. Read Operation Timing Diagram

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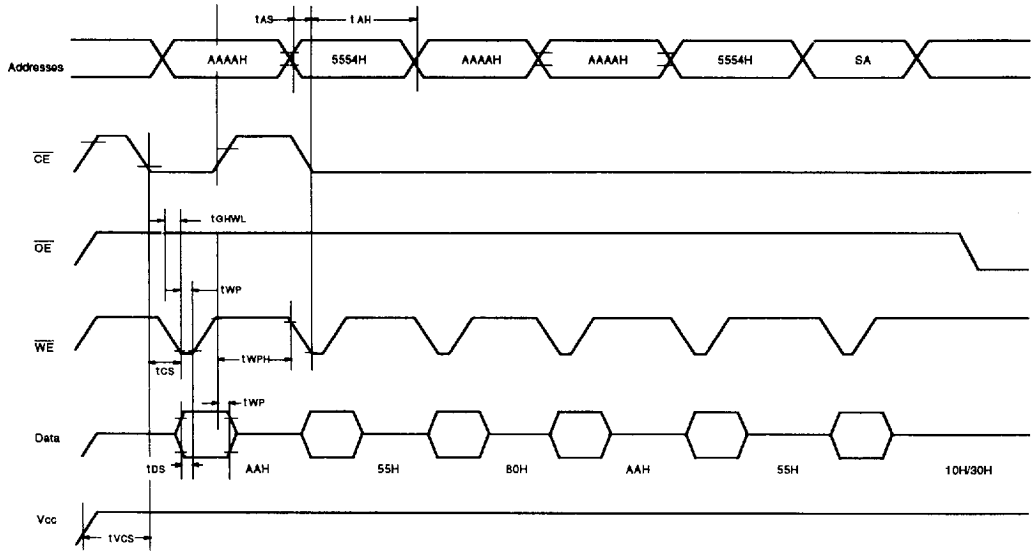

Note :
1. SA is the sector address for sector erase per Table 4.

Figure 6. Segment/Sector Byte Erase Operation Timing Diagram

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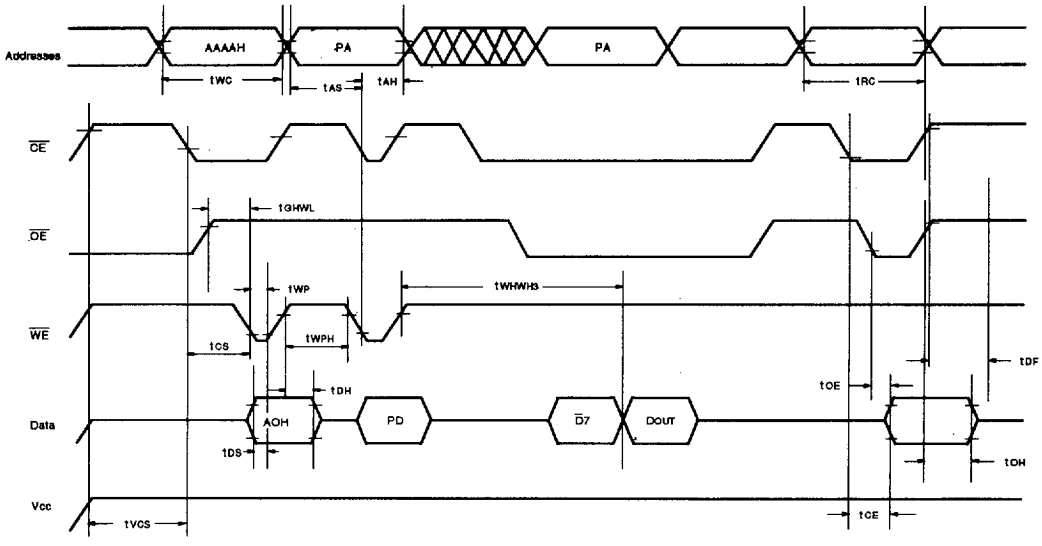

Note :
1. Figure indicates last two bus cycles of four bus cycle sequence.
2. PA is address of the memory location to be programmed.
3. PD is data to be programmed at byte address.
4. $\overline{D7}$ is the output of the complement of the data written to the device.
5. DOUT is the output of the data written to the device.

Figure 7. Byte-Wide Write Operation Timing Diagram

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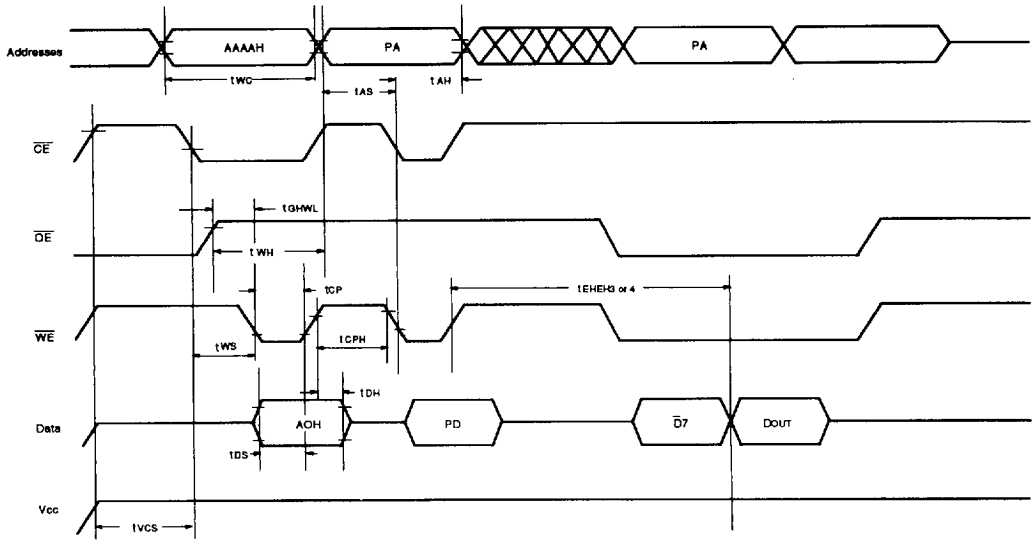

Note :
1. Figure indicates last two bus cycles of four bus cycle sequence.
2. PA is address of the memory location to be programmed.
3. PD is data to be programmed at byte address.
4. $\overline{D7}$ is the output of the complement of the data written to the device.
5. DOUT is the output of the data written to the device.

Figure 8. Alternate $\overline{CE}$ Controlled Byte Write Operation Timing Diagram

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