



FEATURES

- 3 MHz fixed frequency operation**
- Extremely low Iq: 19 μ A**
- Up to 600 mA output current**
- Input voltage 2.3 V to 5.5 V**
- Uses tiny multilayer inductors and capacitors**
- Current mode architecture for fast load and line transient response**
- 100% duty cycle low-dropout mode**
- Internal synchronous rectifier**
- Internal compensation**
- Internal soft start**
- Current overload and thermal shutdown protection**
- 0.1 μ A shutdown supply current**
- 5-ball WLCSP package**

APPLICATIONS

- PDA's and palmtop computers**
- Wireless handsets**
- Digital audio, portable media players**
- Digital cameras, GPS navigation units**

GENERAL DESCRIPTION

The ADP2108 is a high efficiency, low quiescent current step-down dc-to-dc converter in ultrasmall WLCSP package. The total solution only requires three tiny external components. It uses a proprietary high speed current mode, constant frequency PWM control scheme for excellent stability and transient response. To ensure the longest battery life in portable applications, the ADP2108 has a power saving, pulse frequency modulation (PFM) mode that reduces the switching frequency under light load conditions.

The ADP2108 runs from input voltages from 2.3 V to 5.5 V allowing single Li+/Li- polymer cell, multiple alkaline/NiMH cell, PCMCIA, and other standard power sources. The ADP2108 is available in fixed output voltages of 3.3 V, 3.0 V, 2.5 V, 2.3 V, 1.8 V, 1.5 V, 1.3 V, 1.2 V, 1.1 V, and 1.0V. All versions include internal power switch and synchronous rectifier for minimal external part count and high efficiency. ADP2108 has an internal soft start and is internally compensated. During logic controlled shutdown, the input is disconnected from the output and it draws less than 0.1 A from the input source. Other key features include under-voltage lockout to prevent deep battery discharge and soft start to prevent input current overshoot at startup. The ADP2108 is available in a 5-ball WLCSP.

TYPICAL DIAGRAM

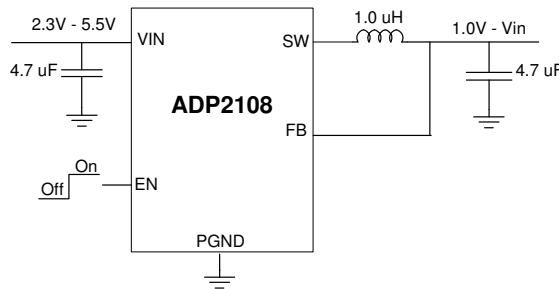


Figure 1 Application Circuit for a fixed output voltage

Rev. PrA

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TABLE OF CONTENTS

Features	1	Control Scheme	7
Applications.....	1	PWM Operation.....	7
General Description	1	PFM Operation.....	7
Function Block Diagram	1	Pulse Skipping Threshold	8
Revision History	2	Slope Compensation	8
Specifications.....	3	Product Features.....	8
Absolute Maximum Ratings.....	4	Applications.....	9
Thermal Resistance	4	External Component Selection	9
ESD Caution.....	4	PCB Layout Guidelines.....	12
Pin Configuration and Function Descriptions.....	5	Evaluation Board	13
Typical Performance Characteristics	6	Outline Dimensions	13
Theory of Operation	7	Ordering Guide	13

REVISION HISTORY

3/08–Rev. 0 Initial Version

SPECIFICATIONS

$V_{IN} = V_{EN} = 3.6\text{ V}$ @ $T_A = 25^\circ\text{C}$, unless otherwise noted; $C_{IN} = C_{OUT} = 4.7\ \mu\text{F}$, $L = 1\ \mu\text{H}$ unless otherwise noted; All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC); Typical values are at $T_A = +25^\circ\text{C}$.

Table 1.

Parameters	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Input Voltage Range		2.3		5.5	V
Undervoltage Lockout Threshold	V_{IN} rising			2.3	V
Undervoltage Lockout Threshold	V_{IN} falling	2.05	2.15	2.25	V
OUTPUT CHARACTERISTICS					
Output Voltage Accuracy ¹	$V_{IN} = 3.6\text{ V}$, $I_{LOAD} = 0\text{ mA}$ to 600 mA	-2		+2	%
	$V_{IN} = 2.5\text{ V}$ to 5.5 V , $I_{LOAD} = 0\text{ mA}$ to 600 mA	-2.5		+2.5	%
Load Regulation	$V_{IN} = 3.6\text{ V}$, $I_{LOAD} = 0\text{ mA}$ to 150 mA , 50 mA to 250 mA , 150 mA to 400 mA , $t_R/t_F = 1\ \mu\text{s}$		50		mV p-p
Line Regulation	$V_{IN} = 600\text{ mV}$ p-p ac square wave. 200 Hz , 12.5% duty, $I_{LOAD} = 50\text{ mA}$		50		mV p-p
INPUT CURRENT CHARACTERISTICS					
DC Operating Current	$I_{LOAD} = 0\text{ mA}$, device not switching		19	30	μA
Shutdown Current	$V_{EN} = 0\text{ V}$, 3.6 V ($EN \leq V_{IN} + 0.2\text{ V}$ maximum)		0.2	1.0	μA
FEEDBACK CHARACTERISTICS					
PFM/PWM Mode Hysteresis	Difference between mode transition points are measured from increasing load vs. decreasing load		50		mA
Max Output Current		600			mA
PSRR	PWM mode, $I_{OUT} = 250\text{ mA}$ (<10 kHz sine wave)		40		dB
LX(SWITCH NODE)CHARACTERISTICS					
SW On Resistance	PFET, $V_{IN} = V_{GS} = 3.6\text{ V}$, $I_{SW} = 150\text{ mA}$		415		$\text{m}\Omega$
	NFET, $V_{IN} = V_{GS} = 3.6\text{ V}$, $I_{SW} = 150\text{ mA}$		210		$\text{m}\Omega$
SW Leakage Current	$V_{EN} = 0\text{ V}$, 3.6 V ($EN \leq V_{IN} + 0.2\text{ V}$ maximum)			1	μA
Current Limit ²	Switch peak current limit (open-loop)	930	1100	1200	mA
Minimum On Time	$V_{IN} = 5.5\text{ V}$, $V_{OUT} = 1.1\text{ V}$, $f_{SW} = 3.3\text{ MHz}$		65		ns
Maximum Duty Cycle		100			%
ENABLE CHARACTERISTICS					
EN Input High Threshold		1.2			V
EN Input Low Threshold				0.4	V
EN Input Leakage Current	$V_{EN} = 0\text{ V}$, 5.5 V	-1	+0.01	+1	μA
OSCILLATOR FREQUENCY					
		2.7	3.0	3.3	MHz
SOFT START PERIOD					
	$C_{OUT} = 4.7\ \mu\text{F}$			300	μs
THERMAL CHARACTERISTICS					
Thermal Shutdown Threshold			150		$^\circ\text{C}$
Thermal Shutdown Hysteresis			20		$^\circ\text{C}$

¹ Limits in bold face type apply over the full operating ambient temperature range $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$

² Open-loop data. Refer to the Typical Performance Characteristics for closed loop data

³ $V_{OUT}(\text{min})$ must be greater than (.19).

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN, EN	-0.3 V to +6 V
FB, SW to PGND	-0.3 V to (VIN + 0.2 V)
Operating Ambient Temperature Range	-40°C to +85°C
Operating Junction Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature Range	TBD
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD Human Body Model	±2000 V
ESD Charged Device Model	±500 V
ESD Machine Model	±100 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for device soldered on a circuit board single layer for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
5-Ball WLCSP	200	°C/W
Maximum Power Dissipation	200	mW

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

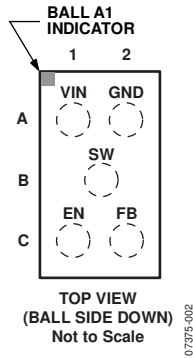


Figure 2. 5-ball WCLSP pin configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VIN	Power Source Input. VIN is the source of the PFET high-side switch. Bypass VIN to GND with a 2.2 μ F or greater capacitor as close to the ADP2108 as possible.
2	GND	Ground. Connect all the input and output capacitors to GND.
3	EN	Enable Input. Drive EN high to turn on the ADP2108. Drive EN low to turn it off and reduce the input current to 0.1 μ A.
4	FB	Feedback Input of the Error Amplifier. Connect FB to the output of the switching regulator.
5	SW	Switch Node Output. SW is the drain of the P-channel MOSFET switch and N-channel synchronous rectifier. Connect the output LC filter between SW and the output voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 3.6V$, $T_A = 25^\circ C$, $V_{EN} = V_{IN}$, unless otherwise noted

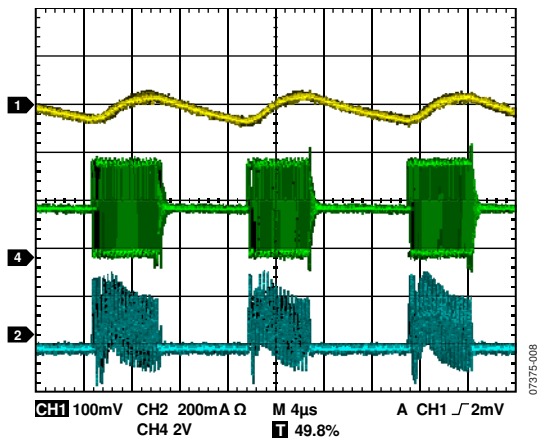


Figure 3 PFM Operation at Iload = 40mA

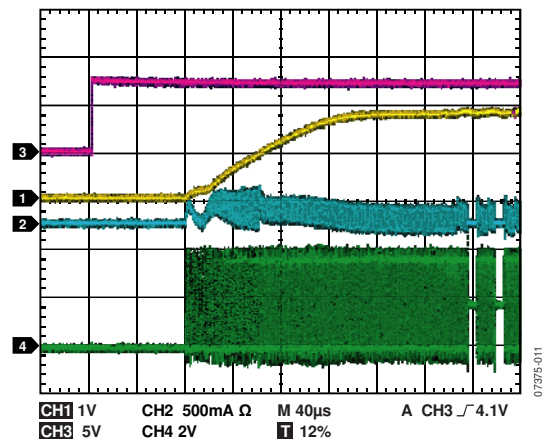


Figure 6 Start Up Waveform Iload = 10mA

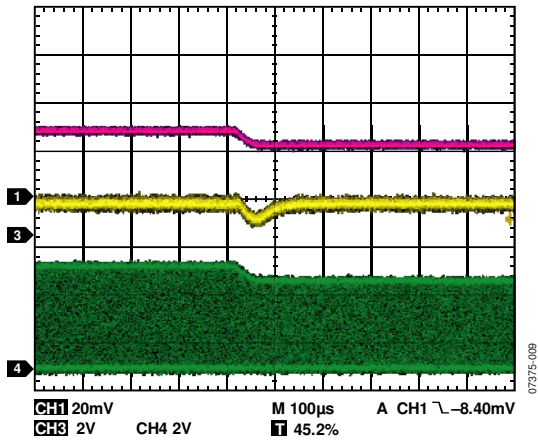


Figure 4 Line Transient Fall Iload = 100mA, $V_{in} = 3.6V - 4.2V$

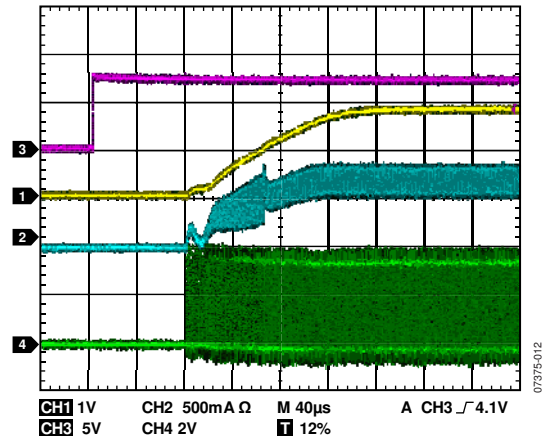


Figure 7 Start Up Waveform Iload = 600mA

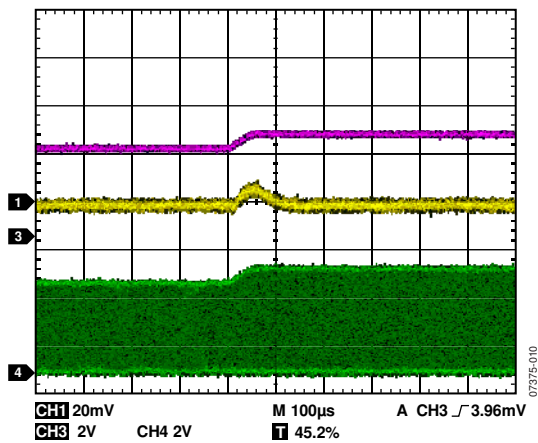


Figure 5 Line Transient Riseload = 100mA, $V_{in} = 3.6V - 4.2V$

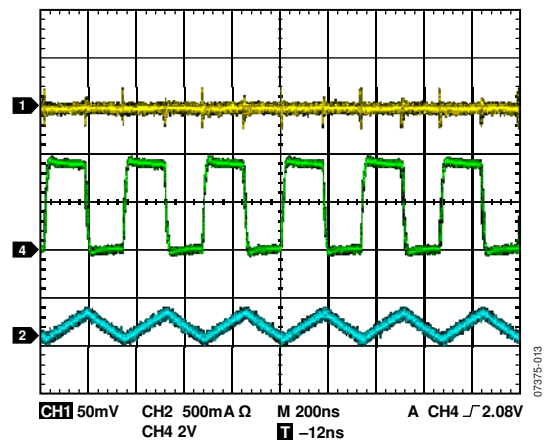


Figure 8 PWM Operation at Iload = 150mA

THEORY OF OPERATION

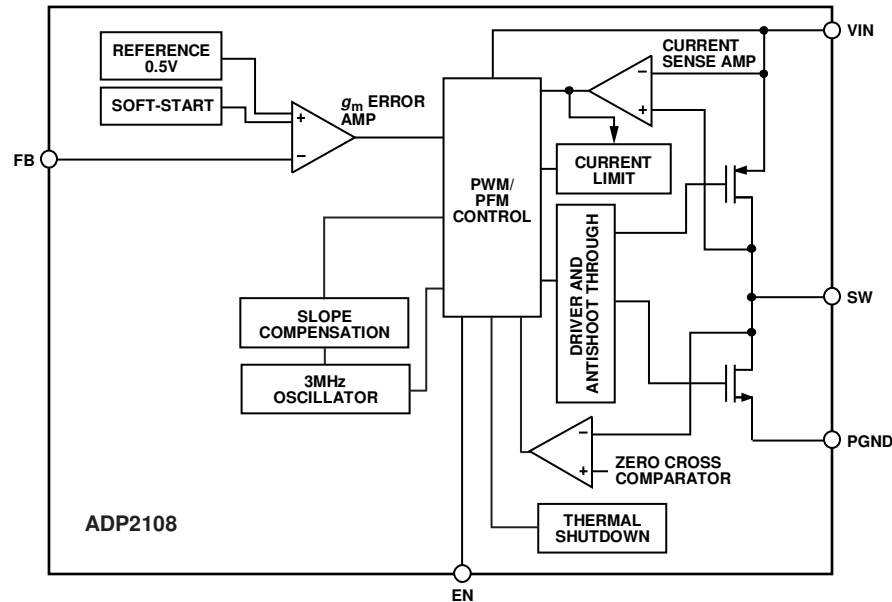


Figure 9. Functional Block Diagram

The ADP2108 is a step-down dc-to-dc converter that uses a fixed frequency and high speed current mode architecture. The high 3 MHz switching frequency and tiny 5-ball, WLCSP package allow for a small step-down dc-to-dc converter solution.

The ADP2108 operates with an input voltage from 2.3 V to 5.5 V and regulate an output voltage down to 0.8 V. Output voltage options are 3.3 V, 3.0 V, 2.5 V, 2.3 V, 1.8 V, 1.5 V, 1.3 V, 1.2 V, 1.1 V, and 1.0 V.

CONTROL SCHEME

The ADP2108 operates with a fixed frequency, current mode PWM control architecture at medium to high loads for high efficiency, but shift to a variable frequency PFM control scheme at light loads for lower quiescent current. When operating in fixed frequency PWM mode, the duty cycle of the integrated switches is adjusted to regulate the output voltage, but when operating in PFM mode at light loads, the switching frequency is adjusted to regulate the output voltage.

The ADP2108 operate in the PWM mode only when the load current is greater than the pulse-skipping threshold current. At load currents below this value, the converter smoothly transitions to the PFM mode of operation.

PWM OPERATION

In PWM mode, the ADP2108 operates at a fixed frequency of 3 MHz set by an internal oscillator. At the start of each

oscillator cycle, the P-channel MOSFET switch is turned on, putting a positive voltage across the inductor. Current in the inductor increases until the current sense signal crosses the peak inductor current level that turns off the P-channel MOSFET switch and turns on the N-channel MOSFET synchronous rectifier. This puts a negative voltage across the inductor, causing the inductor current to decrease. The synchronous rectifier stays on for the rest of the cycle, unless the inductor current reaches zero, which also causes the zero-crossing comparator to turn off the N-channel MOSFET.

PFM OPERATION

The ADP2108 has a smooth transitions to the variable frequency PFM mode of operation when the load current decreases below the pulse skipping threshold current, switching only as necessary to maintain the output voltage within regulation. When the output voltage dips below regulation, the ADP2108 enter PWM mode for a few oscillator cycles to increase the output voltage back to regulation. During the wait time between bursts, both power switches are off, and the output capacitor supplies the entire load current. Because the output voltage dips and recovers occasionally, the output voltage ripple in this mode is larger than the ripple in the PWM mode of operation.

PULSE SKIPPING THRESHOLD

The output current at which the ADP2108 transitions from variable frequency PFM control to fixed frequency PWM control is called the pulse-skipping threshold. The pulse skipping threshold has been optimized for excellent efficiency over all load currents.

SLOPE COMPENSATION

To avoid subharmonic oscillations, slope compensation is introduced to stabilize the ADP2108 internal current loop when operating beyond a 50% duty cycle. It is implemented by summing a fixed scaled voltage ramp to the current sense signal during the on time of the P-channel MOSFET switch. The value of the compensation ramp is important because it is required to determine the minimum inductor to prevent subharmonic oscillations on the selected output voltage.

Table 5. Slop Compensation Rate

Output Voltage	Slope Compensation Rate
1.1	1.8 A/ μ S
1.8	3 A/ μ S
3.3	5.4 A/ μ S

PRODUCT FEATURES

Enable/Shutdown

The ADP2108 starts operation with soft start when the EN pin is toggled from logic low to logic high. Pulling the EN pin low forces the device into shutdown mode, reducing the shutdown current below 1 μ A.

Short-Circuit Protection

The ADP2108 includes frequency foldback to prevent output current runaway on a hard short. When the voltage at the feedback pin falls below 0.3 V, indicating the possibility of a hard short at the output, the switching frequency is reduced to 1/4 of the internal oscillator frequency. The reduction in the

switching frequency gives more time for the inductor to discharge, preventing a runaway of output current.

Undervoltage Lockout

To protect against battery discharge, undervoltage lockout circuitry is integrated on the ADP2108. If the input voltage drops below the 2.15 V undervoltage lockout (UVLO) threshold, the ADP2108 shut down, and both the power switch and synchronous rectifier turns off. When the voltage rises again above the UVLO threshold, the soft start period is initiated, and the part is enabled.

Thermal Protection

In the event the ADP2108 junction temperatures rise above 150°C, the thermal shutdown circuit turns off the converter. Extreme junction temperatures can be the result of high current operation, poor circuit board design, and/or high ambient temperature. A 30°C hysteresis is included so when thermal shutdown occurs, the ADP2108 does not return to operation until the on-chip temperature drops below 120°C. When coming out of thermal shutdown, soft start is initiated.

Soft Start

The ADP2108 has an internal soft start function that ramps the output voltage in a controlled manner upon startup, therefore limiting the inrush current. This prevents possible input voltage drops when a battery or a high impedance power source is connected to the input of the converter.

Current Limit

The ADP2108 have protection circuitry to limit the direction and amount of current to 1200 mA flowing through the power switch and synchronous rectifier. The positive current limit on the power switch limits the amount of current that can flow from the input to the output, and the negative current limit on the synchronous rectifier prevents the inductor current from reversing direction and flowing out of the load.

APPLICATIONS

EXTERNAL COMPONENT SELECTION

The external component selection for the ADP2108 application circuit shown in Figure 1 is dependent on input voltage, output voltage, and load current requirements. Additionally, trade-offs between performance parameters like efficiency and transient response can be made by varying the choice of external components.

Selecting the Inductor

The high frequency switching of the ADP2108 allows the selection of small chip inductors. The inductor value effects the transition between CFM to PFM, efficiency, output ripple and current limit values. The inductor current ripple is calculated using the following equation:

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{sw} \times L}$$

where:

f_{sw} is the switching frequency (3 MHz typical).

L is the inductor value.

The dc resistance (DCR) value of the selected inductor affects efficiency but a decrease in this value typically means an increase in root mean square (rms) with losses in the core and skin. As a minimum requirement, the dc current rating of the inductor is to be equal to the maximum load current plus half of the inductor current ripple as shown by the following equation:

$$I_{PK} = I_{LOAD(MAX)} + \left(\frac{\Delta I_L}{2}\right)$$

Table 6. Suggested 1.0 μH Inductors

Vendor	Model	Dimensions	DCR
Murata	LQM21PN1R0M	2.0 mm x 1.25 mm x 0.5mm	190 mΩ
Murata	LQM31PN1R0M	3.2 mm x 1.6mm x 0.95mm	120 mΩ
Murata	LQM2HPN1R0M	2.5 mm x 2.0mm x 0.95mm	90 mΩ
FDK	MIPSA2520D1R	2.5 mm x 2.0 mm x 1.0mm	100 mΩ

Output Capacitor

Output capacitance is required to minimize the voltage overshoot and ripple present on the output. Capacitors with low equivalent series resistance (ESR) values produce the lowest output ripple and capacitors such as X5R dielectric are to be used. Y5V capacitors are not to be used due to their variation in capacitance over temperature, which does not suit this application. Because ESR is important the capacitor is to be selected using the following equation:

$$ESR_{COUT} \leq \frac{V_{RIPPLE}}{\Delta I_L}$$

Where V_{RIPPLE} is peak-to-peak output voltage ripple and ESR_{COUT} is the ESR of the chosen capacitor. The output capacitor can be chosen use the following:

$$C_{OUT} \geq \frac{V_{IN}}{(2\pi \times f_{SW})2 \times L \times V_{RIPPLE}}$$

$$C_{out} \geq \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT}}$$

Increasing the output capacitor has no effect on stability so it can be increased to reduce output ripple and enhance load transient response. When choosing this value it is also important to account for the loss of capacitance due to output voltage dc bias.

Table 7. Suggested 4.7uF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating
Murata	X5R	GRM188R60J475	0603	6.3V
Taiyo Yuden	X5R	JMK107BJ475	0603	6.3V
TDK	X5R	C1608X5R0J475	0603	6.3V

Input Capacitor

An input capacitor is required to reduce input voltage ripple and is to be placed as close as possible to the VIN pin. As with the output capacitor, a low ESR capacitor is recommended to help to minimize input voltage ripple.

$$I_{CIN} \geq I_{LOAD(MAX)} \sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}}$$

Efficiency

Efficiency is defined as the ratio of output power to input power. The high efficiency of the ADP2108 has two distinct advantages. First, only a small amount of power is lost in the dc-to-dc converter package that reduces thermal constraints. In addition, high efficiency delivers the maximum output power for the given input power, extending battery life in portable applications. The overall efficiency of the ADP2108 can be calculated by adding together the power losses caused by the power switches and inductor.

Power Switch Conduction Losses

Power switch conduction losses are caused by the flow of output current through the P-channel power switch and the N-channel synchronous rectifier, which have internal resistances ($R_{DS(ON)}$) associated with them. The amount of power loss can be approximated by

$$P_{SW_COND} = (R_{DS(ON)_P} \times D + R_{DS(ON)_N} \times (1 - D)) \times I_{OUT}^2$$

where $D = V_{OUT}/V_{IN}$.

The internal resistance of the power switches increases with temperature but decreases with higher input voltage.

Inductor Losses

Inductor conduction losses are caused by the flow of current through the inductor, which has an internal DCR associated with it. Larger sized inductors have smaller DCR, which may decrease inductor conduction losses. Inductor core losses are related to the magnetic permeability of the core material. Because the ADP2108 is a high switching frequency dc-to-dc converter, shielded ferrite core material is recommended for its low core losses and low EMI.

The total amount of inductor power loss can be calculated by

$$P_L = DCR \times I_{OUT}^2 + Core Losses$$

Switching Losses

Switching losses are associated with the current drawn by the driver to turn on and turn off the power devices at the switching frequency. Each time a power device gate is turned on and turned off, the driver transfers a charge ΔQ from the input supply to the gate and then from the gate to ground.

The amount of power loss is calculated by

$$P_{SW} = (C_{GATE_P} + C_{GATE_N}) \times V_{IN}^2 \times f_{SW}$$

where:

C_{GATE_P} is the gate capacitance of the internal high-side switch.

C_{GATE_N} is the gate capacitance of the internal low-side switch.

$$C_{GATE_P} + C_{GATE_N} \approx 100\text{pF}$$

f_{SW} is the switching frequency.

Transition Losses

Transition losses occur because the P-channel switch cannot turn on or turn off instantaneously. In the middle of an LX node transition, the power switch provides all the inductor current. The source to drain voltage of the power switch is half the input voltage, resulting in power loss. Transition losses increase with load current and input voltage and occur twice for each switching cycle.

The amount of power loss is calculated by

$$P_{TRAN} = V_{IN} / 2 \times I_{OUT} \times (t_R + t_F) \times f_{SW}$$

where:

t_R is the rise time of the LX node.

t_F is the fall time of the LX node.

t_R and t_F are both approximately 2nS.

Thermal Considerations

In most applications, the ADP2108 does not dissipate a lot of heat, due to its high efficiency. However, in applications with maximum loads at high ambient temperature, low supply voltage, and high duty cycle, the heat dissipated in the package is great enough that it may cause the junction temperature of the die to exceed the maximum junction temperature of 125°C. Once the junction temperature exceeds 150°C, the converter goes into thermal shutdown. It recovers only after the junction temperature has decreased to below 120°C to prevent any permanent damage. Therefore, thermal analysis for the chosen application solution is very important to guarantee reliable performance over all conditions.

The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to power dissipation, shown in the following equation:

$$T_J = T_A + T_R$$

Where:

T_J is the junction temperature.

T_A is the ambient temperature.

T_R is the rise in temperature of the package due to power dissipation to it.

The rise in temperature of the package is directly proportional to the power dissipation in the package. The proportionality constant for this relationship is defined as the thermal resistance from the junction of the die to the ambient temperature, as shown in the following equation:

$$T_R = \theta_{JA} \times P_D$$

where:

T_R is the rise of temperature of the package.

θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature of the package.

P_D is the power dissipation in the package.

Capacitor Selection

Use any good quality ceramic capacitors with the ADP1208 as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended for best performance. Y5V and Z5U dielectrics are not recommended for use with any dc-to-dc converter because of their poor temperature and dc bias characteristics.

The following equation can be used to determine the worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times 1(1 - TOL)$$

where:

C_{BIAS} is the effective capacitance at the operating voltage.

$TEMPCO$ is the worst-case capacitor temperature coefficient.

TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient ($TEMPCO$) over $-40^{\circ}C$ to $+85^{\circ}C$ is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed

to be 10%, and C_{BIAS} is $4.02165 \mu F$ at 1.8 V from the graph in Figure 10.

Substituting these values in equation yields

$$C_{EFF} = 4.02165 \mu F \times (1 - 0.15) \times (1 - 0.1) = 3.0762 \mu F$$

To guarantee the performance of the ADP2108, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors are evaluated for each application.

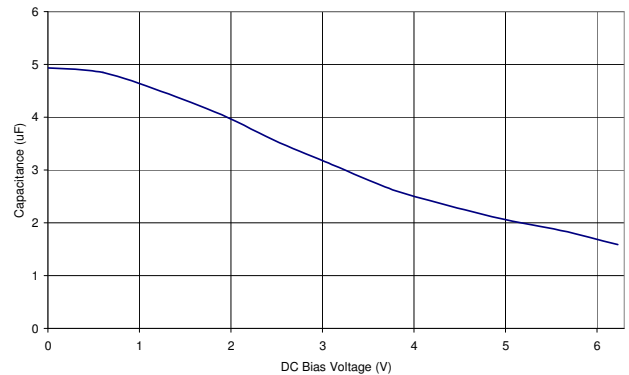


Figure 9 – Typical Capacitor Performance

PCB LAYOUT GUIDELINES

Poor layout can affect the ADP2108 performance causing electromagnetic interference (EMI) and electromagnetic compatibility (EMC) performance, ground bounce, and voltage losses. Poor layout can also affect regulation and stability. A good layout is implemented using the following rules:

- Place the inductor, input capacitor and output capacitor close to the IC using short tracks. These components carry high switching frequencies and large tracks act like antennas.
- Route the output voltage path away from the inductor and SW node to minimize noise and magnetic interference.
- Maximize the size of ground metal on the component side to help with thermal dissipation.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.

EVALUATION BOARD

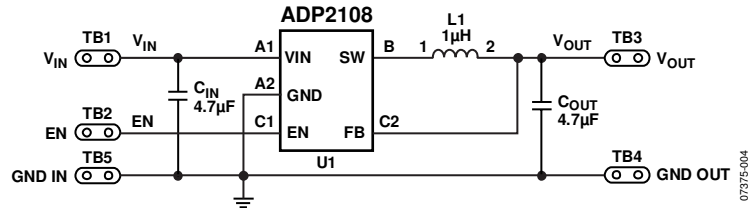


Figure 10.

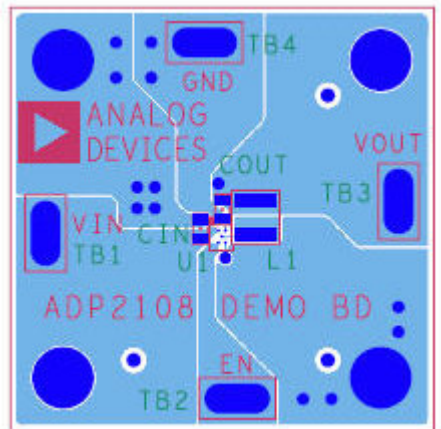


Figure 11. Recommended Top Layer

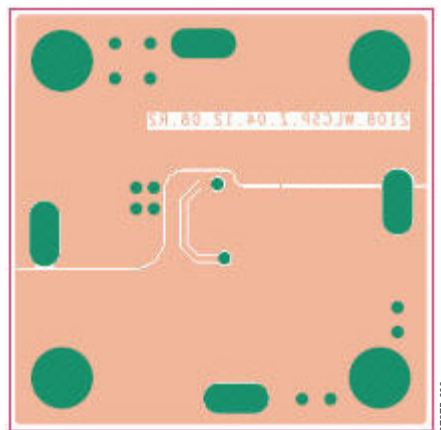
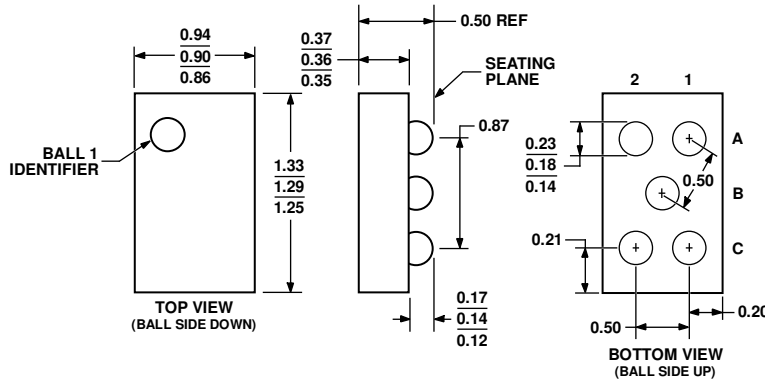


Figure 12. Recommended Bottom Layer

OUTLINE DIMENSIONS



101887-A

Figure 13. 5-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-5-1)

Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Output Voltage (V)	Package Description	Package Option	Branding
ADP2108ACBZ - 1.0 - R7 ¹	-40°C to +85°C	1.0	5-Ball WLCSP	CB	LA6
ADP2108ACBZ - 1.1 - R7 ¹	-40°C to +85°C	1.1	5-Ball WLCSP	CB	LA7
ADP2108ACBZ - 1.2 - R7 ¹	-40°C to +85°C	1.2	5-Ball WLCSP	CB	LA8
ADP2108ACBZ - 1.3 - R7 ¹	-40°C to +85°C	1.3	5-Ball WLCSP	CB	LA9
ADP2108ACBZ - 1.5 - R7 ¹	-40°C to +85°C	1.5	5-Ball WLCSP	CB	LAA
ADP2108ACBZ - 1.8 - R7 ¹	-40°C to +85°C	1.8	5-Ball WLCSP	CB	LAD
ADP2108ACBZ - 1.82 - R7 ¹	-40°C to +85°C	1.82	5-Ball WLCSP	CB	LAE
ADP2108ACBZ - 2.3 - R7 ¹	-40°C to +85°C	2.3	5-Ball WLCSP	CB	LAF
ADP2108ACBZ - 2.5 - R7 ¹	-40°C to +85°C	2.5	5-Ball WLCSP	CB	LAG
ADP2108ACBZ - 3.0 - R7 ¹	-40°C to +85°C	3.0	5-Ball WLCSP	CB	
ADP2108ACBZ - 3.3 - R7 ¹	-40°C to +85°C	3.3	5-Ball WLCSP	CB	LAH

¹Z = RoHS Compliant Part.

NOTES