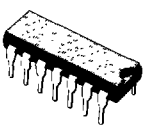
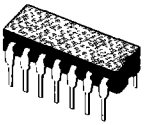
DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION

The T74LS113A offers individual J, K, set and clock inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

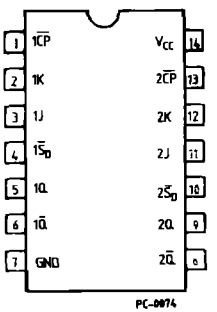
C1
(Plastic Chip Carrier)

ORDER CODES :

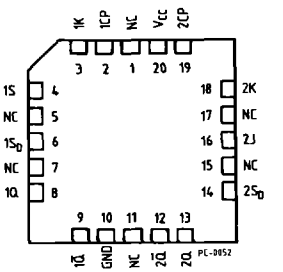
T74LS113A D1	T74LS113A C1
T74LS113A B1	T74LS113A M1

PIN CONNECTION (top view)

DUAL IN LINE

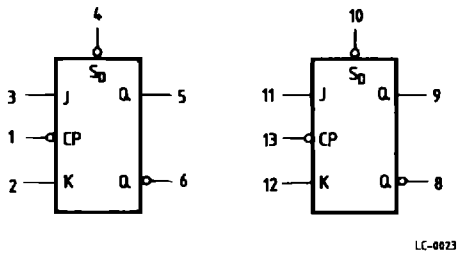


CHIP CARRIER



NC = No Internal Connection

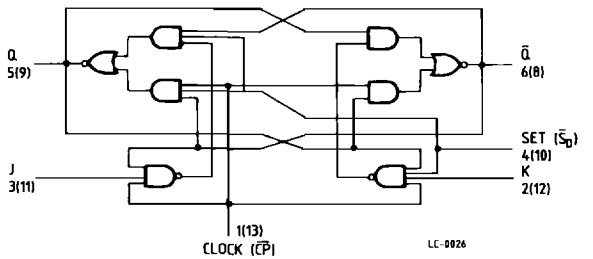
LOGIC SYMBOL



LOGIC DIAGRAM AND TRUTH TABLE

Operating Mode	Inputs			Outputs	
	$\overline{S}_D$	J	K	Q	$\overline{Q}$
Set	L	X	X	H	L
Toggle	H	h	h	$\overline{q}$	q
Load "0" (reset)	H	l	h	L	H
Load "1" (set)	H	h	l	H	L
Hold	H	l	l	q	$\overline{q}$

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h, (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-LOW clock transition



V_{CC} = Pin 14
GND = Pin 7
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	− 0.5 to 7	V
V_I	Input Voltage, Applied to Input	− 0.5 to 15	V
V_O	Output Voltage, Applied to Output	− 0.5 to 10	V
I_I	Input Current, into Inputs	− 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS113AXX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Condition (note 1)		Unit
			Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage		2.0			Guaranteed Input HIGH Voltage for all Inputs		V
V_{IL}	Input LOW Voltage				0.8	Guaranteed Input LOW Voltage for all Inputs		V
V_{CD}	Input Clamp Diode Voltage			- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage		2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage			0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IL} or V_{IH} per Truth Table	V
				0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current	J, K Set Clock			20 60 80	V_{CC} = MAX, V_{IN} = 2.7 V		µA
		J, K Set Clock			0.1 0.3 0.4	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current	J, K Set,Clock			- 0.4 - 0.8	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)		- 20		- 100	V_{CC} = MAX		mA
I_{CC}	Power Supply Current				8.0	V_{CC} = MAX		mA

Notes : 1 For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges
2 Not more than one output should be shorted at a time
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C

AC CHARACTERISTICS : T_A = 25 °C

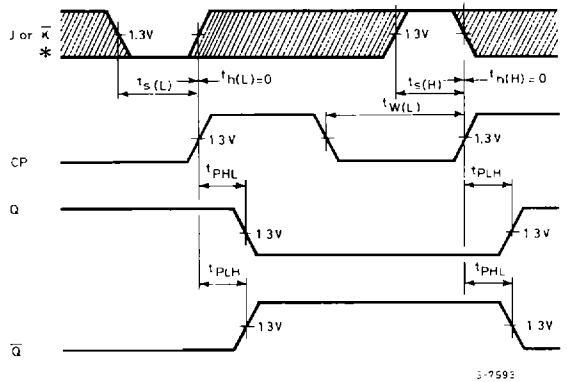
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
f_{MAX}	Maximum Clock Frequency	30	45		V_{CC} = 5.0 V C_L = 15 pF	MHz
t_{PLH} t_{PHL}	Propagation Delay, Clock Set to Output		15 15	20 20		ns

AC SET-UP REQUIREMENTS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_W	Clock Pulse Width	20			V_{CC} = 5.0 V	ns
t_W	Set Pulse Width	25				ns
t_s	Set-up Time	20				ns
t_h	Hold Time	0				ns

AC WAVEFORMS

Figure 1 : Clock to Output Delays, Data Set-up and Hold Times. Clock Pulse Width.



* The shaded areas indicate when the input is permitted is change to predictable output performance.

Figure 2 : Set and Clear to Output Delays, Set and Clear Pulse Widths.

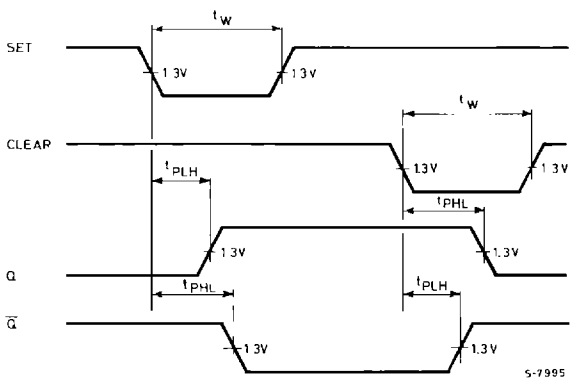
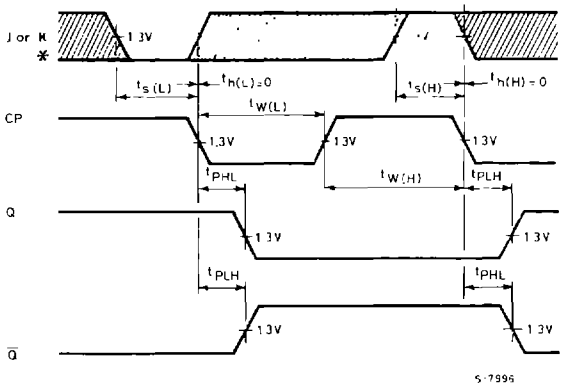


Figure 3 : Clock to Output Delays, Data Set-up and Hold Times. Clock Pulse Width.



* The shaded areas indicate when the input is permitted is change to predictable output performance