

512K x 24 Static RAM Module

Features

- High density 12- Mb SRAM Module
- High Speed CMOS SRAMs
- Access Times of 10 ns
- Single 3.3V Power supply
- Low active power(1620W at 10 ns)
- TTL compatible inputs and outputs
- Available in standard 119 ball BGA
- Interface to Motorola DSP and Analog Devices

Functional Description

The CYM8301 is a 3.3V high performance 12 Megabit static RAM organized as a 512K words by 24 bits. This module is constructed from three 512K x8 SRAM dies mounted on a multi layer laminate substrate combined to form a 24 bit SRAM. CYM8301 is an ideal single chip solution for the Motorola's DSP5630X or a two chip solution to Analog Devices ADSP2106XL.

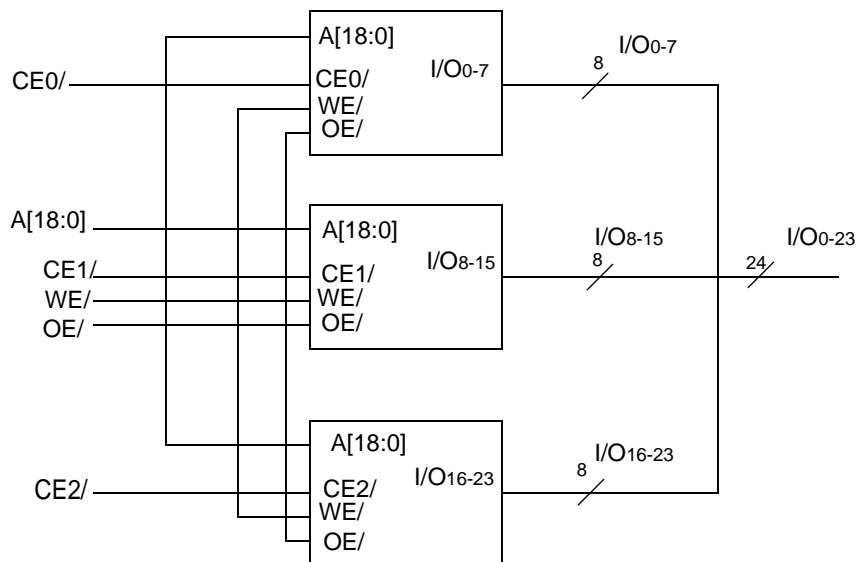
Each data byte is separately controlled by the individual chip selects(CE0,CE1/CE2). CE0/ controls I/O0-7. CE1/ controls I/O8-15. CE2/ controls I/O16-23.

Writing the data bytes into the SRAM is accomplished when the chip select controlling that byte is LOW and write enable (\overline{WE}) input is LOW. Data on the respective input/output pins (I/O) is then written into the memory location specified on the address pins (A0 through A18). Asserting all the chip selects LOW and write enable LOW will write the entire data(I/O0-I/O23) into the SRAM. Output enable (\overline{OE}) is not looked into while in a WRITE mode.

Data bytes can also be individually read from the device. Reading a byte is accomplished when the chip select controlling that byte is LOW and write enable (\overline{WE}) HIGH while output enable (\overline{OE}) remains LOW. Under these conditions, the contents of the memory location specified on the address pins will appear on the specified data input/output pins (I/O). Asserting all the chip selects LOW and write enable HIGH with output enable LOW will read the entire data (I/O0-I/O23) from the SRAM.

The data input/output (I/O0-I/O23) pins stay at high-impedance state when all the chip selects are HIGH or when the output enable (\overline{OE}) is HIGH when in a READ mode. For further details, refer to the truth table in this datasheet.

Functional Block Diagram



Selection Guide

| | CYM8301-10 | CYM8301-12 | CYM8301-15 |
|--------------------------------|------------|------------|------------|
| Maximum Access Time (ns) | 10 | 12 | 15 |
| Maximum Operating Current (mA) | 450 | 420 | 420 |
| Maximum Standby Current (mA) | 90 | 90 | 90 |

Shaded areas contain advance information.

Pin Configurations
**119 BGA
Top View**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|----------|-------|-----------------|------------------|------------------|------------------|-----------------|-------|
| A | NC | A | A | A | A | A | NC |
| B | NC | A | A | $\overline{CE0}$ | A | A | NC |
| C | I/O12 | NC | $\overline{CE1}$ | NC | $\overline{CE2}$ | NC | I/O0 |
| D | I/O13 | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | I/O1 |
| E | I/O14 | V _{SS} | V _{DD} | V _{SS} | V _{DD} | V _{SS} | I/O2 |
| F | I/O15 | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | I/O3 |
| G | I/O16 | V _{SS} | V _{DD} | V _{SS} | V _{DD} | V _{SS} | I/O4 |
| H | I/O17 | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | I/O5 |
| J | NC | V _{SS} | V _{DD} | V _{SS} | V _{DD} | V _{SS} | NC |
| K | I/O18 | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | I/O6 |
| L | I/O19 | V _{SS} | V _{DD} | V _{SS} | V _{DD} | V _{SS} | I/O7 |
| M | I/O20 | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | I/O8 |
| N | I/O21 | V _{SS} | V _{DD} | V _{SS} | V _{DD} | V _{SS} | I/O9 |
| P | I/O22 | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | I/O10 |
| R | I/O23 | A | NC | NC | NC | A | I/O11 |
| T | NC | A | A | \overline{WE} | A | A | NC |
| U | NC | A | A | \overline{OE} | A | A | NC |

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage on V_{CC} to Relative GND^[1] -0.5V to 4.6V

DC Voltage Applied to Outputs in High Z State ^[1] -0.5V to V_{CC} + 0.5V

DC Input Voltage ^[1] -0.5V to V_{CC} + 0.5V

Notes:

- V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- T_A is the "Instant On" case temperature.

Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

| Range | Ambient Temperature ^[2] | V _{CC} |
|------------|------------------------------------|-----------------|
| Commercial | 0°C to +70°C | 3.3V ±5% |
| Industrial | -40°C to +85°C | 3.3V ±5% |

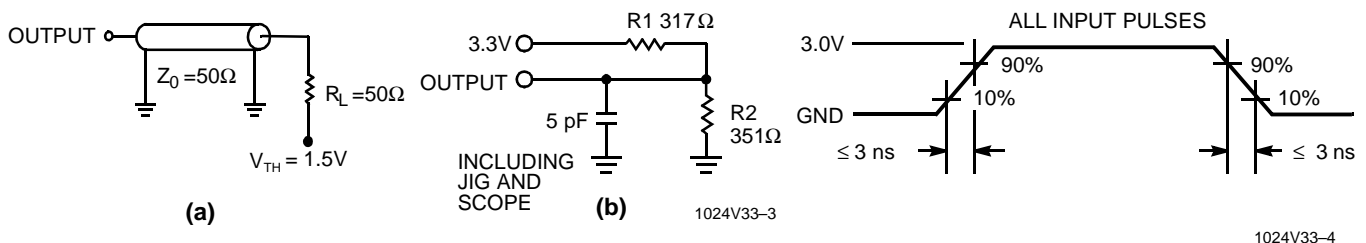
Shaded areas contain advance information.

Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions ^[3] | CYM8301-10 | | CYM8301-12/15 | | Unit |
|------------------|----------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|------------|--------------------------|---------------|--------------------------|------|
| | | | Min. | Max. | Min. | Max. | |
| V _{OH} | Output HIGH Voltage | V _{CC} = Min., I _{OH} = -4.0 mA | 2.4 | | 2.4 | | V |
| V _{OL} | Output LOW Voltage | V _{CC} = Min., I _{OL} = 8.0 mA | | 0.4 | | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 2.2 | V _{CC} + 0.3 | 2.2 | V _{CC} + 0.3 | V |
| V _{IL} | Input LOW Voltage ^[1] | | -0.5 | 0.8 | -0.5 | 0.8 | V |
| I _{Ix} | Input Load Current | GND ≤ V _I ≤ V _{CC} | -10 | +10 | -10 | +10 | μA |
| I _{OZ} | Output Leakage Current | GND ≤ V _I ≤ V _{CC} , Output Disabled | -10 | +10 | -10 | +10 | μA |
| I _{CC} | V _{CC} Operating Supply Current | V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC} | | 450 | | 420 | mA |
| I _{SB1} | Automatic CE Power-Down Current —TTL Inputs | Max. V _{CC} , $\overline{CE} \geq V_{IH}$ V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX} | | 150 | | 150 | mA |
| I _{SB2} | Automatic CE Power-Down Current —CMOS Inputs | Max. V _{CC} , CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0 | | 90 | | 90 | mA |

Capacitance^[4]

| Parameter | Description | Test Conditions | Max. | Unit |
|------------------|--------------------|-------------------------------------------------------------|------|------|
| C _{IN} | Input Capacitance | T _A = 25°C, f = 1 MHz, V _{CC} = 3.3V | 8 | pF |
| C _{OUT} | Output Capacitance | | 8 | pF |

AC Test Loads and Waveforms

Notes:

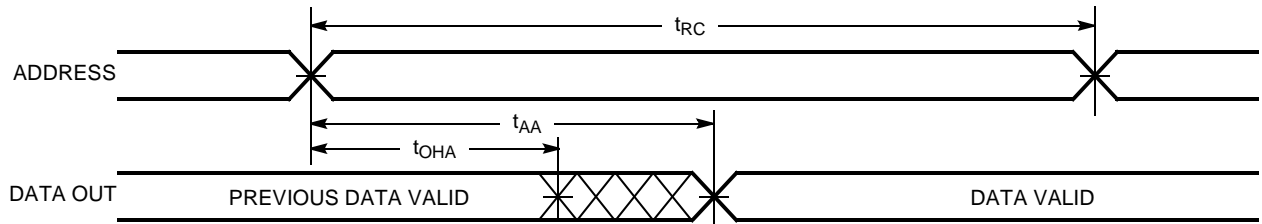
- CE is a combination of $\overline{CE1}$, CE2 and $\overline{CE3}$
- Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics ^[5] Over the Operating Range

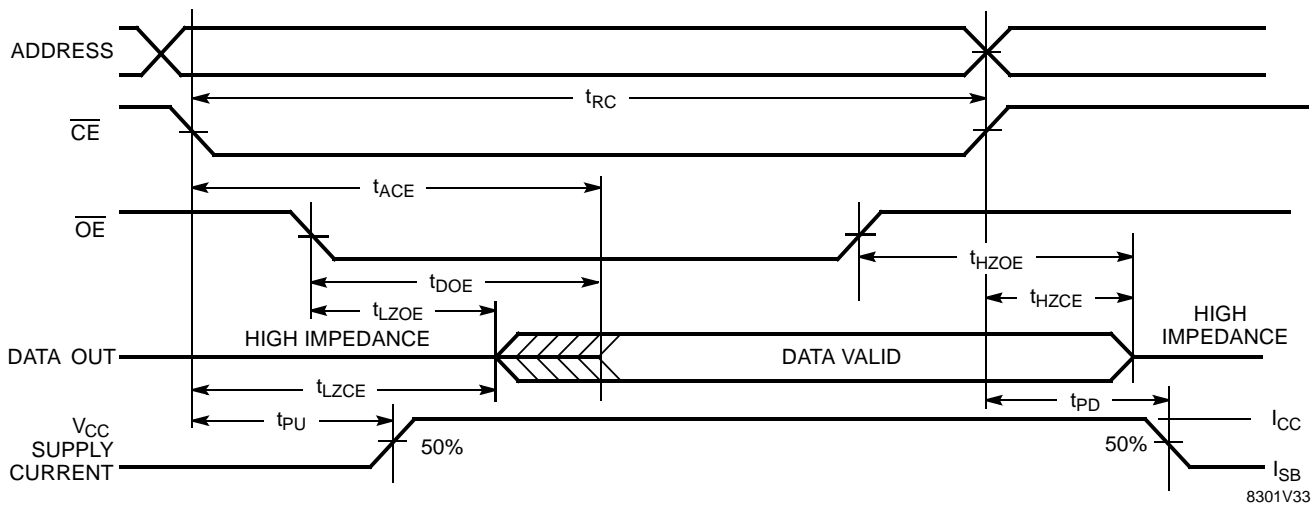
| Parameter | Description ^[3] | CYM8301-10 | | CYM8301-12 | | CYM8301-15 | | Unit |
|--------------------------------------|------------------------------------------------------|------------|------|------------|------|------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | | | |
| t _{RC} | Read Cycle Time | 10 | | 12 | | 15 | | ns |
| t _{AA} | Address to Data Valid | | 10 | | 12 | | 15 | ns |
| t _{OHA} | Data Hold from Address Change | 3 | | 3 | | 3 | | ns |
| t _{ACE} | \overline{CE} active to Data Valid | | 10 | | 12 | | 15 | ns |
| t _{DOE} | \overline{OE} LOW to Data Valid | | 6 | | 7.2 | | 8.5 | ns |
| t _{LZOE} | \overline{OE} LOW to Low Z | 0 | | 0 | | 0 | | ns |
| t _{HZOE} | \overline{OE} HIGH to High Z ^[6, 7] | | 5 | | 6 | | 7 | ns |
| t _{LZCE} | \overline{CE} active to Low Z ^[7] | 3 | | 3 | | 3 | | ns |
| t _{HZCE} | \overline{CE} inactive to High Z ^[6, 7] | | 5 | | 6 | | 7 | ns |
| t _{PU} | \overline{CE} active to Power-Up | 0 | | 0 | | 0 | | ns |
| t _{PD} | \overline{CE} inactive to Power-Down | | 10 | | 12 | | 15 | ns |
| WRITE CYCLE ^[8, 9] | | | | | | | | |
| t _{WC} | Write Cycle Time | 10 | | 12 | | 15 | | ns |
| t _{SCE} | \overline{CE} active to Write End | 9 | | 9 | | 9 | | ns |
| t _{AW} | Address Set-Up to Write End | 9 | | 9 | | 10 | | ns |
| t _{HA} | Address Hold from Write End | 0 | | 0 | | 0 | | ns |
| t _{SA} | Address Set-Up to Write Start | 0 | | 0 | | 0 | | ns |
| t _{PWE} | \overline{WE} Pulse Width | 8 | | 10 | | 11 | | ns |
| t _{SD} | Data Set-Up to Write End | 6 | | 6 | | 7 | | ns |
| t _{HD} | Data Hold from Write End | 0 | | 0 | | 0 | | ns |
| t _{LZWE} | \overline{WE} HIGH to Low Z ^[7] | 3 | | 3 | | 3 | | ns |
| t _{HZWE} | \overline{WE} LOW to High Z ^[6, 7] | | 5 | | 6 | | 7 | ns |

Notes:

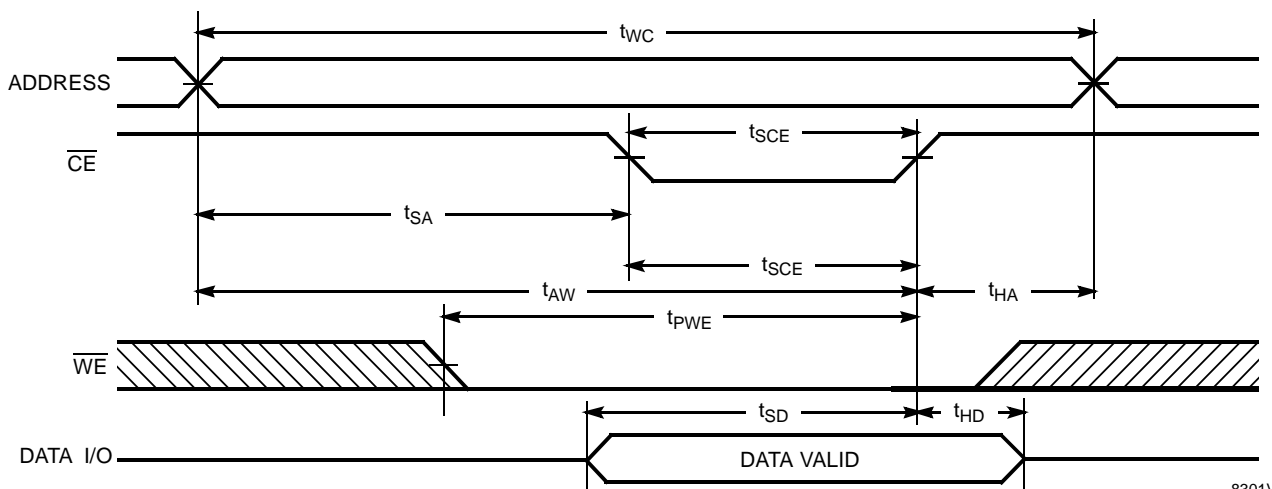
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH}.
- t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms
Read Cycle No. 1^[10, 11]


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Read Cycle No. 2 (\overline{OE} Controlled)^[3, 11, 12]


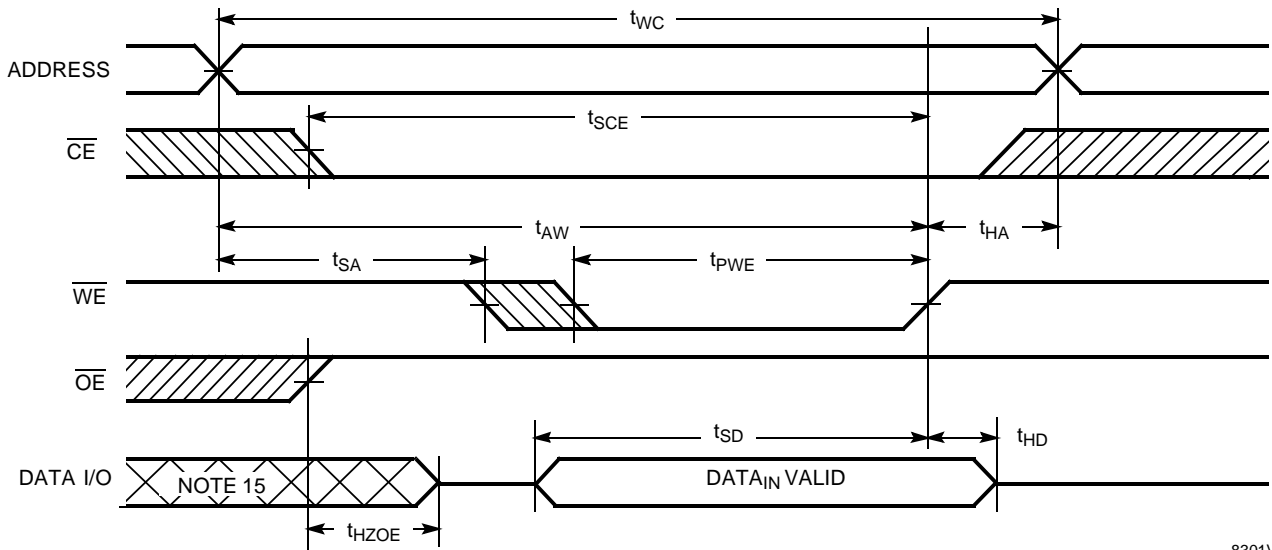
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Write Cycle No. 1 (\overline{CE} Controlled)^[3, 13, 14]


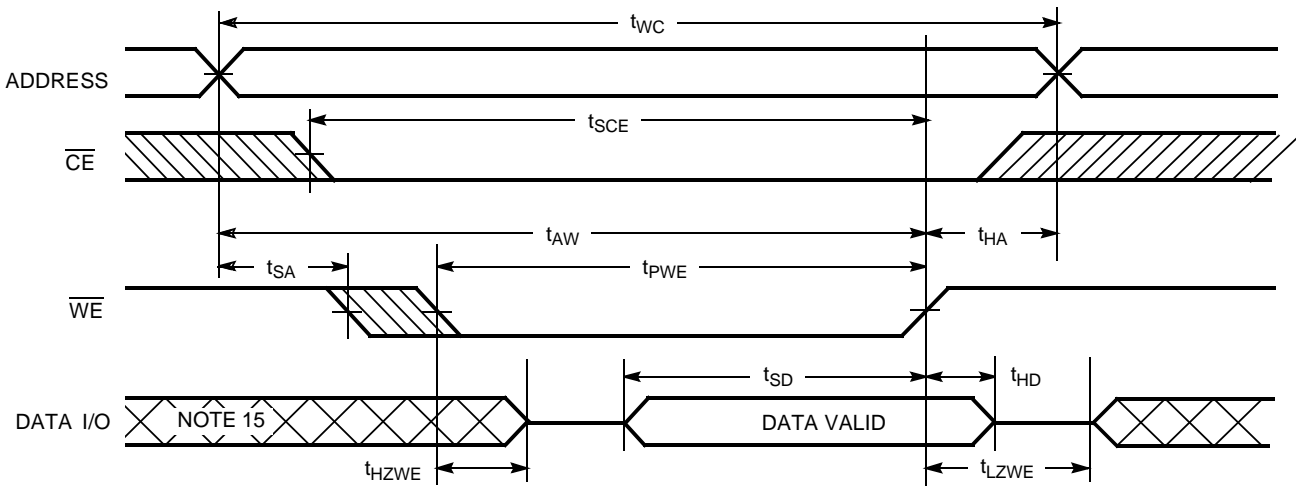
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Notes:

10. Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
11. WE is HIGH for read cycle.
12. Address valid prior to or coincident with \overline{CE} transition LOW.
13. Data I/O is high impedance if $OE = V_{IH}$.
14. If \overline{CE} goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)
Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} HIGH During Write)^[13, 14]


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Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[3, 14]


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Note:

15. During this period the I/Os are in the output state and input signals should not be applied.

Truth Table

| CE1 | CE2 | CE3 | WE | OE | I/O₀-I/O₂₃ | Mode |
|------------|------------|------------|-----------|-----------|-------------------------------------------------------------------|---------------------|
| H | H | H | X | X | High Z | DESELECT/POWER DOWN |
| L | L | L | H | L | Data Out (I/O 0 - 23) | Read |
| L | L | L | H | H | I/O High Z | Power Down |
| L | H | H | H | L | Data Out (I/O 0-7) I/O8-23 in High Z | Read |
| H | L | H | H | L | Data Out (I/O 8-15) I/O 0 -7 in High Z I/O 16- 23 in High Z | Read |
| H | H | L | H | L | Data Out (I/O 16-23) I/O 0 -15 in High Z | Read |
| L | L | L | L | X | Data In (I/O 0 -23) | Write |
| L | H | H | L | X | Data In (I/O 0-7) | Write |
| H | L | H | L | X | Data In (I/O 8 - 15) | Write |
| H | H | L | L | X | Data In (I/O 16- 23) | Write |

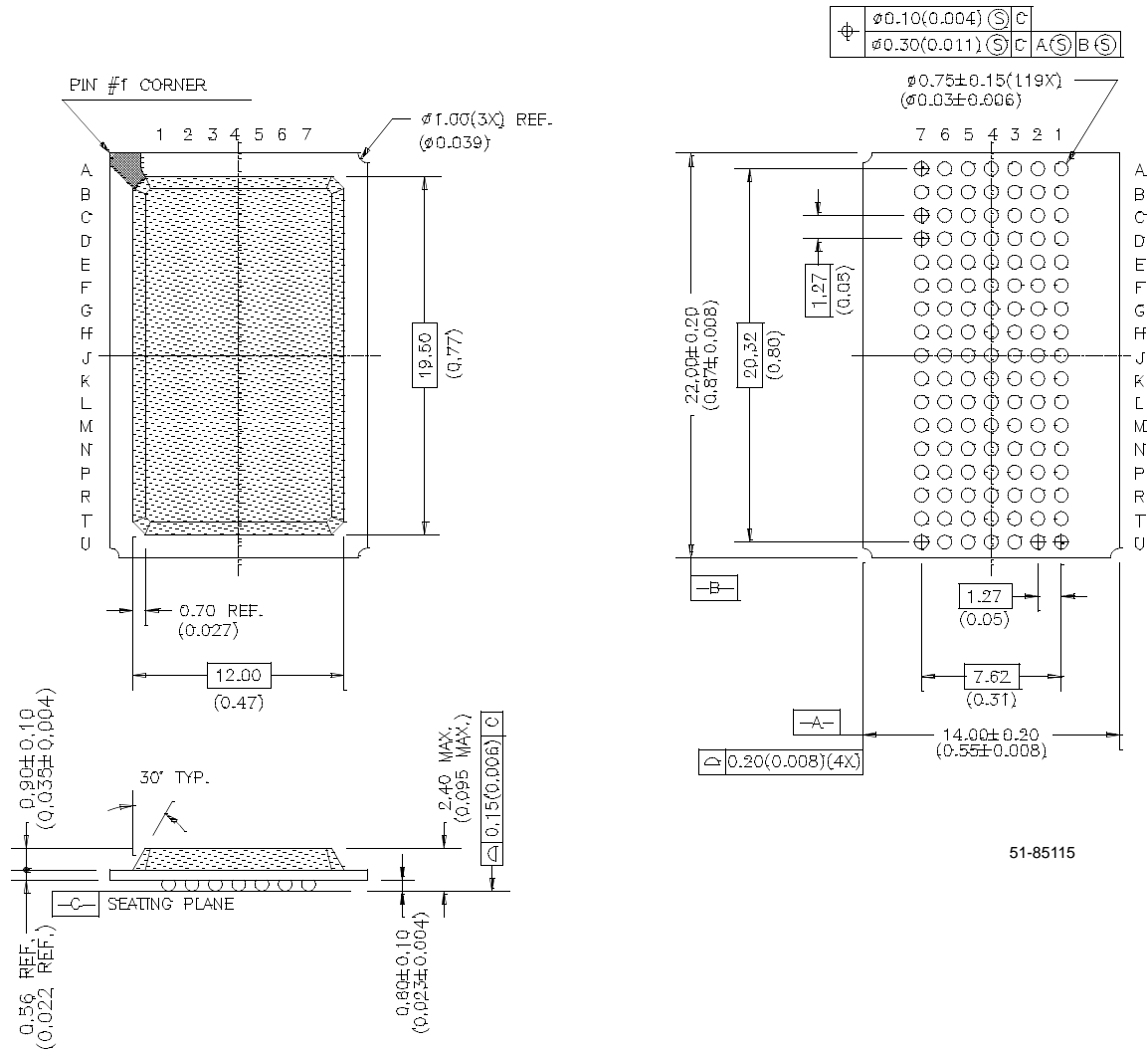
Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|-------------------|----------------------|---------------------|---------------------|------------------------|
| 10 | CYM8301V33 - 10 BGC | BG119 | 119-Ball BGA | Commercial |
| 12 | CYM8301V33 - 12 BGC | BG119 | 119-Ball BGA | Commercial |
| 15 | CYM8301V33 - 15 BGC | BG119 | 119-Ball BGA | Commercial |
| 15 | CYM8301V33 - 15 BGI | BG119 | 119-Ball BGA | Industrial |

Package Diagram

119-Ball BGA (14 x 22 x 2.4 mm) BG119

DIMENSION IN MILLIMETERS (INCHES)





| Document Title: CYM8301V33 512 x 24 Static RAM Module Document Number: 38-05092 | | | | |
|--------------------------------------------------------------------------------------------------|----------------|-------------------|------------------------|------------------------------|
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 107602 | 07/17/01 | MEG | New Data Sheet |