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AMENDENT HISTORY

Version	Date	Description
V1.0	July 14, 2008	First issue
V1.1	Nov 03,2008	Modify Application Circuit
V1.2	Nov 18,2008	Add OTP Mode Programming Pin

1. INTRODUCTION

SNC15120P is a one-channel voice synthesizer One Time Program IC with PWM direct drive circuit. It built in a 4-bit tiny controller with four 4-bit I/O ports. By programming through the tiny controller in SNC15120P, user's varied applications including voice section combination, key trigger arrangement, output control, and other logic functions can be easily implemented.

2. FEATURES

- Single power supply 2.4V – 3.6V
- 120 seconds voice capacity are provided (@6KHZ sample rate)
- Built in a 4-bit tiny controller
- I/O Port
  - Four 4-bit I/O ports P1, P2, P4 and P5 are provided.
  - The driving/sink current of P2 & P5 is up to 8mA/16mA
  - The IO pins P2.3 can be modulated with 38.5Khz carry signal to implement IR function.
- 128*4 bits RAM are provided
- Maximum 64k program ROM is provided
- 244K*12 shared ROM for voice data and program
- Readable ROM code data
- Built in one channel speech synthesizer
- Adaptive playing speed from 2.5k-20kHz is provided
- Built-in an PWM circuit output, can directly connected to Speaker for sound output.
- System clock: 2MHz
- Event Mark function supported
- Low Power Detect
- Watch Dog Timer Supported

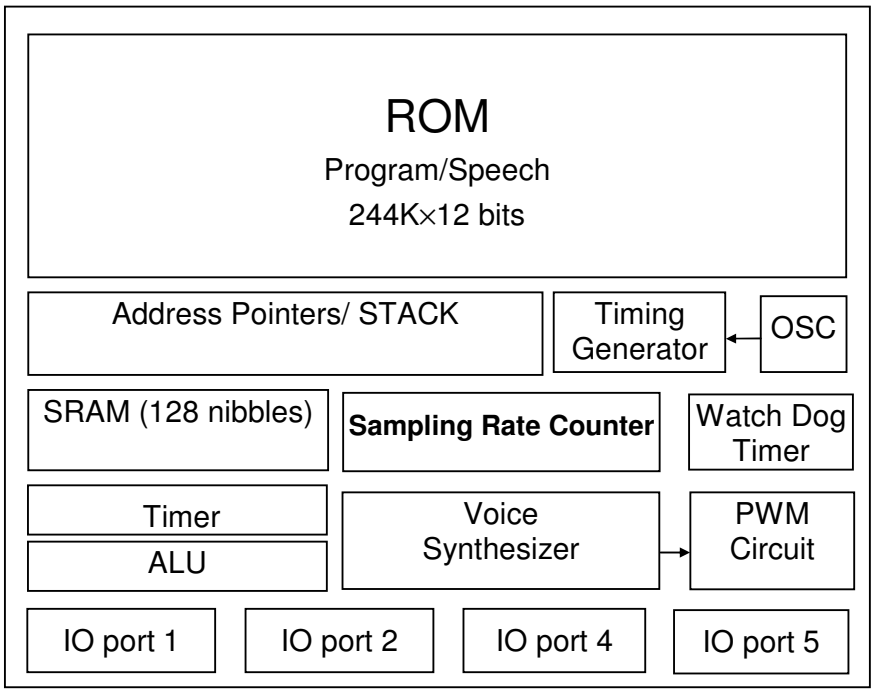
3. PIN ASSIGNMENT

Symbol	I/O	Function Description
P10~P13	I/O	I/O port 1: IO
P20~P23	I/O	I/O port 2: IO
P40~P43	I/O	I/O port 4: IO
P50~P53	I/O	I/O port 5: IO
Rosc	I	Oscillation component connection pin
BUO1	O	PWM output 1
BUO2	O	PWM output 2
RST	I	RST=1→ Reset Chip (Active H)
VDD	I	Positive power supply
GND	I	Negative power supply
CVDD	I	Core circuit positive power supply
CGND	I	Core circuit negative power supply
Test	I	Test pin
VPP0	I	OTP Programming Voltage
VPP1	I	OTP Programming Voltage
VPP2	I	OTP Programming Voltage

OTP Mode Programming Pin

Symbol	Chip pin name	I/O Status	Description
RST	RST	Input	Into OTP mode, High Active.
VPP0	VPP0	Input	VPP0 for OTP Program. (VPP=7.5V)
VPP1	VPP1	Input	VPP1 for OTP Program. (VPP=7.5V)
VPP2	VPP2	Input	VPP2 for OTP Program. (VPP=7.5V)
CLK	P10	Input	OTP mode clock input
PGMB / DATA OUT	P11	Input / Output	PGMB of OTP Program mode. DATA OUT of OTP Verify mode.
DATA IN	P12	Input	Series/Mode/Address/Data Input of OTP mode
OTP RST	P13	Input	OTP Reset of OTP mode, low active
Parity Check	P20	Output	Input Data Parity Check
Parallel DATA IN/OUT	P53 ~ P40	Input / Output	Parallel interface OTP data input/out. P53, P52, P51 ,P50, P43 ,P42 ,P41 ,P40 (MSB → LSB)

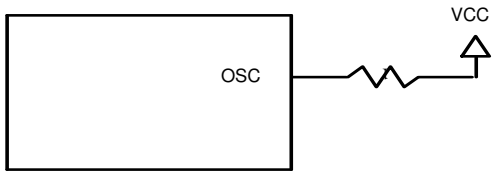
4. Block Diagram



5. FUNCTION DESCRIPTIONS

5.1 Oscillator

SNC15120P accepts RC type oscillator for system clock. The typical circuit diagram for oscillator is listed as follows.



RC Oscillator

5.2 ROM

SNC15120P contains a substantial 244K words (12-bit) internal ROM, which is shared by program and resource data. Program, voice and data are shared within this same 244K words ROM.

5.3 RAM

SNC15120P contains 128 nibble RAM (128 x 4-bits). The 128 nibble RAM is divided into two pages (page 0 to page 1, 64 nibble RAM on each page). In our programming structure, users can use the instructions, PAGE n (n=0 to 1) to switch and indicate the RAM page. Besides, users can use direct mode, M0 ~ M63 in the data transfer type instructions, to access all 64 nibbles of each page.

5.4 Power Down Mode

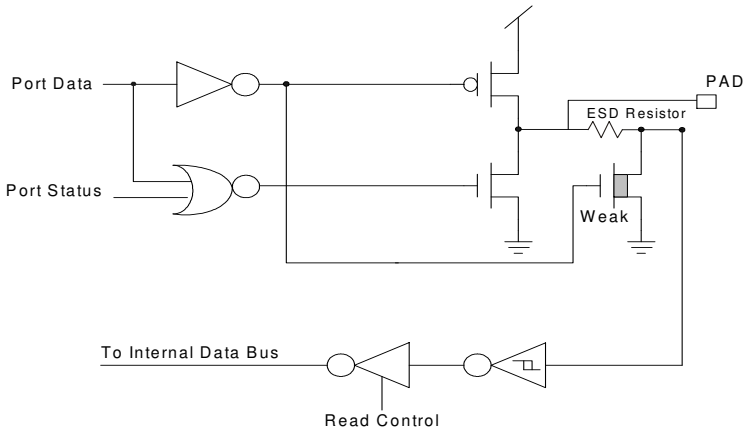
"End" instruction makes the IC entering into Stop Mode will stop the system clock for power savings (<3uA @VDD=3V) Any valid data transition (L→H or H→L) occurring on any IO pin can be used to start the system clock and return to normal operating mode.

5.5 Sampling Rate Counter

The unique sampling rate counter is designed in voice channel to be able to play diverse voices at different sample playing rates. The playing rate can be adaptively set up among from the wide ranges of 2.5KHz to 20KHz. This architecture yields a high-quality voice synthesis that sounds very close to its original source when played through the same amplifier and speaker circuitry.

5.6 I/O Ports

There are four 4-bit I/O ports P1, P2, P4, and P5. Any I/O can be individually programmed as either input pull low or output. Any valid data transition (H→ L or L→H) of P1, P2, P4, and P5 can reactivate the chip when it is in power-down stage.



I/O Port Configuration

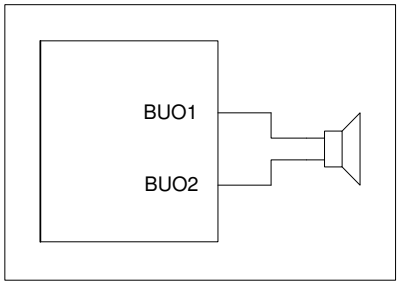
Note:

(1) ***Weak N-MOS can serve as pull-low resistor.***

(2) ***The driving/sink current of P2 & P5 is up to 8mA/16mA***

5.7 PWM Output

An PWM circuit is built-in SNC15120P. The maximum resolution of PWM is 8 bits. Two huge output stage circuits are designed in SNC15120P. With this advanced circuit, the chip is capable of driving speaker directly without external transistors.



PWM Output

5.8 Watch Dog Timer

SNC15120P built an internal WDT (Watch Dog Timer). This Watchdog timer would issue resets signal to this chip if it is not cleared before reaching terminal count (1sec). The watchdog timer is enabled at reset and cannot be disabled.

5.9 IR Function

P23 can be modulated with 38.5KHz square wave before sent out to P23 pin. The IR signal can be achieved by this modulated signal.

6. ABSOLUTE MAXIMUM RATING

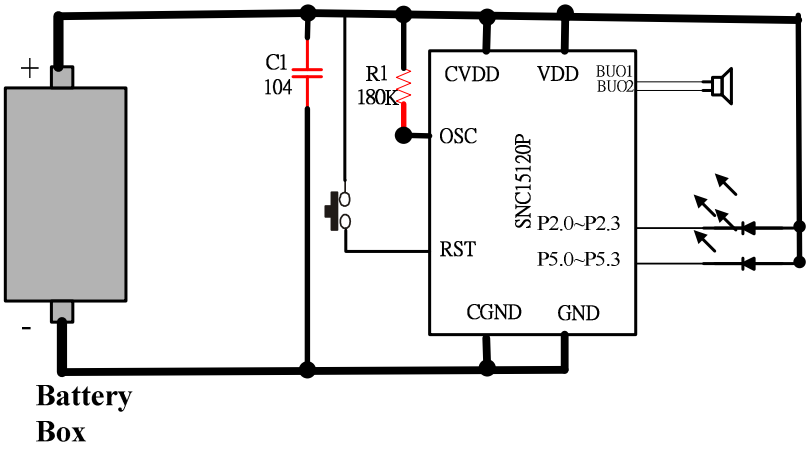
Items	Symbol	Min	Max	Unit.
Supply Voltage	V_{DD}-V	-0.3	+3.7	V
Input Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
Operating Temperature	T_{OP}	0	55.0	°C
Storage Temperature	T_{STG}	-55.0	+125.0	°C

7. ELECTRICAL CHARACTERISTICS

Item	Sym.	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.4	3.0	3.6	V	
Standby current	I_{SBY}	-	2.0	-	uA	V_{DD}=3.0V, no load
Program mode Voltage	V_{PP}	7.25	7.5	7.75	V	OTP Programming Voltage In Normal Mode Vpp can be floating.
Operating Current	I_{OPR}	-	10	-	mA	V_{DD}=3V, no load
Input current of P1, P2, P4, P5	I_{IH}	-	3.0	-	uA	V_{DD}=3V,V_{IN}=3V
Drive current of P1, P4	I_{OD}		4	-	mA	V_{DD}=3V,V_O=2.4V
Sink Current of P1, P4	I_{OS}		6	-	mA	V_{DD}=3V,V_O=0.4V
Drive current of P2, P5	I_{OD}		8	-	mA	V_{DD}=3V,V_O=2.4V
Sink current of P2, P5	I_{OS}		16	-	mA	V_{DD}=3V,V_O=2.4V
PWM Drive current	I_{PP}	-	400	-	mA	VDD=3V,Vbou=1.5V
Oscillation Freq.	F_{OSC}	-	2.0	-	MHz	V_{DD}=3V

8. APPLICATION Circuit

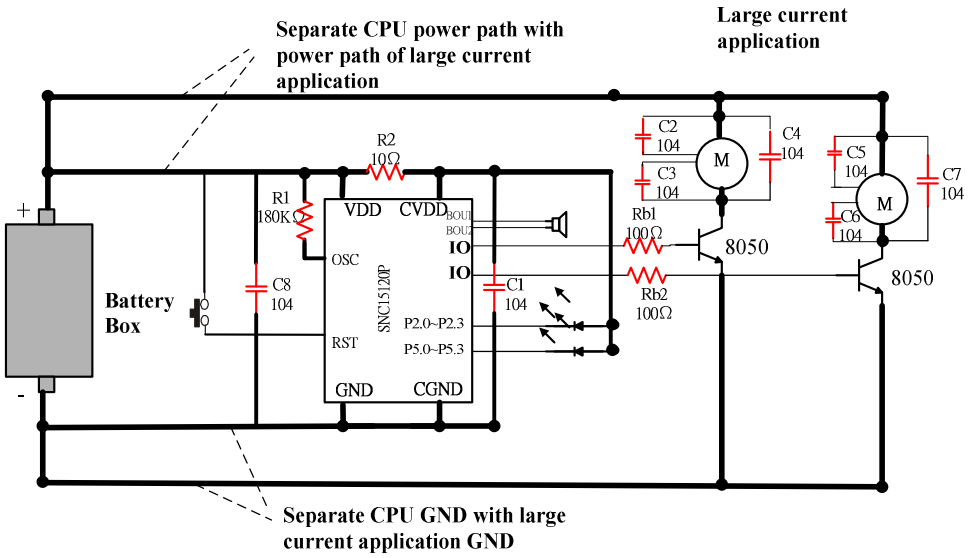
8.1 General application



1. It is suggested to add a capacitor (C1), 104, between VDD with GND to keep power stable with general application. And this capacitor is strongly suggested to be as close to the chip as possible.

2. It is suggested that VDD = 2.4V~3.6V

8.2 Motor application



There are some suggestions about PCB layout when user use SNC15120P IC with motor applications.

(1) The capacitor C1 、C8 (104) is strongly suggested to be as close to the chip as possible.
(2) It had better let OSC components (R) get close to IC chip.

(3) OSC components had better get far away large current applications.

(4) Separate IC power path with large current application power path to avoid affect IC working by power drop from large current application.

(5) R2 (10Ω)separate VDDIO and CVDD.

(6) Let power cable thicker, especially for large current application.

(7) C2 、C3 、C4 and C5、C6、C7 (104) are connected at the shell of motor, positive point and negative point of the motor.

(8) It is suggested that VDD = 2.4V~3.6V.

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