



# SANYO Semiconductors

## DATA SHEET

# LC87F7H32A

CMOS IC  
32K-byte FROM and 2048-byte RAM integrated  
**8-bit 1-chip Microcontroller**

### Overview

The SANYO LC87F7H32A is an 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 250ns, integrates on a single chip a number of hardware features such as 32K-byte flash ROM (onboard programmable), 2048-byte RAM, an on-chip debugger, a LCD controller/driver, sophisticated 16-bit timer/counter (may be divided into 8-bit timers), a 16-bit timer/counter (may be divided into 8-bit timers/counters or 8-bit PWMs), four 8-bit timers with a prescaler, a real time clock function (RTC), a synchronous SIO interface (with automatic block transmission/reception capabilities), an asynchronous/synchronous SIO interface, a UART interface (full duplex), a 12-bit/8-bit 7-channel AD converter, a high-speed clock counter, a system clock frequency divider, a power on reset function and a 21-source 10-vector interrupt feature.

### Features

#### ■Flash ROM

- Capable of on-board-programming with wide range, 3.0 to 5.5V, of voltage source.
- Block-erasable in 128 byte units
- 32768 × 8 bits

#### ■RAM

- 2048 × 9 bits

#### ■Minimum Bus Cycle

- 250ns (4MHz)  $V_{DD}=2.4V$  to 3.6V

Note: The bus cycle time here refers to the ROM read speed.

#### ■Minimum instruction cycle time

- 750ns (4MHz)  $V_{DD}=2.4$  to 3.6V

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## LC87F7H32A

### ■Temperature range

- -40°C to +85°C

### ■Ports

- Input/output ports
  - Data direction programmable for each bit individually: 21 (P0n, P1n, P30, P70-P73)
  - Other function
    - Input ports(for debugger): 3 (DBGP0(P05)-DBGP2(P07))
    - LCD ports (segment output): 8 (P1n)
- LCD ports & General I/O ports
  - Segment output: 32 (S00-S31)
  - Common output: 4 (COM0-COM3)
  - Bias terminals for LCD driver 5 (V1-V3, CUP1, CUP2)
  - Other functions
    - Input/output ports: 36 (LPA<sub>n</sub>, LPB<sub>n</sub>, LPC<sub>n</sub>, LPL<sub>n</sub>, P1n)
- Oscillator pins: 4 (CF1, CF2, XT1, XT2)
- Reset pin: 1 ( $\overline{\text{RES}}$ )
- Power supply: 5 (VSS1-2, VDD1-2, V2)

### ■LCD Controller

- (1) Seven display modes are available
- (2) Duty 1/3duty, 1/4duty
- (3) Bias 1/2bias, 1/3bias
- (4) Segment/common output can be switched to general purpose input/output ports.
- (5) LCD power range
  - 1) 1/3bias
    - V1 : 0.8V to 1.2V
    - V2 : 1.2V to 2.4V
    - V3 : 2.4V to 3.6V
    - Please use the LCD panel for V<sub>DD</sub>[V], when you select 1/3bias.
  - 2) 1/2bias
    - V1 : 1.2V to 1.8V
    - V2 : 2.4V to 3.6V
    - V3 : 2.4V to 3.6V
    - (connect V2 and V3)
    - Please use the LCD panel for V<sub>DD</sub>[V], when you select 1/2bias.

### ■Timers

- Timer 0: 16 bit timer / counter with capture register
  - Mode 0: 2 channel 8-bit timer with programmable 8 bit prescaler and 8 bit capture register
  - Mode 1: 8 bit timer with 8 bit programmable prescaler and 8 bit capture register + 8 bit Counter with 8-bit capture register
  - Mode 2: 16 bit timer with 8 bit programmable prescaler and 16 bit capture register
  - Mode 3: 16 bit counter with 16 bit capture register
- Timer 1: PWM / 16 bit timer/ counter with toggle output function
  - Mode 0: 2 channel 8 bit timer/ counter (with toggle output)
  - Mode 1: 2 channel 8 bit PWM
  - Mode 2: 16 bit timer/ counter (with toggle output) Toggle output from lower 8 bits is also possible.
  - Mode 3: 16 bit timer (with toggle output) Lower order 8 bits can be used as PWM.
- Timer 4: 8-bit timer with 6-bit prescaler
- Timer 5: 8-bit timer with 6-bit prescaler
- Timer 6: 8-bit timer with 6-bit prescaler (with toggle output)
- Timer 7: 8-bit timer with 6-bit prescaler (with toggle output)
- Base Timer
  - (1) The clock signal can be selected from any of the following:
    - Sub-clock (32.768kHz crystal oscillator / Slow RC oscillation), system clock, and prescaler output from timer 0.
  - (2) Interrupts of five different time intervals are possible.

## ■High-speed Clock Counter

- (1) Can count clocks with a maximum clock rate of 8MHz (at a main clock of 4MHz).
- (2) Can generate output real-time.

## ■Serial-interface

### • SIO 0: 8 bit synchronous serial interface

- (1) Synchronous 8-bit serial I/O (2- or 3-wire system, clock rates of (4/3) to (512/3) tCYC)
- (2) Continuous data transmission/reception (Variable length data transmission in bit units from 1 to 256 bits, clock rates of (4/3) to (512/3) tCYC)
- (3) Bi-phase modulation (Manchester, Bi-phase-Space) data transmission
- (4) LSB first / MSB first is selectable
- (5) SPI\_function: serial interface that can release HOLD/X'tal HOLD mode after receiving 1-byte (8-bit clock).

### • SIO 1: 8 bit asynchronous / synchronous serial interface

- Mode 0: Synchronous 8 bit serial IO (2-wire or 3-wire, transmit clock 2–512 tCYC)
- Mode 1: Asynchronous serial IO (half duplex, 8 data bits, 1 stop bit, baud rate 8–2048 tCYC)
- Mode 2: Bus mode 1 (start bit, 8 data bits, transmit clock 2–512 tCYC)
- Mode 3: Bus mode 2 (start detection, 8 data bits, stop detection)

## ■UART

- Full duplex
- 7/8/9 bit data bits selectable
- 1 stop bit (2-bit in continuous data transmission)
- Built-in baudrate generator
- Operating mode: Programmable transfer mode, fixed-rate transfer mode
- Transmission data conversion: Normal (NRZ), Manchester encoding

## ■AD converter: 12 bits/8 bits × 7 channels

- 12 bits/8 bits AD converter resolution selectable

## ■Remote Control Receiver Circuit (Connected to P73 / INT3 / T0IN terminal)

- Noise rejection function (Noise rejection filter's time constant can be selected from 1 / 32 / 128 tCYC)

## ■Watchdog Timer

- Watchdog timer can produce interrupt or system reset.
- Watchdog timer has two types.
  - (1) Use an external RC circuit
  - (2) Use the microcontroller's basetimer
- Watchdog timer that used basetimer can select only one period (1 / 2 / 4 / 8 s) by the user option.

## ■Buzzer Output

- The buzzer output can transmitted from P17 by using basetimer.

## ■Real Time Clock (RTC)

- (1) Used with a basetimer, it can be used as a century + year + month + day + hour + minute + second counter.
- (2) Calendar counts up to December 31, 2799 with automatic leap-year calculation.
- (3) Gregorian calendar capable of keeping GMT (Greenwich Mean Time).

## ■Internal Reset Function

- Power-On-Reset (POR) function
  - POR resets the system when the power supply voltage is applied.

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### ■Interrupts: 21 sources, 10 vectors

- (1) Three priority (Low, high and highest) multiple interrupts are supported. During interrupt handling, an equal or lower priority interrupt request is postponed.
- (2) If interrupt requests to two or more vector addresses occur at once, the higher priority interrupt takes precedence. In the case of equal priority levels, the vector with the lowest address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L
4	0001BH	H or L	INT3/Base timer/RTC
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0/UART1-receive
8	0003BH	H or L	SIO1/UART-send
9	00043H	H or L	ADC/T6/T7/SPI
10	0004BH	H or L	Port 0/T4/T5

- Priority levels  $X > H > L$
- For equal priority levels, vector with lowest address takes precedence

### ■Subroutine Stack Levels: 1024 levels max. Stack is located in RAM.

### ■High-speed Multiplication/Division Instructions

- 16 bits  $\times$  8 bits (5 tCYC execution time)
- 24 bits  $\times$  16 bits (12 tCYC execution time)
- 16 bits  $\div$  8 bits (8 tCYC execution time)
- 24 bits  $\div$  16 bits (12 tCYC execution time)

### ■Oscillation Circuits

- On-chip fast RC oscillation (Typical: 500kHz) for system clock use.
- On-chip slow RC oscillation (Typical: 50kHz) for system clock use.
- CF oscillation (4MHz) for system clock use. (Rf built in, Rd external)
- Crystal oscillation (32.768kHz) low speed system clock use. (Rf built in)
- Frequency variable RC oscillation circuit (internal): For system clock.
  - (1) Adjustable in  $\pm 4\%$  (typ.) step from a selected center frequency.
  - (2) Measures oscillation clock using an input signal from XT1 as a reference.

### ■System Clock Divider

- Low power consumption operation is available.
- Minimum instruction cycle time (750ns, 1.5 $\mu$ s, 3.0 $\mu$ s, 6.0 $\mu$ s, 12 $\mu$ s, 24 $\mu$ s, 48 $\mu$ s, 96 $\mu$ s, 192 $\mu$ s can be switched by program. (when using 4MHz main clock)

### ■System Clock Output

- The system clock output can be transmitted from P04.

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## ■ Standby Function

### • HALT mode

HALT mode is used to reduce power consumption. During the HALT mode, program execution is stopped but peripheral circuits keep operating (Some parts of serial transfer operation stop.)

- (1) Oscillation circuits are not stopped automatically.
- (2) Released by the system reset or interrupts.

### • HOLD mode

HOLD mode is used to reduce power consumption. Program execution and peripheral circuits are stopped.

- (1) CF, RC and crystal oscillation circuits stop automatically.
- (2) Released by any of the following conditions.
  - 1) Low level input to the reset pin
  - 2) Watchdog timer interrupt
  - 3) Specified level input to one of INT0, INT1, INT2
  - 4) Port 0 interrupt
  - 5) SPI interrupt by receiving 1-byte (8-bit clock)

### • X'tal HOLD mode

X'tal HOLD mode is used to reduce power consumption. Program execution is stopped.

All peripheral circuits except the base timer are stopped.

- (1) CF and RC oscillation circuits stop automatically.
- (2) Crystal oscillator operation is kept in its state at HOLD mode inception.
- (3) Released by any of the following conditions.
  - 1) Low level input to the reset pin
  - 2) Watchdog timer interrupt
  - 3) Specified level input to one of INT0, INT1, INT2
  - 4) Port 0 interrupt
  - 5) Base-timer interrupt
  - 6) RTC interrupt
  - 7) SPI interrupt by receiving 1-byte (8-bit clock)

## ■ Onchip Debugger

- Supports software debugging with the IC mounted on the target board.

## ■ Shipping Form

- QIP64E (14×14) (Lead-/Halogen-free type)
- SQFP64 (10×10) (Lead-/Halogen-free type)

## ■ Development Tools

- On-chip debugger: TCB87 TypeB+LC87F7H32A

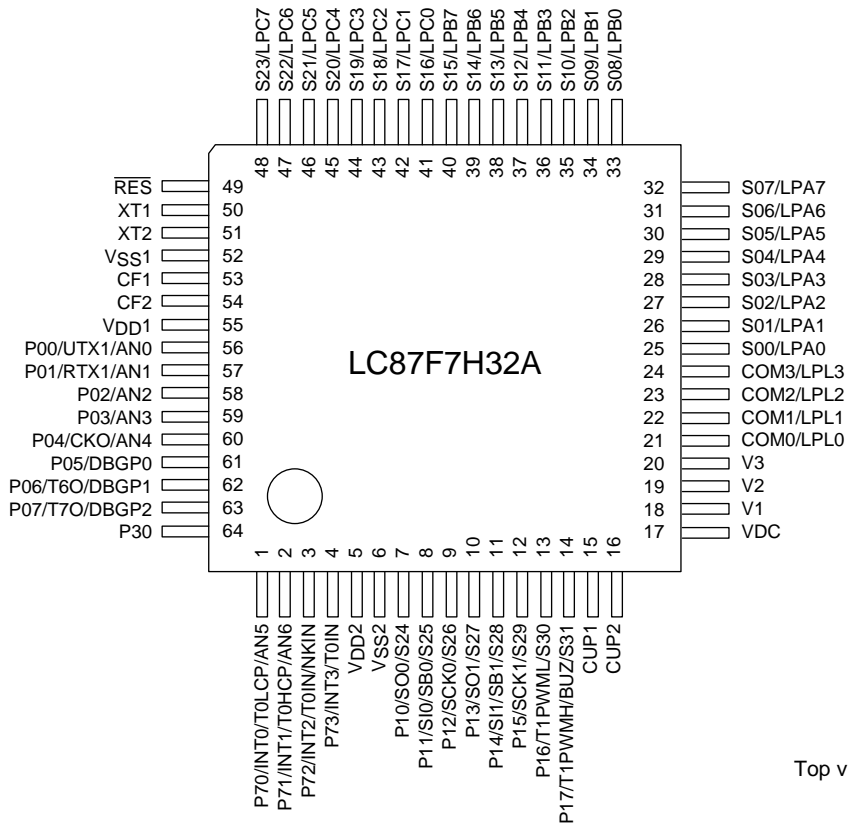
## ■ Flash ROM Programming Boards

Package	Programming boards
QIP64E (14×14)	W87F70256Q
SQFP64 (10×10)	W87F79256SQ



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## Pin Assignment



Top view

SANYO: QIP64E (14×14) “Lead-/Halogen-free type”  
 SANYO: SQFP64 (10×10) “Lead-/Halogen-free type”

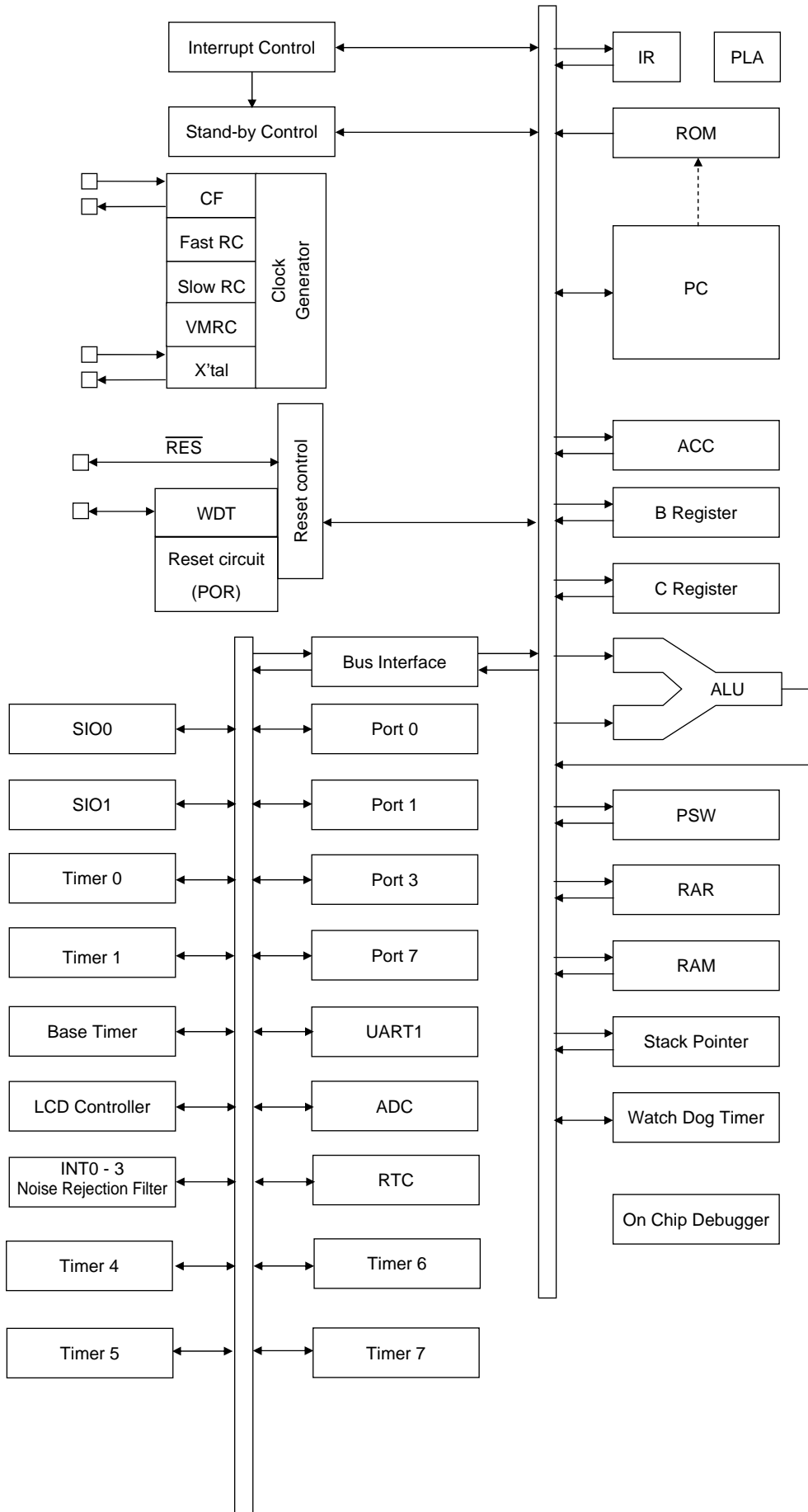
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PIN No.	NAME
1	P70/INT0/T0LCP/AN5
2	P71/INT1/T0HCP/AN6
3	P72/INT2/T0IN/NKIN
4	P73/INT3/T0IN
5	V <sub>DD2</sub>
6	V <sub>SS2</sub>
7	P10/SO0/S24
8	P11/SI0/SB0/S25
9	P12/SCK0/S26
10	P13/SO1/S27
11	P14/SI1/SB1/S28
12	P15/SCK1/S29
13	P16/T1PWML/S30
14	P17/T1PWMLH/BUZ/S31
15	CUP1
16	CUP2
17	VDC
18	V1
19	V2
20	V3
21	COM0/LPL0
22	COM1/LPL1
23	COM2/LPL2
24	COM3/LPL3
25	S00/LPA0
26	S01/LPA1
27	S02/LPA2
28	S03/LPA3
29	S04/LPA4
30	S05/LPA5
31	S06/LPA6
32	S07/LPA7

PIN NO.	NAME
33	S08/LPB0
34	S09/LPB1
35	S10/LPB2
36	S11/LPB3
37	S12/LPB4
38	S13/LPB5
39	S14/LPB6
40	S15/LPB7
41	S16/LPC0
42	S17/LPC1
43	S18/LPC2
44	S19/LPC3
45	S20/LPC4
46	S21/LPC5
47	S22/LPC6
48	S23/LPC7
49	$\overline{\text{RES}}$
50	XT1
51	XT2
52	V <sub>SS1</sub>
53	CF1
54	CF2
55	V <sub>DD1</sub>
56	P00/UTX1/AN0
57	P01/RTX1/AN1
58	P02/AN2
59	P03/AN3
60	P04/CKO/AN4
61	P05/DBGP0
62	P06/T6O/DBGP1
63	P07/T7O/DBGP2
64	P30



System Block Diagram



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## Pin Assignment

Pin name	I/O	Function	Option																														
V <sub>SS1</sub> , V <sub>SS2</sub>	-	• Power supply (-)	No																														
V <sub>DD1</sub> , V <sub>DD2</sub>	-	• Power supply (+)	No																														
VDC	-	• Internal voltage	No																														
CUP1, CUP2	-	• Capacitor connecting terminals for step-up/step-down	No																														
PORT0 P00 to P07	I/O	<ul style="list-style-type: none"> <li>• 8bit input/output port</li> <li>• Data direction programmable for each bit</li> <li>• Use of pull-up resistor can be specified for each bit individually</li> <li>• Input for HOLD release</li> <li>• Input for port 0 interrupt</li> <li>• Other pin functions P00: UART1-send P01: UART1-receive P04: System clock output (CKO) P05: DBGPO (LC87F7H32A) P06: T6O/DBGP1 (LC87F7H32A) P07: T7O/DBGP2 (LC87F7H32A) AD converter input ports: AN0 (P00) – AN4 (P04)</li> </ul>	Yes																														
PORT1 P10/S24 to P17/S31	I/O	<ul style="list-style-type: none"> <li>• 8bit input/output port</li> <li>• Data direction programmable for each bit</li> <li>• Use of pull-up resistor can be specified for each bit individually</li> <li>• Other pin functions P10: SIO0 data output P11: SIO0 data input or bus input/output P12: SIO0 clock input/output P13: SIO1 data output P14: SIO1 data input or bus input/output P15: SIO1 clock input/output P16: Timer 1 PWML output P17: Timer 1 PWMH output/Buzzer output Segment output for LCD: S24 (P10) – S31 (S17)</li> </ul>	Yes																														
PORT3 P30	I/O	<ul style="list-style-type: none"> <li>• 1bit Input/output port</li> <li>• Data direction programmable</li> <li>• Use of pull-up resistor can be specified</li> </ul>	Yes																														
PORT7 P70 to P73	I/O	<ul style="list-style-type: none"> <li>• 4bit Input/output port</li> <li>• Data direction can be specified for each bit</li> <li>• Use of pull-up resistor can be specified for each bit individually</li> <li>• Other functions P70: INT0 input/HOLD release input/Timer0L capture input/output for watchdog timer P71: INT1 input/HOLD release input/Timer0H capture input P72: INT2 input/HOLD release input/timer 0 event input/Timer0L capture input/NKIN P73: INT3 input (noise rejection filter attached)/timer 0 event input/Timer0H capture input AD converter input ports: AN5 (P70), AN6 (P71)</li> <li>• Interrupt detection selection <table border="1" style="margin-left: 20px;"> <thead> <tr> <th></th> <th>Rising</th> <th>Falling</th> <th>Rising and falling</th> <th>H level</th> <th>L level</th> </tr> </thead> <tbody> <tr> <td>INT0</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> </tr> <tr> <td>INT1</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> </tr> <tr> <td>INT2</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> </tr> <tr> <td>INT3</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> </tr> </tbody> </table> </li> </ul>		Rising	Falling	Rising and falling	H level	L level	INT0	enable	enable	disable	enable	enable	INT1	enable	enable	disable	enable	enable	INT2	enable	enable	enable	disable	disable	INT3	enable	enable	enable	disable	disable	No
	Rising	Falling	Rising and falling	H level	L level																												
INT0	enable	enable	disable	enable	enable																												
INT1	enable	enable	disable	enable	enable																												
INT2	enable	enable	enable	disable	disable																												
INT3	enable	enable	enable	disable	disable																												

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Pin name	I/O	Function description	Option
S00/LPA0 to S07/LPA7	I/O	<ul style="list-style-type: none"> <li>Segment output for LCD</li> <li>Can be used as general purpose input/output port (LPA)</li> </ul>	No
S08/LPB0 to S15/LPB7	I/O	<ul style="list-style-type: none"> <li>Segment output for LCD</li> <li>Can be used as general purpose input/output port (LPB)</li> </ul>	No
S16/LPC0 to S23/LPC7	I/O	<ul style="list-style-type: none"> <li>Segment output for LCD</li> <li>Can be used as general purpose input/output port (LPC)</li> </ul>	No
COM0/LPL0 to COM3/LPL3	I/O	<ul style="list-style-type: none"> <li>Common output for LCD</li> <li>Can be used as general purpose input/output port (LPL)</li> </ul>	No
V1, V2, V3	I/O	<ul style="list-style-type: none"> <li>LCD output bias power supply</li> </ul>	No
$\overline{\text{RES}}$	I	<ul style="list-style-type: none"> <li>Reset terminal</li> </ul>	No
XT1	I/O	<ul style="list-style-type: none"> <li>Input for 32.768kHz crystal oscillation</li> <li>When not in use, connect to <math>V_{DD1}</math></li> </ul>	No
XT2	I/O	<ul style="list-style-type: none"> <li>Output for 32.768kHz crystal oscillation</li> <li>When not in use, set to oscillation mode and leave open</li> </ul>	No
CF1	I	<ul style="list-style-type: none"> <li>Input terminal for ceramic oscillator</li> <li>When not in use, connect to <math>V_{DD1}</math></li> </ul>	No
CF2	O	<ul style="list-style-type: none"> <li>Output terminal for ceramic oscillator</li> <li>When not in use, leave open</li> </ul>	No

### Port Configuration

Port form and pull-up resistor options are shown in the following table.

Port status can be read even when port is set to output mode.

Terminal	Option applies to:	Options	Output Form	Pull-up resistor
P00 to P07	each bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P10 to P17	each bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P30	-	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	None	Nch-open drain	Programmable
P71 to P73	-	None	CMOS	Programmable
S00(LPA0) to S23(LPC7)	-	None	CMOS	None
			P-ch Open Drain	
			N-ch Open Drain	
COM0(LPL0) to COM3(LPL3)	-	None	CMOS	None
			P-ch Open Drain	
			N-ch Open Drain	
XT1	-	None	Input only	None
XT2	-	None	32.768kHz crystal oscillator output	None
			Nch-open drain when selected as normal port	

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## User Option Table

Option name	Option to be applied on	Mask version *1	Flash-ROM version	Option Selected in units of	Option selection
Port output type	P00 to P07		○	1 bit	CMOS
					Nch-open drain
	P10 to P17		○	1 bit	CMOS
					Nch-open drain
	P30		○	1 bit	CMOS
					Nch-open drain
Basetimer watchdog timer	Watchdog timer period		○	-	1s
					2s
					4s
					8s
Program start address	-	*2	○	-	00000h
					07E00h

\*1: Mask option selection-No change possible after mask is completed.

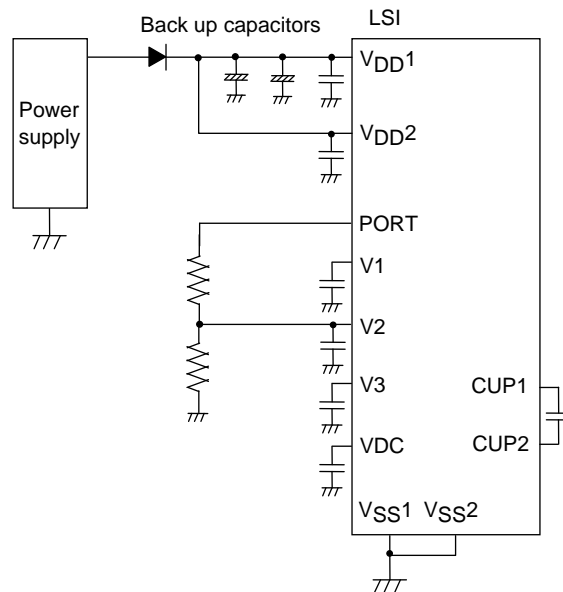
\*2: Program start address of the mask version is 00000h.

\*Note 1: Connect as follows to reduce noise on VDD.

VSS1 and VSS2 must be connected together and grounded.

\*Note 2: The power supply for the internal memory is VDD2. VDD1 and VDD2 are used as the power supply for ports. When VDD1 and VDD2 are not backed up, the port level does not become "H" even if the port latch is in the "H" level. Therefore, when VDD1 and VDD2 are not backed up and the port latch is "H" level, the port level is unstable in the HOLD mode, and the back up time becomes shorter because the through current runs from VDD to GND in the input buffer.

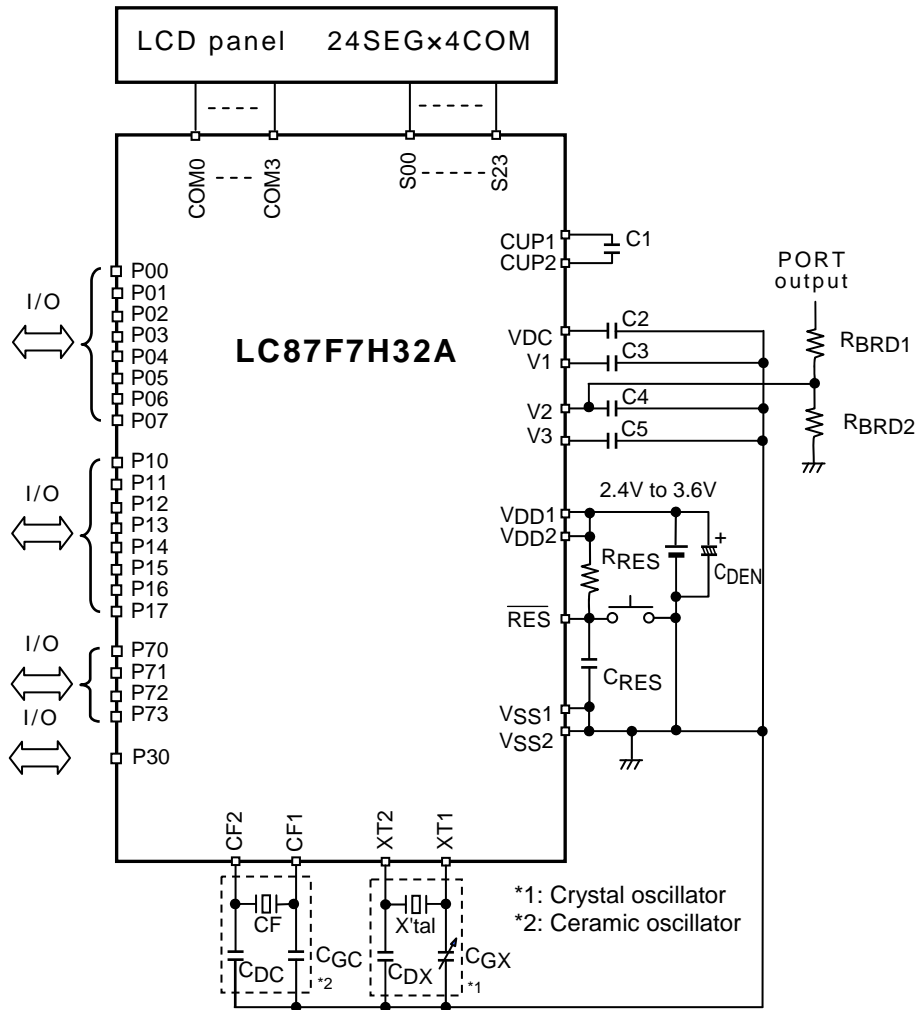
If VDD1 and VDD2 are not backed up, output "L" by the program or pull the port to "L" by the external circuit in the HOLD mode so that the port level becomes "L" level and unnecessary current consumption is prevented.



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## Circuit Example

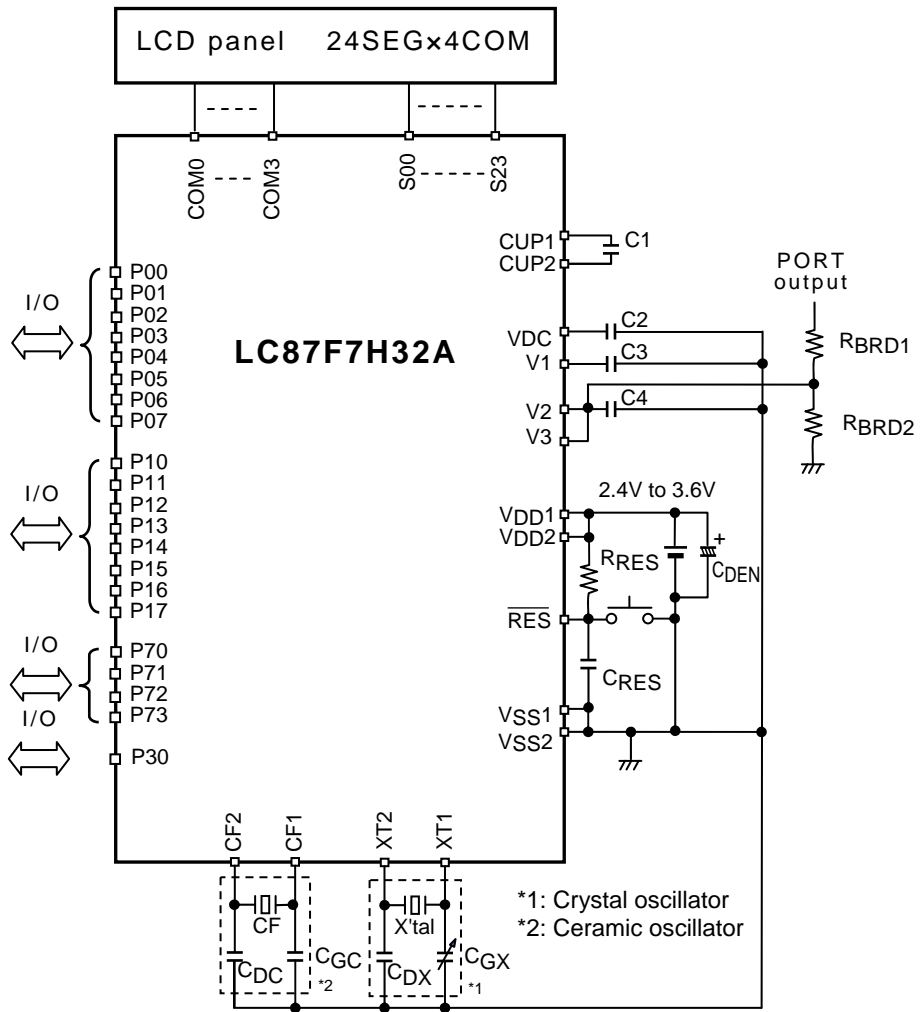
(1)1/3bias, 1/4duty



X'tal	Crystal oscillation	Refer to Page 25 (Characteristic of clock oscillator circuit)
CGX	Trimmer capacitor	
CDX	Capacitor for crystal oscillation	
CF	Ceramic oscillation	Refer to Page 25 (Characteristic of clock oscillator circuit)
CGC	Capacitor for ceramic oscillation	
CDX	Capacitor for ceramic oscillation	
C1 to C5	Capacitor	0.1μF
CDEN	Electrolytic capacitor	Back up
CRES	Capacitor for $\overline{\text{RES}}$	Refer to User's manual "RESET Function"
RRES	Resistor for $\overline{\text{RES}}$	
RBRD1	Breeder Resistor	Adjust to LCD panel
RBRD2	Breeder Resistor	

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(2)1/2bias, 1/3duty



X'tal	Crystal oscillation	Refer to Page 25 (Characteristic of clock oscillator circuit)
CGX	Trimmer capacitor	
CDX	Capacitor for crystal oscillation	
CF	Ceramic oscillation	Refer to Page 25 (Characteristic of clock oscillator circuit)
CGC	Capacitor for ceramic oscillation	
CDG	Capacitor for ceramic oscillation	
C1 to C4	Capacitor	0.1μF
CDEN	Electrolytic capacitor	Back up
CRES	Capacitor for $\overline{\text{RES}}$	Refer to User's manual "RESET Function"
RRES	Resistor for $\overline{\text{RES}}$	
RBRD1	Breeder Resistor	Adjust to LCD panel
RBRD2	Breeder Resistor	

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### Absolute Maximum Ratings at Ta=25°C and VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	Specification				unit	
				VDD[V]	min	typ	max		
Supply voltage	VDD max	VDD1, VDD2	VDD1=VDD2		-0.3		+4.3	V	
Supply voltage For LCD	VLCD	V1			-0.3		1/3VDD		
		V2			-0.3		2/3VDD		
		V3			-0.3		VDD		
Input voltage	VI	XT1, CF1, RES			-0.3		VDD+0.3		
Input/Output voltage	VI/O(1)	<ul style="list-style-type: none"> <li>• Port0, 1, 3, 7</li> <li>• LPA, LPB, LPC</li> <li>• LPL, XT2</li> </ul>			-0.3		VDD+0.3		
High level output current	Peak output current	IOPH(1)	Port 0, 1	<ul style="list-style-type: none"> <li>• CMOS output selected</li> <li>• Current at each pin</li> </ul>		-10		mA	
		IOPH(2)	Port 3	<ul style="list-style-type: none"> <li>• CMOS output selected</li> </ul>		-20			
		IOPH(3)	LPA, LPB, LPC LPL	<ul style="list-style-type: none"> <li>• CMOS output selected</li> <li>• Current at each pin</li> </ul>		-4			
		IOPH(4)	Port71 to P73	<ul style="list-style-type: none"> <li>• Current at each pin</li> </ul>		-5			
	Total output current	ΣIOAH(1)	Port 0	Total of all pins		-20			
		ΣIOAH(2)	Port 3, 7	Total of all pins		-30			
		ΣIOAH(3)	Port 1	Total of all pins		-20			
		ΣIOAH(4)	Port 1, 3, 7	Total of all pins		-45			
		ΣIOAH(5)	LPA, LPB, LPC, LPL	Total of all pins		-30			
Low level output current	Peak output current	IOPL(1)	Port 0, 1	Current at each pin			20		
		IOPL(2)	Port 3	Current at each pin			30		
		IOPL(3)	Port 7	Current at each pin			10		
		IOPL(4)	LPA, LPB, LPC, LPL	Current at each pin			6		
	Total output current	ΣIOAL(1)	Port 0	Total of all pins				40	
		ΣIOAL(2)	Port 3, 7	Total of all pins				50	
		ΣIOAL(3)	Port 1	Total of all pins				40	
		ΣIOAL(4)	Port 1, 3, 7	Total of all pins				65	
		ΣIOAL(5)	LPA, LPB, LPC, LPL	Total of all pins				60	
Maximum power consumption	Pd max	SQFP64 (10×10)	Ta = -40 to +85°C				192	mW	
		QIP64E (14×14)					267		
Operating temperature range	Topr				-40		85	°C	
Storage temperature range	Tstg				-55		125		

Note 1-1: The mean output current is a mean value measured over 100ms.

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## Allowable Operating Conditions at Ta=-40 to +85°C, V<sub>SS1</sub>=V<sub>SS2</sub>=0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification					
				V <sub>DD</sub> [V]	min	typ	max	unit	
Operating supply voltage (Note 2-1)	V <sub>DD</sub> (1)	V <sub>DD1</sub> =V <sub>DD2</sub>	0.75μs≤t <sub>CYC</sub> ≤200μs Normal mode		2.4		3.6	V	
Memory sustaining supply voltage	V <sub>H</sub> D	V <sub>DD1</sub> =V <sub>DD2</sub>	RAM and register contents sustained in HOLD mode.		2.2		3.6		
High level input voltage	V <sub>I</sub> H(1)	Port 0, 3 LPA, LPB, LPC, LPL	Output disabled	2.4 to 3.6	0.3V <sub>DD</sub> +0.7		V <sub>DD</sub>		
	V <sub>I</sub> H(2)	Port 1 Port 71 to 73 P70 port input / interrupt side	• Output disabled • When INT1V <sub>TSL</sub> =0 (P71 only)	2.4 to 3.6	0.3V <sub>DD</sub> +0.7		V <sub>DD</sub>		
	V <sub>I</sub> H(3)	P71 interrupt side	• Output disabled • When INT1V <sub>TSL</sub> =1	2.4 to 3.6	0.85V <sub>DD</sub>		V <sub>DD</sub>		
	V <sub>I</sub> H(4)	P70 watchdog timer Side	Output disabled	2.4 to 3.6	0.9V <sub>DD</sub>		V <sub>DD</sub>		
	V <sub>I</sub> H(5)	XT1, XT2, CF1, RES		2.4 to 3.6	0.75V <sub>DD</sub>		V <sub>DD</sub>		
Low level input voltage	V <sub>I</sub> L(1)	Port 0, 3 LPA, LPB, LPC, LPL	Output disabled	2.4 to 3.6	V <sub>SS</sub>		0.2V <sub>DD</sub>		
	V <sub>I</sub> L(2)	Port 1 Port 71 to 73 P70 port input / interrupt side	• Output disabled • When INT1V <sub>TSL</sub> =0 (P71 only)	2.4 to 3.6	V <sub>SS</sub>		0.2V <sub>DD</sub>		
	V <sub>I</sub> L(3)	P71 interrupt side	• Output disabled • When INT1V <sub>TSL</sub> =1	2.4 to 3.6	V <sub>SS</sub>		0.45V <sub>DD</sub>		
	V <sub>I</sub> L(4)	P70 watchdog timer side		2.4 to 3.6	V <sub>SS</sub>		0.8V <sub>DD</sub> -1.0		
	V <sub>I</sub> L(5)	XT1, XT2, CF1, RES		2.4 to 3.6	V <sub>SS</sub>		0.25V <sub>DD</sub>		
Instruction cycle time (Note 2.2)	t <sub>CYC</sub>			2.4 to 3.6			200		μs
External system clock frequency	F <sub>EXCF</sub> (1)	CF1	• CF2 pin open • System clock frequency division ratio = 1/1 • External system clock duty = 50±5%	2.4 to 3.6	0.1		4		MHz
			• CF2 pin open • System clock frequency division ratio = 1/2	2.4 to 3.6	0.2		8		
Oscillation frequency range (Note 2-3)	F <sub>m</sub> CF(1)	CF1, CF2	• 4MHz ceramic oscillation • See Fig. 1.	2.4 to 3.6		4		MHz	
	F <sub>m</sub> RC(1)		Internal Fast RC oscillation	2.4 to 3.6	250	500	750		
	F <sub>s</sub> RC(1)		Internal Slow RC oscillation	2.4 to 3.6	25	50	75		
	F <sub>s</sub> X <sup>tal</sup>	XT1, XT2	• 32.768kHz crystal oscillation • See Fig. 2.	2.4 to 3.6		32.768			kHz
Frequency variable RC oscillation usable range	OpVMRC(1)		When VMSL4M=0	3.0 to 3.6	8	10	12	MHz	
	OpVMRC(2)		When VMSL4M=1	2.4 to 3.6	3.5	4	4.5		
Frequency variable RC oscillation adjustment range	V <sub>m</sub> ADJ(1)		Each step of VMRAJn (Wide range)	2.4 to 3.6	8	24	64	%	
	V <sub>m</sub> ADJ(2)		Each step of VMFAJn (Small range)	2.4 to 3.6	1	4	8		

Note 2-1: V<sub>DD</sub> must be held greater than or equal to 3.0V in the flash ROM onboard programming mode.

Note 2-2: Relationship between t<sub>CYC</sub> and oscillation frequency is 3/F<sub>m</sub>CF at a division ratio of 1/1 and 6/F<sub>m</sub>CF at a division ratio of 1/2.

Note 2-3: See Tables 1 and 2 for the oscillation constants.



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## Electrical Characteristics at Ta=-40 to +85°C, V<sub>SS1</sub>=V<sub>SS2</sub>=0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V <sub>DD</sub> [V]	min	typ	max	unit
High level input current	I <sub>IH</sub> (1)	Port 0, 1, 3, 7 LPA, LPB, LPC LPL	<ul style="list-style-type: none"> <li>Output disabled</li> <li>Pull-up resistor off</li> <li>V<sub>IN</sub>=V<sub>DD</sub></li> <li>(Including output Tr's off leakage current)</li> </ul>	2.4 to 3.6			1	μA
	I <sub>IH</sub> (2)	$\overline{\text{RES}}$	V <sub>IN</sub> =V <sub>DD</sub>	2.4 to 3.6			1	
	I <sub>IH</sub> (3)	XT1, XT2	<ul style="list-style-type: none"> <li>For input port specification</li> <li>V<sub>IN</sub>=V<sub>DD</sub></li> </ul>	2.4 to 3.6			1	
	I <sub>IH</sub> (4)	CF1	V <sub>IN</sub> =V <sub>DD</sub>	2.4 to 3.6			15	
Low level input current	I <sub>IL</sub> (1)	Port 0, 1, 3, 7 LPA, LPB, LPC LPL	<ul style="list-style-type: none"> <li>Output disabled</li> <li>Pull-up resistor off</li> <li>V<sub>IN</sub>=V<sub>SS</sub></li> <li>(Including output Tr's off leakage current)</li> </ul>	2.4 to 3.6	-1			μA
	I <sub>IL</sub> (2)	$\overline{\text{RES}}$	V <sub>IN</sub> =V <sub>SS</sub>	2.4 to 3.6	-1			
	I <sub>IL</sub> (3)	XT1, XT2	<ul style="list-style-type: none"> <li>For input port specification</li> <li>V<sub>IN</sub>=V<sub>SS</sub></li> </ul>	2.4 to 3.6	-1			
	I <sub>IL</sub> (4)	CF1	V <sub>IN</sub> =V <sub>SS</sub>	2.4 to 3.6	-15			
High level output voltage	V <sub>OH</sub> (1)	Port 0, 1	I <sub>OH</sub> =-0.4mA	3.0 to 3.6	V <sub>DD</sub> -0.4			V
	V <sub>OH</sub> (2)		I <sub>OH</sub> =-0.2mA	2.4 to 3.6	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (3)	Port 3	I <sub>OH</sub> =-1.6mA	3.0 to 3.6	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (4)		I <sub>OH</sub> =-1mA	2.4 to 3.6	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (5)	Port 71 to 73	I <sub>OH</sub> =-0.4mA	3.0 to 3.6	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (6)		I <sub>OH</sub> =-0.2mA	2.4 to 3.6	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (7)	LPA, LPB, LPC LPL	I <sub>OH</sub> =-0.1mA	2.4 to 3.6	V <sub>DD</sub> -0.4			
Low level output voltage	V <sub>OL</sub> (1)	Port 0, 1	I <sub>OL</sub> =1.6mA	3.0 to 3.6			0.4	V
	V <sub>OL</sub> (2)		I <sub>OL</sub> =1mA	2.4 to 3.6			0.4	
	V <sub>OL</sub> (3)	Port 3	I <sub>OL</sub> =5mA	3.0 to 3.6			0.4	
	V <sub>OL</sub> (4)		I <sub>OL</sub> =2.5mA	2.4 to 3.6			0.4	
	V <sub>OL</sub> (5)	Port 7 XT2	I <sub>OL</sub> =1.6mA	3.0 to 3.6			0.4	
	V <sub>OL</sub> (6)		I <sub>OL</sub> =1mA	2.4 to 3.6			0.4	
	V <sub>OL</sub> (7)	LPA, LPB, LPC LPL	I <sub>OL</sub> =0.1mA	2.4 to 3.6			0.4	
LCD output voltage regulation	VODLS	S00 to S31	<ul style="list-style-type: none"> <li>I<sub>O</sub>=0mA</li> <li>V1, V2, V3 LCD level output</li> <li>See Fig. 8.</li> </ul>	2.4 to 3.6	0		±0.2	V
	VODLC	COM0 to COM3	<ul style="list-style-type: none"> <li>I<sub>O</sub>=0mA</li> <li>V1, V2, V3 LCD level output</li> <li>See Fig. 8.</li> </ul>	2.4 to 3.6	0		±0.2	
Resistance of pull-up MOS Tr.	Rpu(1)	Port 0, 1, 3, 7	V <sub>OH</sub> =0.9V <sub>DD</sub>	2.4 to 3.6	18	50	150	kΩ
Hysteresis voltage	VHYS(1)	Port 1, 7 $\overline{\text{RES}}$		2.4 to 3.6		0.1V <sub>DD</sub>		V
Pin capacitance	CP	All pins	<ul style="list-style-type: none"> <li>For pins other than that under test: V<sub>IN</sub>=V<sub>SS</sub></li> <li>f=1MHz</li> <li>Ta=25°C</li> </ul>	2.4 to 3.6		10		pF

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**Serial I/O Characteristics** at Ta = -40°C to +85°C, V<sub>SS1</sub> = V<sub>SS2</sub> = 0V

## 1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter	Symbol	Pin/Remarks	Conditions	V <sub>DD</sub> [V]	Specification								
					min	typ	max	unit					
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	2.4 to 3.6				tCYC				
		Low level pulse width	tSCKL(1)							See Fig. 6.	2		
		High level pulse width	tSCKH(1)	• Continuous data transmission/reception mode • See Fig. 6. • (Note 4-1-2)							1		
			tSCKHA(1)							4			
	Output clock	Frequency	tSCK(2)	SCK0(P12)	2.4 to 3.6				tSCK				
		Low level pulse width	tSCKL(2)							• CMOS output selected • See Fig. 6.	4/3		
High level pulse width		tSCKH(2)	• Continuous data transmission/reception mode • CMOS output selected • See Fig. 6.	1/2									
		tSCKHA(2)		1/2									
Serial input	Data setup time	tsDI(1)	SB0(P11), SIO(P11)	2.4 to 3.6									
	Data hold time	thDI(1)							0.03				
Serial output	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	2.4 to 3.6				μs					
									Input clock	• Continuous data transmission/reception mode • (Note 4-1-3)			(1/3)tCYC +0.05
													Output clock
		(Note 4-1-3)	2.4 to 3.6				(1/3)tCYC +0.15						

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SIORUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

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## 2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter	Symbol	Pin/Remarks	Conditions	Specification						
				V <sub>DD</sub> [V]	min	typ	max	unit		
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	See Fig. 6.	2.4 to 3.6	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected • See Fig. 6.	2.4 to 3.6	2			tSCK
		Low level pulse width	tSCKL(4)				1/2			
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time	tsDI(2)	SB1(P14), SI1(P14)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 6.	2.4 to 3.6	0.03			μs	
	Data hold time	thDI(2)				2.4 to 3.6	0.03			
Serial output	Output delay time	tdO(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 6.	2.4 to 3.6			(1/3)tCYC +0.05		

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

### Pulse Input Conditions at Ta = -40°C to +85°C, V<sub>SS1</sub> = V<sub>SS2</sub> = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V <sub>DD</sub> [V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72),	• Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled.	2.4 to 3.6	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.4 to 3.6	2			
	tPIH(3) tPIL(3)	INT3(P73) when noise filter time constant is 1/32	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.4 to 3.6	64			
	tPIH(4) tPIL(4)	INT3(P73) when noise filter time constant is 1/128	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.4 to 3.6	256			
	tPIL(5)	RES	Resetting is enabled.	2.4 to 3.6	200			μs

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### AD Converter Characteristics at $V_{SS1} = V_{SS2} = 0V$

<12bits AD Converter Mode at  $T_a = -40$  to  $+85^\circ C$ >

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				$V_{DD}[V]$	min	typ	max	unit
Resolution	N	AN0(P00) to AN4(P04), AN5(P70) to AN6(P71)		3.0 to 3.6		12		bit
Absolute accuracy	ET		(Note 6-1)	3.0 to 3.6			$\pm 16$	LSB
Conversion time	TCAD		• See Conversion time calculation formulas. (Note 6-2)	3.0 to 3.6	64		115	$\mu s$
Analog input voltage range	VAIN			3.0 to 3.6	$V_{SS}$		$V_{DD}$	V
Analog port input current	I <sub>A</sub> INH		VAIN= $V_{DD}$	3.0 to 3.6			1	$\mu A$
	I <sub>A</sub> INL	VAIN= $V_{SS}$	3.0 to 3.6	-1				

<8bits AD Converter Mode at  $T_a = -40$  to  $+85^\circ C$ >

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				$V_{DD}[V]$	min	typ	max	Unit
Resolution	N	AN0(P00) to AN4(P04), AN5(P70) to AN6(P71)		3.0 to 3.6		8		bit
Absolute accuracy	ET		(Note 6-1)	3.0 to 3.6			$\pm 1.5$	LSB
Conversion time	TCAD		• See Conversion time calculation formulas. (Note 6-2)	3.0 to 3.6	40		90	$\mu s$
Analog input voltage range	VAIN			3.0 to 3.6	$V_{SS}$		$V_{DD}$	V
Analog port input current	I <sub>A</sub> INH		VAIN= $V_{DD}$	3.0 to 3.6			1	$\mu A$
	I <sub>A</sub> INL	VAIN= $V_{SS}$	3.0 to 3.6	-1				

#### Conversion Time Calculation Formulas:

12bits AD Converter Mode :  $TCAD(\text{Conversion time}) = ((52/(\text{division ratio}))+2) \times (1/3) \times t_{CYC}$

8bits AD Converter Mode :  $TCAD(\text{Conversion time}) = ((32/(\text{division ratio}))+2) \times (1/3) \times t_{CYC}$

External oscillation (F <sub>m</sub> CF)	Operating supply voltage range ( $V_{DD}$ )	System division ratio (SYS <sub>DIV</sub> )	Cycle time (t <sub>CYC</sub> )	AD division ratio (ADDIV)	AD conversion time (TCAD)	
					12bit AD	8bit AD
CF-4MHz	3.0V to 3.6V	1/1	750ns	1/8	104.5 $\mu s$	64.5 $\mu s$

Note 6-1: The quantization error ( $\pm 1/2LSB$ ) must be excluded from the absolute accuracy. The absolute accuracy must be measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.

Note 6-2: The conversion time refers to the period from the time an instruction for starting a conversion process till the time the conversion results register(s) are loaded with a complete digital conversion value corresponding to the analog input value.

The conversion time is 2 times the normal-time conversion time when:

- The first AD conversion is performed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is performed after the AD conversion mode is switched from 8-bit to 12-bit conversion mode.

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### Current Consumption Characteristics at Ta = -40°C to +85°C, VSS1 = VSS2 = 0V

Parameter	Symbol	Pin	Conditions	Specification				
				V <sub>DD</sub> [V]	min	typ	max	unit
Current consumption during normal operation (Note 7-1)	IDDOP(1)	V <sub>DD1</sub> = V <sub>DD2</sub>	<ul style="list-style-type: none"> <li>• FmCF=4MHz Ceramic resonator oscillation</li> <li>• FsX'tal=32.768kHz crystal oscillation</li> <li>• System clock: CF 4MHz oscillation</li> <li>• Internal RC oscillation stopped.</li> <li>• Divider: 1/1</li> </ul>	2.4 to 3.6		2.0	4.2	mA
	IDDOP(2)		<ul style="list-style-type: none"> <li>• FmCF=0Hz (No oscillation)</li> <li>• FsX'tal=32.768kHz crystal oscillation</li> <li>• System clock: Fast RC oscillation</li> <li>• Divider: 1/1</li> </ul>	2.4 to 3.6		250	900	μA
	IDDOP(3)		<ul style="list-style-type: none"> <li>• FmCF=0Hz (No oscillation)</li> <li>• FsX'tal=32.768kHz crystal oscillation</li> <li>• System clock: Slow RC oscillation</li> <li>• Divider: 1/1</li> </ul>	2.4 to 3.6		30	120	
	IDDOP(4)		<ul style="list-style-type: none"> <li>• FmCF=0Hz (No oscillation)</li> <li>• FsX'tal=32.768kHz crystal oscillation</li> <li>• Internal RC oscillation stopped.</li> <li>• System clock: VMRC oscillation (4MHz)</li> <li>• Divider: 1/1</li> </ul>	2.4 to 3.6		2.0	5.4	mA
	IDDOP(5)		<ul style="list-style-type: none"> <li>• FmCF=0Hz (No oscillation)</li> <li>• FsX'tal=32.768kHz crystal oscillation</li> <li>• System clock: 32.768kHz</li> <li>• Internal RC oscillation stopped.</li> <li>• Divider: 1/1</li> <li>• Normal XT Amp mode</li> </ul>	2.4 to 3.6		20	86	μA
	IDDOP(6)		<ul style="list-style-type: none"> <li>• FmCF=0Hz (No oscillation)</li> <li>• FsX'tal=32.768kHz crystal oscillation</li> <li>• System clock: 32.768kHz</li> <li>• Internal RC oscillation stopped.</li> <li>• Divider: 1/1</li> <li>• Low XT Amp mode</li> </ul>	2.4 to 3.6		15	72	

Note 7-1: The currents through the output transistors and the pull-up MOS transistors are ignored.

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Continued from preceding page.

Parameter	Symbol	Pin	Conditions	Specification				
				V <sub>DD</sub> [V]	min	typ	max	unit
Current consumption during HALT mode (Note 7-1)	IDDHALT(1)	V <sub>DD1</sub> = V <sub>DD2</sub>	HALT mode • FmCF=4MHz Ceramic resonator oscillation • FsX'tal=32.768kHz crystal oscillation • System clock : CF 4MHz oscillation • Internal RC oscillation stopped • Divider: 1/1	2.4 to 3.6		0.55	1.55	mA
	IDDHALT(2)		HALT mode • FmCF=0Hz (No oscillation) • FsX'tal=32.768kHz crystal oscillation • System clock: Fast RC oscillation • Divider: 1/1	2.4 to 3.6		68	280	μA
	IDDHALT(3)		HALT mode • FmCF=0Hz (No oscillation) • FsX'tal=32.768kHz crystal oscillation • System clock: Slow RC oscillation • Divider: 1/1	2.4 to 3.6		7	85	
	IDDHALT(4)		HALT mode • FmCF=0Hz (No oscillation) • FsX'tal=32.768kHz crystal oscillation • Internal RC oscillation stopped • System clock: VMRC oscillation (4MHz) • Divider: 1/1	2.4 to 3.6		650	1460	
	IDDHALT(5)		HALT mode • FmCF=0Hz (Oscillation stop) • FsX'tal=32.768kHz crystal oscillation • System clock : 32.768kHz • Internal RC oscillation stopped • Divider: 1/1 • Normal XT Amp mode	2.4 to 3.6		8	70	
	IDDHALT(6)		HALT mode • FmCF=0Hz (Oscillation stop) • FsX'tal=32.768kHz crystal oscillation • System clock : 32.768kHz • Internal RC oscillation stopped • Divider: 1/1 • Low XT Amp mode	2.4 to 3.6		4	50	

Note 7-1: The currents through the output transistors and the pull-up MOS transistors are ignored.

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Continued from preceding page.

Parameter	Symbol	Pin	Conditions	Specification				
				V <sub>DD</sub> [V]	min	typ	max	unit
Current consumption during HOLD mode	IDDHOLD(1)	V <sub>DD1</sub> = V <sub>DD2</sub>	HOLD mode • CF1=V <sub>DD</sub> or open (when using external clock)	2.4 to 3.6		0.05	30	μA
Current consumption during Date/time clock HOLD mode	IDDHOLD(2)		Date/time clock HOLD mode • CF1=V <sub>DD</sub> or open (when using external clock) • FmX'tal=32.768kHz crystal oscillation • LCD display off • Normal XT Amp mode	2.4 to 3.6		6.5	67	
	IDDHOLD(3)		Date/time clock HOLD mode • CF1=V <sub>DD</sub> or open (when using external clock) • FmX'tal=32.768kHz crystal oscillation • LCD display off • Low XT Amp mode	2.4 to 3.6		0.45	46	
	IDDHOLD(4)		Date/time clock HOLD mode • CF1=V <sub>DD</sub> or open (when using external clock) • FsRC=Slow RC oscillation (Typ.50kHz) • LCD display off	2.4 to 3.6		1.5	70	

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## F-ROM Programming Characteristics at Ta = +10°C to +55°C, VSS1 = VSS2 = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				VDD[V]	min	typ	max	unit
Onboard programming current	IDDFW(1)	VDD1	<ul style="list-style-type: none"> <li>128-byte programming</li> <li>Erasing current included</li> </ul>	3.0 to 5.5		5	10	mA
Programming time	tFW(1)		Erasing time	3.0 to 5.5		20	30	ms
			Programming time			45	60	μs

## UART (Full Duplex) Operating Conditions at Ta = -40°C to +85°C, VSS1 = VSS2 = 0V

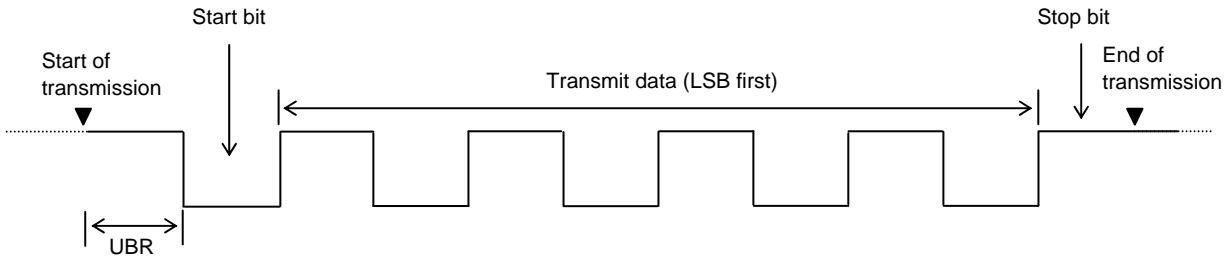
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				VDD[V]	min	typ	max	unit
Transfer rate	UBR	UTX(P00), URX(P01)		2.4 to 3.6	16/3		8192/3	tCYC

Data length: 7/8/9 bits (LSB first)

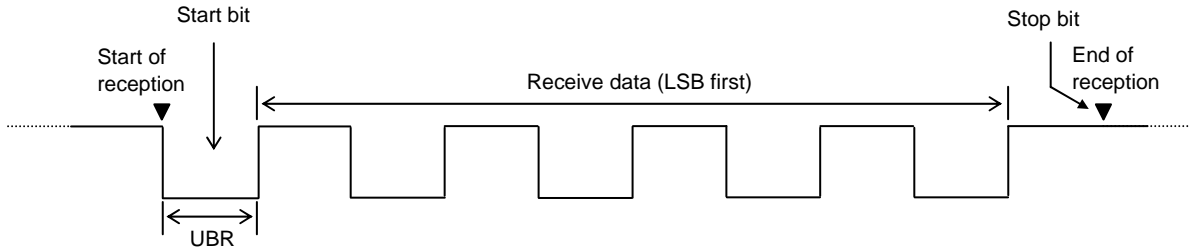
Stop bits: 1 bit (2-bit in continuous data transmission)

Parity bits: None

Example of 8-bit Data Transmission Mode Processing (Transmit Data=55H)



Example of 8-bit Data Reception Mode Processing (Receive Data=55H)





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## Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf1 [Ω]	Rd1 [Ω]		typ [ms]	max [ms]	
4.00MHz	Murata	CSTCR4M00G53-R0	(15)	(15)	Open	1k	2.4 to 3.6	0.03	0.15	Internal C1, C2
		CSTLS4M00G53-B0	(15)	(15)	Open	1k	2.4 to 3.6	0.02	0.15	

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after  $V_{DD}$  goes above the operating voltage lower limit (see Figure 4).

- Till the oscillation gets stabilized after the instruction for starting the main clock oscillation circuit is executed.
- Till the oscillation gets stabilized after the HOLD mode reset.
- Till the oscillation gets stabilized after the HOLD mode reset with CFSTOP(the OCR register bit0)=0.

## Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf2 [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768KHz	Epson Toyocom	MC-306	9	9	-	330k	2.4 to 3.6	1	3	CL=7.0pF Normal mode
			3	3	-	0	2.4 to 3.6	2	6	CL=7.0pF Low Amp mode

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode with EXTOSC (the OCR register bit6)=1 is reset (see Figure 4).

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

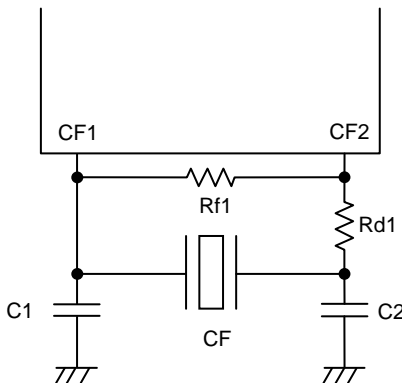


Figure 1 CF Oscillator Circuit

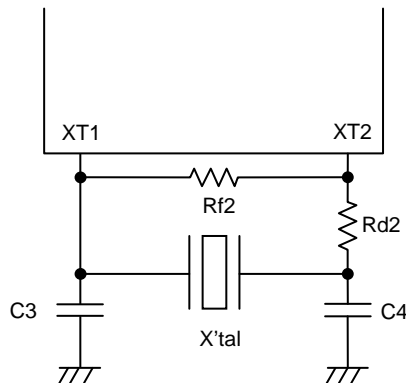


Figure 2 XT Oscillator Circuit

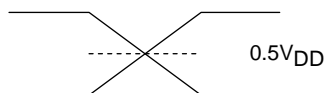
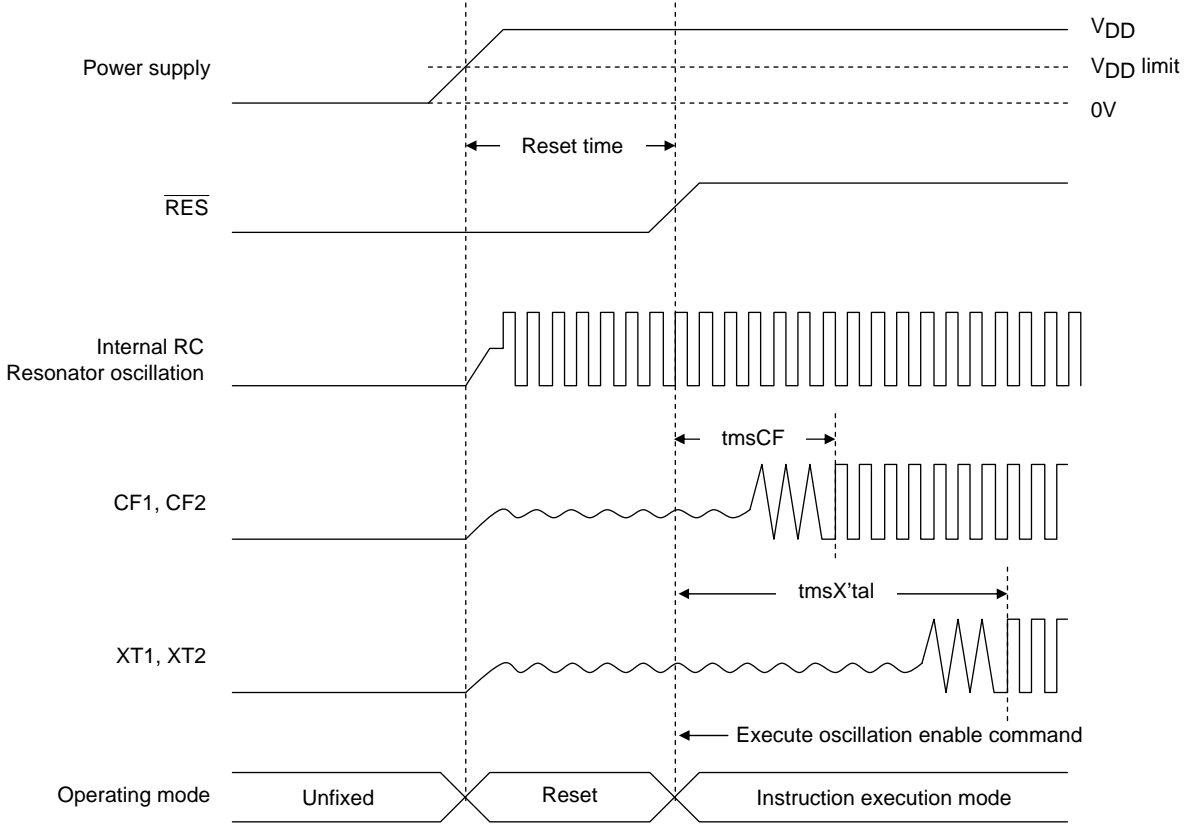
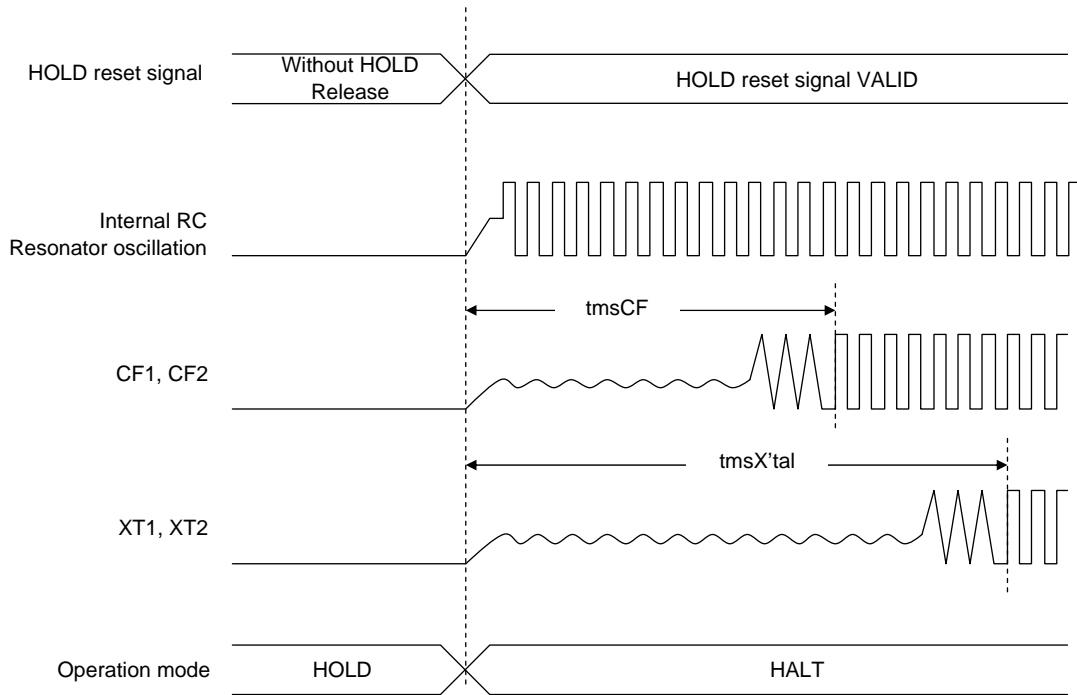


Figure 3 AC Timing Measurement Point

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## Reset Time and Oscillation Stabilizing Time

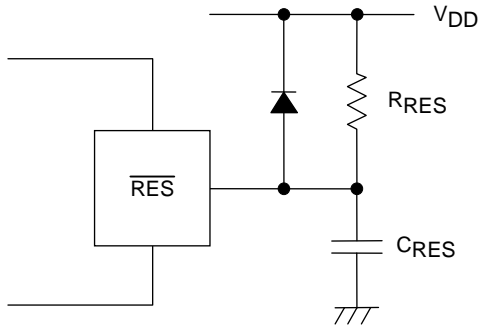


## HOLD Release Signal and Oscillation Stable Time

Note: External oscillation circuit is selected.

Figure 4 Oscillation Stabilization Times

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Note:  
External circuits for reset may vary depending on the usage of POR. Please refer to the user's manual for more information.

Figure 5 Reset Circuit

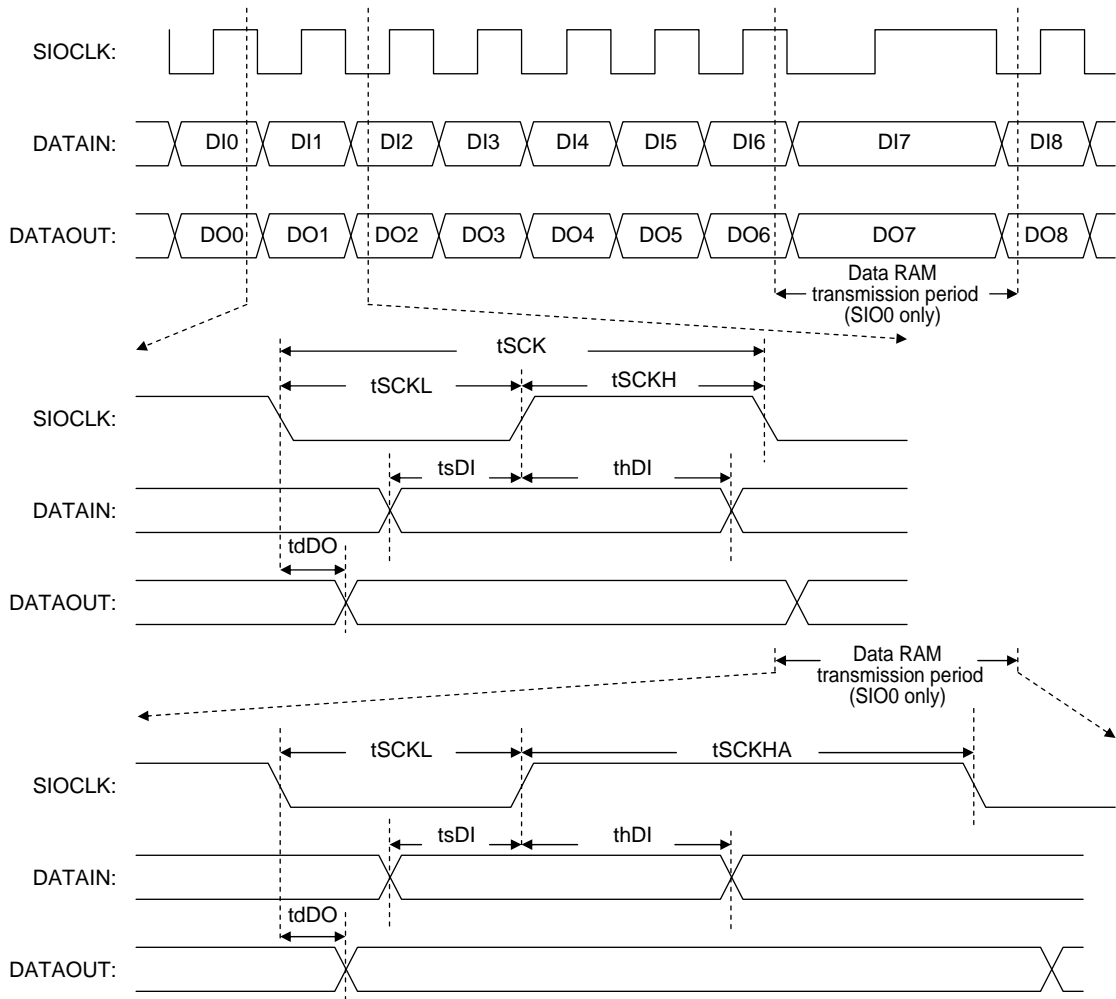


Figure 6 Serial Input/Output Wave Form

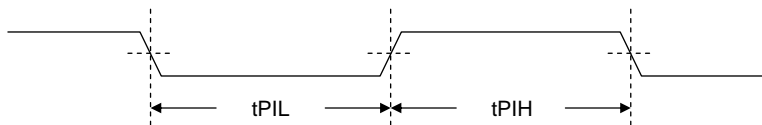


Figure 7 Pulse Input

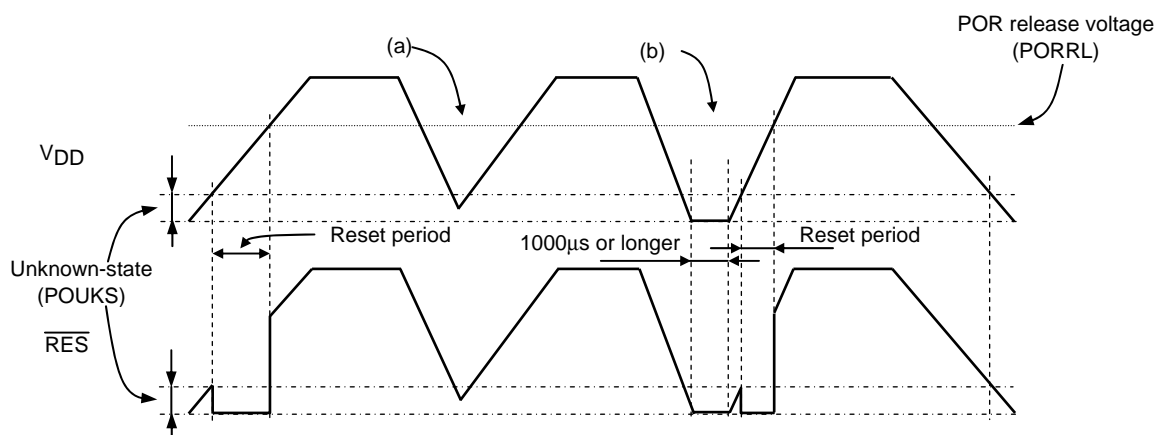


Figure 8 Waveform observed when POR is used  
(RESET pin: Pull-up resistor RRES only)

- The POR function generates a reset only when power is turned on starting at the  $V_{SS}$  level.
- No stable reset will be generated if power is turned on again when the power level does not go down to the  $V_{SS}$  level as shown in (a).
- A reset is generated only when the power level goes down to the  $V_{SS}$  level as shown in (b) and power is turned on again after this condition continues for 1000µs or longer.

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