

Section 22 Electrical Characteristics

22.1 Absolute Maximum Ratings

Table 22.1 shows the absolute maximum ratings.

Table 22.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage	V_{CC}	-0.3 to +7.0	V
Programmable voltage (FZTAT version only)	V_{PP}	-0.3 to +13.5	V
Input voltage (other than A/D ports)	V_{in}	-0.3 to $V_{CC} + 0.3$	V
Input voltage (A/D ports)	V_{in}	-0.3 to $AV_{CC} + 0.3$	V
Analog supply voltage	AV_{CC}	-0.3 to +7.0	V
Analog reference voltage (QFP-144 only)	AV_{ref}	-0.3 to $AV_{CC} + 0.3$	V
Analog input voltage	V_{AN}	-0.3 to $AV_{CC} + 0.3$	V
Operating temperature	T_{opr}	-20 to +75	°C
Storage temperature	T_{stg}	-55 to +125	°C

Note: Operating the LSI in excess of the absolute maximum ratings may result in permanent damage.

22.2 DC Characteristics—Preliminary

Table 22.2 DC Characteristics (Conditions: $V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5 \text{ V}$ to AV_{CC} , $V_{SS} = AV_{SS} = 0 \text{ V}$, $T_a = -20$ to $+75^\circ \text{ C}$)

Item	Pin	Symbol	Min	Typ	Max	Unit	Measurement Conditions
Input high-level voltage	$\overline{RES}$, NMI, MD3–MD0, PA2, PA5, PA6–PA9, PE0–PE15	V_{IH}	$V_{CC} - 0.7$	—	$V_{CC} + 0.3$	V	—
	EXTAL		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	—
	A/D port		2.2	—	$AV_{CC} + 0.3$	V	—
	Other input pins		2.2	—	$V_{CC} + 0.3$	V	—
Input low-level voltage	$\overline{RES}$, NMI, MD3–MD0, PA2, PA5, PA6–PA9, PE0–PE15	V_{IL}	–0.3	—	0.5	V	—
	Other input pins		–0.3	—	0.8	V	—
Schmitt trigger input voltage	PA2, PA5, PA6–PA9, PE0–PE15	VT^+	4.0	—	—	V	—
		VT^-	—	—	1.0	V	—
		$VT^+ - VT^-$	0.4	—	—	V	—
Input leak current	$\overline{RES}$, NMI, MD3–MD0, PA2, PA5, PA6–PA9, PE0–PE15	$ I_{in} $	—	—	1.0	μA	$V_{in} = 0.5 \text{ to } V_{CC} - 0.5 \text{ V}$
	A/D port		—	—	1.0	μA	$V_{in} = 0.5 \text{ to } AV_{CC} - 0.5 \text{ V}$
	Other input pins		—	—	1.0	μA	$V_{in} = 0.5 \text{ to } V_{CC} - 0.5 \text{ V}$
Three-state leak current (while off)	A21–A0, D31–D0, CS3–CS0, RDWR, RAS, CASxx, WRxx, $\overline{RD}$, ports A, B, C, D, E	$ I_{TSI} $	—	—	1.0	μA	$V_{in} = 0.5 \text{ to } V_{CC} - 0.5 \text{ V}$

Table 22.2 DC Characteristics (Conditions: $V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5 \text{ V}$ to AV_{CC} , $V_{SS} = AV_{SS} = 0 \text{ V}$, $T_a = -20$ to $+75^\circ \text{C}$) (cont)

Item	Pin	Symbol	Min	Typ	Max	Unit	Measurement Conditions
Output high-level voltage	All output pins	V_{OH}	$V_{CC} - 0.5$	—	—	V	$I_{OH} = -200 \mu A$
			3.5	—	—	V	$I_{OH} = -1 \text{ mA}$
Output low-level voltage	All output pins	V_{OL}	—	—	0.4	V	$I_{OL} = 1.6 \text{ mA}$
	PE9, PE11–PE15		—	—	1.5	V	$I_{OL} = 15 \text{ mA}$
Input capacitance	$\overline{RES}$	C_{in}	—	—	60	pF	$V_{in} = 0 \text{ V}$, $f = 1 \text{ Mhz}$, $T_a = 25^\circ\text{C}$
	NMI		—	—	30	pF	
	All other input pins		—	—	20	pF	
Current consumption	Ordinary operation	I_{CC}	—	TBD	TBD	mA	$f = 20 \text{ MHz}$
			—	TBD	TBD	mA	$f = 24 \text{ MHz}$
			—	TBD	TBD	mA	$f = 28 \text{ MHz}$
	Sleep		—	TBD	TBD	mA	$f = 20 \text{ MHz}$
			—	TBD	TBD	mA	$f = 24 \text{ MHz}$
			—	TBD	TBD	mA	$f = 28 \text{ MHz}$
	Standby		—	TBD	TBD	μA	$T_a \leq 50^\circ\text{C}$
			—	—	TBD	μA	$T_a > 50^\circ\text{C}$
Analog supply current	During A/D conversion	AI_{CC}	—	TBD	TBD	mA	
	Awaiting A/D conversion		—	TBD	TBD	μA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

- Notes: 1. When the A/D converter is not used (including during standby), do not release the AV_{CC} , AV_{SS} , and AV_{ref} pins. Connect the AV_{CC} and AV_{ref} pins to V_{CC} and the AV_{SS} pin to V_{SS} .
2. The current consumption is measured when $V_{IH\text{min}} = V_{CC} - 0.5 \text{ V}$, $V_{IL\text{max}} = 0.5 \text{ V}$, with all output pins unloaded.

Table 22.3 Permitted Output Current Values (Conditions: $V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5 \text{ V}$ to AV_{CC} , $V_{SS} = AV_{SS} = 0 \text{ V}$, $T_a = -20$ to $+75^\circ \text{ C}$)

Item	Symbol	Min	Typ	Max	Unit
Output low-level permissible current (per pin)	I_{OL}	—	—	2.0*	mA
Output low-level permissible current (total)	ΣI_{OL}	—	—	80	mA
Output high-level permissible current (per pin)	$-I_{OH}$	—	—	2.0	mA
Output high-level permissible current (total)	$\Sigma (-I_{OH})$	—	—	25	mA

Notes: 1. PE9, PE11–PE15 are IOL = 15 mA (max). Make sure that no more than three of these pins exceed an I_{OL} of 2.0 mA simultaneously.

2. To assure LSI reliability, do not exceed the output values listed in this table.

22.3 AC Characteristics—Preliminary

22.3.1 Clock Timing

Table 22.4 Clock Timing (Conditions: $V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5 \text{ V}$ to AV_{CC} , $V_{SS} = AV_{SS} = 0 \text{ V}$, $T_a = -20$ to $+75^\circ \text{ C}$)

Item	Symbol	Min	Max	Unit	Figures
Operating frequency	f_{OP}	4	28	MHz	22.1
Clock cycle time	t_{cyc}	35	250	ns	
Clock low-level pulse width	t_{CL}	10	—	ns	
Clock high-level pulse width	t_{CH}	10	—	ns	
Clock rise time	t_{CR}	—	5	ns	
Clock fall time	t_{CF}	—	5	ns	
EXTAL clock input frequency	f_{EX}	4	10	MHz	22.2
EXTAL clock input cycle time	t_{EXcyc}	100	250	ns	
EXTAL clock low-level input pulse width	t_{EXL}	40	—	ns	
EXTAL clock high-level input pulse width	t_{EXH}	40	—	ns	
EXTAL clock input rise time	t_{EXR}	—	5	ns	
EXTAL clock input fall time	t_{EXF}	—	5	ns	
Reset oscillation settling time	t_{OSC1}	10	—	ms	22.3
Standby return clock settling time	t_{OSC2}	10	—	ms	

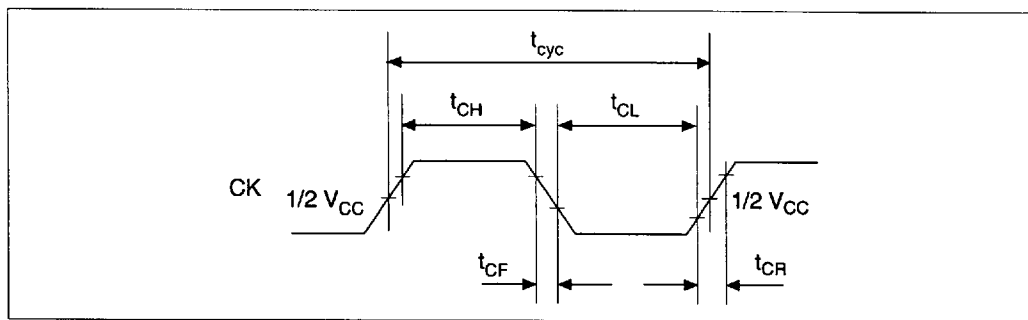


Figure 22.1 System Clock Timing

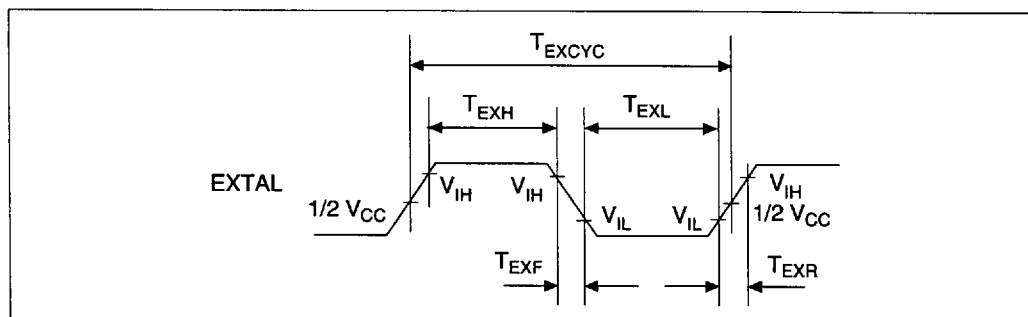


Figure 22.2 EXTAL Clock Input Timing

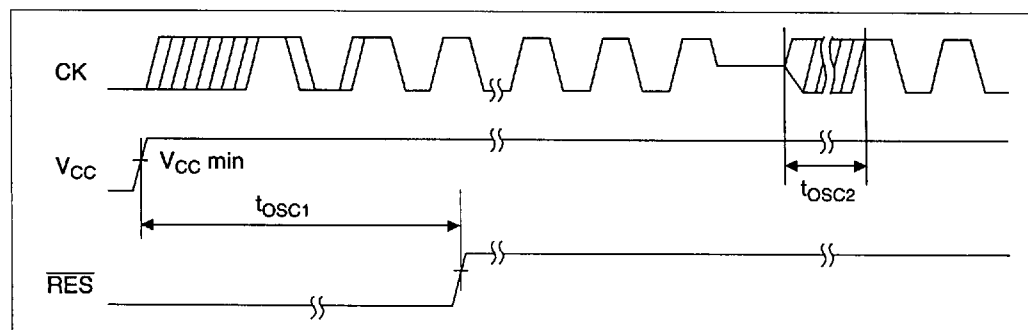


Figure 22.3 Oscillation Settling Time

22.3.2 Control Signal Timing

Table 22.5 Control Signal Timing (Conditions: $V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5 \text{ V}$ to AV_{CC} , $V_{SS} = AV_{SS} = 0 \text{ V}$, $T_a = -20$ to $+75^\circ \text{ C}$)

Item	Symbol	Min	Max	Unit	Figure
RES rise/fall	t_{RESr} , t_{RESf}	—	200	ns	22.4
RES pulse width	t_{RESW}	20	—	t_{cyc}	
NMI reset/setup time	t_{NMIRS}	4	—	t_{cyc}	
NMI reset/hold time	t_{NMIRH}	4	—	t_{cyc}	
NMI rise/fall	t_{NMIr} , t_{NMIf}	—	200	ns	
RES setup time*	t_{RESS}	35	—	ns	22.4, 22.5
NMI setup time*	t_{NMIS}	35	—	ns	
IRQ7–IRQ0 setup time (edge detection)	t_{IROES}	35	—	ns	
IRQ7–IRQ0 setup time (level detection)	t_{IROLS}	35	—	ns	
NMI hold time	t_{NMIH}	35	—	ns	22.5
IRQ7–IRQ0 hold time	t_{IROEH}	35	—	ns	
IRQOUT hold time	t_{IRQOD}	—	35	ns	22.6
Bus request setup time	t_{BRQS}	35	—	ns	22.7
Bus acknowledge delay time 1	t_{BACKD1}	—	35	ns	
Bus acknowledge delay time 2	t_{BACKD2}	—	35	ns	
Bus three-state delay time	t_{BZD}	—	35	ns	

Note: The RES, NMI, and IRQ7–IRQ0 signals are asynchronous inputs, but when the setup times shown here are provided, the signals are considered to have produced changes at clock rise (for RES) or clock fall (for NMI and IRQ7–IRQ0). If the setup times are not provided, recognition is delayed until the next clock rise or fall.

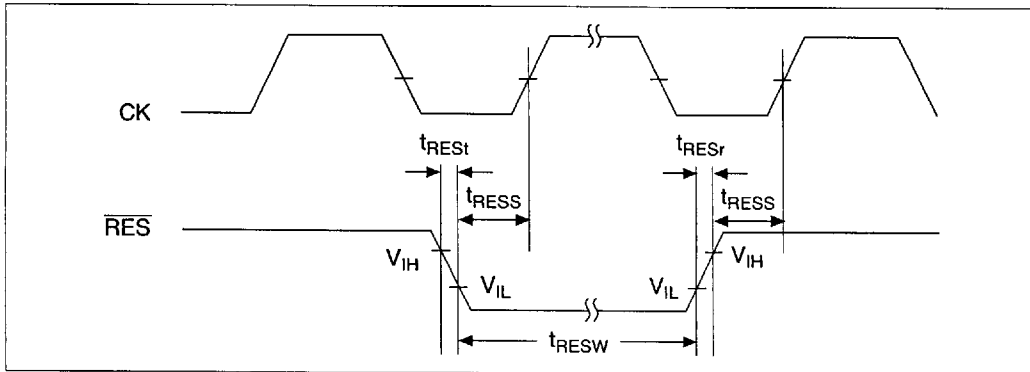


Figure 22.4 Reset Input Timing

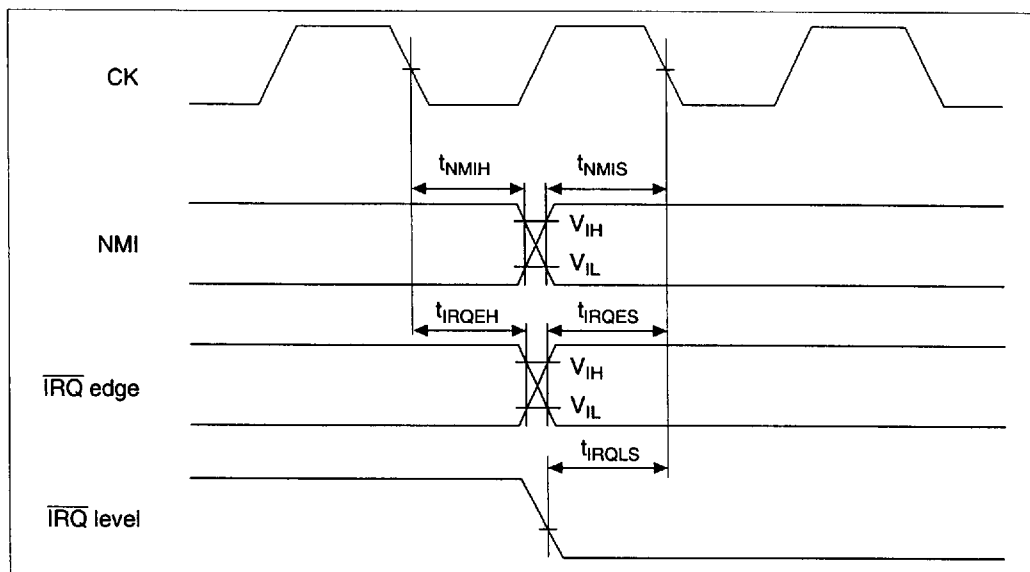


Figure 22.5 Interrupt Signal Input Timing

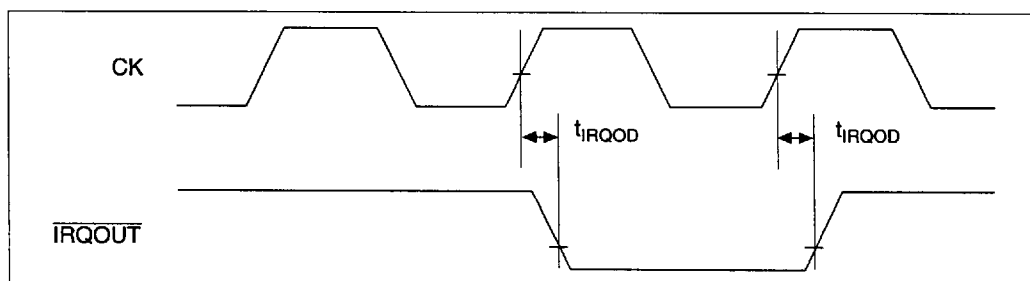


Figure 22.6 Interrupt Signal Output Timing

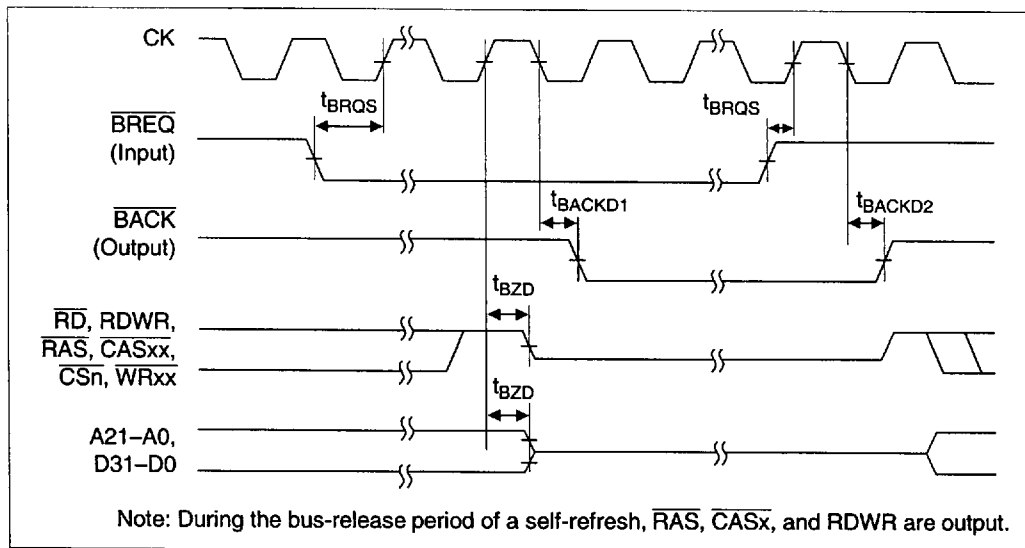


Figure 22.7 Bus Right Release Timing

22.3.3 Bus Timing

**Table 22.6 Bus Timing (Conditions: $V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{REF} = 4.5 \text{ V}$
– AV_{CC} , $V_{SS} = AV_{SS} = 0 \text{ V}$, $T_a = 20 \text{ to } +75^\circ\text{C}$)**

Item	Symbol	Min	Max	Unit	Figure
Address delay time	t_{AD}	TBD	18	ns	22.8, 22.9, 22.11–22.16, 22.19
CS delay time 1	t_{CSD1}	—	21	ns	22.8, 22.9, 22.19
CS delay time 2	t_{CSD2}	—	21	ns	
Read strobe delay time 1	t_{RSD1}	—	18	ns	22.8, 22.9,
Read strobe delay time 2	t_{RSD2}	—	18	ns	22.11–22.16, 22.19
Read data setup time	t_{RDS}	15	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
Write strobe delay time 1	t_{WSD1}	TBD	18	ns	
Write strobe delay time 2	t_{WSD2}	TBD	18	ns	
Write data delay time	t_{WDD}	—	35	ns	
Write data hold time	t_{WDH}	0	10*1	ns	
WAIT setup time	t_{WTS}	15	—	ns	22.10, 22.15,
WAIT hold time	t_{WTH}	10	—	ns	22.19
RAS delay time 1	t_{RASD1}	TBD	18	ns	22.11–22.18
RAS delay time 2	t_{RASD2}	TBD	18	ns	
CAS delay time 1	t_{CASD1}	TBD	18	ns	
CAS delay time 2	t_{CASD2}	TBD	18	ns	
Read data access time	t_{ACC}^{*2}	$t_{cyc} \times (n + 2) - 30$	—	ns	22.8, 22.9
Access time from read strobe	t_{OE}^{*2}	$t_{cyc} \times (n + 1.5) - 30$	—	ns	
Access time from column address	t_{AA}^{*2}	$t_{cyc} \times (n + 2) - 30$	—	ns	22.11–22.16
Access time from RAS	t_{RAC}^{*2}	$t_{cyc} \times (n + RCD + 2.5) - 30$	—	ns	
Access time from CAS	t_{CAC}^{*2}	$t_{cyc} \times (n + 1) - 30$	—	ns	
Row address hold time	t_{RAH}	$t_{cyc} \times (RCD + 0.5) - 15$	—	ns	
Row address setup time	t_{ASR}	$t_{cyc} \times 0.5 - 17$	—	ns	
Data input setup time	t_{DS}	$t_{cyc} \times (m + 0.5) - 25$	—	ns	
Data input hold time	t_{DH}	20	—	ns	

Notes: 1. t_{WDH} (max) is a reference value.

2. If the access time is satisfied, t_{RDS} need not be satisfied.

3. n is the number of waits. m is 0 when the number of DRAM waits is 0. Otherwise m is 1. RCD is the DCR's RCD bit setting value.

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Table 22.7 Bus Timing (Conditions: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{REF} = 4.5\text{ V}$ to AV_{CC} , $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = 20$ to $+75^\circ\text{C}$)

Item	Symbol	Min	Max	Unit	Figure
Read/write strobe delay time 1	t_{RWD1}	TBD	18	ns	22.11–22.16
Read/write strobe delay time 2	t_{RWD2}	TBD	18	ns	
High-speed page mode CAS precharge time	t_{CP}	$t_{cyc} - 25$	—	ns	22.16
RAS precharge time	t_{RP}	$t_{cyc} \times (TPC + 1.5) - 15$	—	ns	22.11–22.16
CAS setup time	t_{CSR}	10	—	ns	22.17, 22.18
AH delay time 1	t_{AHD1}	—	18	ns	22.19
AH delay time 2	t_{AHD2}	—	18	ns	
Multiplex address delay time	t_{MAD}	—	18	ns	
Multiplex address hold time	t_{MAH}	0	—	ns	
DACK delay time	t_{DACKD1}	—	21	ns	22.8, 22.9, 22.11–22.16, 22.19

Note: TPC is the DCR's TPC bit setting value.

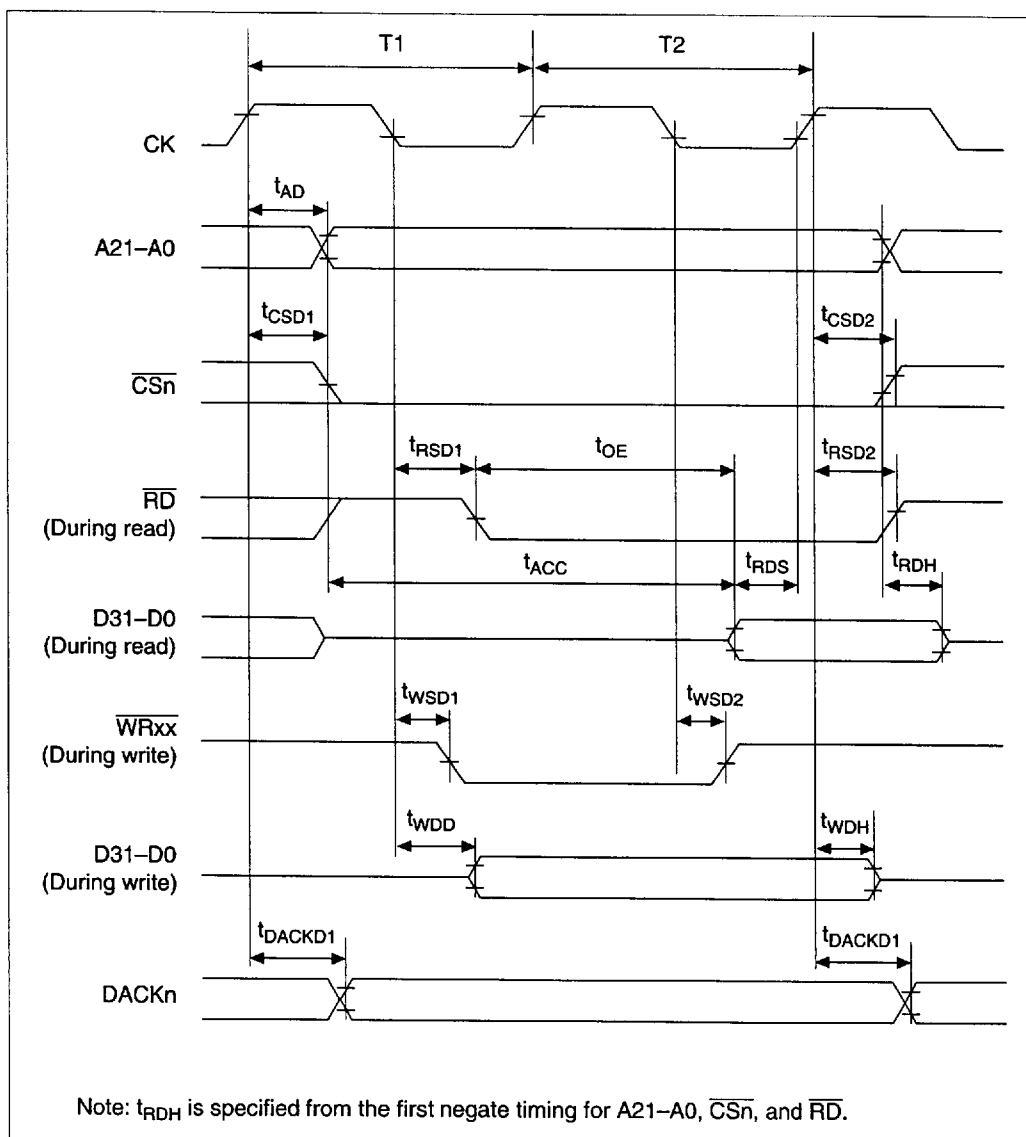


Figure 22.8 Basic Cycle (No Waits)

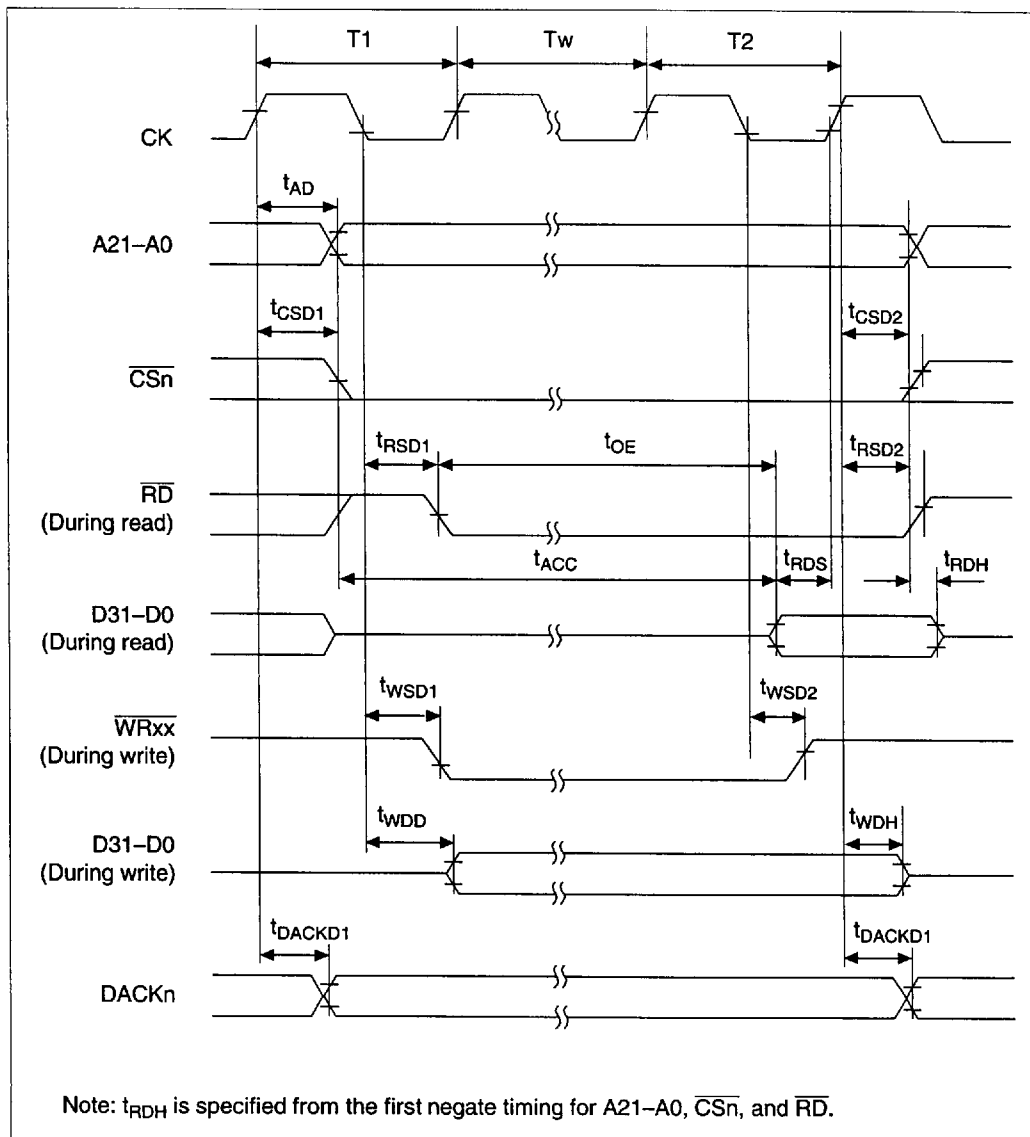


Figure 22.9 Basic Cycle (Software Waits)

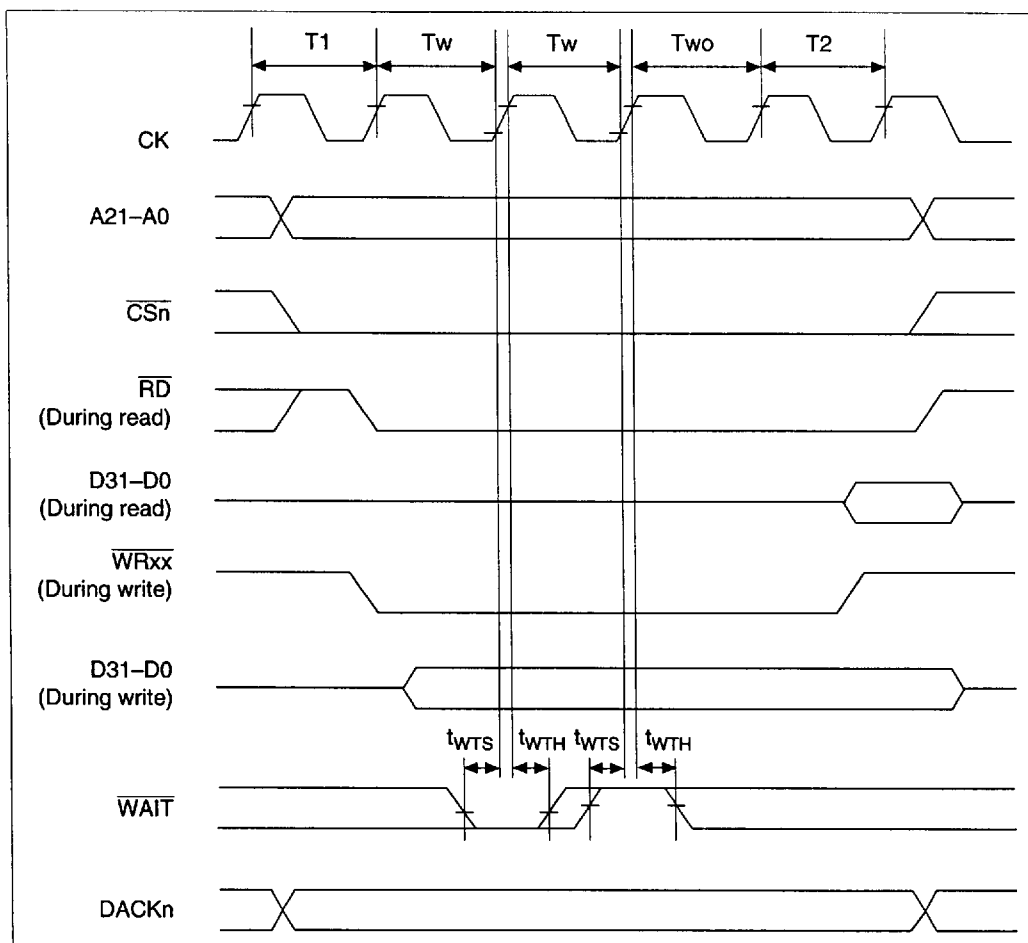


Figure 22.10 Basic Cycle (2 Software Waits + Wait due to $\overline{WAIT}$ Signal)

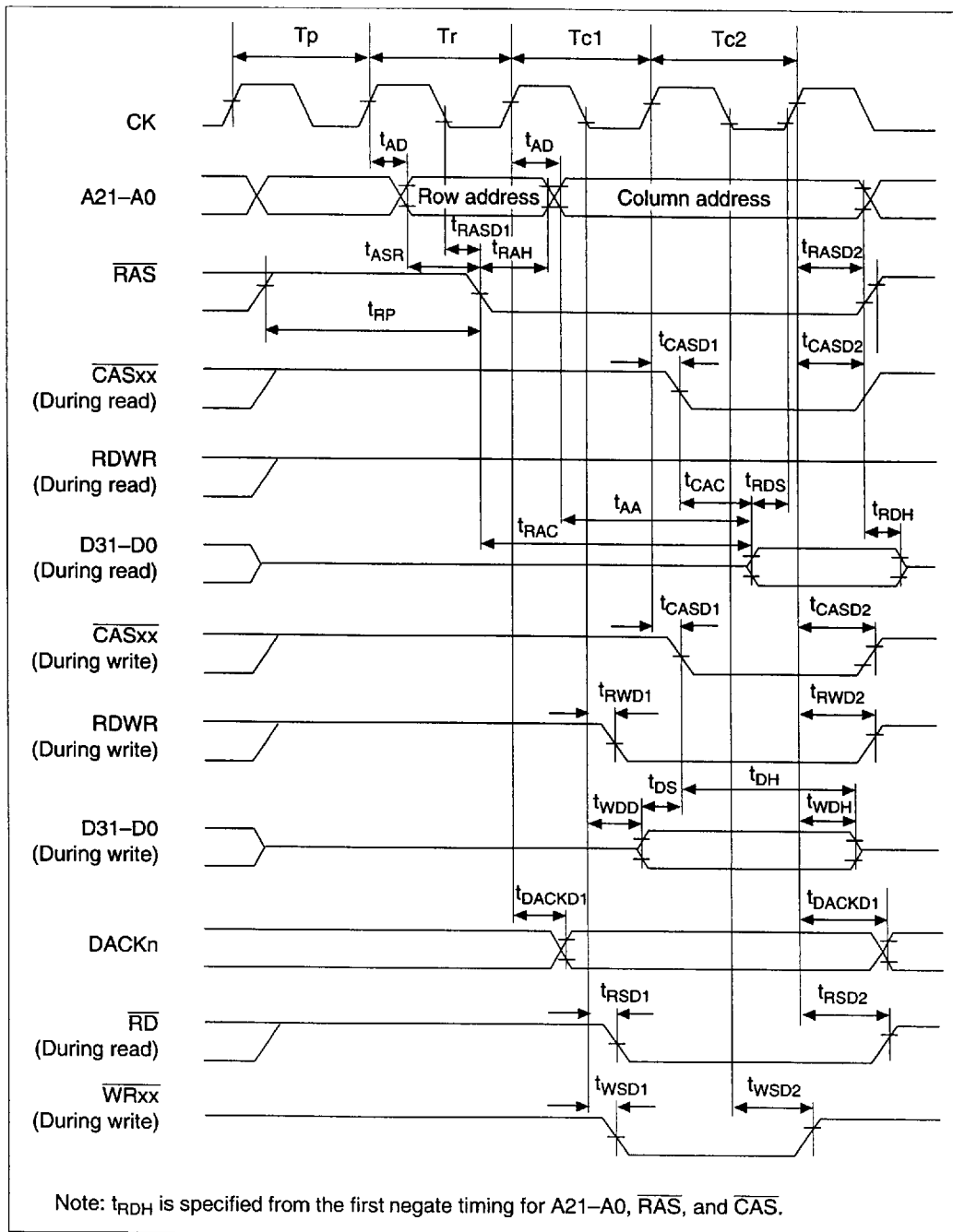


Figure 22.11 DRAM Cycle (Normal Mode, No Waits)

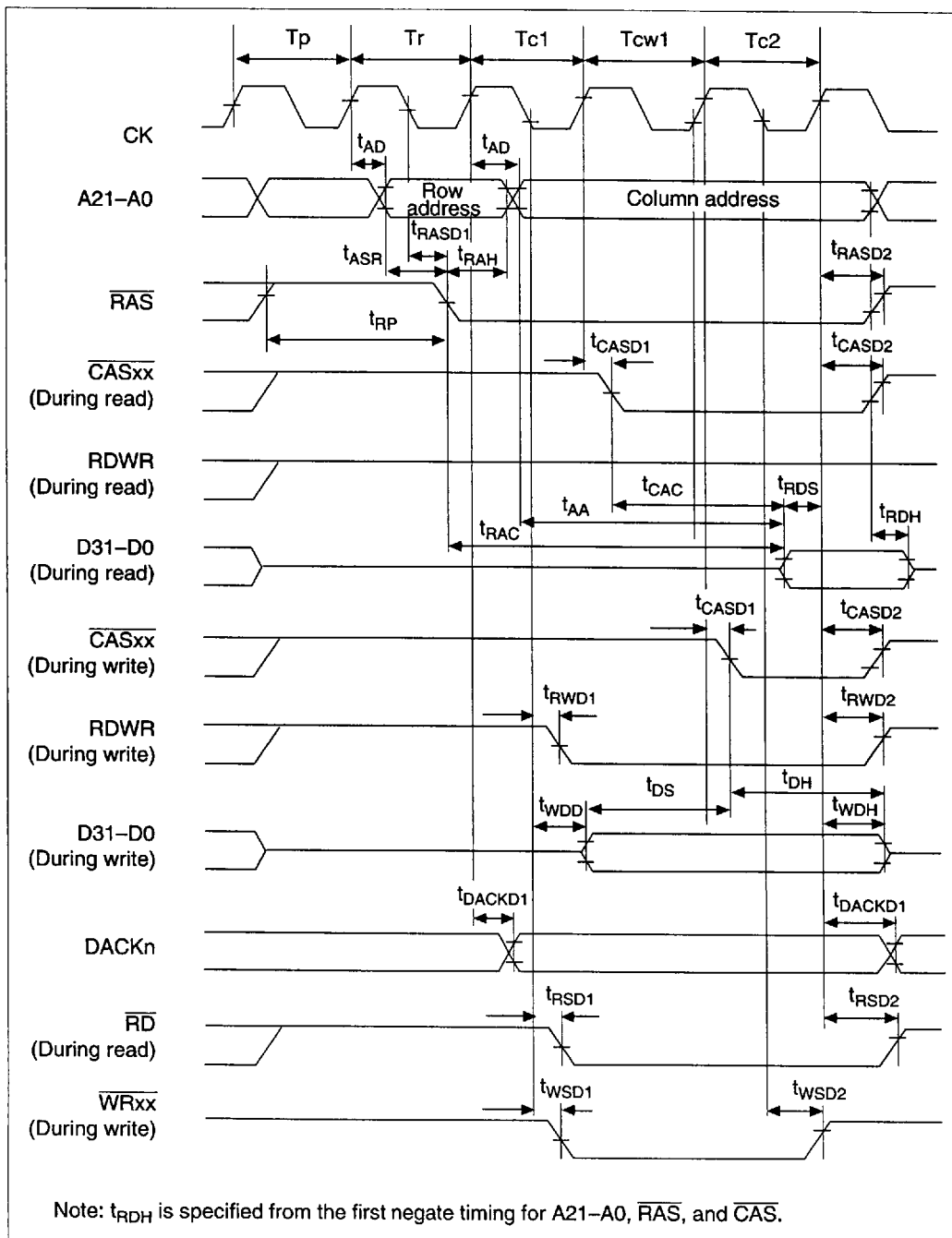


Figure 22.12 DRAM Cycle (Normal Mode, 1 Wait, TPC = 0, RCD = 0)

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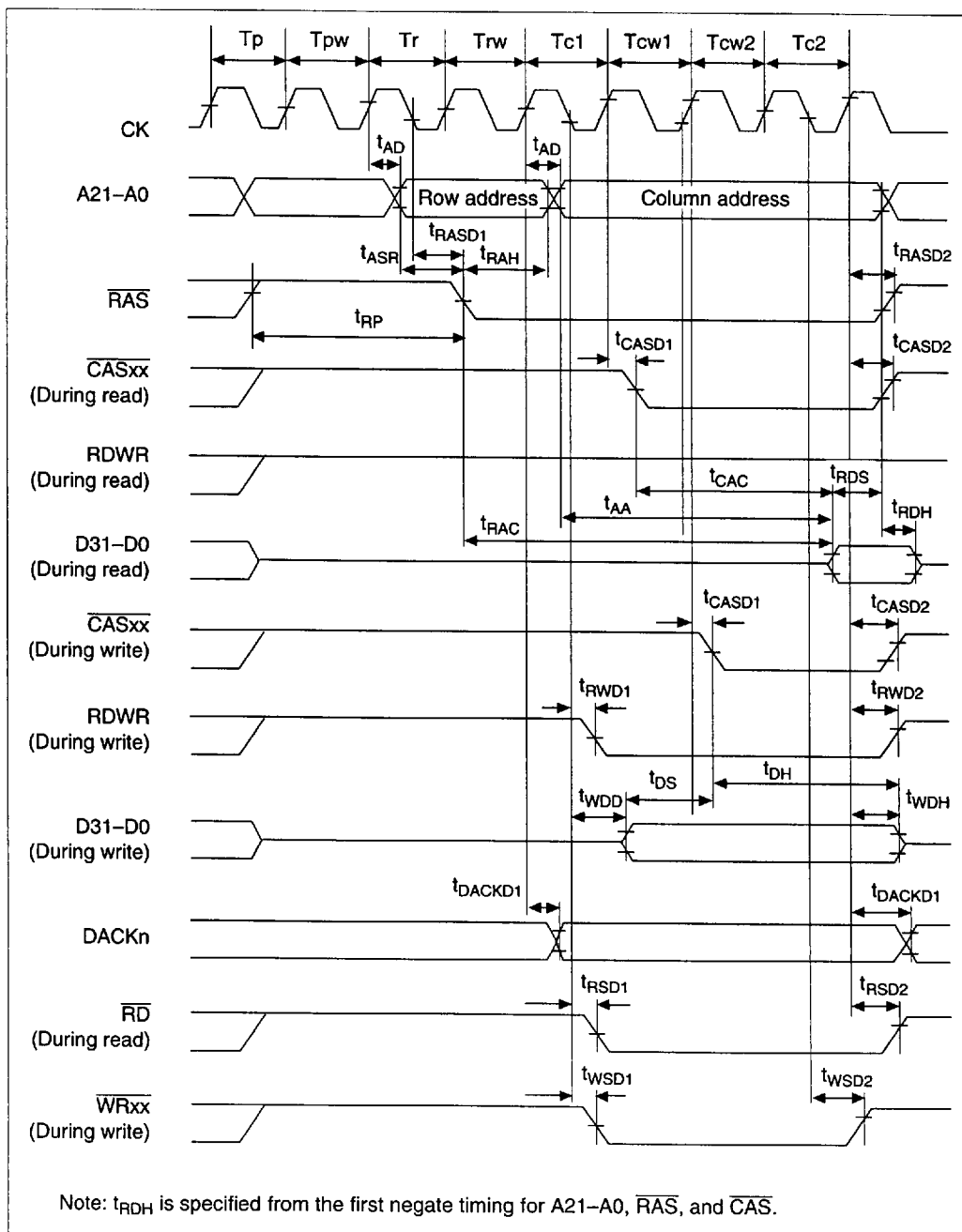


Figure 22.13 DRAM Cycle (Normal Mode, 2 Waits, TPC = 1, RCD = 1)

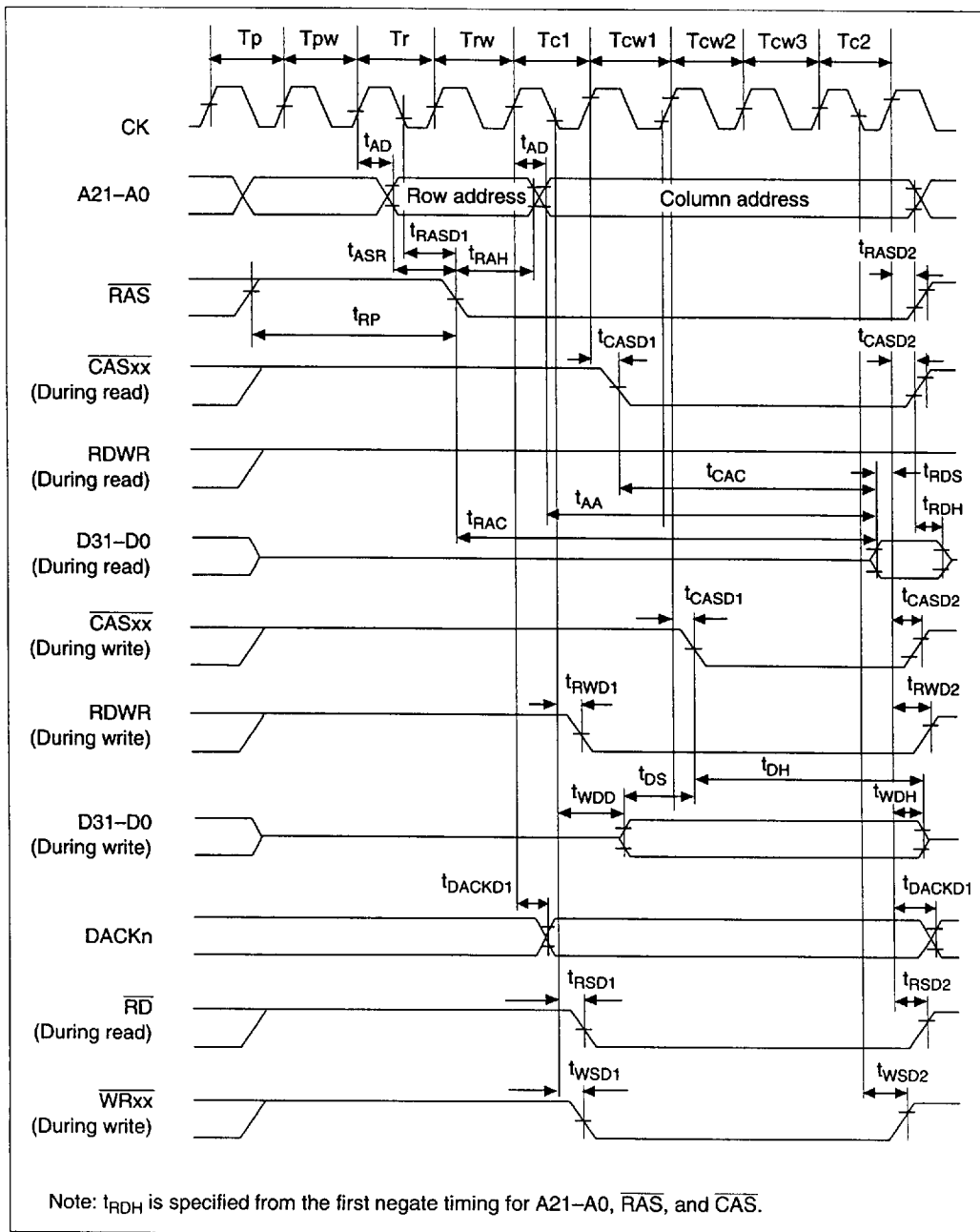


Figure 22.14 DRAM Cycle (Normal Mode, 3 Waits, TPC = 1, RCD = 1)

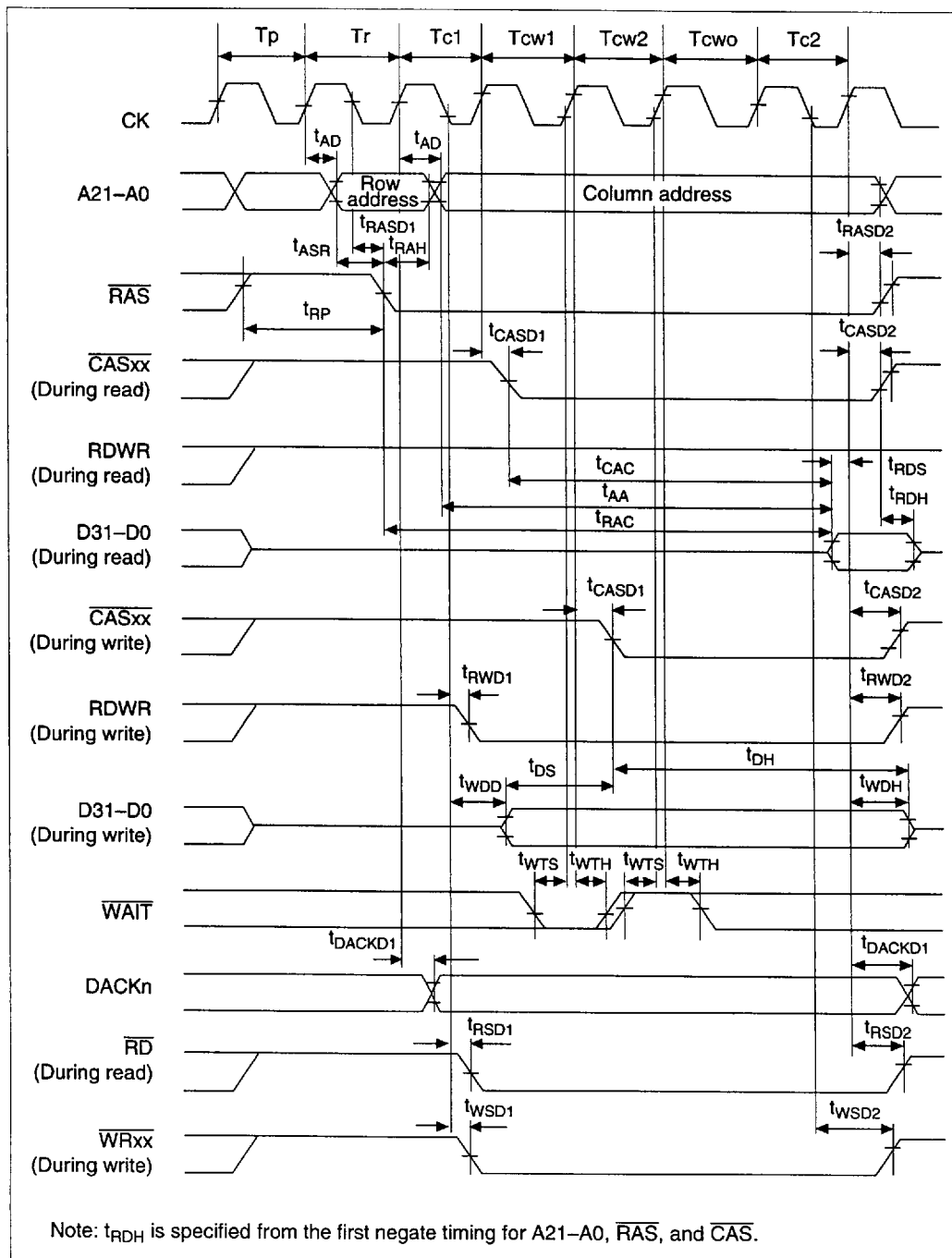


Figure 22.15 DRAM Cycle (Normal Mode, 2 Waits + Wait due to $\overline{WAIT}$ Signal)

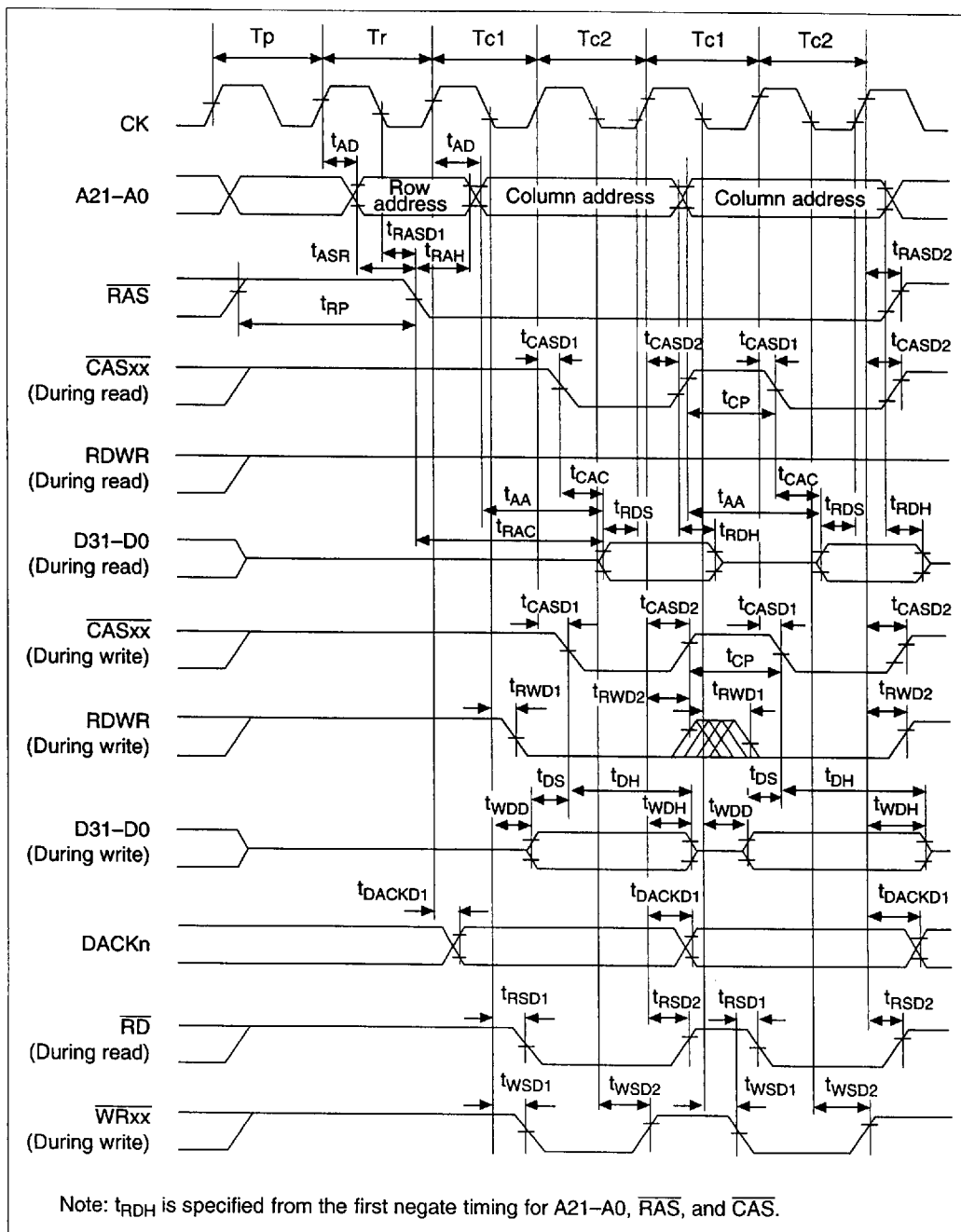


Figure 22.16 DRAM Cycle (High-Speed Page Mode)

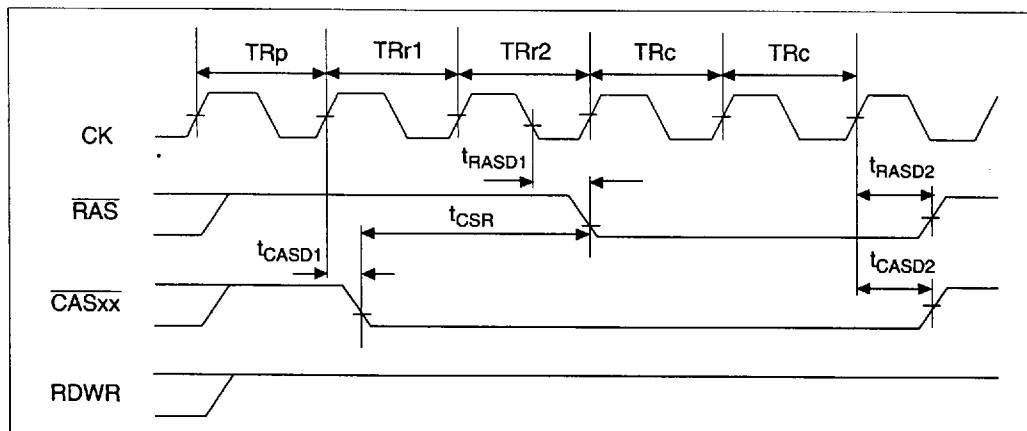


Figure 22.17 CAS Before RAS Refresh (TRAS1 = 0, TRAS0 = 0)

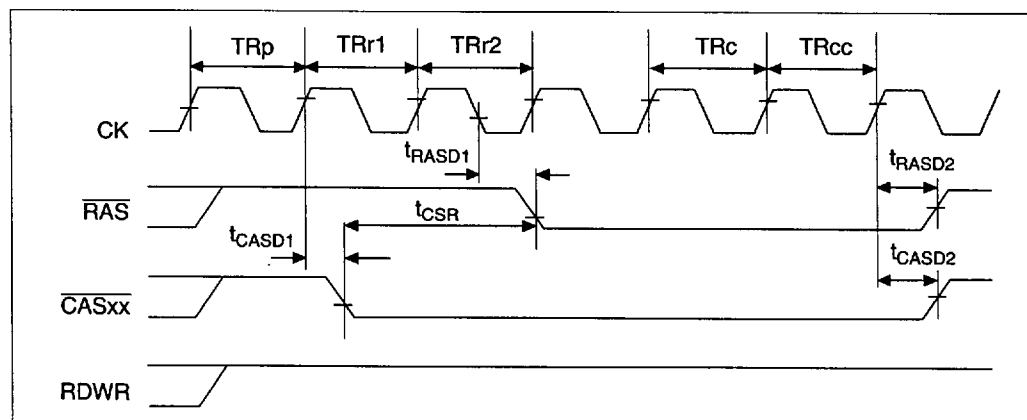


Figure 22.18 Self Refresh

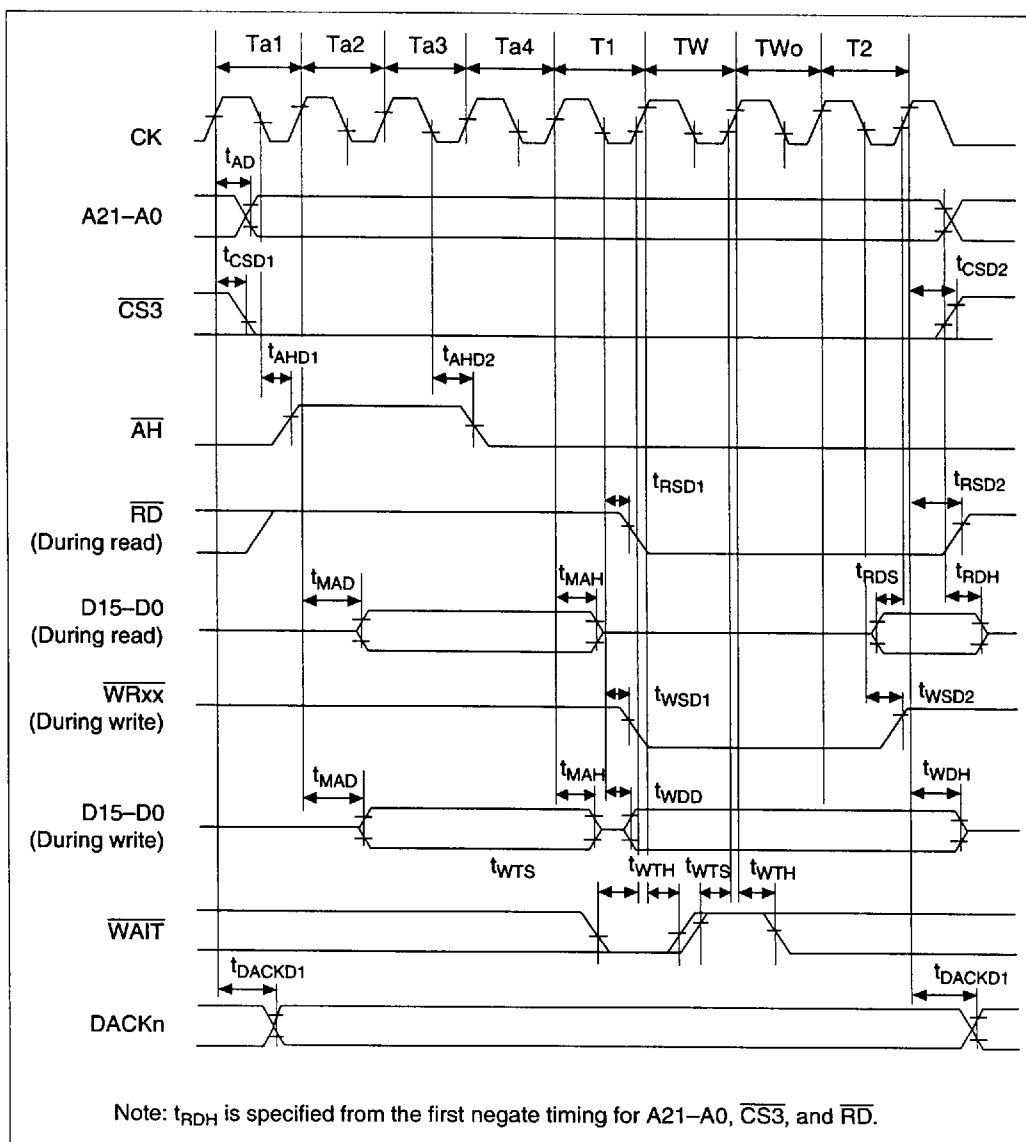


Figure 22.19 Address Data Multiplex I/O Space Cycle (1 Software Wait + External Wait)

22.3.4 Direct Memory Access Controller Timing

Table 22.8 Direct Memory Access Controller Timing (Conditions: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{REF} = 4.5\text{ V}$ to AV_{CC} , $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = 20$ to $+75^\circ\text{C}$)

Item	Symbol	Min	Max	Unit	Figure
DREQ0 and DREQ1 setup time	t_{DRQS}	18	—	ns	22.20
DREQ0 and DREQ1 hold time	t_{DRQH}	18	—	ns	
DREQ0 and DREQ1 pulse width	t_{DRQW}	1.5	—	t_{cyt}	22.21
DRAK output delay time	t_{DRAKD}	—	18	ns	22.22

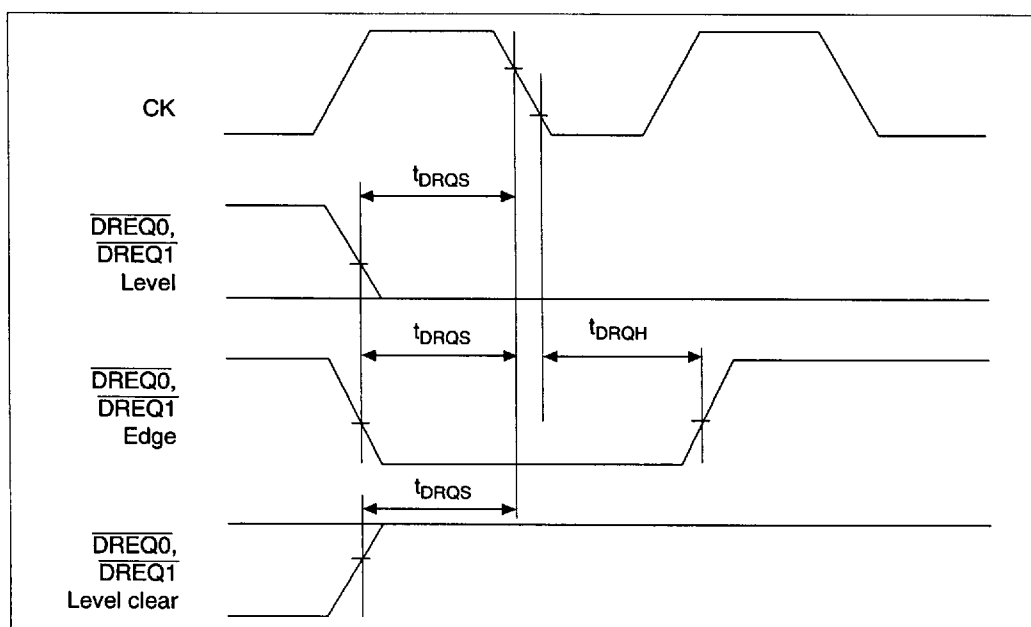


Figure 22.20 DREQ0 and DREQ1 Input Timing (1)

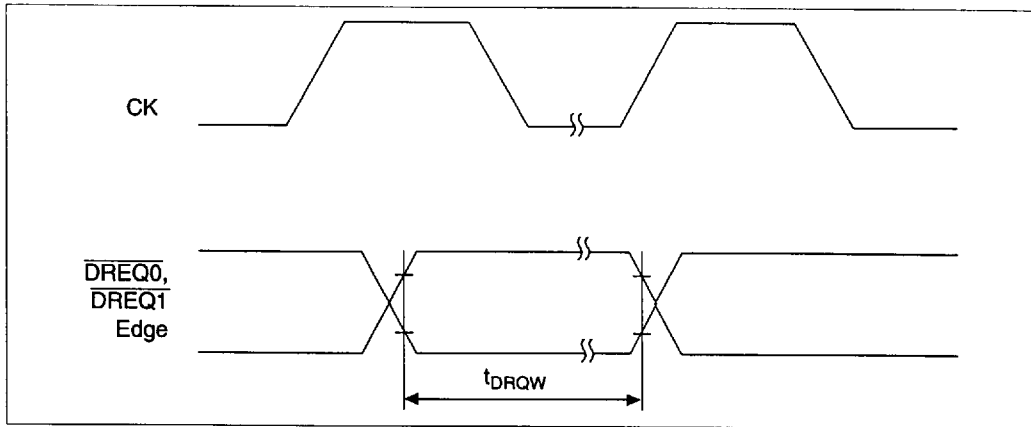


Figure 22.21 DREQ0 and DREQ1 Input Timing (2)

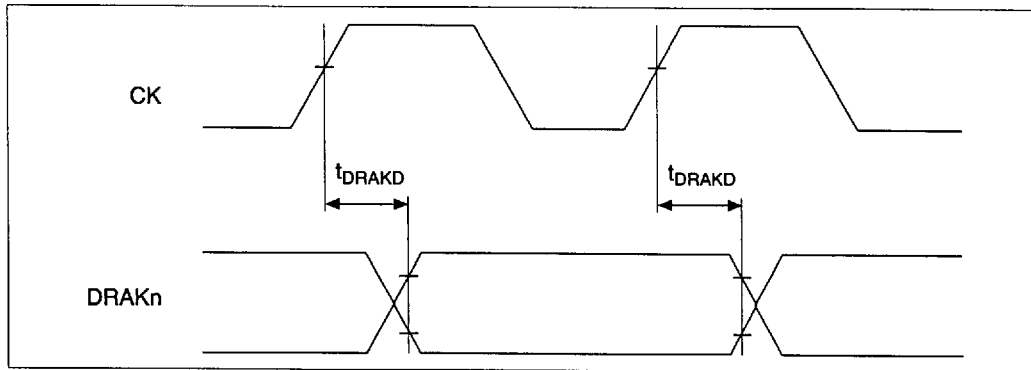


Figure 22.22 DRAK Output Delay Time

22.3.5 Multifunction Timer Pulse Unit Timing

Table 22.9 Multifunction Timer Pulse Unit Timing (Conditions: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{REF} = 4.5\text{ V}$ to AV_{CC} , $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = 20$ to $+75^\circ\text{C}$)

Item	Symbol	Min	Max	Unit	Figure
Output compare output delay time	t_{TOCD}	—	100	ns	22.23
Input capture input setup time	t_{TICS}	30	—	ns	
Timer input setup time	t_{TCKS}	35	—	ns	
Timer clock pulse width (single edge specification)	t_{TCKWHL}	1.5	—	t_{cyc}	22.24
Timer clock pulse width (both edges specified)	t_{TCKWHL}	2.5	—	t_{cyc}	
Timer clock pulse width (phase measurement mode)	t_{TCKWHL}	2.5	—	t_{cyc}	

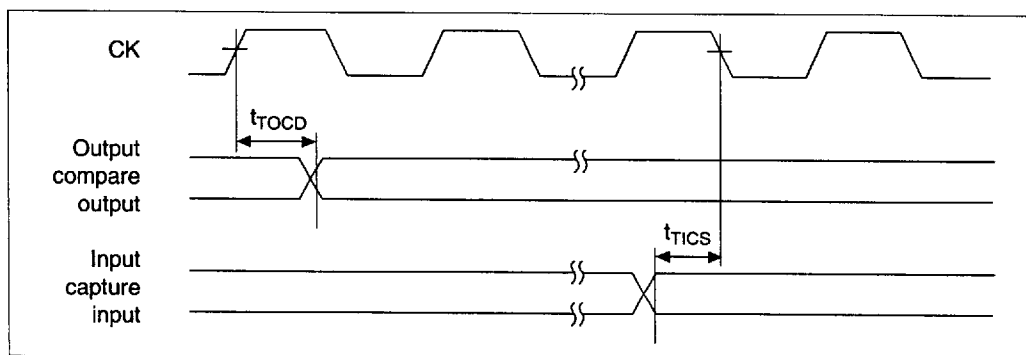


Figure 22.23 MTU I/O Timing

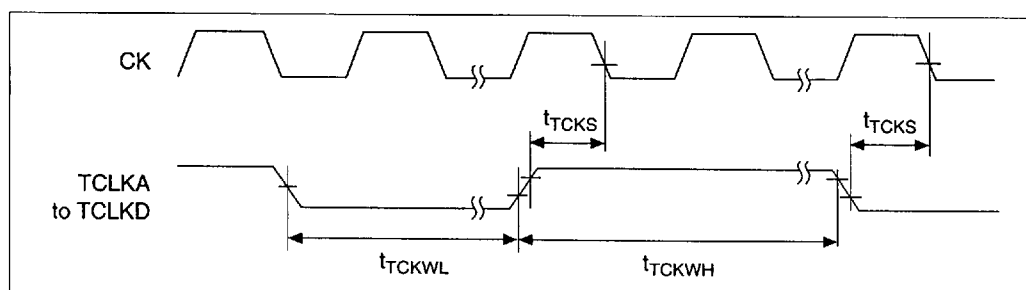


Figure 22.24 MTU Clock Input Timing

22.3.6 I/O Port Timing

Table 22.10 I/O Port Timing (Conditions: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{REF} = 4.5\text{ V to } AV_{CC}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = 20\text{ to } +75^\circ\text{C}$)

Item	Symbol	Min	Max	Unit	Figure
Port output data delay time	t_{PWD}	—	100	ns	22.25
Port input hold time	t_{PRH}	35	—	ns	
Port input setup time	t_{PRS}	35	—	ns	

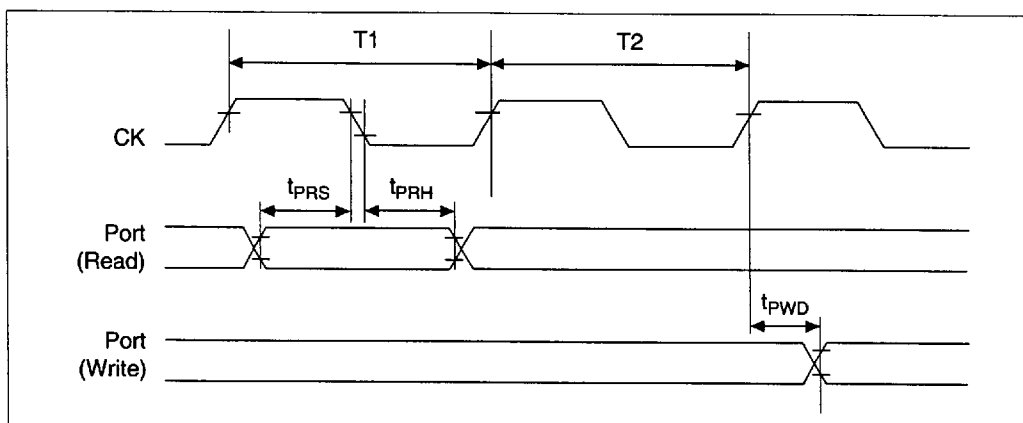


Figure 22.25 I/O Port I/O Timing

22.3.7 Watchdog Timer Timing

Table 22.11 Watchdog Timer Timing (Conditions: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{REF} = 4.5\text{ V to } AV_{CC}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = 20\text{ to } +75^\circ\text{C}$)

Item	Symbol	Min	Max	Unit	Figure
WDTOVF delay time	t_{WOVD}	—	100	ns	22.26

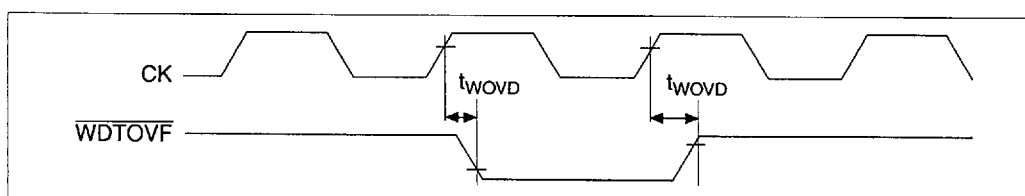


Figure 22.26 Watchdog Timer Timing

22.3.8 Serial Communication Interface Timing

Table 22.12 Serial Communication Interface Timing (Conditions: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{REF} = 4.5\text{ V}$ to AV_{CC} , $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = 20$ to $+75^\circ\text{C}$)

Item	Symbol	Min	Max	Unit	Figure
Input clock cycle	t_{scyc}	4	—	t_{cyc}	22.27
Input clock cycle (clock sync)	t_{scyc}	6	—	t_{cyc}	
Input clock pulse width	t_{sckw}	0.4	0.6	t_{cyc}	
Input clock rise time	t_{sckr}	—	1.5	t_{cyc}	
Input clock fall time	t_{sckf}	—	1.5	t_{cyc}	
Transmit data delay time (clock sync)	t_{TXD}	—	100	ns	22.28
Receive data setup time (clock sync)	t_{RXS}	100	—	ns	
Receive data hold time (clock sync)	t_{RXH}	100	—	ns	

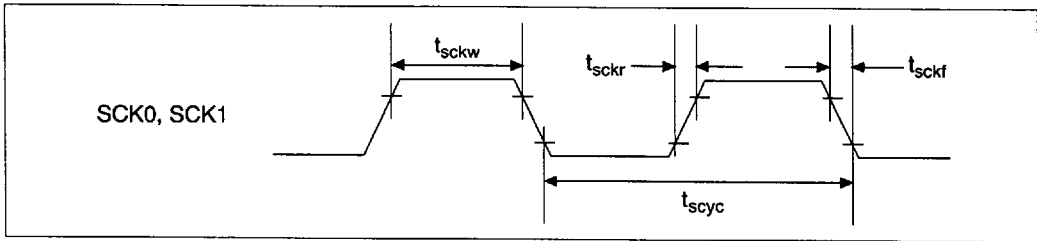


Figure 22.27 Input Clock Timing

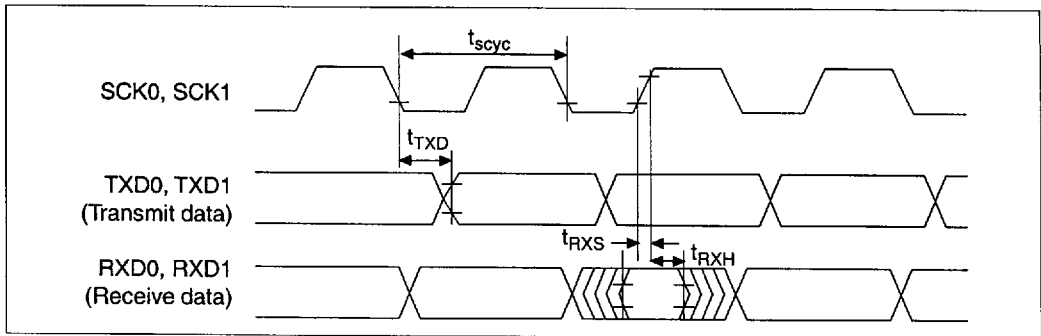


Figure 22.28 SCI I/O Timing (Clock Sync Mode)

22.3.9 A/D Converter Timing

Table 22.13 A/D Converter Timing (Conditions: $V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{REF} = 4.5 \text{ V}$ to AV_{CC} , $V_{SS} = AV_{SS} = 0 \text{ V}$, $T_a = 20$ to $+75^\circ\text{C}$)

Item	Symbol	Min	Max	Unit	Figure
External trigger input pulse width	t_{TRGW}	2	—	t_{cyt}	22.29
External trigger input start delay time	t_{TRGS}	50	—	ns	
A/D conversion time (40 states)	t_{CONV}	42.5	42.5	t_{cyt}	22.30
A/D conversion time (80 states)	t_{CONV}	82.5	82.5		

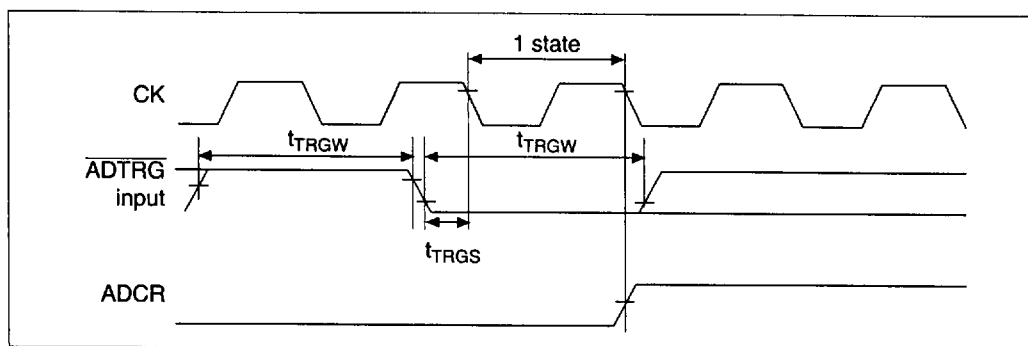


Figure 22.29 External Trigger Input Timing

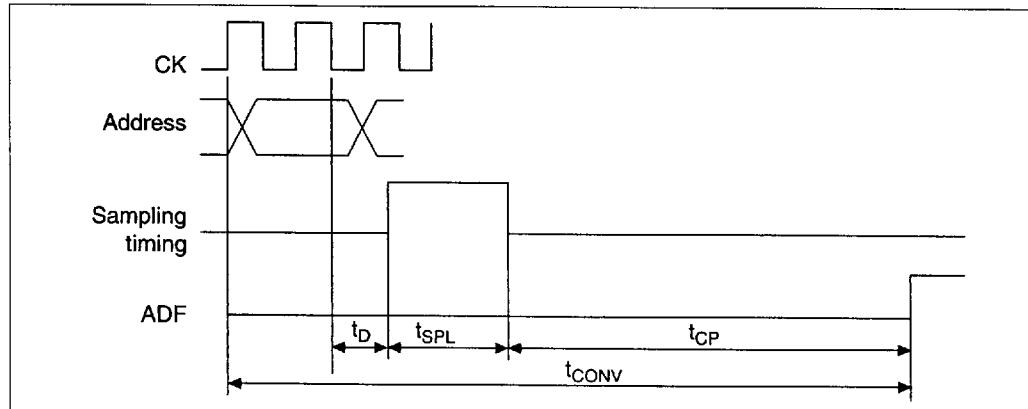


Figure 22.30 Analog Conversion Timing

22.3.10 Measuring Conditions for AC Characteristics

- Input reference levels:
 - High level: 2.2 V
 - Low level: 0.8 V
- Output reference levels:
 - High level: 2.0 V
 - Low level: 0.8 V

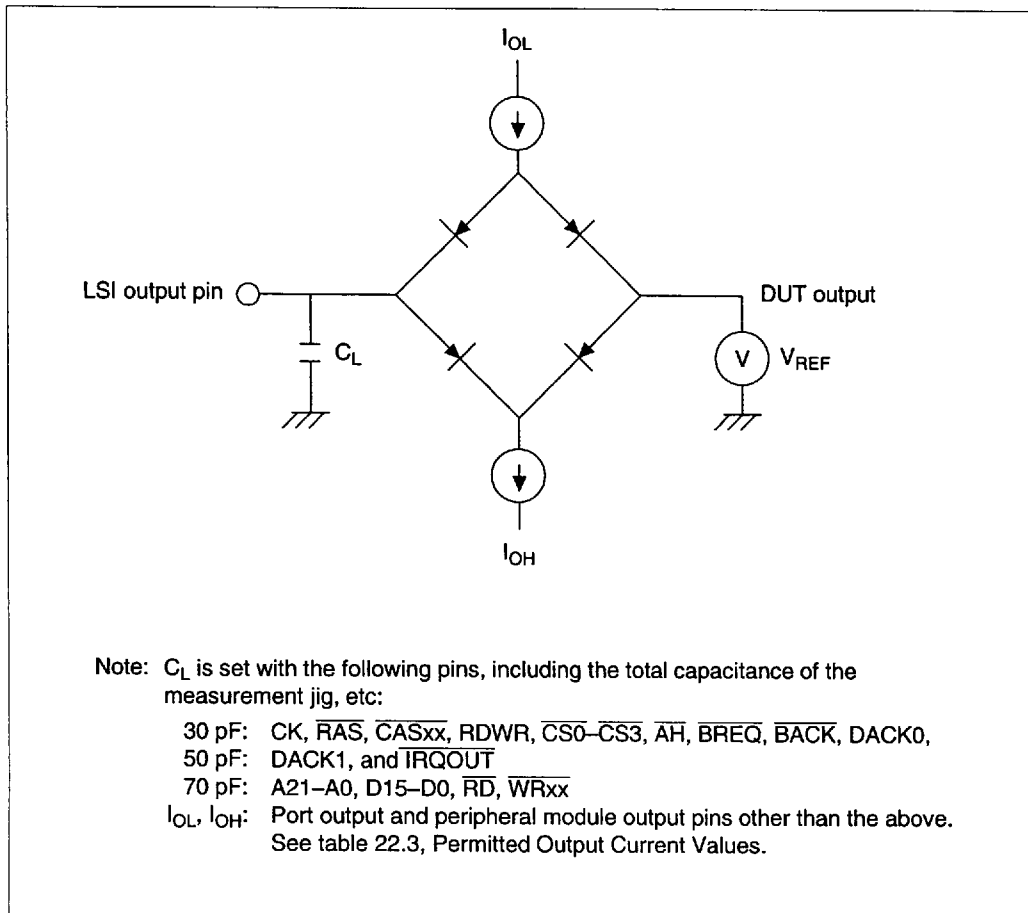


Figure 22.31 Output Test Circuit

22.4 A/D Converter Characteristics

Table 22.14 A/D Converter Timing (Conditions: $V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = 5.0 \text{ V} \pm 10\%$,
 $AV_{CC} = V_{CC} \pm 10\%$, $AV_{REF} = 4.5 \text{ V to } AV_{CC}$, $V_{SS} = AV_{SS} = 0 \text{ V}$, $T_a = 20 \text{ to } +75^\circ\text{C}$)

Item	28 MHz			20 MHz			Unit
	Min	Typ	Max	Min	Typ	Max	
Resolution	10	10	10	10	10	10	Bits
Conversion time	—	—	2.9	—	—	4	μs
Analog input capacitance	—	—	20	—	—	20	pF
Permitted signal source impedance	—	—	1	—	—	1	k Ω
Non-linear error	—	—	TBD	—	—	TBD	LSB
Offset error	—	—	TBD	—	—	TBD	LSB
Full-scale error	—	—	TBD	—	—	TBD	LSB
Quantization error	—	—	TBD	—	—	TBD	LSB
Absolute error	—	—	8	—	—	8	LSB