



**V61C67 FAMILY  
HIGH PERFORMANCE LOW POWER  
16K x 1 BIT  
CMOS STATIC RAM**

**Features**

- High Speed
  - Maximum access time of 25/35/45/55/70 ns
  - Equal access and cycle times
- Low Power
  - 0.5  $\mu$ W typical standby
  - 150 mW typical operating
- Capable of Battery Backup Operation (V61C67\* \* \*L)
- Six transistor CMOS memory cell
- VICMOS process virtually eliminates alpha particle soft errors without die coating
- Single +5V Supply and High Density 20 Pin Packages
- Completely static Memory
  - No Clock or Timing Strobe Required
- TTL compatible

**Description**

The V61C67 is a high speed, low power, 16,384-word by 1-bit CMOS static RAM fabricated using high-performance VICMOS process technology. This high reliability process coupled with innovative circuit design techniques, yields access times of 25 ns maximum.

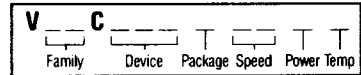
When the chip select is high, the device assumes a standby mode in which the device power dissipation is reduced to 0.5  $\mu$ W (typically). The V61C67\* \* \*L has a data retention mode that guarantees that data will remain valid at a minimum power supply voltage of 2.0 volts.

Using VICMOS technology, supply voltages from 2.0 to 5.5 volts have little effect on supply current in data retention mode. Reducing the supply voltage to minimize current drain is unnecessary with the V61C67 family.

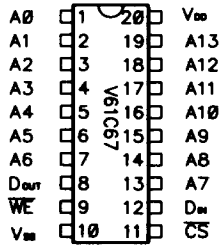
**Device Usage Chart**

| Operating Temperature Range | Package Outline |   |   | Access Time (ns) |    |    |    |    | Power |      | Temperature Mark |
|-----------------------------|-----------------|---|---|------------------|----|----|----|----|-------|------|------------------|
|                             | P               | D | F | 25               | 35 | 45 | 55 | 70 | Low   | Std. |                  |
| 0°C to 70°C                 | •               |   | • | •                | •  | •  | •  | •  | •     | •    | Blank            |
| -40°C to +85°C              | •               | • | • |                  | •  | •  | •  | •  | •     | •    | I                |
| -55°C to +125°C             |                 | • |   |                  |    | •  | •  | •  | •     | •    | X                |

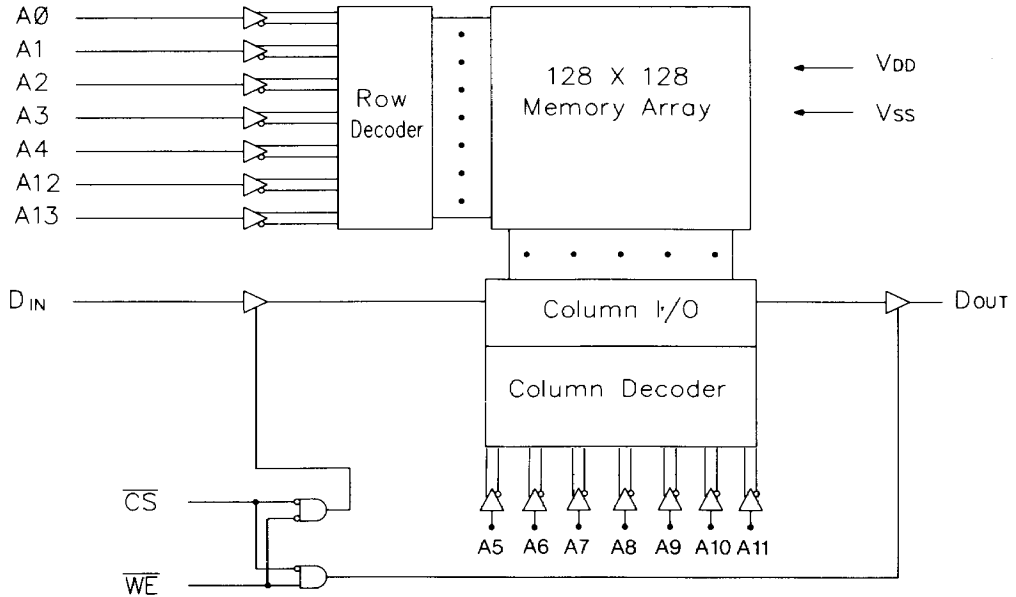
| Package               | Std. | Pin Count |
|-----------------------|------|-----------|
| Plastic DIP           | P    | 20        |
| SOIC (Mini Flat Pack) | F    | 20        |
| Cer DIP               | D    | 20        |



**PIN CONFIGURATION**  
Top View



**BLOCK DIAGRAM**



**Absolute Maximum Ratings (1)**

| Symbol     | Parameter                                   | Rating        | Unit |
|------------|---|---------------|------|
| $V_{TERM}$ | Voltage on any Pin with Respect to $V_{SS}$ | -0.5* to +7.0 | V    |
| $T_A$      | Operating Temperature Under Bias            | -55 to +125   | °C   |
| $T_{STG}$  | Storage Temperature                         | -65 to +150   | °C   |
| $P_T$      | Power Dissipation                           | 1.0           | W    |
| $I_{OUT}$  | DC Output Current                           | 50            | mA   |

\*-3.5V for 20 ns pulse.

**NOTE:**

1. Operation at or near absolute maximum ratings can affect device reliability.

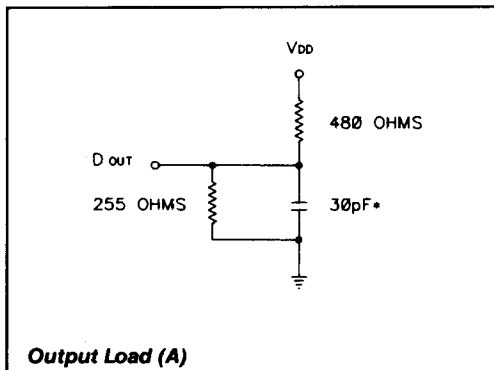
**Recommended Operating Conditions**

| Symbol   | Parameter          | Min.  | Typ. | Max.     | Unit |
|----------|--------------------|-------|------|----------|------|
| $V_{DD}$ | Supply Voltage     | 4.5   | 5.0  | 5.5      | V    |
| $V_{SS}$ | Supply Voltage     | 0.0   | 0.0  | 0.0      | V    |
| $V_{IH}$ | Input High Voltage | 2.2   | 3.5  | $V_{DD}$ | V    |
| $V_{IL}$ | Input Low Voltage  | -0.5* | —    | +0.8     | V    |

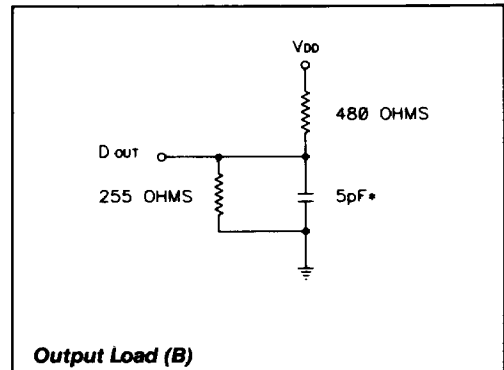
\*-3.5V for 20 ns pulse.

**AC Test Conditions**

Signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0.0 to 3.0V, output loading as shown in diagrams below.



\*Including scope and jig


**Truth Table**

| Mode         | $\overline{CS}$ | $\overline{WE}$ | $V_{DD}$ Current  | $D_{out}$ Pin | Ref. Cycle  |
|--------------|-----------------|-----------------|-------------------|---------------|-------------|
| Not Selected | H               | X               | $I_{SB}, I_{SB1}$ | High-Z        | Standby     |
| Read         | L               | H               | $I_{DD}$          | $D_{out}$     | Read Cycle  |
| Write        | L               | L               | $I_{DD}$          | High-Z        | Write Cycle |

**Capacitance**

$T_A = 25^\circ\text{C}$ ,  $f = 1 \text{ MHz}$

| Symbol    | Parameter          | Conditions     | Typ. | Max. | Unit |
|-----------|--------------------|----------------|------|------|------|
| $C_{IN}$  | Input Capacitance  | $V_{IN} = 0V$  | 3    | 4    | pF   |
| $C_{OUT}$ | Output Capacitance | $V_{OUT} = 0V$ | 4    | 6    | pF   |

**NOTE:**

These parameters are sampled and not 100% tested.

**Commercial Temperature Range**
**DC Characteristics**
 $T_A = 0^\circ\text{C to } 70^\circ\text{C}$ ,  $V_{DD} = 5\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$ , unless otherwise noted.

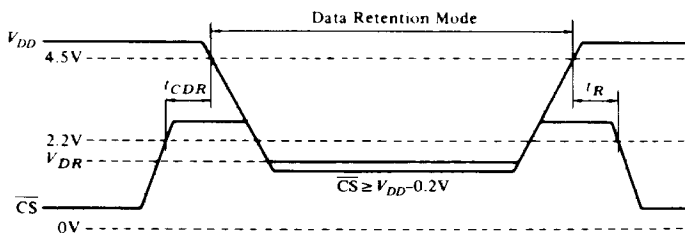
| Parameter                      | Symbol     | Test Conditions   | Min. | Typ. | Max. | Unit          |
|--------------------------------|------------|---|------|------|------|---------------|
| Input Leakage Current          | $ I_{LI} $ | $V_{DD} = 5.5\text{V}$ , $V_{IN} = 0.0\text{V to } V_{DD}$                  | —    | —    | 2    | $\mu\text{A}$ |
| Output Leakage Current         | $ I_{LO} $ | $\overline{CS} = V_{IH}$ , $V_{OUT} = 0.0\text{V to } V_{DD}$               | —    | —    | 2    | $\mu\text{A}$ |
| Operating Power Supply Current | $I_{DD}$   | $\overline{CS} = V_{IL}$ , Output Open                                      | —    | 30   | 60   | mA            |
| Standby Power Supply Current   | $I_{SB}$   | $\overline{CS} = V_{IH}$  | —    | 2    | 5    | mA            |
|                                | $I_{SB1}$  | $\overline{CS} = V_{DD} - 0.2\text{V}$<br>$V_{IN} = 0.0\text{V to } V_{DD}$ | —    | 4    | 100  | $\mu\text{A}$ |
|                                |            | V61C67  | —    | 0.1  | 2.0  |               |
|                                |            | V61C67** **L  | —    | 0.1  | 2.0  |               |
| Output Low Voltage             | $V_{OL}$   | $I_{OL} = 8.0\text{ mA}$  | —    | —    | 0.4  | V             |
| Output High Voltage            | $V_{OH}$   | $I_{OH} = -4.0\text{ mA}$   | 2.4  | —    | —    | V             |

**NOTE:**

 Typical values are at  $V_{DD} = 5.0\text{V}$ ,  $T_A = 25^\circ\text{C}$  and specified loading

**Low  $V_{DD}$  Data Retention Characteristics**
 $T_A = 0^\circ\text{C to } 70^\circ\text{C}$ 

| Parameter                            | Symbol     | Test Condition   | V61C67** **L |      |      | Unit          |
|--------------------------------------|------------|--|--------------|------|------|---------------|
|                                      |            |  | Min.         | Typ. | Max. |               |
| $V_{DD}$ for Data Retention          | $V_{DR}$   |  | 2.0          | —    | 5.5  | V             |
| Data Retention Current               | $I_{DDDR}$ | $\overline{CS} \geq V_{DD} - 0.2\text{V}$<br>$V_{IN} = 0.0\text{V to } V_{DD}$<br>$V_{DD} = 3.0\text{V}$ |              | 0.05 | 2.0  | $\mu\text{A}$ |
| Chip Deselect to Data Retention Time | $t_{CDR}$  |  | 0.0          | —    | —    | ns            |
| Operation Recovery Time              | $t_R$      |  | $t_{RC}^*$   | —    | —    | ns            |

 $t_{RC}^* = \text{Read Cycle Time}$ 
**Low  $V_{DD}$  Data Retention Waveform**


**Industrial Temperature Range**
**DC Characteristics**
 $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} = 5\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$ , unless otherwise noted.

| Parameter                      | Symbol     | Test Conditions  | Min.        | Typ. | Max. | Unit          |
|--------------------------------|------------|--|-------------|------|------|---------------|
| Input Leakage Current          | $ I_{LI} $ | $V_{DD} = 5.5\text{V}$ , $V_{IN} = 0.0\text{V}$ to $V_{DD}$                            | —           | —    | 5    | $\mu\text{A}$ |
| Output Leakage Current         | $ I_{LO} $ | $\overline{\text{CS}} = V_{IH}$ , $V_{OUT} = 0.0\text{V}$ to $V_{DD}$                  | —           | —    | 5    | $\mu\text{A}$ |
| Operating Power Supply Current | $I_{DD}$   | $\overline{\text{CS}} = V_{IL}$ , Output Open  | —           | 30   | 70   | $\text{mA}$   |
| Standby Power Supply Current   | $I_{SB}$   | $\overline{\text{CS}} = V_{IH}$  | —           | 2    | 5    | $\text{mA}$   |
|                                | $I_{SB1}$  | $\overline{\text{CS}} \geq V_{DD} - 0.2\text{V}$<br>$V_{IN} = 0.0\text{V}$ to $V_{DD}$ | V61C67<br>— | 4    | 150  | $\mu\text{A}$ |
|                                |            | V61C67** **L   | —           | 0.1  | 40   |               |
| Output Low Voltage             | $V_{OL}$   | $I_{OL} = 8.0\text{mA}$  | —           | —    | 0.4  | $\text{V}$    |
| Output High Voltage            | $V_{OH}$   | $I_{OH} = -4.0\text{mA}$   | 2.4         | —    | —    | $\text{V}$    |

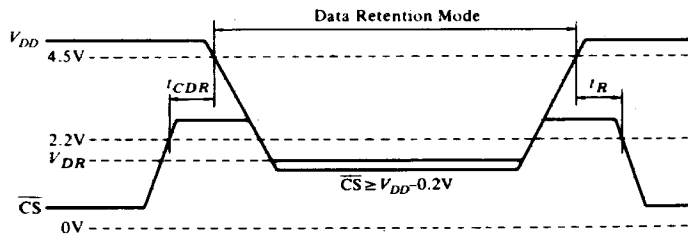
**NOTE:**

 Typical values are at  $V_{DD} = 5.0\text{V}$ ,  $T_A = 25^{\circ}\text{C}$  and specified loading.

**Low  $V_{DD}$  Data Retention Characteristics**
 $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ 

| Parameter                            | Symbol     | Test Condition   | V61C67** **L |      |      | Unit          |
|--------------------------------------|------------|--|--------------|------|------|---------------|
|                                      |            |  | Min.         | Typ. | Max. |               |
| $V_{DD}$ for Data Retention          | $V_{DR}$   |  | 2.0          | —    | 5.5  | $\text{V}$    |
| Data Retention Current               | $I_{DDDR}$ | $\overline{\text{CS}} \geq V_{DD} - 0.2\text{V}$<br>$V_{IN} = 0.0\text{V}$ to $V_{DD}$<br>$V_{DD} = 3.0\text{V}$ |              | 0.05 | 5.0  | $\mu\text{A}$ |
| Chip Deselect to Data Retention Time | $t_{CDR}$  |  | 0.0          | —    | —    | $\text{ns}$   |
| Operation Recovery Time              | $t_R$      |  | $t_{RC}^*$   | —    | —    | $\text{ns}$   |

 $t_{RC}^*$  = Read Cycle Time

**Low  $V_{DD}$  Data Retention Waveform**


**Extended Temperature Range**
**DC Characteristics**
 $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{DD} = 5\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$ , unless otherwise noted.

| Parameter                      | Symbol     | Test Conditions  | Min.        | Typ. | Max. | Unit          |
|--------------------------------|------------|--|-------------|------|------|---------------|
| Input Leakage Current          | $ I_{LI} $ | $V_{DD} = 5.5\text{V}$ , $V_{IN} = 0.0\text{V}$ to $V_{DD}$                            | —           | —    | 10   | $\mu\text{A}$ |
| Output Leakage Current         | $ I_{LO} $ | $\overline{\text{CS}} = V_{IH}$ , $V_{OUT} = 0.0\text{V}$ to $V_{DD}$                  | —           | —    | 10   | $\mu\text{A}$ |
| Operating Power Supply Current | $I_{DD}$   | $\overline{\text{CS}} = V_{IL}$ , Output Open  | —           | 30   | 80   | $\text{mA}$   |
| Standby Power Supply Current   | $I_{SB}$   | $\overline{\text{CS}} = V_{IH}$  | —           | 2    | 5    | $\text{mA}$   |
|                                | $I_{SB1}$  | $\overline{\text{CS}} \geq V_{DD} - 0.2\text{V}$<br>$V_{IN} = 0.0\text{V}$ to $V_{DD}$ | V61C67<br>— | 4    | 200  | $\mu\text{A}$ |
|                                |            | V61C67***L<br>—  | 0.1         | 100  |      |               |
| Output Low Voltage             | $V_{OL}$   | $I_{OL} = 8.0\text{mA}$  | —           | —    | 0.4  | V             |
| Output High Voltage            | $V_{OH}$   | $I_{OH} = -4.0\text{mA}$   | 2.4         | —    | —    | V             |

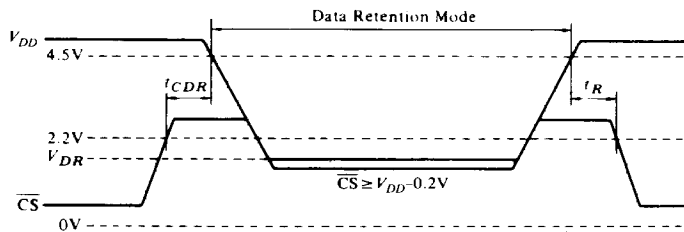
**NOTE:**

 Typical values are at  $V_{DD} = 5.0\text{V}$ ,  $T_A = 25^\circ\text{C}$  and specified loading.

**Low  $V_{DD}$  Data Retention Characteristics**
 $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ 

| Parameter                            | Symbol     | Test Condition   | V61C67***L |      |      | Unit          |
|--------------------------------------|------------|--|------------|------|------|---------------|
|                                      |            |  | Min.       | Typ. | Max. |               |
| $V_{DD}$ for Data Retention          | $V_{DR}$   |  | 2.0        | —    | 5.5  | V             |
| Data Retention Current               | $I_{DDDR}$ | $\overline{\text{CS}} \geq V_{DD} - 0.2\text{V}$<br>$V_{IN} = 0.0\text{V}$ to $V_{DD}$<br>$V_{DD} = 3.0\text{V}$ |            | 0.05 | 10.0 | $\mu\text{A}$ |
| Chip Deselect to Data Retention Time | $t_{CDR}$  |  | 0.0        | —    | —    | ns            |
| Operation Recovery Time              | $t_R$      |  | $t_{RC}^*$ | —    | —    | ns            |

 $t_{RC}^*$  = Read Cycle Time

**Low  $V_{DD}$  Data Retention Waveform**


**Temperature/Access Range**

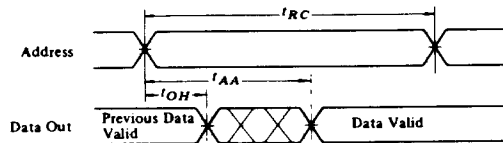
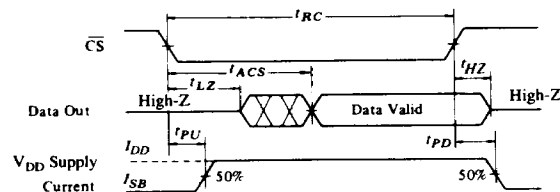
| Temperature Range | Access Time Range |
|-------------------|-------------------|
| 0°C to 70°C       | 25/35/45/55/70 ns |
| -40°C to +85°C    | 35/45/55/70 ns    |
| -55°C to +125°C   | 45/55/70 ns       |

**AC Characteristics**

At recommended operating conditions, unless otherwise noted.

**Read Cycle**

| Symbol    | Parameter                           | V61C67 *25 |      | V61C67 *35 |      | V61C67 *45 |      | V61C67 *55 |      | V61C67 *70 |      | Unit | Notes   |
|-----------|-------------------------------------|------------|------|------------|------|------------|------|------------|------|------------|------|------|---------|
|           |                                     | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.       | Max. |      |         |
| $t_{RC}$  | Read Cycle Time                     | 25         | —    | 35         | —    | 45         | —    | 55         | —    | 70         | —    | ns   | 1       |
| $t_{AA}$  | Address Access Time                 | —          | 25   | —          | 35   | —          | 45   | —          | 55   | —          | 70   | ns   |         |
| $t_{ACS}$ | Chip Select Access Time             | —          | 25   | —          | 35   | —          | 45   | —          | 55   | —          | 70   | ns   |         |
| $t_{OH}$  | Output Hold from Address Change     | 3          | —    | 3          | —    | 5          | —    | 10         | —    | 10         | —    | ns   |         |
| $t_{LZ}$  | Chip Selection to Output in Low Z   | 5          | —    | 5          | —    | 5          | —    | 10         | —    | 10         | —    | ns   | 2, 3, 7 |
| $t_{HZ}$  | Chip Selection to Output in High Z  | 0          | 15   | 0          | 15   | 0          | 20   | 0          | 20   | 0          | 20   | ns   | 2, 3, 7 |
| $t_{PU}$  | Chip Selection to Power Up Time     | 0          | —    | 0          | —    | 0          | —    | 0          | —    | 0          | —    | ns   |         |
| $t_{PD}$  | Chip Deselection to Power Down Time | —          | 20   | —          | 25   | —          | 30   | —          | 30   | —          | 30   | ns   |         |

**Timing Waveform of Read Cycle 1 (4, 5)**

**Timing Waveform of Read Cycle 2 (4, 6)**

**NOTES:**

- All Read Cycle timings are referenced from last valid address to the first transitioning address.
- At any given temperature and voltage condition,  $t_{HZ}$  max. is less than  $t_{LZ}$  min. both for a given device and from device to device.
- Transition is measured  $\pm 500$ mV from steady state voltage with specified loading in Load B.
- WE is High for read cycle.
- Device is continuously selected,  $\overline{CS} = V_{IL}$ .
- Addresses valid prior to or coincident with  $\overline{CS}$  transition low.
- This parameter is sampled and not 100% tested.

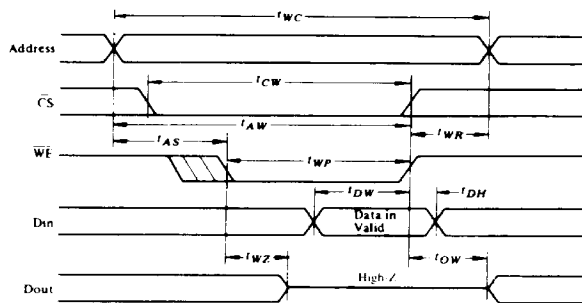
### AC Characteristics

At recommended operating conditions, unless otherwise noted.

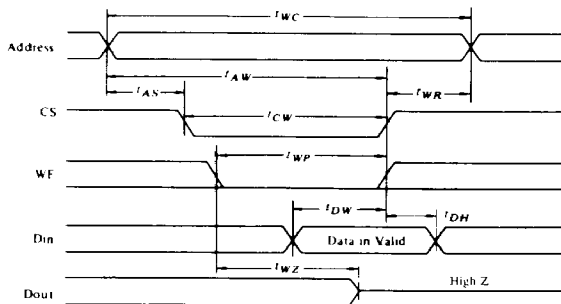
#### Write Cycle

| Symbol   | Parameter                        | V61C67 *25 |      | V61C67 *35 |      | V61C67 *45 |      | V61C67 *55 |      | V61C67 *70 |      | Unit | Notes |
|----------|----------------------------------|------------|------|------------|------|------------|------|------------|------|------------|------|------|-------|
|          |                                  | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.       | Max. |      |       |
| $t_{WC}$ | Write Cycle Time                 | 25         | —    | 35         | —    | 45         | —    | 55         | —    | 70         | —    | ns   | 2     |
| $t_{CW}$ | Chip Selection to End of Write   | 25         | —    | 30         | —    | 40         | —    | 50         | —    | 60         | —    | ns   |       |
| $t_{AW}$ | Address Valid to End of Write    | 25         | —    | 30         | —    | 40         | —    | 50         | —    | 60         | —    | ns   |       |
| $t_{AS}$ | Address Set-up Time              | 0          | —    | 0          | —    | 0          | —    | 0          | —    | 0          | —    | ns   |       |
| $t_{WP}$ | Write Pulse Width                | 20         | —    | 30         | —    | 30         | —    | 35         | —    | 40         | —    | ns   |       |
| $t_{WR}$ | Write Recovery Time              | 0          | —    | 0          | —    | 0          | —    | 0          | —    | 0          | —    | ns   |       |
| $t_{DW}$ | Data Valid to End of Write       | 15         | —    | 20         | —    | 25         | —    | 25         | —    | 30         | —    | ns   |       |
| $t_{DH}$ | Data Hold Time                   | 0          | —    | 0          | —    | 0          | —    | 0          | —    | 0          | —    | ns   |       |
| $t_{WZ}$ | Write Enable to Output in High Z | 0          | 10   | 0          | 15   | 0          | 20   | 0          | 20   | 0          | 25   | ns   | 3, 4  |
| $t_{OW}$ | Output Active from End of Write  | 0          | —    | 0          | —    | 0          | —    | 0          | —    | 0          | —    | ns   | 3, 4  |

#### Timing Waveform of Write Cycle 1 ( $\overline{WE}$ Controlled)



#### Timing Waveform of Write Cycle 2 ( $\overline{CS}$ Controlled) (Note 1)



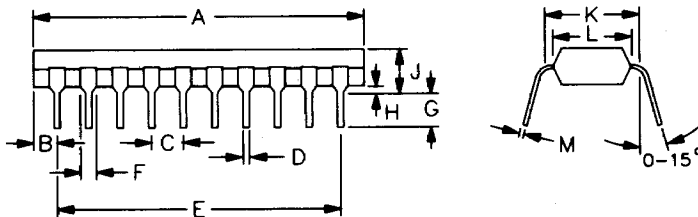
#### NOTES:

1. If  $\overline{CS}$  goes high simultaneously with  $\overline{WE}$  high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured  $\pm 500\text{mV}$  from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

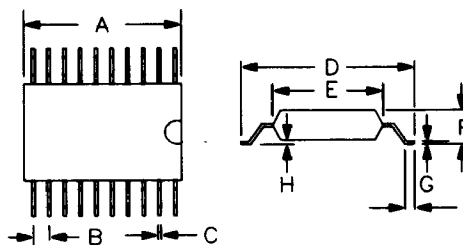


**Package Outline**
**20 Pin Plastic DIP**

| Dimension | Inches     | Millimeters |
|-----------|------------|-------------|
| A         | 1.050 max. | 26.670 max. |
| B         | .074       | 1.905       |
| C         | 0.90/1.10  | 2.286/2.794 |
| D         | .015/.020  | .381/.508   |
| E         | .900       | 22.86       |
| F         | 0.40/.065  | 1.018/1.651 |
| G         | .125/.150  | 3.175/3.810 |
| H         | .005/.050  | .127/1.270  |
| J         | .130/.180  | 3.302/4.572 |
| K         | .330 max.  | 8.382 max.  |
| L         | .300 max.  | 7.62 max.   |
| M         | .009/.012  | .229/.305   |


**20 Pin SOIC Package**

| Dimension | Inches    | Millimeters |
|-----------|-----------|-------------|
| A         | .512      | 13.00       |
| B         | .050      | 1.27        |
| C         | .011/.019 | 0.278/.483  |
| D         | .420 max. | 10.65 max.  |
| E         | .299      | 7.60        |
| F         | .105      | 2.65        |
| G         | .009/.013 | .23/.32     |
| H         | .003/.012 | 0.10/0.30   |
| I         | .015/.050 | 0.40/1.27   |


**20 Pin Cer DIP**

| Dimension | Inches    | Millimeters |
|-----------|-----------|-------------|
| A         | 1.060     | 26.92       |
| B         | .080      | 2.03        |
| C         | .100      | 2.54        |
| D         | .014/.023 | .36/0.58    |
| E         | .900      | 22.86       |
| F         | 0.30/.070 | 0.76/1.78   |
| G         | .125/.200 | 3.18/5.08   |
| H         | .015/.060 | 0.38/1.52   |
| J         | .200      | 5.08        |
| K         | .290/.320 | 7.37/8.13   |
| L         | .220/.310 | 5.59/7.87   |
| M         | .008/.015 | 0.20/0.38   |

