Integrated Device Technology, Inc.

CMOS SYNCHRONOUS RAM 64K (64K x 1-BIT)

PRELIMINARY IDT71501S

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FEATURES:

- Internal pipeline registers on Address, Data and control lines
- Very fast write cycle time
- High-speed
  - Military: 45ns (max.)
  - Commercial: 35/45ns (max.)
- Low power consumption: 385mW (typ.)
- All inputs/outputs TTL-compatible (V_{OL} = 0.4V @ I_{OL} = 8mA)
- Separate, latched data input and output
- Three-state output
- Available in JEDEC standard 24-pin, 300 mil Sidebraze and Plastic DIP, 24-pin, 300 mil SOIC and 28-pin LCC
- Produced with advanced CEMOS™ high-performance technology
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

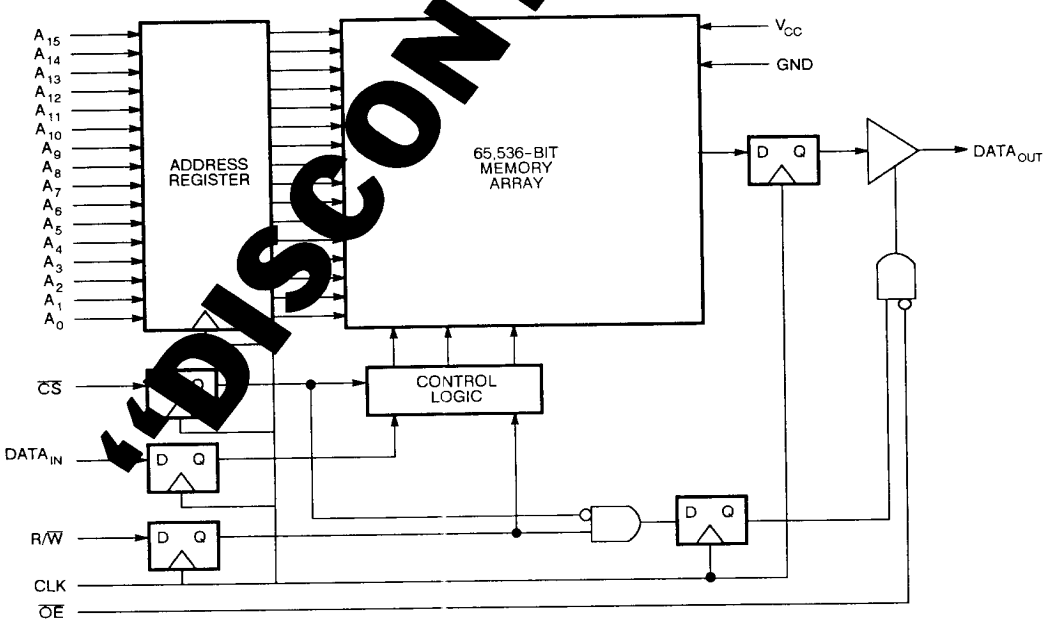
The IDT71501 is a high-speed 64K x 1 static RAM synchronized with pipeline registers on the Address, Data, Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) pins. This product is designed to assist in the design of pipelined processing systems by removing the need for external pipeline registers. The internal registers offer speed improvements through high integration of system functions.

Read cycle times are as fast as 35ns, with higher speed Output Enable ($\overline{OE}$) and Clock to Valid Data Output functions to enable the high-speed system designer maximum throughput possible in an efficient large memory pipelined system. Write cycles are as fast as 25ns. Fabricated using IDT's CEMOS high-performance technology, these devices typically operate on 385mW of power.

The IDT71501 is packaged in industry standard 24-pin, 300 mil plastic and ceramic DIPs, as well as a 28-pin leadless chip carrier (LCC) and 24-pin, 300 mil gullwing SOIC.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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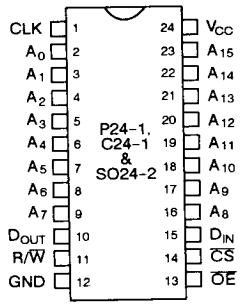
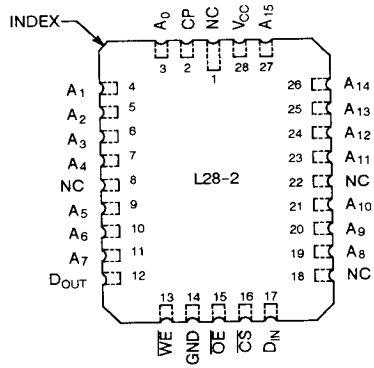
PIN CONFIGURATIONS



DIP/SOIC
TOP VIEW



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITIONS		IDT71501S MIN.	IDT71501S MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	MIL.	–	10	µA
			COM'L.	–	5	
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC} V_{CC} = Max.	MIL.	–	10	µA
			COM'L.	–	5	
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open V_{CC} = Max.	MIL.	–	140	mA
			COM'L.	–	125	
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100% V_{CC} = Max., Output Open	MIL.	–	140	mA
			COM'L.	–	125	
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		–	0.4	V
		I_{OL} = 10mA, V_{CC} = Min.		–	0.5	
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = Min.		2.4	–	V

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

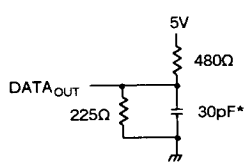


Figure 1. Output Load

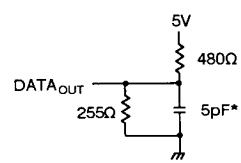


Figure 2. Output Load (for t_{OLZ}, t_{OHZ})

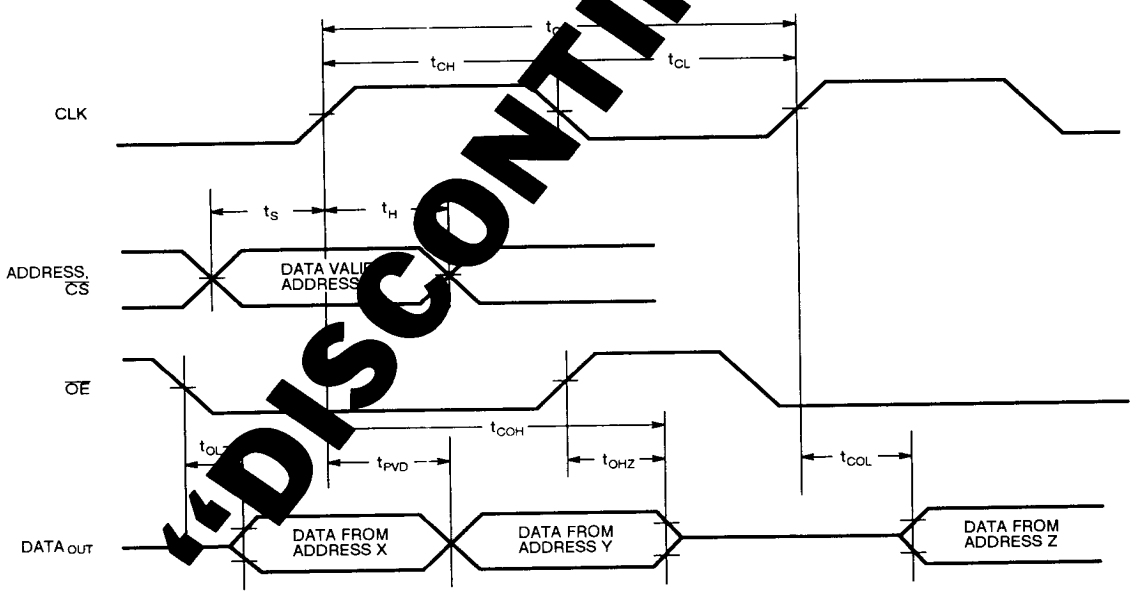
*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

SYMBOL	PARAMETER	IDT71501S35 MIN.	IDT71501S35 MAX.	IDT71501S45 MIN.	IDT71501S45 MAX.	UNIT
READ CYCLE						
t_{CP}	Clock Period (Read Cycle Time)	35	–	45	–	ns
t_{CH}	Clock High Time	7	–	7	–	ns
t_{CL}	Clock Low Time	7	–	7	–	ns
t_S	Data, Address, $\overline{WE}$, $\overline{CS}$ Set-up Time	5	–	5	–	ns
t_H	Data, Address, $\overline{WE}$, $\overline{CS}$ Hold Time	5	–	5	–	ns
t_{OLZ}	Output Low Z Time (1, 2)	0	–	0	–	ns
t_{OHZ}	Output High Z Time (1, 2)	–	15	–	20	ns
t_{PVD}	Prop. Delay, CLK to Valid Data Out	13	–	1[illegible]	–	ns
t_{COL}	Clock to Output in Low Z (2)	0	–	[illegible]	–	ns
t_{COH}	Clock to Output in High Z (2)	–	20	–	25	ns

NOTES:
1. Transition is measured ±200mV from low or high impedance voltage with load (Figures 1 a[illegible]
2. This parameter is guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE (1)



NOTE:
1. The device must be selected by a $\overline{CS}$ level for the conditions above to take place.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

SYMBOL	PARAMETER	IDT71501S35 MIN.	IDT71501S35 MAX.	IDT71501S45 MIN.	IDT71501S45 MAX.	UNIT
WRITE CYCLE						
t_{CP}	Clock Period (Write Cycle Time)	25	–	35	–	ns
t_{CH}	Clock High Time	7	–	7	–	ns
t_{CL}	Clock Low Time	7	–	7	–	ns
t_S	Data, Address, $\overline{WE}$, $\overline{CS}$ Set-up Time	5	–	5	–	ns
t_H	Data, Address, $\overline{WE}$, $\overline{CS}$ Hold Time	5	–	5	–	ns

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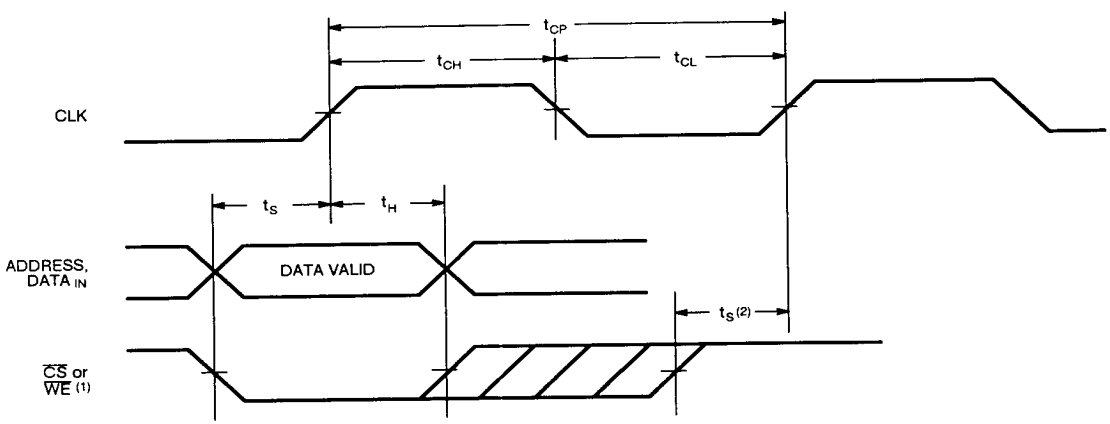
TIMING WAVEFORM OF WRITE CYCLE



NOTES:
1. Either $\overline{CS}$ or $\overline{WE}$ can be used to trigger a write cycle, provided that the other signal is low at the same time.
2. When a write is terminated, either $\overline{CS}$ or $\overline{WE}$ must become high at least one t_S before the next rising edge of CLK.

TRUTH TABLE

MODE	INPUT BEFORE CLK↑ A_{0-15}	$\overline{CS}$	D_{IN}	$\overline{WE}$	$\overline{OE}$	AFTER CLK↑ D_{OUT}
Read	ADDR	L	X	H	L	Data
Write	ADDR	L	Data	L	X	High Z
Deselect	X	H	X	X	X	High Z
Disable	X	X	X	X	H	High Z

ORDERING INFORMATION