TMS50C20: A CMOS SPEECH SYNTHESIZER

USER'S MANUAL

SEPTEMBER 1988

ADVANCE INFORMATION: This document contains information on a new product. Specifications are subject to change without notice.

TABLE OF CONTENTS

1.0 KEY FEATURES

The TMS50C20 is a monolithic CMOS synthesizer. Its key features are:

- CMOS Speech synthesizer
- 40 pins package in DIL or 44 pins in PLCC
- Easy interface in the two major modes of operation:

  I) The READ EPROM MODE where TMS50C20
  ---
  a) Receives a sentence number to be synthesized as an input on
     - Parallel 8 bit port (from switch or microprocessor)
     - Keyboard (3*8 lines).
     - Single pulse that increments the sentence number
     - Serial interface
  b) Reads the speech data corresponding to the all the words of the sentence on EPROM (Rom or RAM)
  c) Speaks all the words corresponding to the sentence.

  II) The MICROPROCESSOR MODE where TMS50C20
  ---
  a) Reads speech data on an 8 bit port (from a microprocessor).
  b) Synthesizes the speech data.

- Minimum requirements hardware for all the interfaces.
- Two coding schemes for the speech data.
  One of the coding scheme is completely compatible with TMS5220 speech data.
- Possibility of automatic setoff for extremely low power consumption
- Possibility to address eproms up to 27C512 without additionnal hardware
- 8 or 10 KHz speech.
- Pulse width D/A converter.

2.0 PACKAGING TYPES

TMS50C20 is available in 40 pin Dual In Line (DIL) standard package, in 40 pin Dual In Line (DIL-YS) shrink package, and in 44 pin lead plastic Chip Carrier (PLCC) package. For mechanical data concerning these packages, consult mechanical data page 64. The pinning of these devices is given below:

2.1 TMS50C20 DUAL IN LINE PACKAGE: FRONT VIEW

Figures 1 and 2 shows the pin assignments for the TMS50C20

Tables 1.1 , 1.2 and 1.3 provide pin function descriptions.

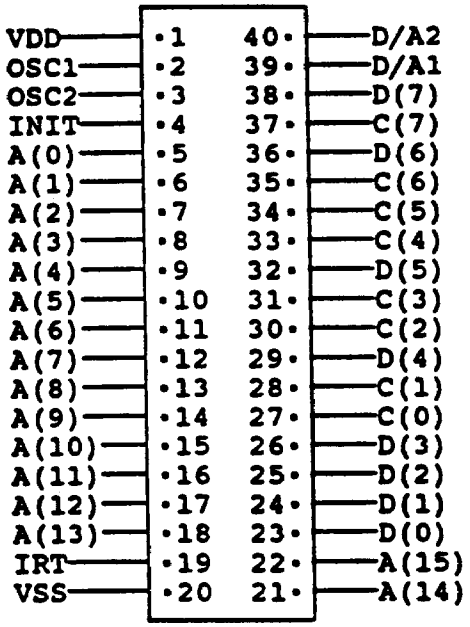

Figure 1 DIL TOP VIEW

2.2 TMS50C20 PLATIC LEAD CHIP CARRIER PACKAGE: FRONT VIEW

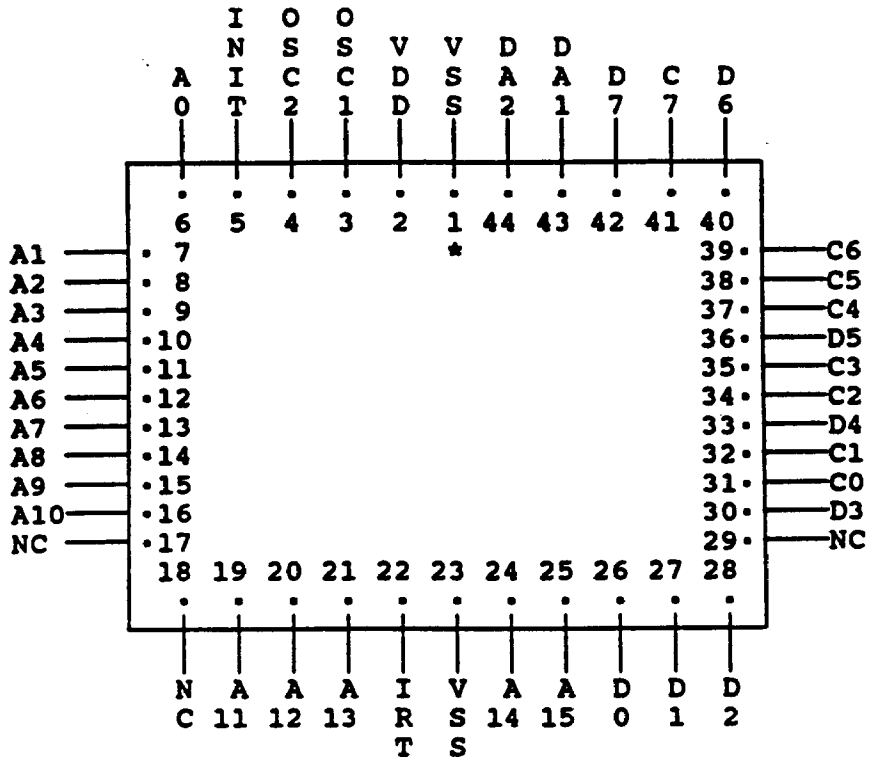

Figure 2 TMS50C20 PLCC TOP View

3.0 PIN DESCRIPTION

The differents pins of Address Port A, Control Port C and Data Port D are described below:

Table 1.1 Pin Function Description of Control PORT C: Parallel Input

PIN NAME	FUNCTIONS	PIN No	I/O		DESCRIPTION
C(0)	μP/EP	27	I/O	0 1	Microprocessor Mode Read Eprom Mode
C(1)	SW/KS	28	I/O	0 1	Parallel or Pulse interface Keyscan interface
C(2)	SETOFF	30	I/O	0 1	Setoff mode (low power consumption) Normal mode
C(3)	VALID	31	I/O		A 1 to 0 transition enables speech
C(4)	RDY	33	I/O		A 1 to 0 transition indicates valid has been read A 0 to 1 transition indicates sentence number has been read
C(5)	SPK	34	I/O	0 1	TMS50C20 speaking TMS50C20 not speaking/waiting for valid signal to go low
C(6)	EPEN	35	I/O		A 1 to 0 transition selects the eprom
C(7)	ALATEN	37	I/O		Address latch enable zero to one transition informs that TMS50C20 is about to read
	PORT C is both input and output				

Table 1.1 Pin Function Description of Control PORT C: Keyscan Interface

PIN NAME	FUNCTIONS	PIN No	I/O		DESCRIPTION
C(0)	μP/EP	27	I/O	0 1	Microprocessor Mode Read Eprom Mode
C(1)	SW/KS	28	I/O	0 1	Parallel or Pulse interface Keyscan interface
C(2)	KS1	30	I/O		Output signal to scan line 1 of keyboard allows scanning of keys 0,3,6,9,12,15,18,21 with each pin of D(0)-D(7)
C(3)	KS2	31	I/O		Output signal to scan line 2 of keyboard allowing scanning of keys 1,4,7,10,13,16,19,22 with each pin of D(0)-D(7)
C(4)	KS3	33	I/O		Output signal to scan line 3 of keyboard allowing scanning of keys 2,5,8,11,14,17,20,23 with each pin of D(0)-D(7)
C(5)	SPK	34	I/O	0 1	TMS50C20 speaking TMS50C20 not speaking/waiting for sentence number
C(6)	EPEN	35	I/O		A 1 to 0 transition selects the Eprom
C(7)	ALATEN	37	I/O		Address latch enable Zero to one transition informs that TMS50C20 is about to read
	PORT C is both input and output				

Table 1.1 Pin Function Description of Control PORT C: Serial

PIN NAME	FUNCTIONS	PIN No	I/O		DESCRIPTION
C(0)	μP/EP	27	I/O	0 1	Microprocessor Mode Read Eprom Mode
C(1)	SW/KS	28	I/O	0 1	Parallel or pulse interface Keyscan interface
C(2)	TX	30	I/O		Serial interface transmit line voltage 0 and 5 Volts
C(3)	RX	31	I/O		Serial interface receive line voltage 0 and 5 Volts
C(4)	RDY	33	I/O		Not used
C(5)	SPK	34	I/O		Not used
C(6)	EPEN	35	I/O		A 1 to 0 transition selects the eprom
C(7)	SERINT	37	I/O	0 1	Serial mode Indicates serial mode is required Indicates any other mode required
	PORT C is both input and output				

Table 1.1 Pin Function Description of Control PORT C: Interface Pulse

PIN NAME	FUNCTIONS	PIN No	I/O		DESCRIPTION
C(0)	µP/EP	27	I/O	0 1	Microprocessor Mode Read Eprom Mode
C(1)	SW/KS	28	I/O	0 1	Parallel or pulse interface Keyscan interface
C(2)	SETOFF	30	I/O	0 1	Setoff mode Normal mode
C(3)	VALID	31	I/O		A 1 to 0 transition enables speech and increments the sentence number to be synthesized
C(4)	RDY	33	I/O		A 1 to 0 transition indicates valid has been read A 1 to 0 transition indicates number has been read
C(5)	SPK	34	I/O	0 1	TMS50C20 speaking TMS50C20 not speaking/waiting for sentence number
C(6)	EPEN	35	I/O		A 1 to 0 transition selects the eprom
C(7)	ALATEN	37	I/O		Address latch enable Zero to one transmission informs that TMS50C20 is about to read
	PORT C is both input and output				

Table 1.2 Pin Function Description of Address Port A and Data Port D

PIN NAME	PIN No	I/O	DESCRIPTION
A(0)	5	O	Address Port A:
A(1)	6	O	- This 16 Pin Port allows to
A(2)	7	O	send an address to an Eprom,
A(3)	8	O	a RAM or a ROM
A(4)	9	O	- The size of the memory can
A(5)	10	O	be up to 512 Kbits
A(6)	11	O	
A(7)	12	O	
A(8)	13	O	
A(9)	14	O	
A(10)	15	O	
A(11)	16	O	
A(12)	17	O	
A(13)	18	O	
A(14)	21	O	
A(15)	22	O	
D(0)	23	I	Data Port D:
D(1)	24	I	- This 8 pin Port reads the
D(2)	25	I	data coming from the Eprom. It
D(3)	26	I	also reads the sentence number
D(4)	29	I	in case of keyscan interface
D(5)	32	I	and parallel interface.
D(6)	36	I	
D(7)	38	I	

Table 1.3 Pin Function Description of other Pins

PIN NAME	PIN No	I/O	DESCRIPTION
IRT	19	O	Not used
DA1	39	O	Noninverting digital-to-analog converter output (PWM)
DA2	40	O	Inverting digital-to-analog converter output (PWM)
INIT	4	I	Initialize input, when low ; device is initialized and goes into the low-power mode, address Port A is latched low. Port A is put into input mode. When INIT goes from low to high the program counter is loaded with zeroes.
OSC1	2	I	Clock input. Chrystal or ceramic resonator between OSC1 OSC2. 3.07 MHz crystal/ceramic resonator for 8 kHz sampling rate. 3.84 MHz crystal/ceramic resonator for 10 kHz sampling rate.
OSC2	3	O	Clock return
VDD	1	I	5 V nominal supply voltage
VSS	20	I	Ground

4.0 INTRODUCTION

The TMS50C20 is a CMOS speech synthesizer. It synthesizes LPC coded data. Three coding schemes are permitted:

1) The 5220 coding scheme.
2) The enhanced coding scheme (654P74 coding scheme)
3) A non coded (8 bits per parameter) scheme.

The first, two schemes are easily obtained with the PC Speech Development Station. The first coding scheme is fully compatible with speech data developped for TMS5220. The second coding scheme is the 654P74 coding table. It is available with version 1.31 of the P.C Speech Development Station (CPC-SDS). It is different form the 654P64 coding table. Please refer to the Speech Development Station user's manual for further information. Also consult the Annex 1 to see how to generate the speech data with PC Speech Development Station.

TMS50C20 is designed to interface easily with any type of applications. There are two major modes of operation:

1) READ EPROM MODE : The synthesizer gets the sentence number from a parallel interface, a serial interface or a keyscan and reads the necessary data directly on RAM or ROM or EPROM.

2) MICROPROCESSOR MODE : The synthesizer reads speech data on its port 3. The speech data is given by an external microprocessor.

Each of these modes is treated separately since it implies a totally different architecture. READ EPROM MODE is treated in chapter 5 and MICROPROCESSOR MODE is treated in chapter 6. For each of these modes, the required hardware is reduced to a minimal number of components. The analog output is available on pins D/A1 and D/A2. Different filters and amplifiers are shown chapter 7 The oscillator frequencies required are:

- 3.84 MHz for 10KHz speech
- 3.07 MHz for 8KHz speech

4.1 APPLICABLE DOCUMENTS

- PC SPEECH DEVELOPMENT STATION USER'S GUIDE

5.0 READ EPROM MODE

In this option, the TMS50C20 can play different sentences. The sentence number to be synthesized is selected:

1)- From a parallel input port. The sentence number is available on the 8 lines of DATA PORT D of the TMS50C20. This bus can be connected to a switch or to a microprocessor. The number of possible sentences is then 256 (2**8).

2)- From an impulse. The TMS50C20 speaks a new sentence each time a negative pulse is sent on VALID pin.

3)- From a keyscan using 3 output lines KS1, KS2, KS3 and up to 8 input lines of DATA PORT D. Therefore, any keyscan 3*8 to 3*1 can be used. Each key addresses a different sentence. In order to play more than 24 sentences, the concept of page is introduced. A page is a set of 24 (or 3 times the number of input lines) sentences. If increment mode is not selected, the last key turns to the next page allowing to play the next 24 (or 3*x) sentences. If increment mode is selected, any key turns to the next page allowing to play the next 24 (or 3*X) sentences.

4)- From a serial asynchronous line at 1200 b/s using only RX and TX signals.

A sentence is made of any word stored in ROM, EPROM or RAM. An addressing scheme for each sentence is described in the ROM description paragraph 5.1.6.

EPROM (RAM or ROM) space for speech data and addressing sheme is up to 512 Kbits (64 Kbytes). EPROM is addressed using a 16 bits address bus A0-A15. Speech data is fed to the TMS50C20 through an 8 line data bus (DATA PORT D).

DATA Port D is sometimes shared between sentence number bus and speech data bus from the EPROM. In this case, a tristate buffer LS244 is required.

Most of the options are available Control Port C. The READ EPROM mode requires µP/EP=1. The distinction between keyscan and parallel interface is made with SW/KS. The Serial interface is obtained with SERINT=0 or ALENTEN=0.

The other options and sub-options are available in the first three EPROM bytes

5.1 READ EPROM MODE: PARALLEL INTERFACE

The mode takes place when SW/KS=0. In this mode, the sentence number is read on DATA Port D. A tristate buffer is required to avoid conflict with the EPROM data bus. Note that the increment mode must be off for this mode. (See paragraph 5.1.6)

5.1.1 READ EPROM MODE WITH PARALLEL INTERFACE: PORT CONFIGURATION

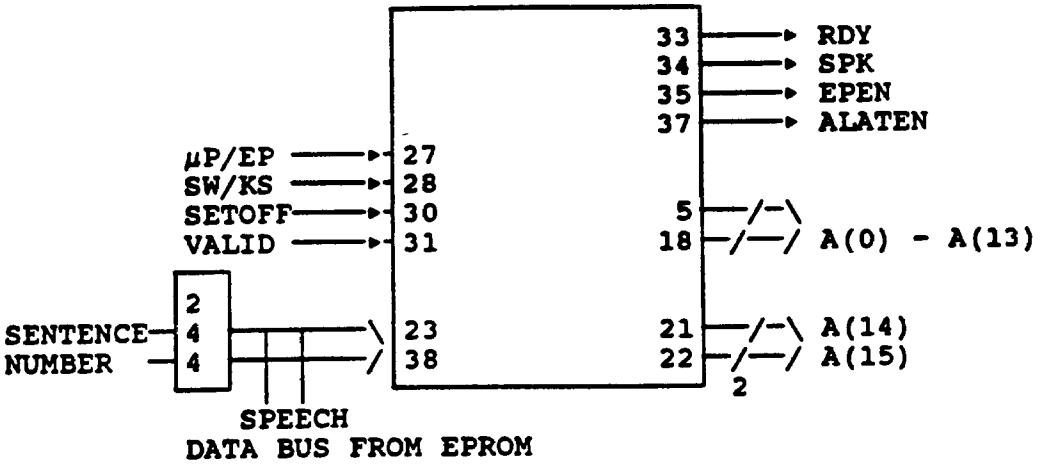

Figure 3 Parallel interface : Port description

5.1.2 EPROM MODE WITH PARALLEL INTERFACE: CONTROLS AND SIGNALS

NAME	PORT	TYPE	VALUE	SIGNIFICATION
µP/EP	27	INPUT	0	MICROPROCESSOR MODE
			1*	READ EPROM MODE
SW/KS	28	INPUT	0*	PARALLEL OR PULSE INTERFACE REQUIRED
			1	KEYSCAN INTERFACE REQUIRED
SETOFF	30	INPUT	0	SETOFF REQUIRED
			1	NORMAL MODE
VALID	31	INPUT		A 1 TO 0 TRANSITION ENABLES SPEECH
RDY	33	OUTPUT		A 1 TO 0 TRANSITION INDICATES VALID HAS BEEN READ A 0 TO 1 TRANSITION INDICATES SENTENCE NUMBER HAS BEEN READ
SPK	34	OUTPUT	0	TMS50C20 SPEAKING
			1	TMS50C20 NOT SPEAKING, WAITING FOR VALID SIGNAL TO GO LOW
EPEN	35	OUTPUT	0	A 1 TO 0 TRANSITION SELECTS THE EPROM
ALATEN	37	OUTPUT		ADDRESS LATCH ENABLE ZERO TO ONE TRANSITION INFORMS THAT TMS50C20 IS ABOUT TO READ.
SERINT	37	INPUT		SERIAL MODE
			0	INDICATES SERIAL MODE IS REQUIRED
			1*	INDICATES ANY OTHER MODE

REMARK 1: A star (*) indicates that these values are required at initialization in order to configurate the TMS50C20 in READ EPROM mode with PARALLEL interface.

REMARK 2: PORT C is both input and output. It is first input to read which configuration is chosen then goes output mode when a control signal is requiered. The two names for the same pin 37 indicate this dual type input/output.

REMARK 3: For TMS50C20, SETOFF, VALID, RDY, SPK, EPEN,as well as DATA PORT have internal pullup resistor. No external pullup are required for these pins.
For TMX50C20, µP/EP, SW/KS, and ALATEN also have a pullup.

5.1.3 READ EPROM MODE WITH PARALLEL INTERFACE: SCHEMATICS

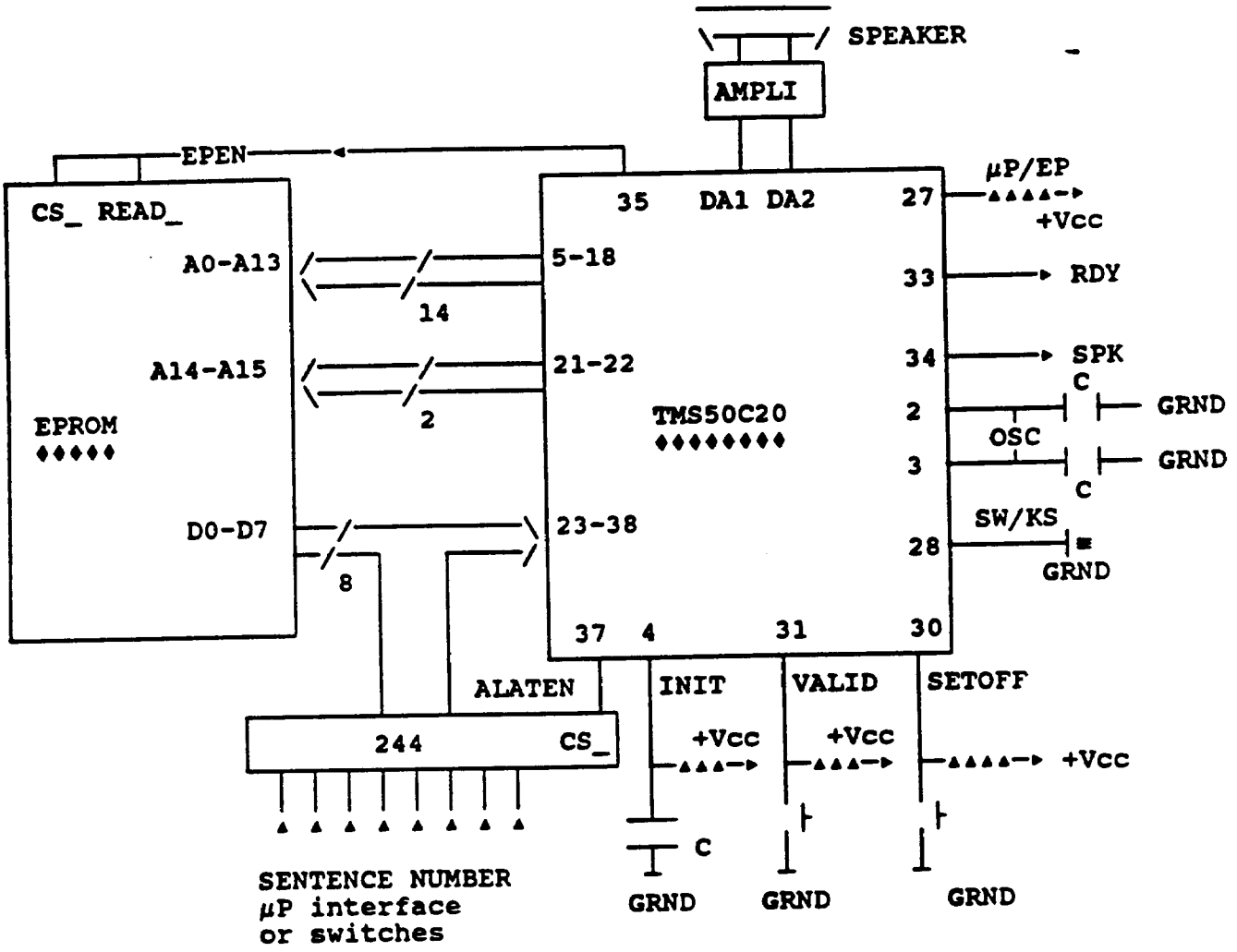

Figure 4 Parallel interface: schematics

5.1.4 READ EPROM MODE WITH PARALLEL INTERFACE: SEQUENCE OF EVENTS

The different steps done by the TMS50C20 are:

1. Read μP/EP and SW/KS to know which configuration to be in.

   If μP/EP=1, SW/KS=0, SETOFF=1 and SERINT=1, then:

2. Read setoff time on EPROM.

3. Set SPK to 1.

4. Test setoff while waiting VALID to go low.
   If SETOFF time expired, then go into low power consumption and waits for a new INIT

5. When VALID is low put Port C in output and send SPK=0, RDY=0

6. Read the sentence number on DATA PORT, set RDY to 1.

7. Read header byte and decode it (see 5.1.6.2).
   If header HB1(2)=1 we are in non increment mode then:

8. Verify if sentence number is correct.

9. Get speech data corresponding to the selected sentence.

10. When end of sentence detected, go to step 3.

5.1.5 READ EPROM MODE WITH PARALLEL INTERFACE: TIMING

Timing describing all the sentence selected.

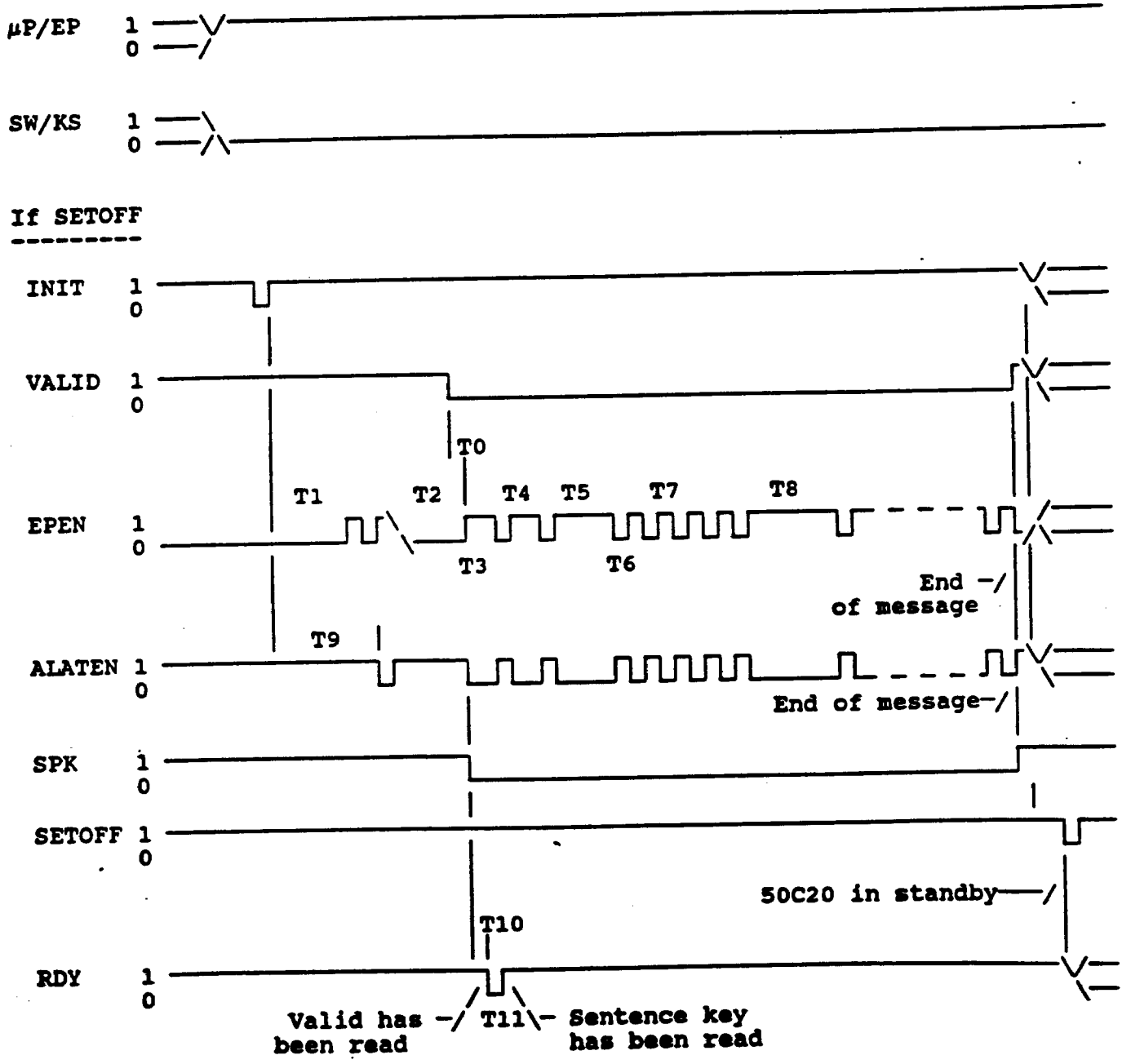

Figure 5 Parallel interface: Timing

T0 = 200us

T1 = 2.3 ms

T2 = time between two keys selected.

T3 = 360 us

T4 = 400 us

T5 = 2.4 ms

T6 = 85 us

T7 = 200 us

T8 = 2.7 ms

T9 = 2.5 ms

T10 = 10 us

T11 = 70 us

5.1.6 EPROM MODE WITH PARALLEL INTERFACE: ROM DESCRIPTION

The ROM contains

1. Three information bytes.
2. The beginning address for each sentence
3. The sentence address table (i.e. the address of the beginning of each word of the sentence).
4. Speech data.

5.1.6.1 EXAMPLE OF ROM

ADDRESS	NAME	DESCRIPTION
0000	HEADER BYTE	See description paragraph 5.1.6.2
0001	SETOFF TIME	Automatic setoff time see paragraph 5.1.6.3
0002	#OF SENTENCE	Number of sentences in EPROM
0003	MSB 0	Most signif bits of the address of sentence 0
0004	LSB 0	Least signif bits of the address of sentence 0
0005	MSB 1	Most signif bits of the address of sentence 1
0006	LSB 1	Least signif bits of the address of sentence 1
0007	MSB 2	Most signif bits of the address of sentence 2
0008	LSB 2	Least signif bits of the address of sentence 2
0009	MSB 3	Most signif bits of the address of sentence 3
000A	LSB 3	Least signif bits of the address of sentence 3
000B	MSB 4	Most signif bits of the address if sentence 4
000C	LSB 4	Least signif bits of the address if sentence 4

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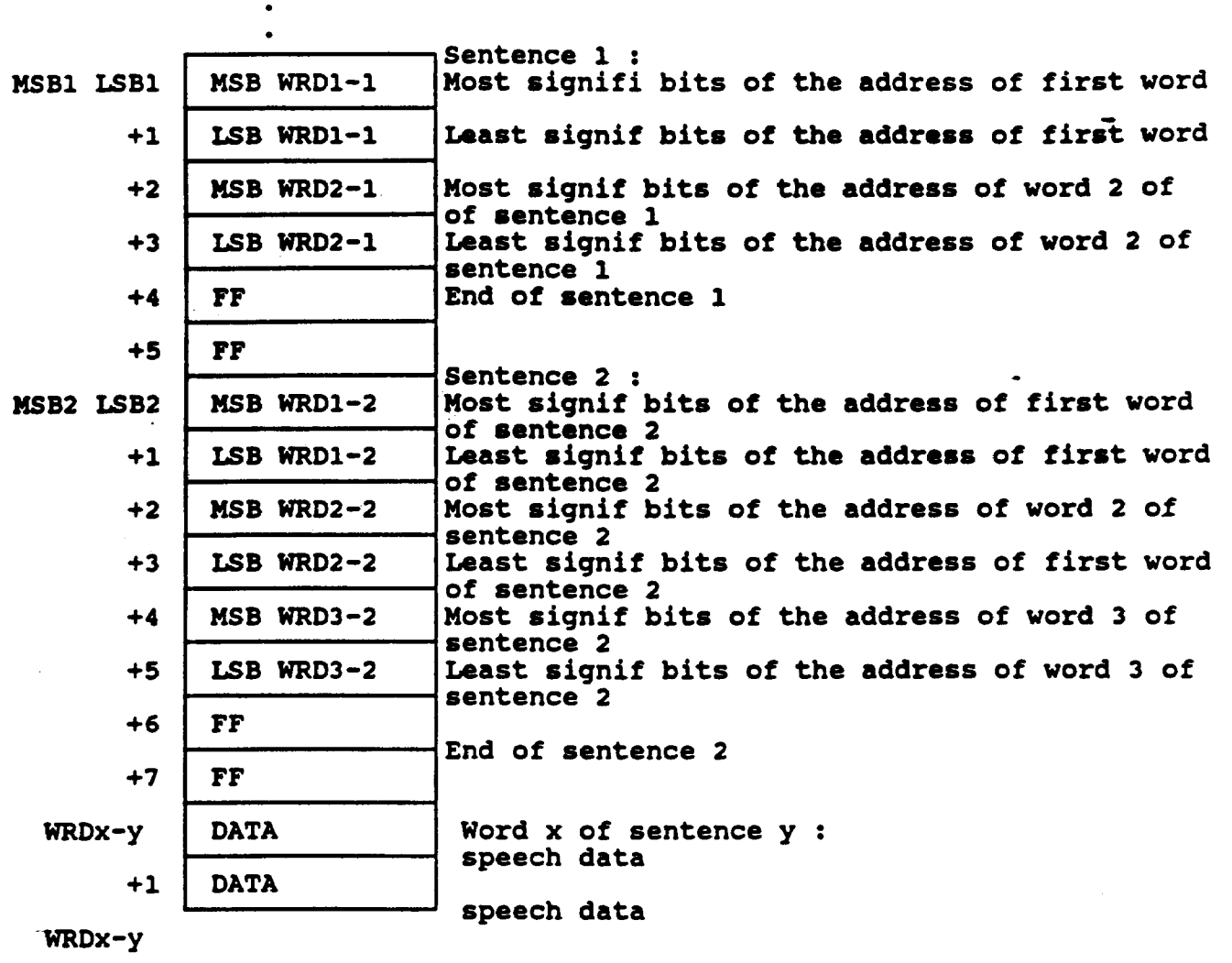

MSB1 LSB1
MSB WRD1-1
Sentence 1 :
Most signifi bits of the address of first word
+1
LSB WRD1-1
Least signif bits of the address of first word
+2
MSB WRD2-1
Most signif bits of the address of word 2 of sentence 1
+3
LSB WRD2-1
Least signif bits of the address of word 2 of sentence 1
+4
FF
End of sentence 1
+5
FF
MSB2 LSB2
MSB WRD1-2
Sentence 2 :
Most signif bits of the address of first word of sentence 2
+1
LSB WRD1-2
Least signif bits of the address of first word of sentence 2
+2
MSB WRD2-2
Most signif bits of the address of word 2 of sentence 2
+3
LSB WRD2-2
Least signif bits of the address of first word of sentence 2
+4
MSB WRD3-2
Most signif bits of the address of word 3 of sentence 2
+5
LSB WRD3-2
Least signif bits of the address of word 3 of sentence 2
+6
FF
End of sentence 2
+7
FF
WRDx-y
DATA
Word x of sentence y :
speech data
+1
DATA
speech data
WRDx-y

5.1.6.2 DESCRIPTION OF HEADER BYTE

The first byte of the ROM describes the coding table that is used as well as other indications. The MSB of the header byte is called -bit 7 (HB1(7)) and the LSB is called bit 0 (HB1(0)). The header byte is as follows:

BITS	VALUE	DESCRIPTION
HB1(0)		Coded/Uncoded
	1	data is coded
	0	data is uncoded
HB1(1)		Type of coding table
	1	5220 coding scheme
	0	enhanced coding scheme
HB1(2)		Increment mode
	0	Increment mode for PULSE interface (see 5.2) and for KEYSCAN interface (5.3)
	1	Normal mode

For parallel interface, we must have HB1(2) = 1.

5.1.6.3 DESCRIPTION OF THE SETOFF TIME

The second byte indicates the time elapsed between any new input and the instant that the chip goes into setoff. This time is expressed in 1/4 seconds (250ms).

Once in setoff mode, the chip needs to be initialized again by setting the INIT pin low.

5.1.6.4 NUMBER OF SENTENCES

The third byte indicates the number of sentences that are available in the EPROM.

5.2 READ EPROM MODE: PULSE INTERFACE

Read eprom mode with pulse interface is very similar to read eprom mode with parallel interface.
The only differences are:

- The header byte must be in increment mode HB1(2)=0.
- DATA PORT is only used for data coming from the EPROM (RAM, ROM).

Each time VALID goes low, the sentence number is incremented and the new sentence is synthesized. If the sentence number becomes greater than the total number of sentences HB1(3), then sentence counter comes to 0 again.

5.2.1 READ EPROM MODE WITH PULSE INTERFACE: PORT CONFIGURATION

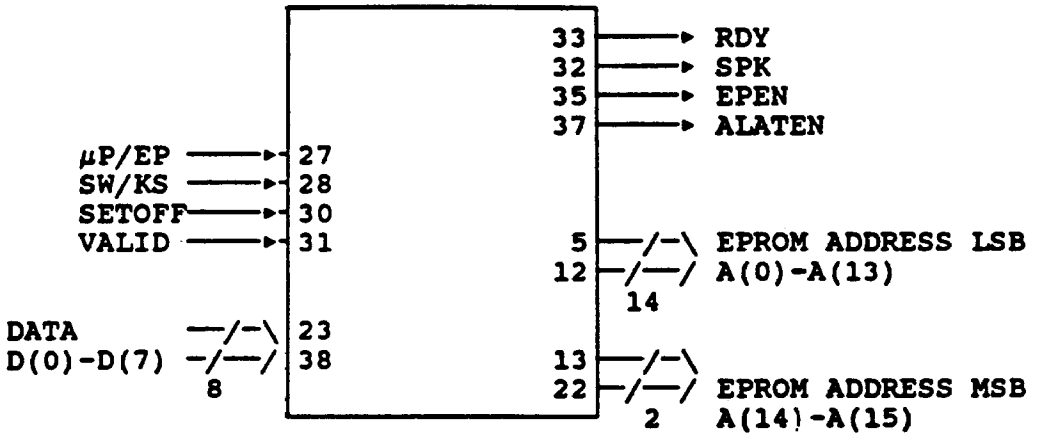


Figure 6 Pulse interface: port configuration

5.2.2 EPROM MODE WITH PULSE INTERFACE: CONTROLS AND SIGNALS

NAME	PORT	TYPE	VALUE	SIGNIFICATION
µP/EP	27	INPUT	0	MICROPROCESSOR MODE
			1*	READ EPROM MODE
SW/KS	28	INPUT	0*	PARALLEL OR PULSE INTERFACE REQUIRED
			1	KEYSCAN INTERFACE REQUIRED
SETOFF	30	INPUT	0	SETOFF REQUIRED
			1	NORMAL MODE
VALID	31	INPUT		A 1 TO 0 TRANSITION ENABLES SPEECH AND INCREMENTS THE SENTENCE NUMBER TO BE SYNTHESIZED
RDY	33	OUTPUT	0	A 1 TO 0 TRANSITION INDICATES VALID HAS BEEN READ
			1	A 1 TO 0 TRANSITION INDICATES NUMBER HAS BEEN READ
SPK	34	OUTPUT	0	50C20 SPEAKING
			1	50C20 NOT SPEAKING/WAITING FOR SENTENCE NUMBER
EPEN	35	OUTPUT	0	A 1 TO 0 TRANSITION SELECTS THE EPROM
ALATEN	37	OUTPUT		ADDRESS LATCH ENABLE ZERO TO ONE TRANSMISSION INFORMS THAT TMS50C20 IS ABOUT TO READ.
SERINT	37	INPUT		SERIAL MODE
		0		INDICATES SERIAL MODE IS REQUIRED
		1		INDICATES ANY OTHER MODE REQUIRED

REMARK 1: A star (*) indicates that these values are required at initialization in order to configurate the TMS50C20 in READ EPROM mode with PULSE interface.

REMARK 2: PORT C is both input and output. It is first input to read which configuration is chosen then goes output mode when a control signal is requiered. The two names for the same pin 37 indicate this dual type input/output.

REMARK 3: For TMS50C20, SETOFF, VALID, RDY, SPK, EPEN,as well as DATA PORT have internal pullup resistor. No external pullup are required for these pins.

For TMX50C20, µP/EP, SW/KS, and ALATEN also have a pullup.

5.2.3 READ EPROM MODE WITH PULSE INTERFACE: SCHEMATICS

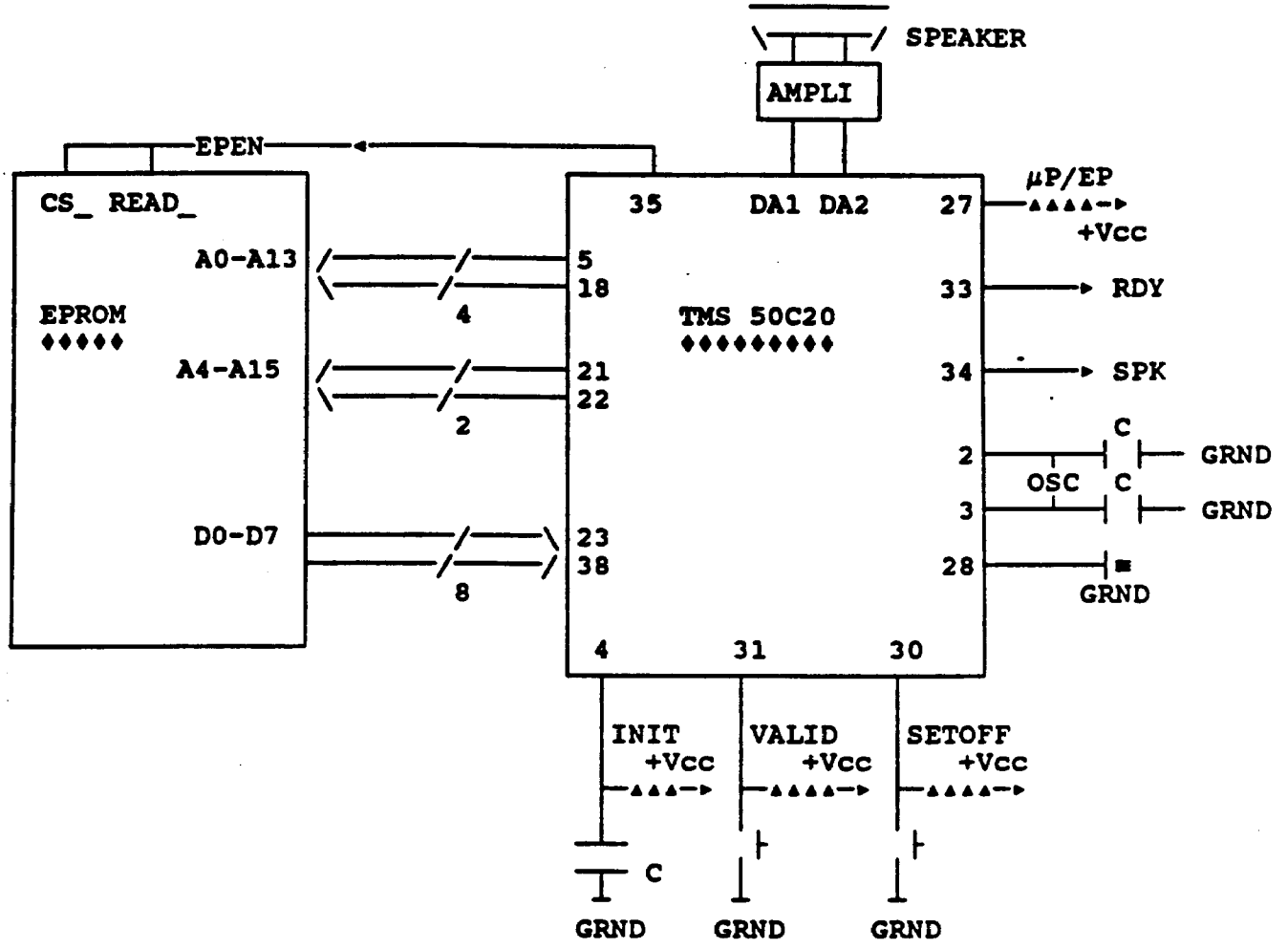


Figure 7 Pulse interface: schematics

5.2.4 READ EPROM MODE WITH PULSE INTERFACE: SEQUENCE OF EVENTS

The different steps done by the TMS50C20 are:

1. Read μP/EP and SW/KS to know which configuration to be in.

   If μP/EP=1, SW/KS=0, SETOFF=1 and SERINT=1, then:

2. Read setoff time on EPROM.

3. Test setoff while waiting VALID to go low
   If SETOFF time expired, then go into low power consumption and waits for a new INIT

4. When VALID is low put Port C in output and send
   ALATEN=0, EPEN=1, SPK=0, RDY=0

5. Read the sentence number on Port D, set RDY to 1.

6. Read header byte and decode it.
   If header HB1(2)=0 we are in increment mode then:

7. The sentence number read on Port D is discarded.
   The previous sentence number is retrieved in a RAM location and incremented. If the sentence number is greater than the total number of sentences, the sentence number is set to 0.

8. Get speech data corresponding to the selected sentence.

9. When end of sentence detected, set SPK to 1 and go to step 3.

5.2.5 READ EPROM MODE WITH PULSE INTERFACE: TIMING

PULSE TIMING IS THE SAME AS INTERFACE PARALLEL MODE

Timing describing all the sentence selected.

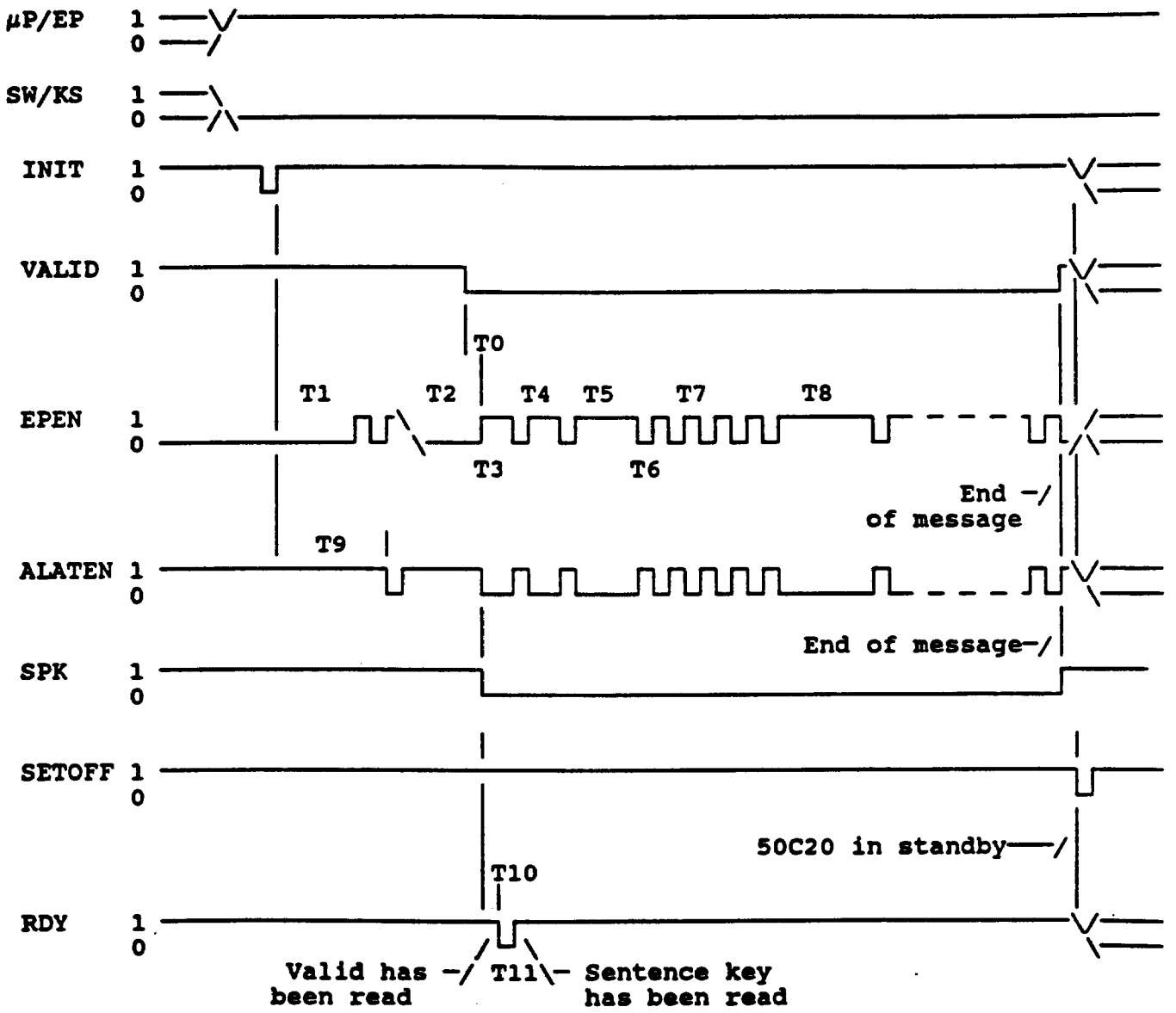


Figure 8 Pulse interface: Timing

T0 = 200us

T1 = 2.3 ms

T2 = time between two keys selected.

T3 = 360 us

T4 = 400 us

T5 = 2.4 ms

T6 = 85 us

T7 = 200 us

T8 = 2.7 ms

T9 = 2.5 ms

T10 = 10 us

T11 = 70 us

5.2.6 EPROM MODE WITH PULSE INTERFACE: ROM DESCRIPTION

The ROM content is:

1. Three information bytes.
2. The beginning address for each sentence
3. The sentence address table (i.e. the address of the beginning of each word of the sentence).
4. Speech data.

See the example of speech ROM paragraph 5.1.6
The first header byte is the same as in section 5.1.6.2 In this option HB1(2) must be equal to 0
The second header byte indicates the setoff time in number of 250ms
The third byte indicates the number of total number of sentences in the EPROM.

5.3 READ EPROM MODE: KEYSCAN INTERFACE

The READ EPROM mode with a KEYSCAN interface allows one to connect a keysboard directly to the TMS50C20. The key board may be a 3*1, 3*2, 3*3, ... 3*8 . Once a key is pressed, the corresponding sentence number is immediately synthesized. As in parallel interface, a tristate buffer must be used to avoid bus conflict between keyscan and eprom data bus.

5.3.1 READ EPROM MODE WITH KEYSCAN INTERFACE: PORT CONFIGURATION

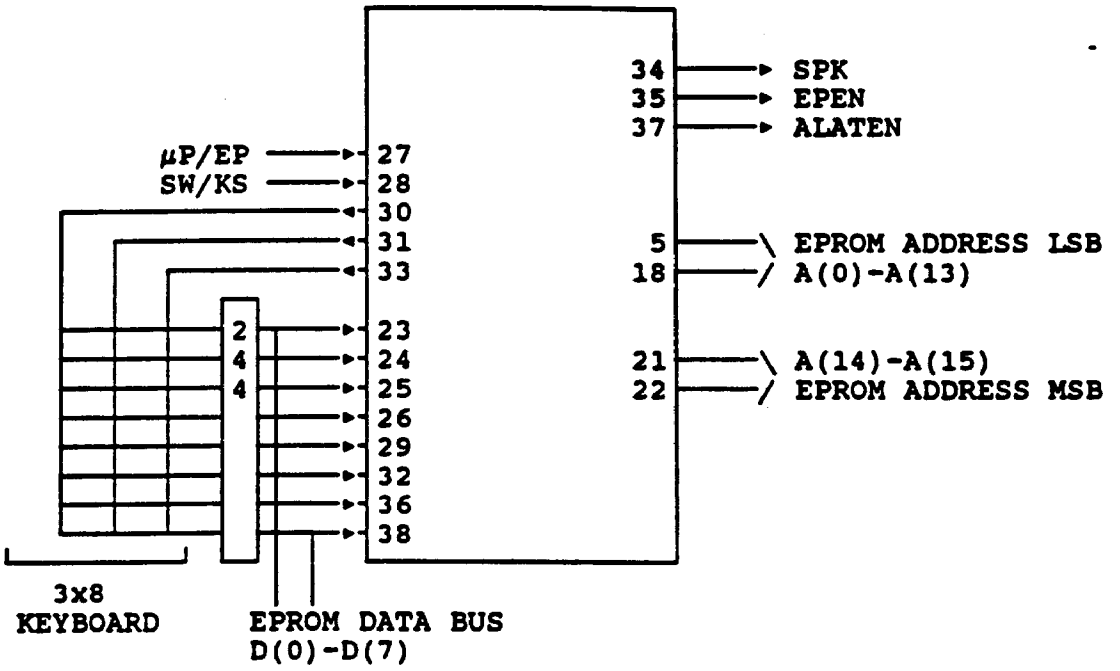


Figure 9 Keyscan interface: port configuration

5.3.2 EPROM MODE WITH KEYSCAN INTERFACE: CONTROLS AND SIGNALS

NAME	PIN	TYPE	VALUE	SIGNIFICATION
µP/EP	27	INPUT	0	MICROPROCESSOR MODE
			1*	READ EPROM MODE
SW/KS	28	INPUT	0	PARALLEL OR PULSE INTERFACE REQUIRED
			1*	KEYSCAN INTERFACE REQUIRED
KS1	30	OUTPUT		OUTPUT SIGNAL TO SCAN LINE 1 OF KEYBOARD ALLOWS SCANNING OF KEYS 0,3,6,9 12,15,18,21 WITH EACH PIN OF D(0)-D(7)
KS2	31	OUTPUT		OUTPUT SIGNAL TO SCAN LINE 2 OF KEYBOARD ALLOWING SCANNING OF KEYS 1,4,7,10 13,16,19,22 WITH EACH PIN OF D(0)-D(7)
KS3	33	OUTPUT		OUTPUT SIGNAL TO SCAN LINE 3 OF KEYBOARD ALLOWING SCANNING OF KEYS 2,5,8,11 14,17,20,23 WITH EACH PIN OF D(0)-D(7)
SPK	34	OUTPUT	0	50C20 SPEAKING
			1	50C20 NOT SPEAKING/WAITING FOR SENTENCE #
EPEN	35	OUTPUT		A 1 TO 0 TRANSITION SELECTS THE EPROM
ALATEN	37	OUTPUT		ADDRESS LATCH ENABLE ZERO TO ONE TRANSMISSION INFORMS THAT TMS50C20 IS ABOUT TO READ.
SERINT	37	INPUT		DURING INITIALIZATION:SERIAL MODE
			0	INDICATES SERIAL MODE IS REQUIRED
			1*	INDICATES ANY OTHER MODE REQUIRED

REMARK 1: A star (*) indicates that these values are required at initialization in order to configurate the TMS50C20 in READ EPROM mode with Keyscan interface.

REMARK 2: PORT C is both input and output. It is first input to read which configuration is chosen then goes output mode when a control signal is requiered. The two names for the same pin 37 indicate this dual type input/output.

REMARK 3: For TMS50C20, SETOFF, VALID, RDY, SPK, EPEN,as well as DATA POR have internal pullup resistor. No external pullup are required for these pins.
For TMX50C20, µP/EP, SW/KS, and ALATEN also have a pullup.

5.3.3 READ EPROM MODE WITH KEYSCAN INTERFACE: SCHEMATICS

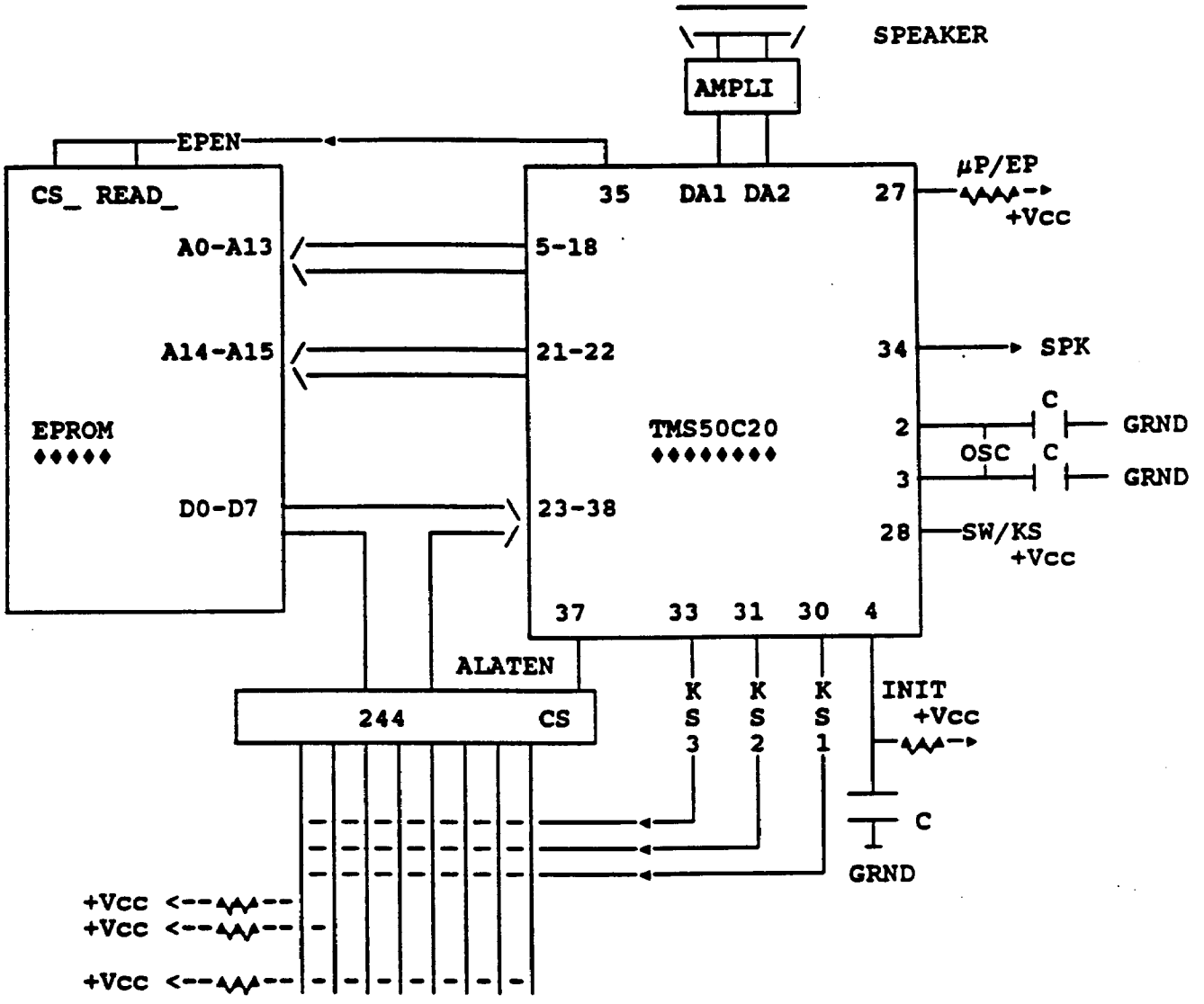


Figure 10 Pulse interface: schematics

5.3.4 READ EPROM MODE WITH KEYSCAN INTERFACE: SEQUENCE OF EVENTS

The different steps done by the TMS50C20 are:

1. Read μP/EP and SW/KS to know which configuration to be in.

   If μP/EP=1, SW/KS=1, and SERINT=1, then:

2. Read setoff time on EPROM.

3. Test setoff while waiting for a key of the keyboard to be pressed. If SETOFF time expired, then go into low power consumption and waits for a new INIT

4. When key is pressed send ALATEN=0, EPEN=0, SPK=0
   (A Key is pressed when a 0 sent in KS is read on data Port D)

5. Read the sentence number from keyboard.

6. Read header byte and decode it.

7. Verify if sentence number is correct.

8. Get speech data corresponding to the selected sentence.

9. When end of sentence detected, set SPK to 1 and go to step 3.

5.3.5 EPROM MODE WITH KEYSCAN: TIMING

Timing describing all the sentence selected.

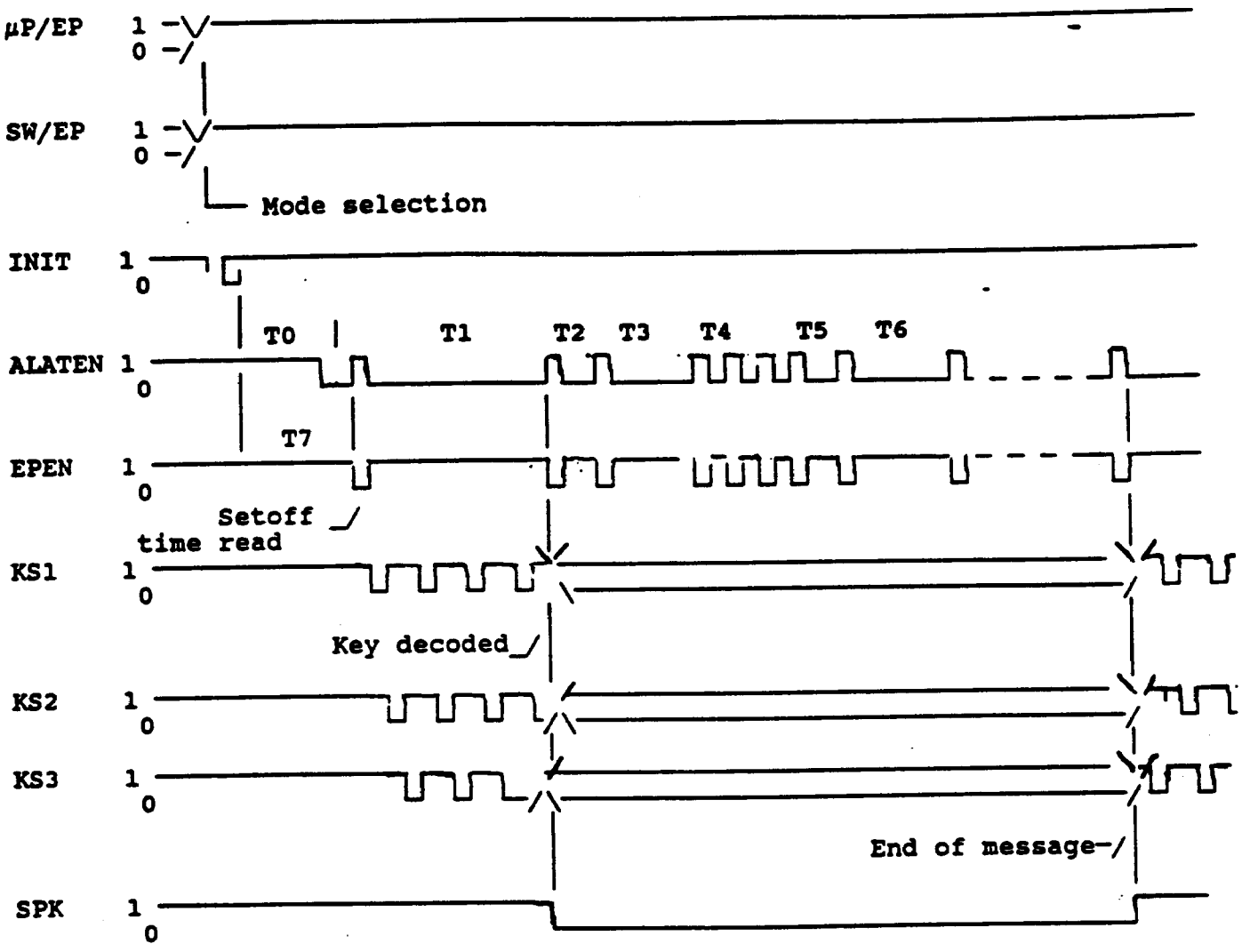


Figure 11 Pulse interface: General Timing

*Note: T1 Would be < To setoff time

Means 1 or 0 (here according range key pressed)

T0 = 3.2 ms.

T1 = time between two keys selected.

T2 = 0.4 ms.

T3 = 2.4 ms

T4 = 0.2 ms

T5 = 0.6 ms

T6 = 2.7 ms

T7 = 3.8 ms

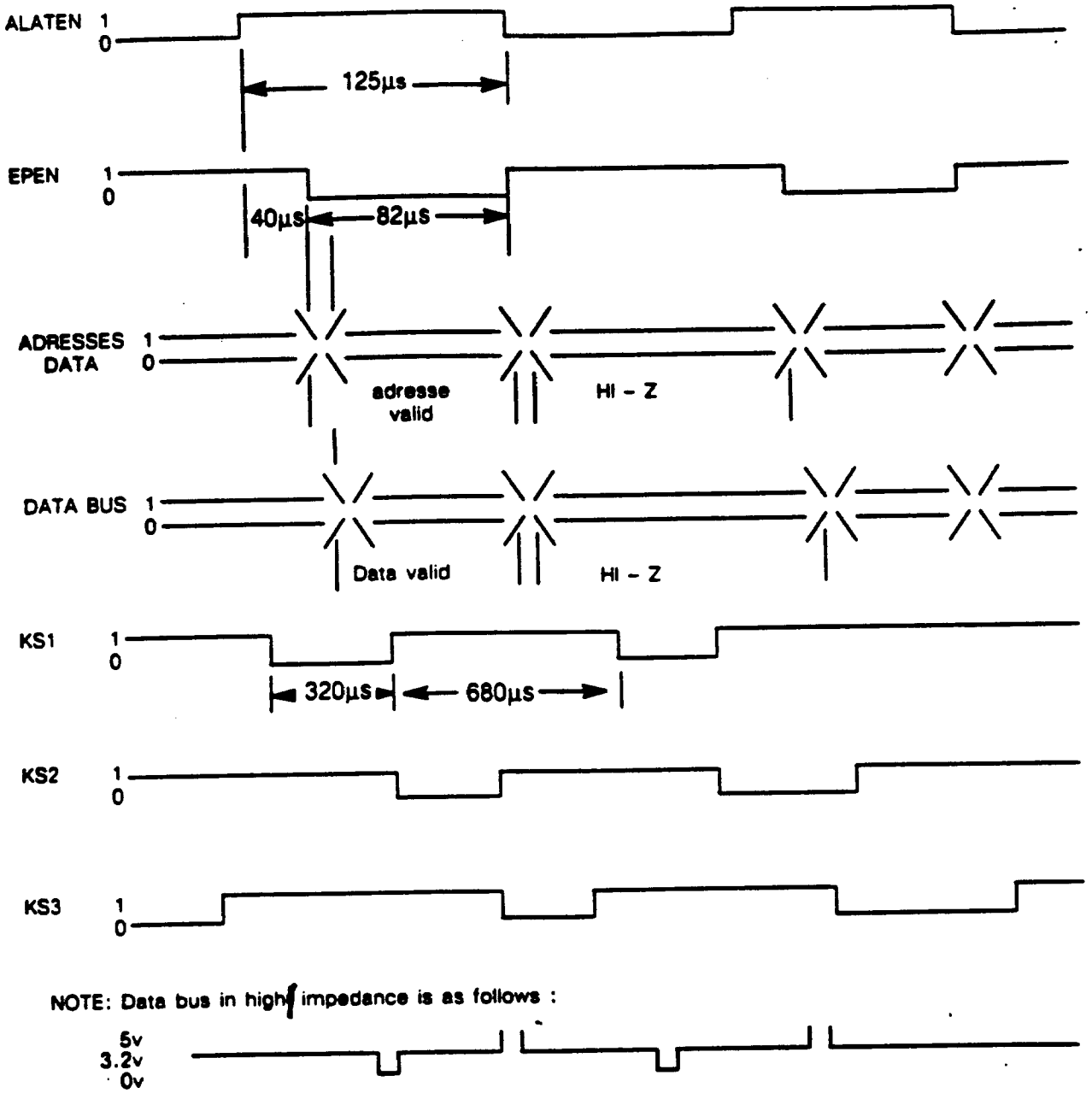


Figure 12 Pulse interface: detailled timing

5.3.6 EPROM MODE WITH KEYSCAN: ROM DESCRIPTION

The ROM content is:

1. Three information bytes.
2. The beginning address for each sentence
3. The sentence address table (i.e. the address of the beginning of each word of the sentence).
4. Speech data.

See the example of speech ROM paragraph 5.1.6

The first header byte is similar to the one explained section 5.1.6.2 However, the MSB indicates the number of pins of D used for the keyscan see 5.1.6.2
The second header byte indicates the setoff time in number of 250 ms
The third byte indicates the total number of pages in the EPROM. This value is called NBPAGE (number of pages).

5.3.6.1 DESCRIPTION OF KEYSCAN HEADER BYTE

The first byte of the ROM describes the coding table that is used as well as the number of pins of D used for keyscan. The MSB of the header byte is called bit 7 (HB1(7)) and the LSB is called bit 0 (HB1(0)). The header byte is decribed as follows:

BITS	VALUE	DESCRIPTION
HB1(0)		Coded/Uncoded
	1	data is coded
	0	data is uncoded
HB1(1)		Type of coding table
	1	5220 coding table
	0	enhanced coding table
HB1(2)		Increment mode
	0	Page number is incremented each time a key is pressed
	1	Page number is incremented each time last key is pressed Page number is decremented each time one before last key is pressed
HB1(5-7)		Number of pins from D used for the keyscan minus one. HB1(5) is the LSB. The number may vary from 0 to 7. By adding one to this value, the number of pins used by by the keysboard is obtained. This last number is is referred to as NB3.

The description of the setoff time HB2 is described in paragraph 5.1.6.

CASE OF NON INCREMENT MODE: HB(2)=1

A page is a set of 3*NB3 sentences. For each page, there is a one to one correspondance between the key pressed and the sentence number which is synthesized. For example, pressing on key 4 will synthesize sentence 4 of the current page. If the current page is 5, the absolute sentence number is 5*(3*NB3)+4-1. The last substraction is necessary since the first sentence is sentence number 0.

If increment mode is not selected, (i.e. HB1(2)=1), then each time one presses on last key (3*NB3-1 i.e. 23 in case of 3*8 keyscan, 20 in case of 3*7 keyscan ..) the corresponding sentence is synthesized and then the page number is incremented.

Each time one presses on the one before last key (3*NB3 -2, i.e. 22 in case of 3*8 keyscan, 19 in case of 3*7 keyscan ...) the corresponding sentence is synthesized and the page number is decremented.

If the page number is greater than the total number of pages NBPAGE, then the page number is set equal to 0.

If the page number is less than 0, then the page number is set equal to NBPAGE.

The maximum number of sentences in this option is 3*NB3*NBPAGE.

CASE OF INCREMENT MODE: HB(2)=0

In case the bit 2 of the first header byte HB1 is 0, then each time any key is pressed, the page number is incremented.

5.4 READ EPROM MODE: SERIAL INTERFACE

The serial mode allows one to enter the sentence number to be synthesized with one Receive line : RX
The line characteristics are :
- 1200 bits/second.
- 8 bits data.
- Even parity.

In order to have the same speed for the two different quartz frequencies (3.07 MHz and 3.84 MHz), an indication of the quartz frequency is required in the header byte.

The RX and TX signals must vary between 0 and 5V.

5.4.1 READ EPROM MODE WITH SERIAL INTERFACE: PORT CONFIGURATION

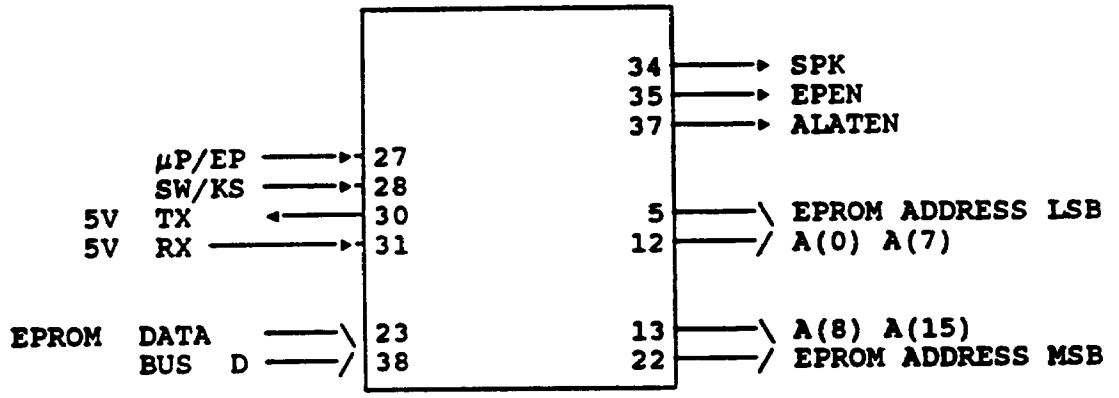


Figure 13 Serial interface: port configuration

5.4.2 EPROM MODE WITH SERIAL INTERFACE: CONTROLS AND SIGNALS

NAME	PIN	TYPE	VALUE	SIGNIFICATION
µP/EP	27	INPUT	0	MICROPROCESSOR MODE
			1*	READ EPROM MODE
SW/KS	28	INPUT	0*	PARALLEL OR PULSE INTERFACE REQUIRED
			1	KEYSCAN INTERFACE REQUIRED
TX	30	OUTPUT		SERIAL INTERFACE TRANSMIT LINE VOLTAGE 0 AND 5 VOLTS
RX	31	INPUT		SERIAL INTERFACE RECEIVE LINE VOLTAGE 0 AND 5 VOLTS
EPEN	35	OUTPUT		A1 TO 0 TRANSITION SELECTS THE EPROM
ALATEN	37	OUTPUT		ADDRESS LATCH ENABLE ZERO TO ONE TRANSMISSION INFORMS THAT TMS50C20 IS ABOUT TO READ.
SERINT	37	INPUT		SERIAL MODE
			0*	INDICATES SERIAL MODE IS REQUIRED
			1	INDICATES ANY OTHER MODE REQUIRED

REMARK 1: A star (*) indicates that these values are required at initialization in order to configurate the TMS50C20 in READ EPROM mode with SERIAL interface.

REMARK 2: PORT C is both input and output. It is first input to read which configuration is chosen then goes output mode when a control signal is requiered. The two names for the same pin 37 indicate this dual type input/output.

REMARK 3: For TMS50C20, SETOFF, VALID, RDY, SPK, EPEN,as well as DATA PORT have internal pullup resistor. No external pullup are required for these pins.
For TMX50C20, µP/EP, SW/KS, and ALATEN also have a pullup.

5.4.3 READ EPROM MODE WITH SERIAL INTERFACE: SCHEMATICS

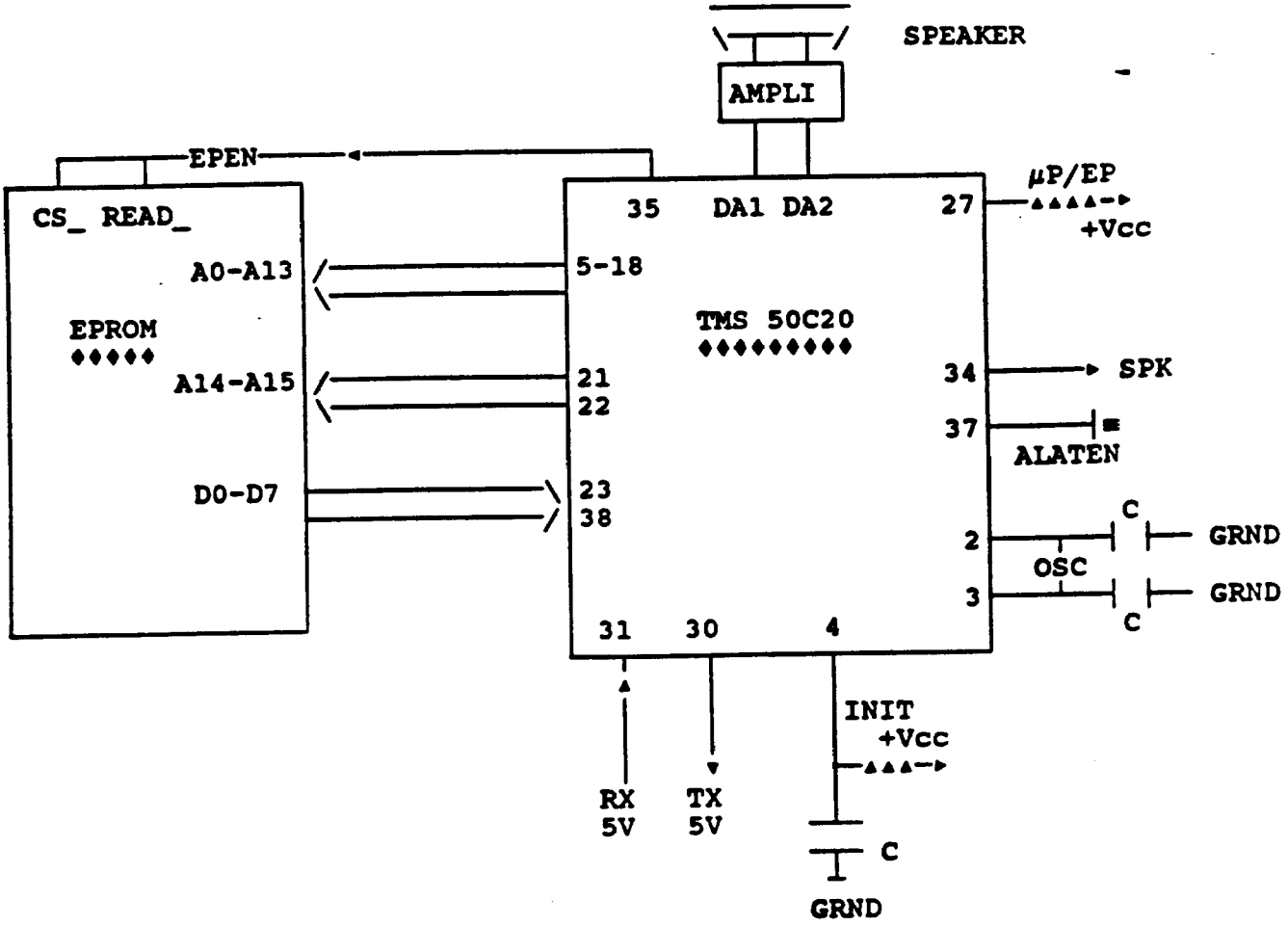


Figure 14 Serial interface: schematics

5.4.4 READ EPROM MODE WITH SERIAL INTERFACE: SEQUENCE OF EVENTS

The different steps done by the TMS50C20 are:

1. Read μP/EP and SW/KS to know which configuration to be in. If μP/EP=1 and SW/KS=0 and SERINT=0 Then:
2. Wait for byte received on RX line
3. When byte is received, the command is interpreted.
4. Acknowledge is sent. Typical handshake is decribed in 5.4.5
5. If command is a speak command then:
6. Read header byte on EPROM and decode it.
7. Verify if sentence number is correct. If it is not correct send the character >
8. Get speech data corresponding to the selected sentence.
9. When end of sentence detected, wait for another command. The host knows speech is over when its command is aknowledged.

5.4.5 EPROM MODE WITH SERIAL INTERFACE: HANDSHAKE

The different handshake used serial interface:

RX	SIGNAL RECEIVED
# (23)	SENTENCE NUMBER COMMAND: THE NEXT BYTE SENT WILL BE A SENTENCE NUMBER. THE ACKNOWLEDGE IS #.
XX	ANY BYTE INDICATING THE SENTENCE NUMBER THE ACKNOWLEDGE IS XX.
CR (0D)	SPEAK SENTENCE COMMAND: THE 50C20 MUST NOW SPEAK THE SENTENCE CORRESPONDING TO THE SENTENCE NUMBER. NO ACKNOWLEDGE.
ESC(1B)	SETOFF COMMAND: THE 50C20 MUST NOW GO IN SETOFF MODE I.E. LOW POWER CONSUMPTION. NO ACKNOWLEDGE.

TX	SIGNAL TRANSMITTED
# (23)	SENTENCE NUMBER AKNOWLEDGE: THE SENTENCE NUMBER COMMAND WAS CORRECTLY RECEIVED.
XX	ANY BYTE INDICATING THE SENTENCE NUMBER WHICH WAS RECEIVED
P (50)	PARITY ERROR ON RX LINE
? (3F)	COMMAND UNKNOWN
> (3E)	SENTENCE NUMBER GREATER THAN THE MAXIMUM NUMBER OF SENTENCES NMAX

SPEAK COMMAND (0D) AND SETOFF COMMAND (1B) DO NOT HAVE ACKNOWLEDGE

A typical sequence of command is:

```
RX : #  (23)    SENTENCE NUMBER COMMAND
TX : #  (23)    SENTENCE NUMBER AKNOWLEDGE
RX : SP (20)    SENTENCE NUMBER 20 IS TO BE SYNTHESIZED
TX : SP (20)    AKNOWLEDGE
RX : CR (0D)    SPEAK COMMAND
```

NOTE: The TX signal is not correct on the TMX50C20. It is available in TMS50C20 and TMP50C20. On TMX50C20, all bits are shifted on left and a parity error can happen on TX.

5.4.6 EPROM MODE WITH SERIAL INTERFACE: TIMING

SERIAL MODE

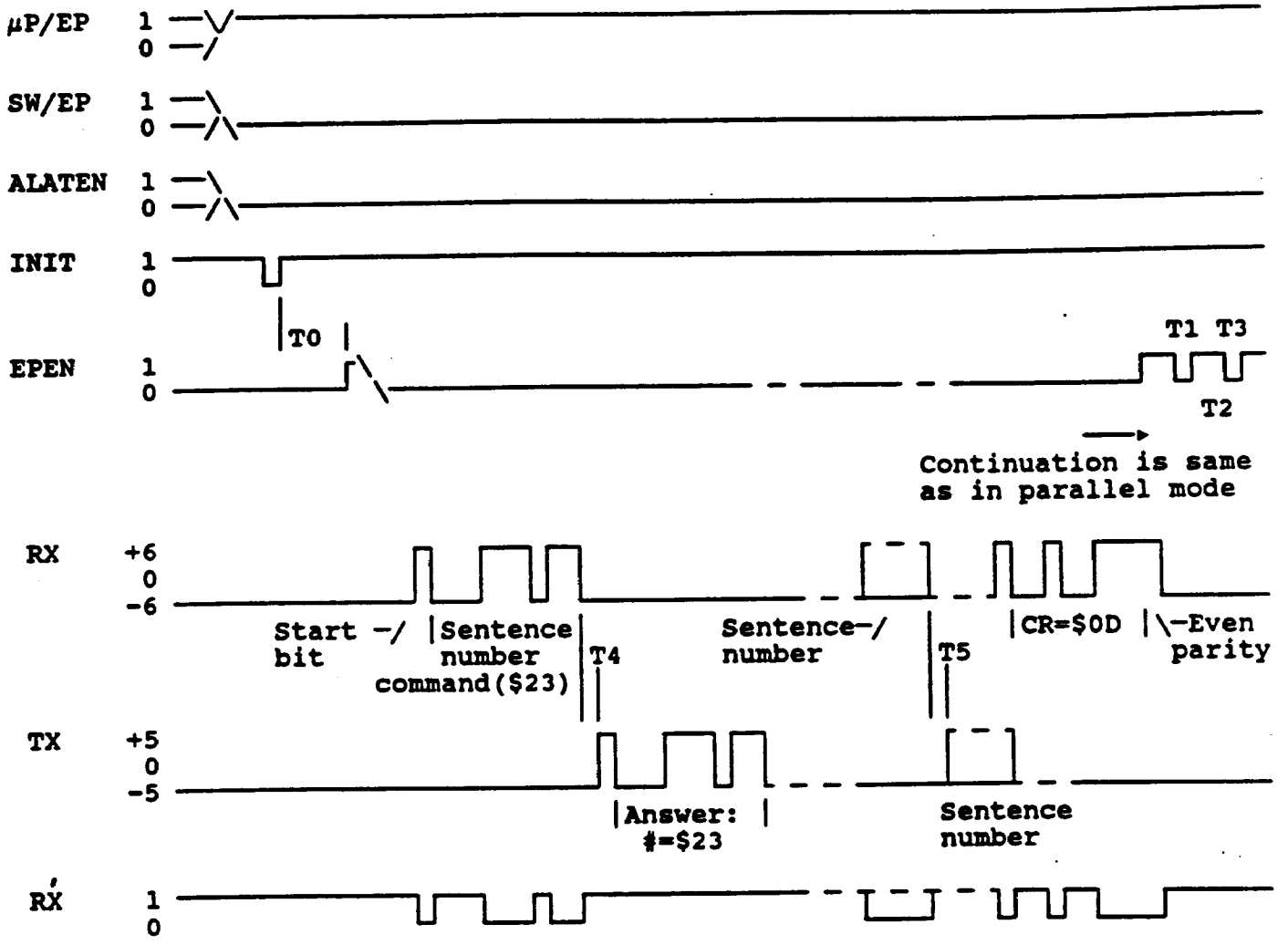


Figure 15 Serial interface: timing

T0 = 1.2 ms

T1 = 360 us

T2 = 85 us

T3 = 400 us

T4 = T5 = 0.6 ms

Note: Bit duration : 800 us
Line characteristics: 1200 bauds

5.4.7 EPROM MODE WITH SERIAL INTERFACE: ROM DESCRIPTION

The ROM content is:

1. Three information bytes.
2. The beginning address for each sentence
3. The sentence address table (i.e. the address of the beginning of each word of the sentence).
4. Speech data.

See section 5.1.6 for an example of ROM description.

5.4.8 DESCRIPTION OF HEADER BYTE

The first byte of the ROM describes the coding table that is used as well as the frequency of the ocillator:
- 3.84 MHz for 10 KHz speech
- 3.07 MHz for 8 KHz speech

The MSB of the header byte is called bit 7 (HB1(7)) and the LSB is called bit 0 (HB1(0)). The header byte description is as follows:

BITS	VALUE	DESCRIPTION
HB1(0)		Coded/Uncoded
	1	data is coded
	0	data is uncoded
HB1(1)		Type of coding table
	1	5220 coding table
	0	enhanced coding table
HB1(2)		Increment mode
	0	Increment mode for PULSE interface (see 5.2) and for KEYSCAN interface (5.3)
	1	Normal mode
HB1(3)		Clock frequency
	0	for 3.84 MHz
	1	for 3.07 MHz

The description of the setoff time (HB2) is described in paragraph 5.1.6.
The last byte HB3 indicates the number of sentences.
See paragraph 5.1.6.4

6.0 MICROPROCESSOR MODE

In this option, the TMS50C20 is able to synthesize speech data fed by a microprocessor. The data is given on the 8 line port 3 of the TMS50C20. This possibility is specially useful when one wants to have the microprocessor modify the speech parameters and have them synthesized.

Most of the options are available on port 1. The MICROPROCESSOR mode requires μP/EP=0.

The other options and sub-options (like type of coding table ..) are given by the microprocessor during initialization phase.

All input signals are available on Port C.

All output signals are available on Port A.

6.1 MICROPROCESSOR MODE: PORT CONFIGURATION

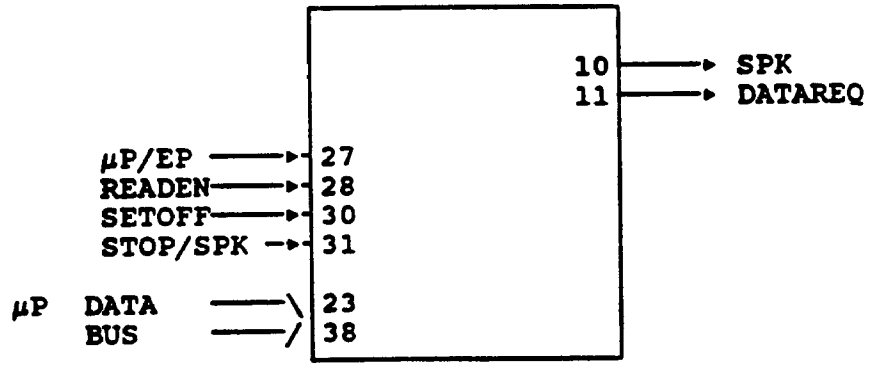


Figure 16 Microprocessor mode: port configuration

6.2 MICROPROCESSOR MODE: CONTROLS AND SIGNALS

NAME	PIN	TYPE	VALUE	SIGNIFICATION
µP/EP	27	INPUT	0*	MICROPROCESSOR MODE
			1	READ EPROM MODE
READEN	28	INPUT		A ONE TO 0 TRANSITION INDICATES DATA IS READY TO BE READ BY THE TMS50C20
SETOFF	30	INPUT	0	SETOFF COMMAND
			1	NORMAL MODE
STOPSPK	31	INPUT		A 0 TO 1 TRANSITION ENABLES SPEECH.
SPK	10	OUTPUT	0	TMS50C20 IS SPEAKING
			1	TMS 50C20 NOT SPEAKING
DATAREQ	11	OUTPUT	0	DATA REQUIRED
			1	NO DATA REQUIRED

REMARK 1: A star (*) indicates that these values are required at initialization in order to configurate the TMS50C20 in READ EPROM mode with Microprocessor interface.

REMARK 2: PORT C is both input and output. It is first input to read which configuration is chosen then goes output mode when a control signal is requiered. The two names for the same pin 37 indicate this dual type input/output.

REMARK 3: For TMS50C20, SETOFF, VALID, RDY, SPK, EPEN,as well as DATA POR have internal pullup resistor. No external pullup are required for these pins.
For TMX50C20, µP/EP, SW/KS, and ALATEN also have a pullup.

6.3 MICROPROCESSOR INTERFACE: SCHEMATICS

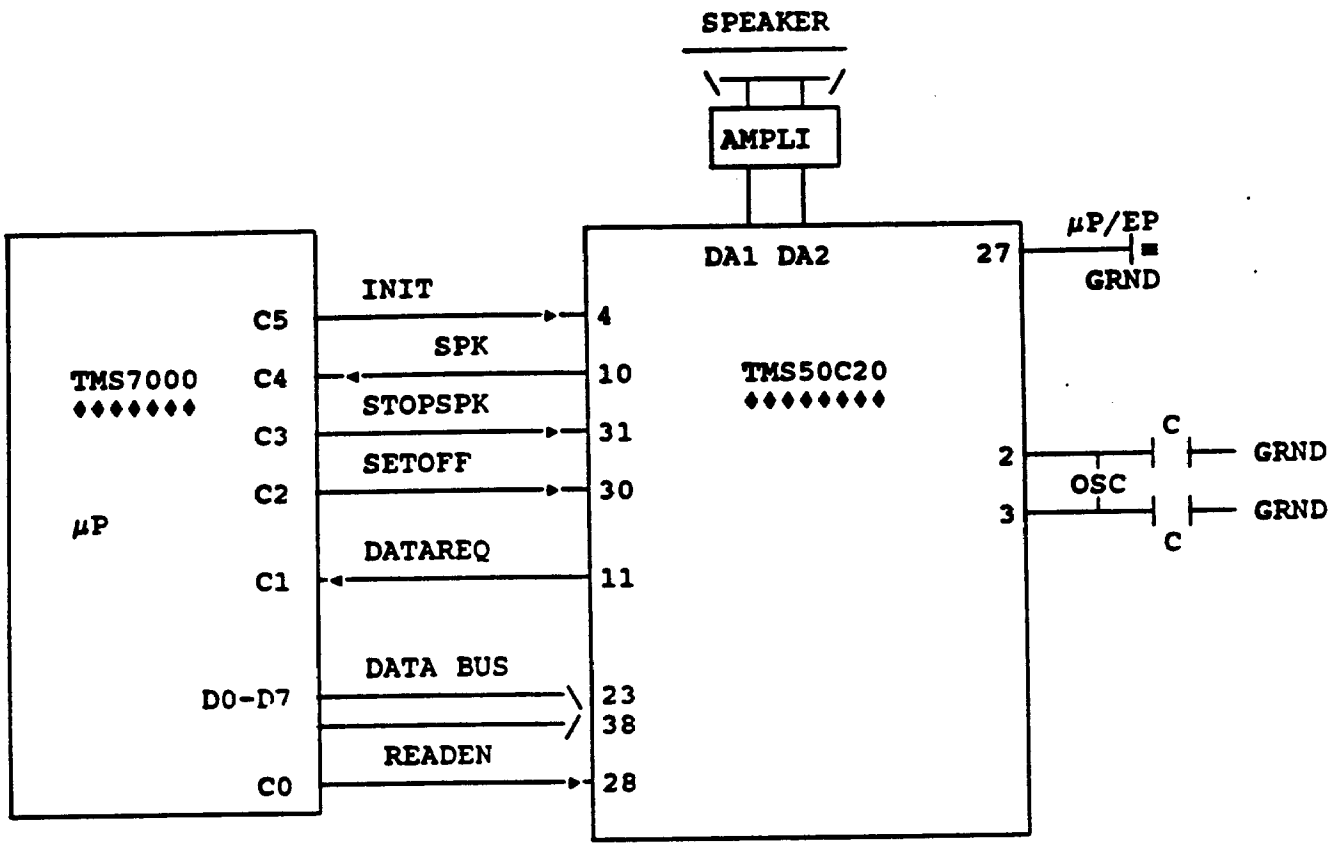


Figure 17 Microprocesseur mode: schematics

REMARK 1 The signals INIT, and SETOFF are not necessarily required for a proper interface between the microprocessor and the TMS50C20.

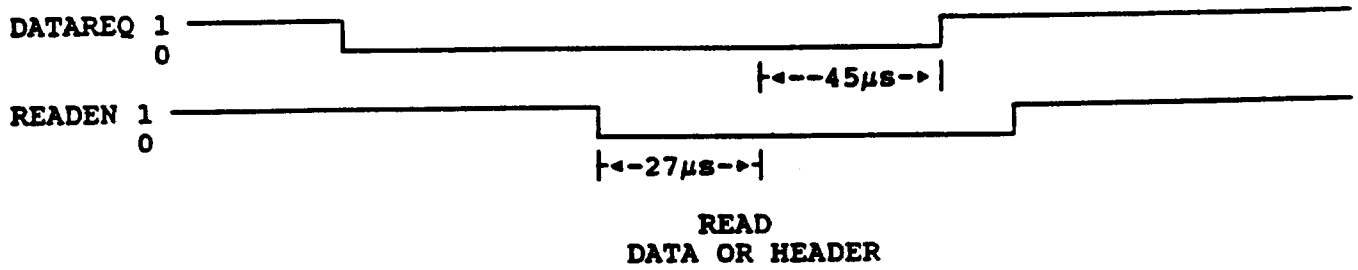
6.4 MICROPROCESSOR INTERFACE: SEQUENCE OF EVENTS

The different steps performed by the TMS50C20 are:

1. Read µP/EP to know which configuration to be in.
   If µP/EP=0 Then:
2. Send DATAREQ=1 and SPK=1
3. Wait for STOPSPK to go high and READEN to go high.
4. Set SPK to 0.
5. Send DATAREQ = 0 and wait for READEN go low.
6. Read Header byte on Port D
7. Send DATAREQ=1.
8. Requests data as required:
   Send DATAREQ = 0 and wait for READEN go low.
   Read Next speech byte on Port D
   Send DATAREQ=1.
9. When Speech is over go to step 2.

6.5 MICROPROCESSOR INTERFACE: TIMING

ONE READ CYCLE



TIMING FOR ONE SENTENCE

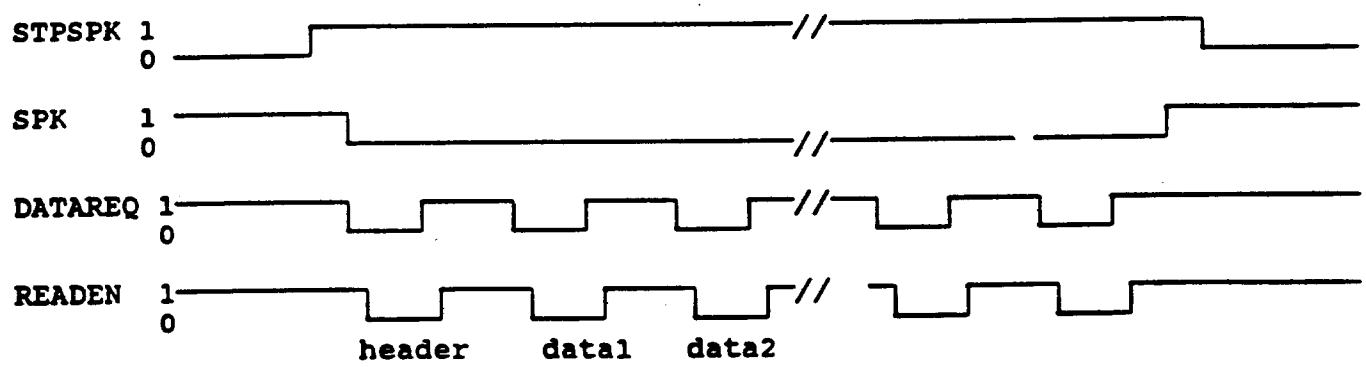


Figure 18 Microprocessor mode: timing

6.6 MICROPROCESSOR MODE: HEADER BYTE

The first byte to be fed to the synthesizer must be similar to the ROM header byte of the previous configurations: The MSB of the header byte is called bit 7 (HB1(7)) and the LSB is called bit 0 (HB1(0)). The header byte description is as follows:

BITS	VALUE	DESCRIPTION
HB1(0)		Coded/Uncoded
	1	data is coded
	0	data is uncoded
HB1(1)		Type of coding table
	1	5220 coding table
	0	enhanced coding table

7.0 LPC-10 SPEECH SYNTHESIZER

The LPC-10 speech synthesizer section contains a pulse generator as a speech excitation source and an LPC-10 flattice filter that models the human vocal tract.

The LPC lattice filter, shown in Figure 19. uses the compressed speech data provided by the processor to reconstruct speech. The initial input to the lattice filter is provided by an excitation source which is either periodic (for voiced sounds) or pseudorandom (for unvoiced sounds).

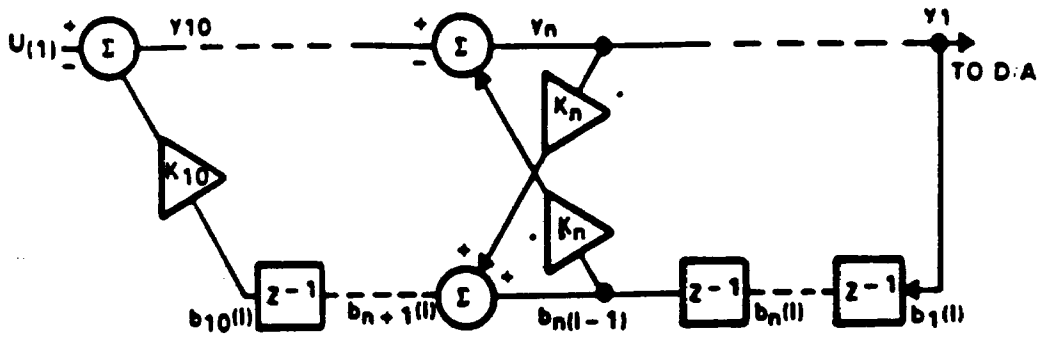


Figure 19 LPC Lattice Filter

7.1 DIGITAL-TO-ANALOG CONVERTER

The TMS50C20A contains an on-chip digital-to-analog converter. Input to the digital-to-analog is the output of the lattice filter (T-latch). The digital-to-analog coverter uses a modulated pulse-width implementation and has two pins compatible with a push-pull output drive to achieve a high power efficiency.

Figure 20. illustrates the digital-to-analog outputs resulting from a sampled digitized sine wave input. The digital-to-analog outputs are capable of driving a small 100-ohm speaker directly, or external components may be used if more power is required.

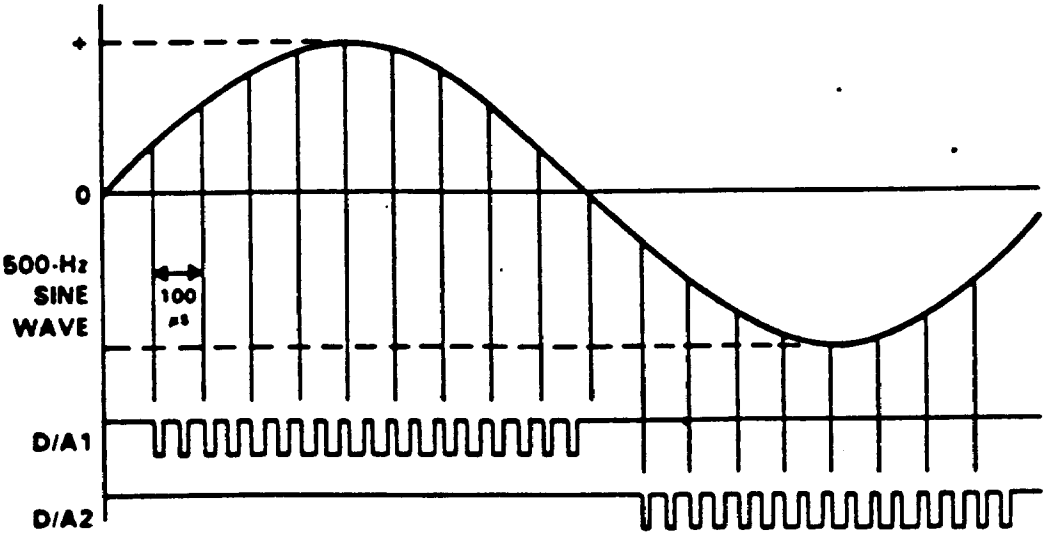


Figure 20 500-Hz Sine-Wave Output

7.2 AUDIO CIRCUITS

A key factor in the quality of a speech system is its audio circuit. This usually consists of a pulse-width interface and conversion circuit, a low pass filter, and an audio amplifier. The TMS50C20 has a pulse-width modulating D/A coverter that provides digital speech samples through two pins : D/A1 and D/A2. The normal state of both D/A output pins is high (while the active pulse is low). The output of these pins must be converted to an amplitude-modulated signal, passed through a low-pass filter with the proper cut-off frequency to eliminate the aliasing and finally be audio amplified.

Figure 21. shows the functional elements which should be included in an analog output circuit. Several circuit options are shown in the following figures. In the simplest circuits, such as Figure 22. and Figure 23. special care must be taken to select a loudspeaker that provides an effective cut-off frequency relative to the sampling rate (fc of 4KHz for 8KHz speech data and fc of 5KHz for 10KHz KHz speech data).

Figure 24. Figure 25. and Figure 26. provide other alternatives to filter and amplify the D/A output signal.

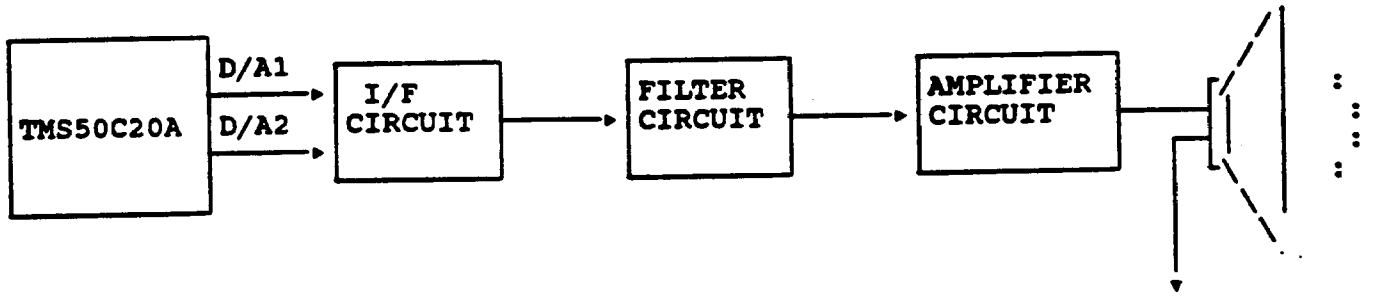
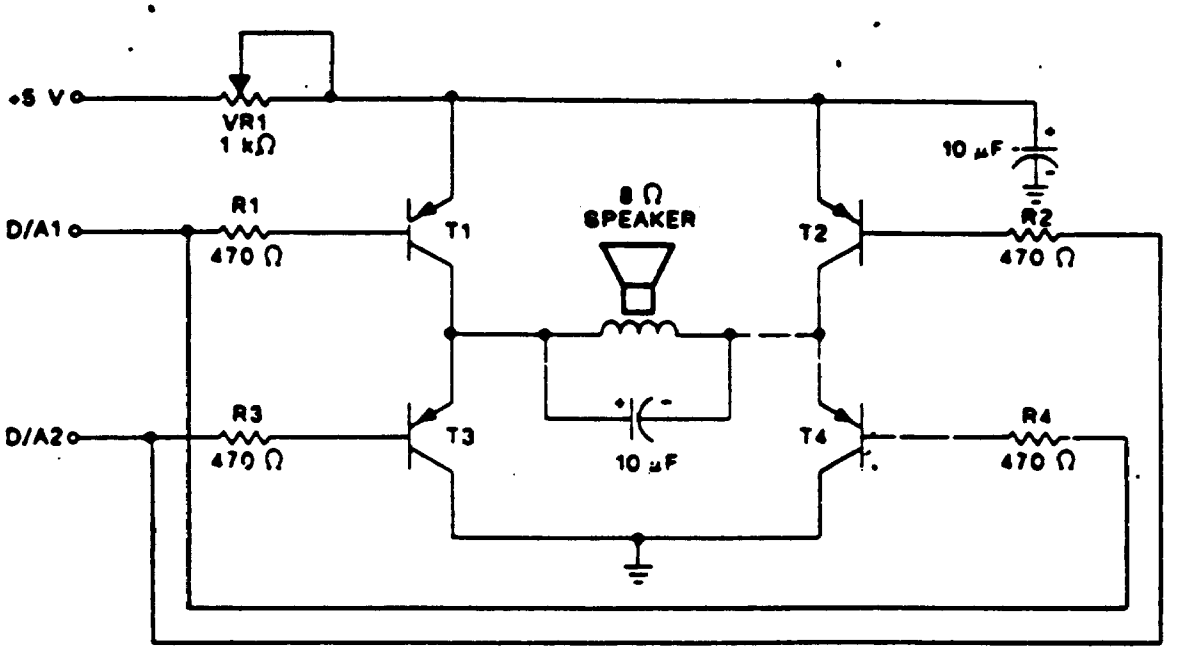
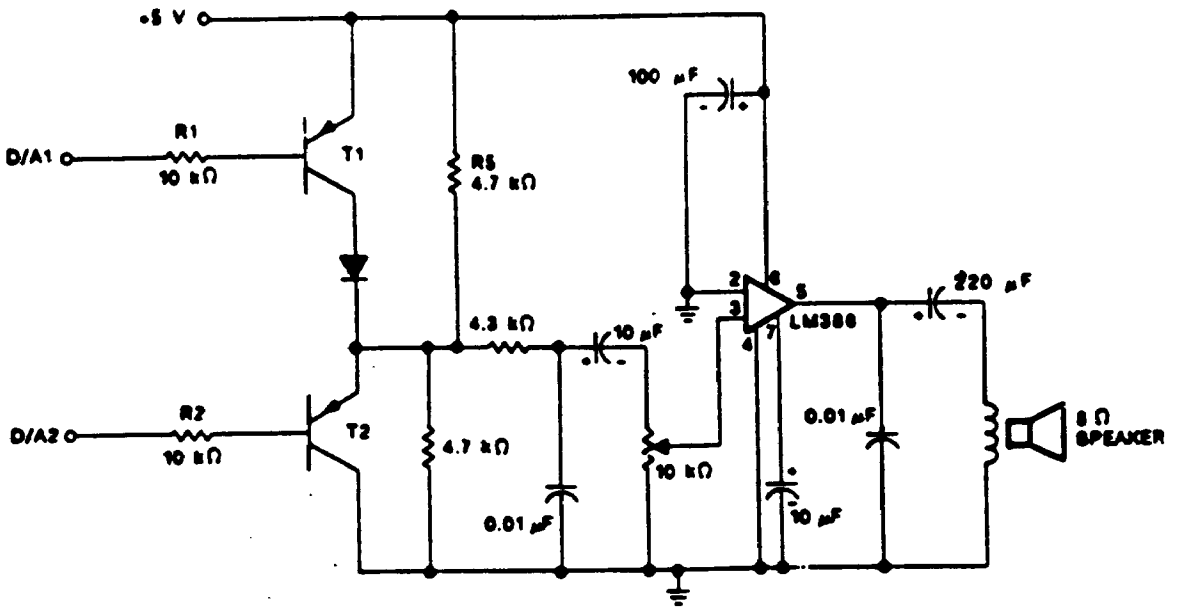


Figure 21 Analog block Diagram



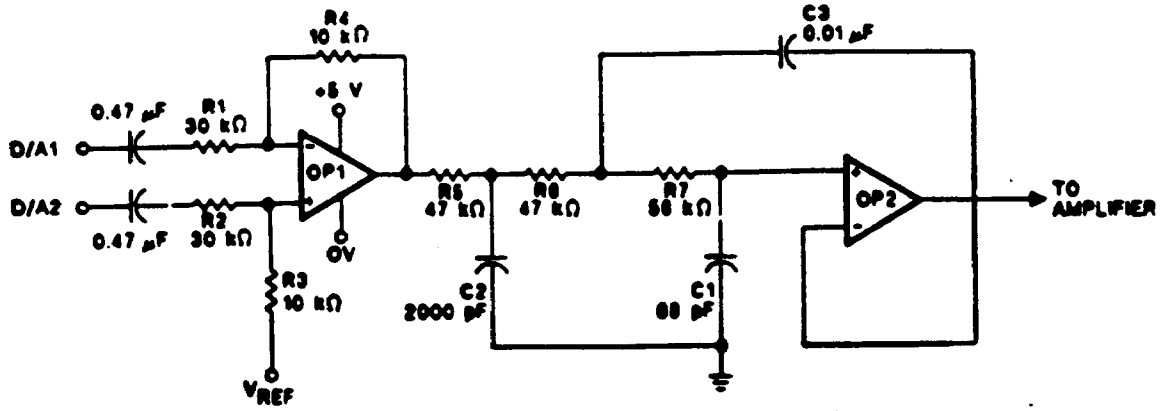
T1, T2,T3, T4 are 2905 transistors

Figure 22 Push-Pull Amplifier



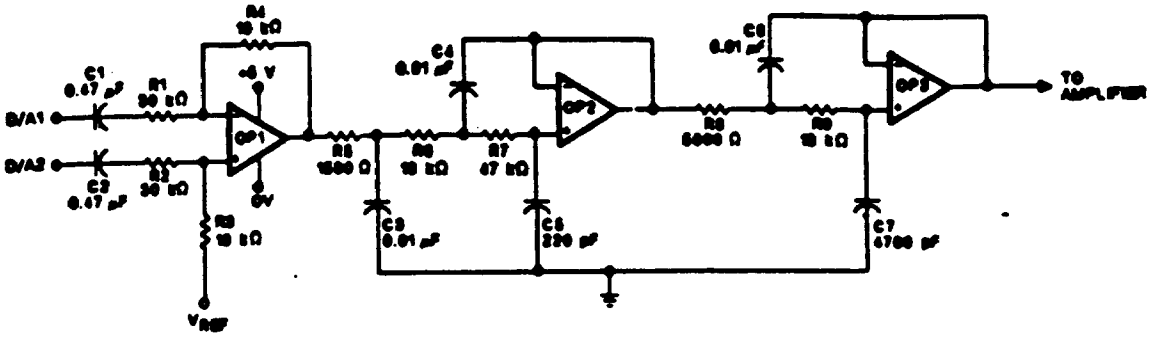
note : f = 2100 Hz

Figure 23 RC Filter and Differental Amplifier



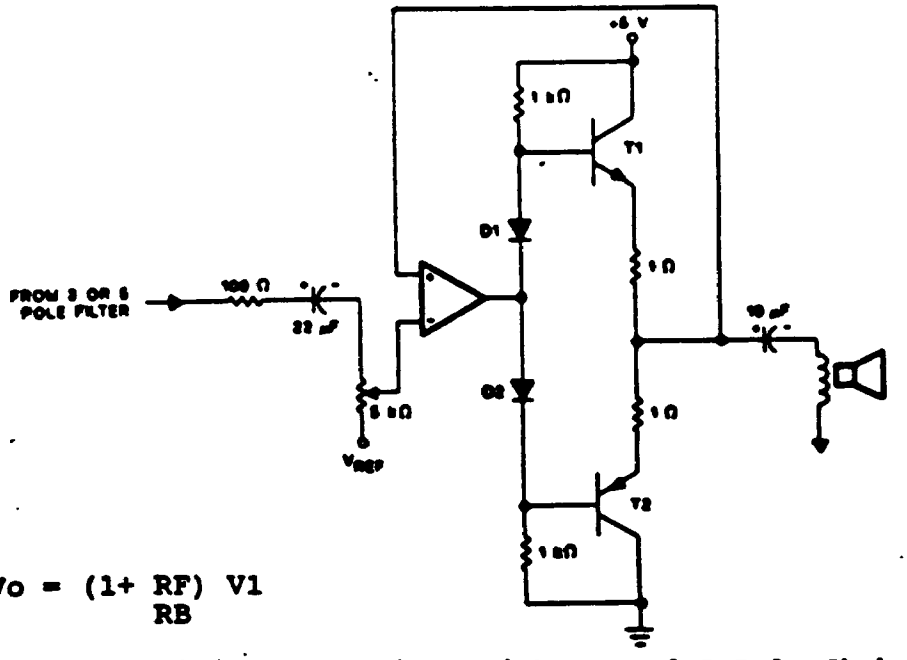
Notes : 1- OP1 and OP2 are TLC272CP
2- VREF = 2.5 V
3- fc = 3.8 KHz

Figure 24 3-Pole Chebychev Filter



Notes : 1- OP1, OP2, and PO3 are TLC272CP
2- 0.5 dB
3- fc = 3.8 KHz

Figure 25 5-Pole Chebychev Filter



Note : Vo = (1+ RF) V1
RB

Figure 26 Amplifier compatible with 3- and 5-Pole Chebychev Filters

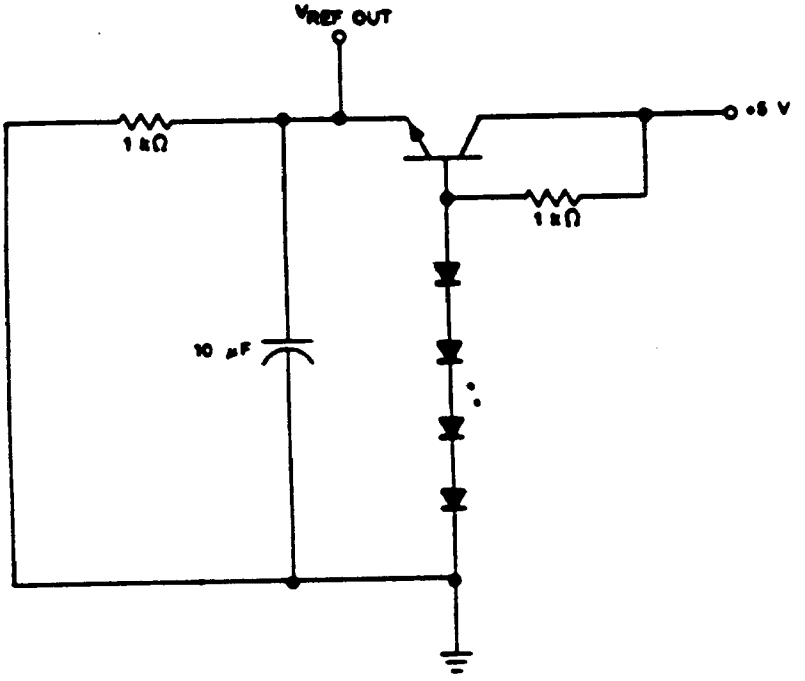


Figure 27 Reference voltage for 3- and 5-Pole Chebychev Filters

8.0 FUNCTIONAL DESCRIPTION

Linear Predictive Coding (LPC) synthesizes human speech by recovering enough data from the original speech to contruct a time-varying digital filter model of the vocal tract. This filter is excited with a digital representation of either glottal air impulses (voices sound) or the rush of air (unvoiced sounds). The output of this filter model is passed through a digital-to-analog converter to produce a synthetic speech waveform.

The LPC analysis program begins with a set of digitized speech samples. These digitized samples are usually derived with an analog-to-digital converter by sampling an analog waveform at 8 or 10 kHz. Consecutive samples are grouped together to form a "frame" of digitized samples. The LPC analysis operates on these digitized samples, a frame at a time, by pre-emphasizing the samples. Next, each parameter is coded according to a binary search on a preselected coding table.

The speech processor retrieves the speech data from the eprom (ROM or RAM). It then unpacks, decodes, and makes the data available as inputs to the LPC-10 lattice filter. Since the speech data has been coded and stored on a frame-by-frame basis, the processor interpolates (or smooths) the filter inputs for a smoother approximatiom of the human vocal tract. The frequency of interpolation may vary, but usually occurs in pitch synchronous way for voiced frames and every 12 samples for unvoiced frames. There is no interpolation between voiced and unvoiced frames as well between zero energy frames and any other frame. The output of the lattice filter network is the digitized speech signal which is sent to the digital-to-analog converter.

8.1 LPC LATTICE FILTER AND EXCITATION

The filter structure used in the TMS50C20 is a two-multiply-two-add lattice filter shown in Figure 2-2. A 10-section filter is used that performs two's complement arithmetic with 10-bit time-varying coefficients and 14-bit intermediate results. In each 100-microsecond sample period, the filter computes 22 values. The main components of the filter are the multiplier, the adder, the adder delay, the B stack (shift register memory), and the appropriate timing control.

In addition to lattice filter calculations, the multiplier and adder are used to calculate the next excitation address by operating on the pitch value and the current excitation address.

The value of pitch parameter, zero or non-zero, is used to determine the source of the filter excitation. The source is pseudorandom for unvoiced sounds (such as the sound's' as in speech) or pitch-controlled for voiced sounds (such as vowels or tones). The excitation waveform required for voiced sounds is stored in digital form in an excitation ROM. The period between adjacent waveforms is controlled by the pitch parameter.

The pitch parameter is divided into an 8-bit (implied positive sign) interger part and a 4-bit fractional part. The stored excitation sequence is 16 times oversampled to allow 1/16-sample resolution to the pitch period (6.25-μs resolution). This increased pitch period resolution is important for sound effects (music), as well as for female synthesized speech.

9.0 ELECTRICAL SPECIFICATION

9.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE AIR TEMPERATURE RANGE

Supply Voltage, VDD ..... -0.3 to 7 V
Input Voltage, VI ..... -0.3 to VDD + 0.3 V
Output Voltage, VO ..... -0.3 to VDD + 0.3 V
Storage Temperature Range ..... -30 to 125 oC

* All voltages are with respect to VSS

9.2 RECOMMENDED OPERATING CONDITIONS - DC

Parameter	Condition	Min	Typ	Max	Units
VDD *		4	5	6	V
TA	Operating free-air temperature	0		70	oC
VIH	VDD = 4V = 5V = 6V	3 3.8 4.5		4 5 6	V
VIL	VDD = 4V = 5V = 6V			1 1.2 1.5	V
VL	VDD = 5V RL = 50 Ω VDD = 5V RL = 100 Ω VDD = 4V RL = 50 Ω VDD = 4V RL = 100 Ω	1.9 2.9 1.3 2	2.8 3.6 2 2.7		V
OUTPUT POWER	VDD = 5V RL = 50 Ω VDD = 5V RL = 100 Ω VDD = 4V RL = 50 Ω VDD = 4V RL = 100 Ω	72 84 34 40	157 130 80 73		mW mW mW mW
PULLUP		10	20	30	KΩ

9.3 RECOMMENDED OPERATING CONDITIONS - AC

tr	VDD=5V, PA,B,D into 100 pF 10% to 90%	150	ns
tf	VDD=5V, PA,B,D Into 100 pF 10% to 90%	100	ns
fosc	Speech Sample Rate = 10 kHz Speech Sample Rate = 8 kHz	3.84 3.07	MHz

9.4 ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

Parameter	Condition	Min	Typ	Max	Units
ICC	VDD = 5V Standby mode = SETOFF executed or INIT high, no pullup resistor on INIT, All port pins are open.		10		µA
	VDD = 5V Operating mode = INIT low and SETOFF not excuted, DA pins are open.		1.5		mA
VOH	VDD = 5V IOH = 0.3 mA IOH = 1.2 mA	4.7 4	4.85 4.5		V
VOL	VDD = 5V IOL = 1.7 mA		0.3	0.4	V
II	input current			5.0	µA
IOH	VDD = 4V VOH = 3.5 V = 5V VOH = 4.5 V = 6V VOH = 5.5 V	0.3 0.6 0.8	0.8 1.2 1.5		mA mA ma
IOL	VDD = 4V VOL = 0.4 V = 5V " = 6V "	1.2 1.7 2	1.8 2.4 2.8		mA mA mA
ro	VDD = 5V DA1 And DA2 pins		50		Ω

Unless otherwise noted, all voltages are with respect to VSS.

9.5 OSCILLATOR

The oscillator pins OSC1 and OSC2 are provided for either a crystal or ceramic resonator connection in the typical phase shift oscillator connection. The recommended value for circuit components C1 and C2 are shown.

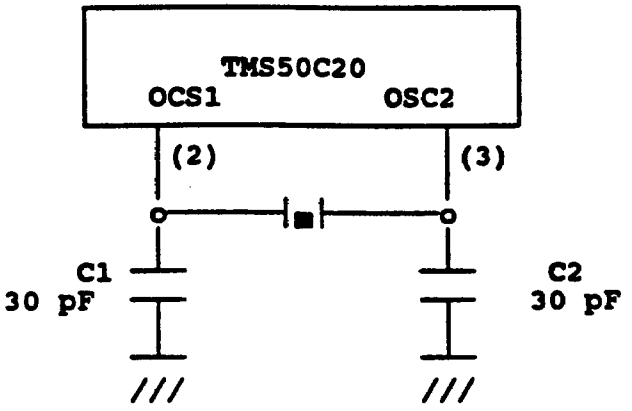


Figure 3.1 Typical Phase Shift Oscillator Connection

9.6 DIRECT SPEAKER DRIVE

The analog buffers at DA1 and DA2 are designed to directly drive a 50- to 100-Ω speaker with approximately 120 to 150 mW of peak power. Average power is considerably below this figure. The reduction in power is caused by the nature of speech.

The effective analog output impedance at 5V is typically 50 Ω for output currents less than 60 mA. For output currents more than 60 mA, the DAC buffers acts as currents sources. The outputs can also be used to drive transistors or operational amplifiers.

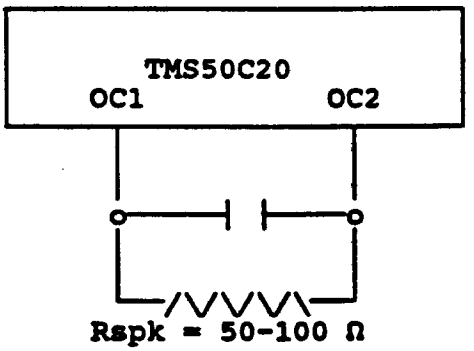
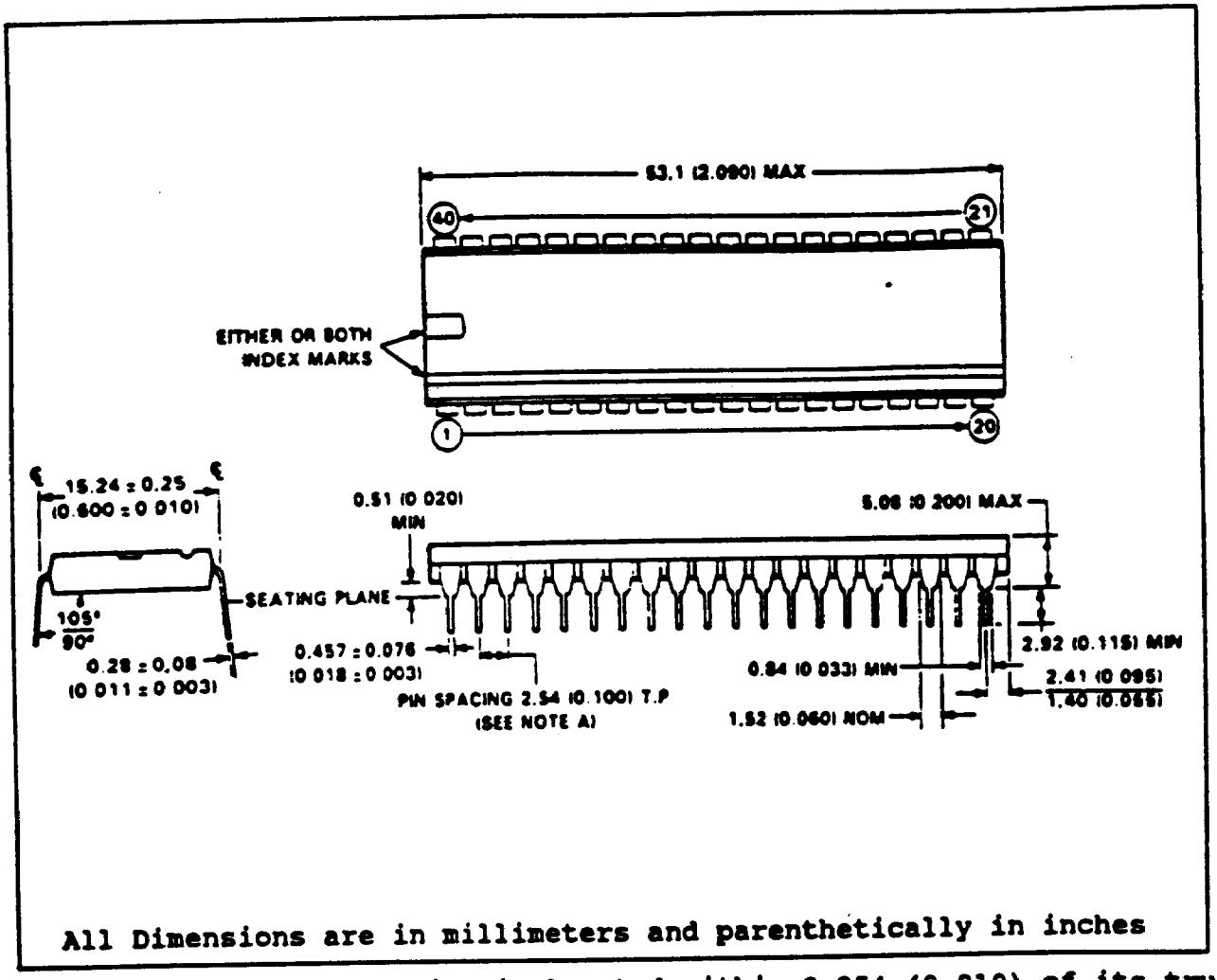


Figure 3.2 Typical Direct Speaker Drive Connection

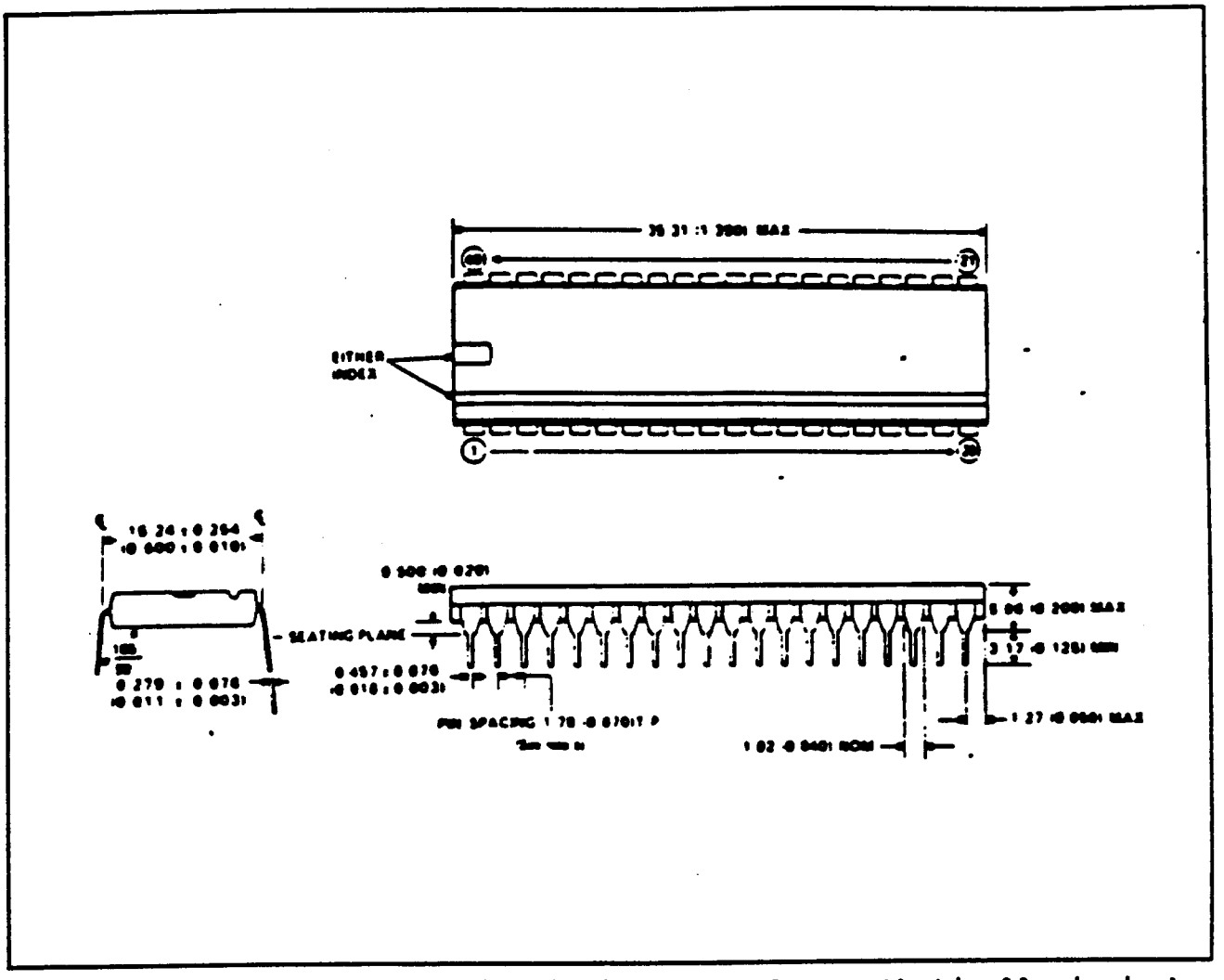
10.0 MECHANICAL DATA

40-pin plastic dual-in-line package



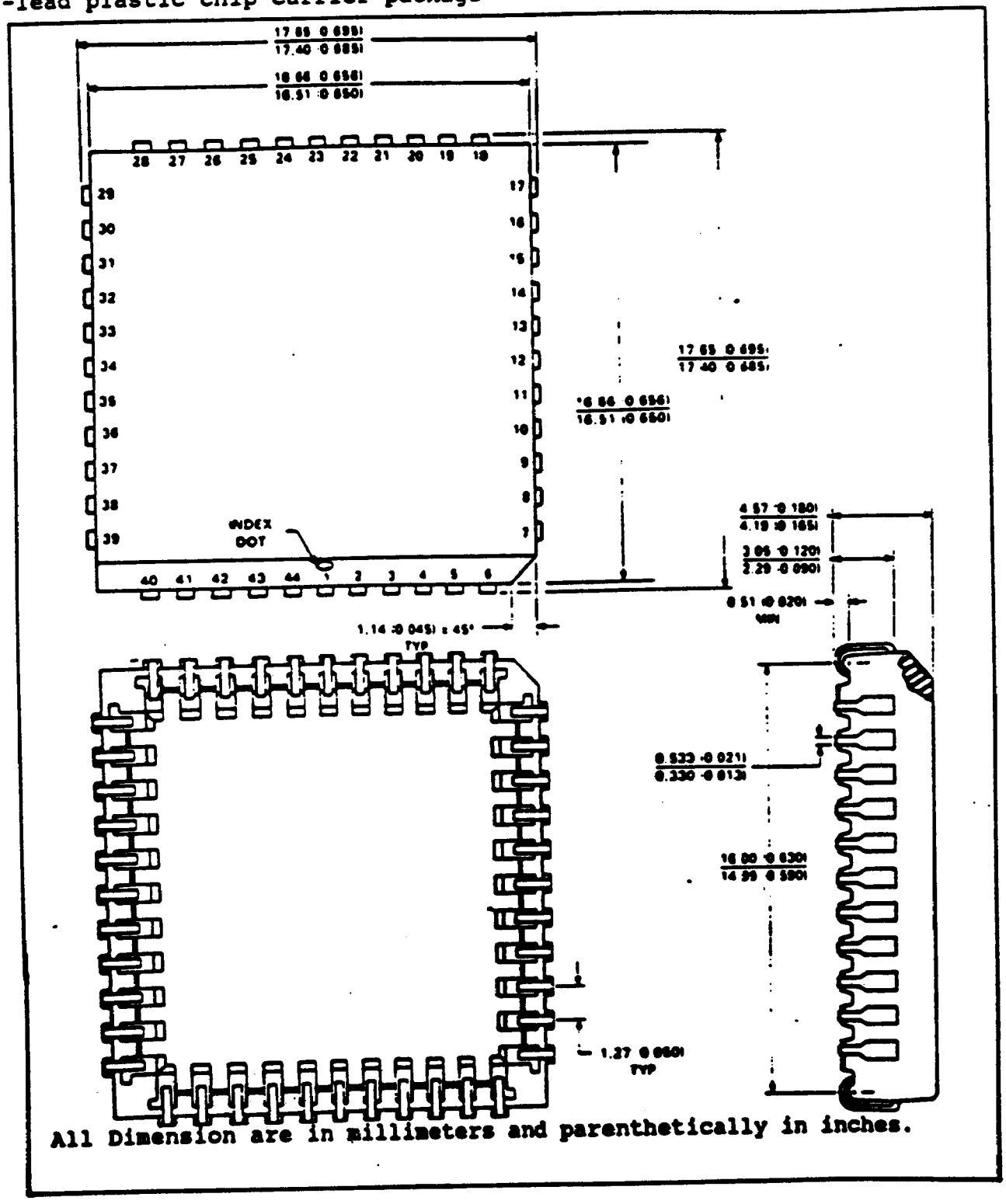
Note A: Each pin centerline is located within 0.254 (0.010) of its true longitudinal position.

40-pin plastic package (70 mil spacing)

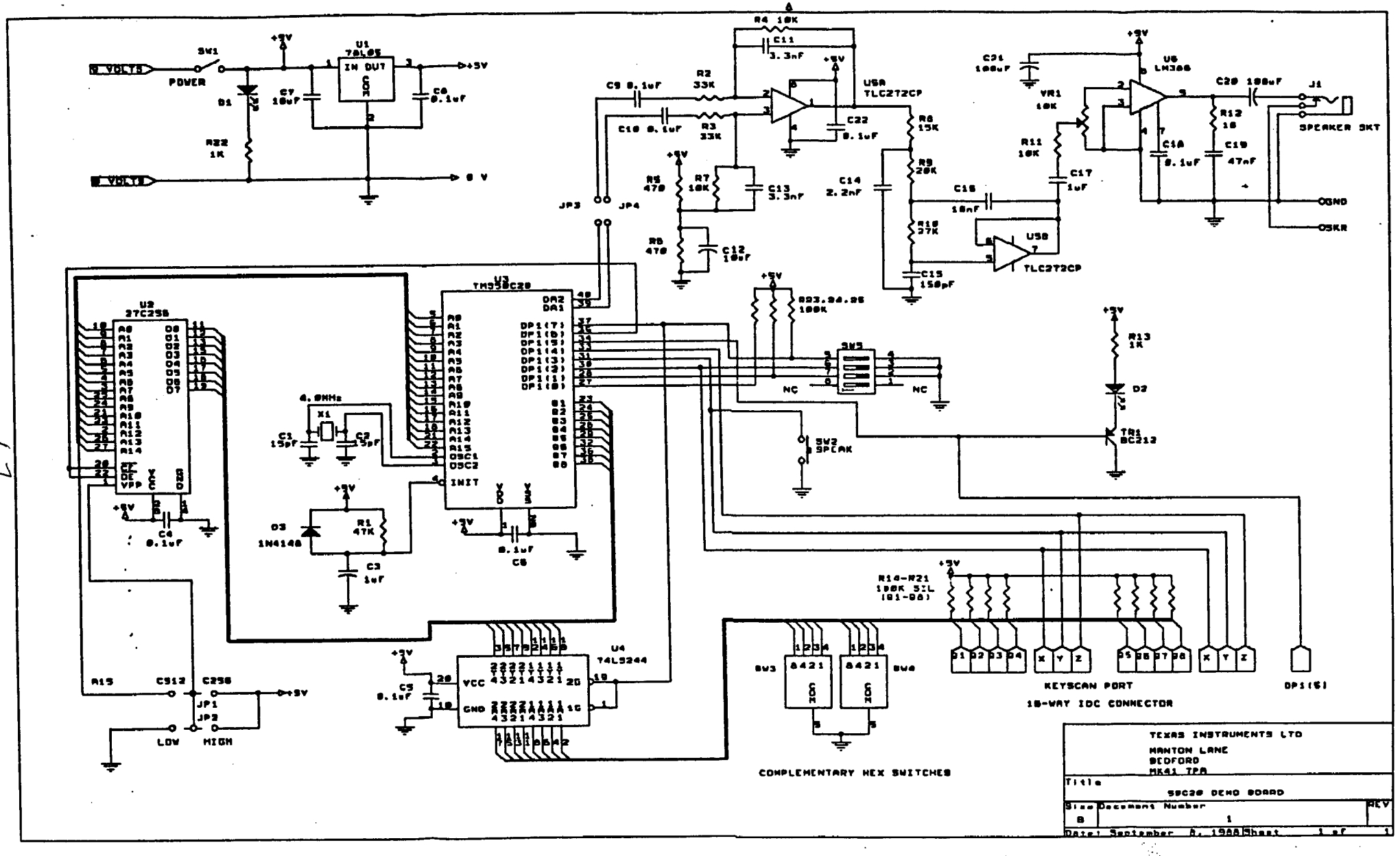


Note : All dimensions are in millimeters and parenthetically in inches.

44-lead plastic chip carrier package



All Dimension are in millimeters and parenthetically in inches.


9 VOLTS
SW1
POWER
D1
R22
1K
U1
78L05
IN OUT
COM
C7
10uF
C6
0.1uF
+5V
0 V
R4 10K
C11
3.3nF
C9 0.1uF
R2
33K
C10 0.1uF
R3
33K
U5A
TLC272CP
C22
0.1uF
R6
15K
R5
470
R7
10K
C13
3.3nF
R8
470
C12
10nF
JP3
JP4
C14
2.2nF
R9
20K
R10
27K
C15
150pF
C16
18nF
U5B
TLC272CP
C21
100uF
U6
LM386
VR1
10K
R11
10K
C17
1uF
C18
0.1uF
C20 100uF
R12
10
C19
47nF
J1
SPEAKER SKT
GND
SKR
U2
27C256
U3
TMS38C20
4.9MHz
X1
C1
15pF
C2
15pF
D3
1N4148
R1
47K
C3
1uF
C8
0.1uF
C4
0.1uF
R23,24,25
100K
SW3
NC
NC
SW2
SPEAK
R13
1K
D2
TR1
BC212
R16-R21
100K SIL
(B1-B8)
R15
C512
C256
JP1
JP2
LOW
HIGH
U4
74LS244
C5
0.1uF
VCC
GND
SW3
SW4
8421
COM
KEYSCAN PORT
18-WAY IDC CONNECTOR
DP1(8)
COMPLEMENTARY HEX SWITCHES
TEXAS INSTRUMENTS LTD
MANTON LANE
BEDFORD
MK41 7PA
Title
SBC20 DEMO BOARD
Size
B
Document Number
1
REV
Date: September 8, 1988
Sheet 1 of 1

ANNEXE A :

USING THS PC-SDS TO GENERATE SPEECH FOR THE 50C20 SPEECH SYNTHESIZER

1.0 The PC Speech Development Station

The PC-Speech development station allows to generate speech data for TMS50C20 on IBM-PC XT/AT.

The speech development station consists in two PC add-on boards and a software package permiting to produce speech data for the TMS5220 and the TMS50C4X speech synthesizer family TMS50C20. The PC SDS is an easy-to-use tool, but still powerful enough to permit any non speech expert to produce high quality LPC speech. The station allows for digital recording (directly into the PC) from an external source (microphone or line). It automatically computes and codes linear prediction parameters, but allows for their hand modification. Moreover the system is complete speech editor permitting word cutting, silence appending, speech insertion, deletion or displacement. Upon request it saves LPC data into disk files, constituting a speech library. A powerful ROM generation software supplied with the station creates complete data with the speech library previously recorded.

Three programs must be sequentially run on the PC-SDS in order to obtain EPROM ready speech data :

A)- Initialize the SDS with the appropriate analysis-synthesis parameters (run INITSDS),
B)- Record, analyse, edit and code speech data (run SDV),
C)- Transform speech data into EPROM ready format (run ROMSDS).

2.0 Initialization of the PC Speech Development Station for the 50C20

The PC-SDS does not contain a 50C20 speech synthesizer but since this chip is a masked version of the 50C42 its operation can then be emulated by loading an adapted software into the 50C4x, contained in the station. The 50C20 provides 2 possible speech coding schemes (one strictly compatible with the 5220 coding and an enhanced coding mode permiting to obtain a higher synthetic speech quality). It is hence in this sense that the setting of the initialization parameters must be done.

2.1 Initializing for the 5220 coding scheme

This working option on the 50C20 permits to use data developed for the 5220 and then having newly developed data remaining compatible. When working in this conditions, FOUR PARTICULAR PARAMETERS MUST BE CORRECTLY INITIALIZED IN THE STATION :

1)- Load in the synthesizer the 5220 decoding tables.
2)- Load into the SDS the 5220 scheme coding and decoding tables.
3)- Declare synthesis frame length equal to 200 points.

This operations are done by running the following commands on INITSDV

```
PROG=P5220.C42
TABLE=I5220.C42
FILTRE=FILTRE.C42
NFRAME=200
```

The first three commands can be resumed into one by using

```
CHIP=5220.c42
```

An example of initialization with this working conditions is found in file 50C20522.SET, which follows :

```
PC Speech Development System
 50C20 in 5220 like-scheme

; Select Chip
CHIP=5220.C42;        Chip
; Select Acquisition Parameters
BFRSIG=450;       ms    Time Before Word
AFRSIG=300;       ms    Time After Word
ENDSIG=1200;     ms    Time for End of Phrase
; Select LPC Analysis Parameters
FREQ=8;          KHz   Sampling Frequency
NFRAME=200;             Number of Sample by Frame
LPCV=150;         %     LPC Analysis Period
NKIV=10;
NKIU=4;
KEXIV=3;         Voiced Frame Energy Coefficient
KEXIU=1;
KSIGO=1;
; Select Listing Option
LIST;                   Listing of Parameters
```

Notice that the rest of the parameters can be modified -within the standard limits- to adapt them to a particular application (i.e. 8 or 10 KHz sampling frequency, size of analysis window, weighting, etc...)

The command necessary for this case is:

INITSDV 50C20522.SET (See PC SDS User's Guide).

2.2 Initializing for the enhanced coding scheme

This coding scheme permits to obtain a better speech quality, since more bits are allowed for the encoding of the synthetic speech parameters. The annoyance of this coding is that it produces a higher bit-rate speech.

As in the preceeding case, when working in this conditions, FOUR PARTICULAR PARAMETERS MUST BE COORECTLY INITILIAZED IN THE STATION :

1)- Load in the synthesizer the enhanced decoding tables.
2)- Load into the SDS the enhanced coding and deciding tables.
3)- Declare synthesis frame length equalto 200 points.

This operations are done by running the following commands on INITSDV

```
PROG=P654P74.C42
TABLE=I654P74.C42
FILTRE=FILTRE.C42
NFRAME=200
```

The first three commands can be resumed into one by using

```
CHIP=654P74.C42
```

The following lines reproduce an example setup file fixing this working conditions (50C20P74.SET) :

```
                PC   Speech Development System
          Parameters For Analysis
               USE OF THE ENHANCED CODING TABLE I654P74.C42
                        FOR THE 50C20 CHIP
```

```
; Select Chip
CHIP=654P74.C42;        Chip
; Select Acquisition Parameters
BFRSIG=450;       ms    Time Before Word
AFRSIG=300;       ms    Time After Word
ENDSIG=1200;     ms     Time for End of Phrase
; Select LPC Analysis Parameters
FREQ=8;         KHz    Sampling Frequency
NFRAME=200;             Number of Samples per Frame
LPCV=150;         %     LPC Analysis Period
NKIV=10;
NKIU=4;
KEXIV=1.62;          Voiced Frame Energy Coefficient
KEXIU=0.64;
KSIGO=1;
; Select Listing Option
LIST;                   Listing of Parameters
```

Notice again that the rest of the parameters can be modified-within the standard limits- to adapt them to a particular application (i.e. 8 or 10 KHz sampling frequency, size of analysis window, weighting, etc..). See p. 66

INITDV 50C20P74

3.0 Recording

After Initializing the station, the recording is activated by SDV command, the coding is immediate and one can listen directly to the coded speech through a TMS50C42 (emulating exactly the TMS50C20). It is also possible to compress the speech data, to edit the words and to modify the codes. For further informations concerning the station , please verify to the SPEECH DEVELOPMENT STATION User's Guide.

4.0 Using romsds to transform synthetic data generated by the PC-SDS into a 50C20 ready-to-read format for an EPROM PROGRAMMER

ROMSDS can be used in order to format data for speech EPROM's for the 50C20. Data is separated into headers -defining the type of interface, the coding scheme, etc- phrase addresses, word addresses and speech data. Allmost all this information is filled by ROMSDS, which needs to be set up in a particular way :

Rom base address	: 0
Vocabulary data format	: 8 bits [7..0] normal
Address format	: 16 bits [15..8] [7..0] swapped
Terminate code format	: 16 bits [15..8] [7..0] swapped
Word/sentence number format	: 8 bits [7..0] normal
Number of sentences location	: 2
Sentence address array location	: 3
Sentence terminate code	: 65535 ($FFFF)
Word array location	: not selected
Number of words location	: not selected

The sentences location address as well as the vocabulary location must be defined by the user in function of the total number of phrases and of the mean number of words per phrase. For example these values can set to :

Sentences location	: 100 ($64)
Vocabulary location	: 500 ($1F4)

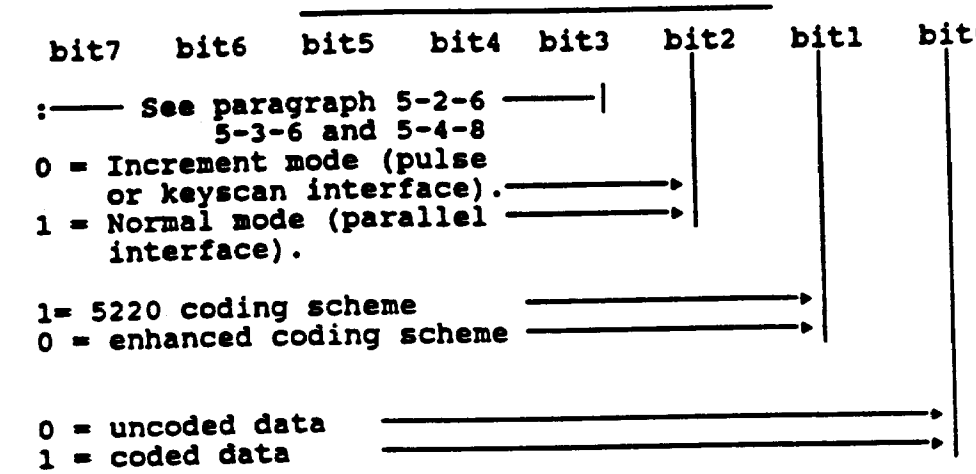
If ROMSDS stops with a message "ROM area overlay", this means that there is not enough space in the sentences array (move sentences locations higher up) or that the space reserved for the sentences is not enough (move vocabulary location higher up) or that that the global ROM size is to small (declare a larger ROM).

There are 2 bytes that are not yet directly programmable from ROMSDS:the header byte and the setoff time byte.These are the 2 first bytes (Bytes 0 and 1). These 2 locations must hence be filled directly by the EPROM burner editor :

The header byte

Byte 0 is the header byte. The 5 most significant bits (bits 7 to 3) are used the define the type interface used. Refer to your TMS50C20 manual for their set-up. The least significant bit (uncoded/coded data) should allways be set to 1. Bit 1 : defines the coding scheme : 1 =5220 coding table, 0=enhanced coding table. Bit 2 : relates to address increment mode : 0=Increment mode for pulse or keyscan interface, 1=normal mode, parallel interface :

Header byte configuration :



An example configuration for data coded using the 5220 scheme and a normal mode interface gives :
3 LSB on header byte : 00000111 (7) For the setting of the other bits in the header byte in your application refer to paragraphs 5.1.6, 5.2.6, 5.3.6 and 5.4.7 of this manual.

The setoff time byte

Byte 1 indicates the time elapsed between any new input and the instant the chip goes into setoff, expressed in quarter-second units (250 ms). The desired value must then be written into this byte by the user. (see paragraphs 5.1.6, 5.2.6, 5.3.6 and 5.4.7)

Number of sentences byte

The third byte in the EPROM contains the total number of sentences in the chip. This value is written by the ROMSDS software. However care should be taken when using a keyscan interface. In this case this byte should not contain the total number of phrases, but the total number of phrase divided by the number of phrases in the keyscan keyboard page. For example, if there are 36 phrases and the keyboard is 3*4 (page=12) byte 3 must contain value 3. If a keyscan page is not completely full, it is adviceable to completely fill it up by declaring silent phrases (word=FF). (see paragraphs 5.1.6, 5.2.6, 5.3.6 and 5.4.7)

ANNEX B: DATA PACKING FOR 5220 CODING TABLES

The 12 synthesis parameters (pitch, energy, K1, K10) are stored in ROM or EPROM. Each parameter occupies between 3 and 6 bits. During synthesis, the coded values select a 10-bit or 8 bit actual parameter from the parameter lookup ROM stored in the lookup rom of the TMS50C20. Table 3 summarizes the 5220 coding table

IN ORDER TO PACK IN 5220 FORMAT LET US GIVE AN EXAMPLE :

IF THE NUMBER OF BITS IS:

FR#	COD	LEN	NRG	R/N	PIT	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
	0	4	1	7	6	6	5	5	4	4	4	3	3	3	

AND THE CODES ARE

FR#	COD	LEN	NRG	R/N	PIT	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
1	0		8	0	86	40	28	21	16	10	4	1	2	3	6

IN BINARY

1000 0 1010110 101000 011100 10101 10000

IN HEXA

8 | 5 | 6 | A | 1 | C | A | C |

IF BITS ARE INVERTED IN NIBBLE

1 A 6 5 8 3 5 3

IF NIBBLES ARE SWAPPED

A 1 5 6 3 8 3 5

WHICH GIVES THE RESULT:

BA156B3835B94A0BBC50BABC5B5311BA54EBCA8DBECF0B847ABAFC5B3ADEB1BE5BBAD3F TMS

MORE GENERALLY THE FIVE FRAMES:

1	0	8	0	86	40	28	21	16	10	4	1	2	3	6
2	0	8	0	86	43	17	28	21	1	1	4	5	3	4
3	0	9	0	78	49	13	24	15	2	1	5	7	3	6
4	0	11	0	70	46	15	15	12	5	3	10	7	3	4
5	0	11	0	66	36	19	10	10	9	4	13	5	1	3

ARE CODED AS FOLLOWS:

00000PACKCODE90000F TMS
90000F PREVOIR CONTROLE PROCHAINEMENT TMS
BA156B3835B94A0BBC50BABC5B5311BA54EBCA8DBECF0B847ABAFC5B3ADEB1BE5BBAD3F TMS
B4289BAC54BCA96B4E7EB4692BB66ABADC6BB002BA8B4BC502B3057B170BBC0D2B5626F TMS
B004FBBB15B03FCBE3D0B0270B0F0EB177BB2072B1E2EB4B4BBD0D4B8B21BD425B2520F TMS

INVERSION TABLE

0	0
1	8
2	4
3	C
4	2
5	A
6	6
7	E
8	1
9	9
A	5
B	D
C	3
D	B
E	7
F	F