Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

T-51-09-12

SP9395

12-Bit Ultra High-Speed Voltage Output D/A Converter

FEATURES

- 200ns Setting Time
- Monotonicity Guaranteed Over Temperature
- 0.5 LSB Integral Linearity
- Low Glitch Energy
- Internal Voltage Reference

APPLICATIONS

- Direct Digital Synthesis
- High-Speed Waveform Generators
- ECM Systems
- Electronic Warfare System

DESCRIPTION

The **SP9395** is a very high speed, voltage output 12-bit DAC. It settles to 0.5 LSB in 200ns. integral linearity is ±0.5 LSB maximum, while monotonicity is guaranteed over the operating temperature range. The **SP9395** combines a proprietary hgih speed, dielectrically-isolated current switch, a specially-designed nichrome resistor network, and a buffered reference circuit.

The **SP9395** is packaged in a 24-pin ceramic DIP. It is offered in commercial and military temperature ranges. Please contact the factory for product screened to MIL-STD-883C.

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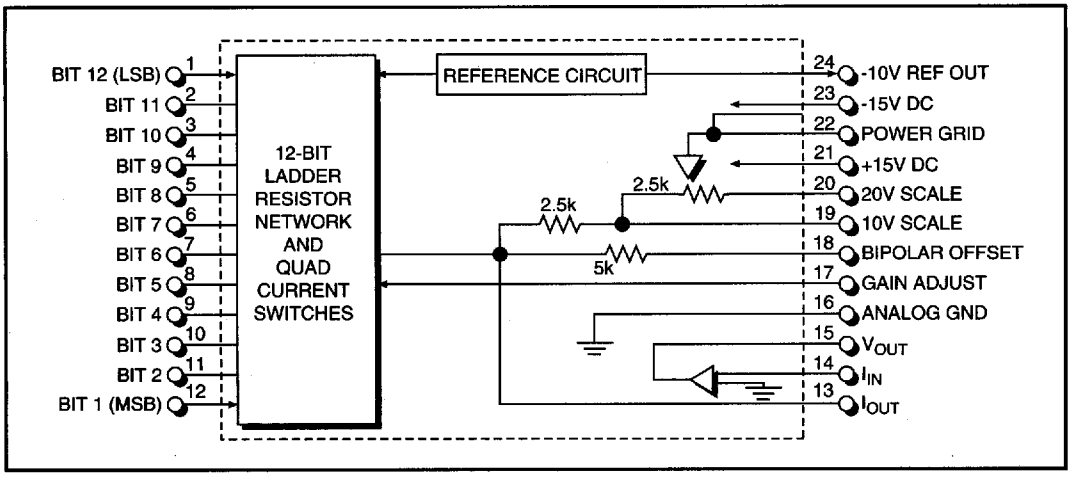

ABSOLUTE MAXIMUM RATINGS

(T_A=25°C unless otherwise noted)

+15V Supply ..... +18V
–15V Supply ..... –18V
Digital Input Voltage ..... 0 to +7V
Output Short Circuit Duration
Voltage Output ..... continuous
Reference Output ..... 2 seconds
Storage Temperature ..... –65°C to +150°C

CAUTION: ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

SPECIFICATIONS

T_A=25°C; V_S =±15V unless otherwise noted

	MIN.	TYP.	MAX.	UNIT	CONDITIONS
STATIC PERFORMANCE					
Integral Non-Linearity					
–C		±0.25	±0.5	LSB	T_A = 25°C
		±0.5		LSB	T_{MIN} to T_{MAX}
–B		±0.25	±0.5	LSB	T_A = 25°C
		±0.5		LSB	T_{MIN} to T_{MAX}
Differential Non-Linearity		±0.5	±1.0	LSB	
Guaranteed Monotonicity					
–C	0		+70	°C	
–B	–55		+125	°C	
Offset Error					Note 2
Unipolar (000...000)		±2	±4	LSB	
Bipolar (100...000)		±0.5	±2	LSB	
Gain Error		±0.1	±1.0	%	Note 2 and 3
AC PERFORMANCE CHARACTERISTICS					
Output Settling Time			200	ns	10V step to ±0.5 LSB
			250	ns	Full scale; T_{MIN} to T_{MAX}
Slew Rate		75		V/µs	
Small Scale Signal Settling		150		ns	1 LSB change
STABILITY					
Offset Drift					
Unipolar		±3	±15	ppm FSR/°C	
Bipolar		±10	±25	ppm FSR/°C	
Gain Drift		±10	±20	ppm/°C	
Reference Drift		±5	±15	ppm/°C	
Warm-Up Time		30		seconds	to ±1 LSB
Power Supply Rejection Ratio		±0.001	±0.0024	%/%	% FSR/%ΔV_S
REFERENCE INPUT					
Voltage		–10.00		V	
Accuracy		±1		%	
External Load			2	mA	
DIGITAL INPUTS					
Logic Levels					
Logic "1"	+2.0		+5.5	V	
Logic "0"	0		0.45	V	
Logic Loading			2	TTL Loads	Note 1
Coding					
Unipolar		Straight Binary			
Bipolar		Offset Binary			
ANALOG OUTPUT					
Voltage Range					
Unipolar		0V to –5V, 0V to –10V			
Bipolar		±2.5V, ±5.0V, ±10.0V			
Compliance Current	±5.0			mA	
Output Resistance		0.05		Ω	

SPECIFICATIONS

T_A=25°C; V_S =± 15V unless otherwise noted

	MIN.	TYP.	MAX.	UNIT	CONDITIONS
POWER REQUIREMENTS					
Supply Accuracy		±2.0		%	
Current Drain					
+15V Supply		40	46	mA	
−15V Supply		20	26	mA	
Power Dissipation		900	1,000	mW	
ENVIRONMENTAL					
Operating Temperature					
−C	0		+70	°C	
−B	−55		+125	°C	
Storage Temperature	-65		+150	°C	

Notes and Cautions:
1. 1 TTL load is defined as sinking 40µA with a logic "1" and sourcing 1.6mA with a logic "0" applied.
2. Gain and offset errors can be adjusted to zero using external trim potentiometers.
3. Gain error is defined as the error in the slope of the converter transfer fjuction. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full output voltage span from the 000...000 to the 111...111 output.

PIN ASSIGNMENTS

Pin	Function	Pin	Function
1	Bit 12 (LSB)	24	−10V Ref Out
2	Bit 11	23	−15V
3	Bit 10	22	Power GND
4	Bit 9	21	+15V
5	Bit 8	20	20V Scale
6	Bit 7	19	10V Scale
7	Bit 6	18	Bipolar Offset
8	Bit 5	17	Gain Adjust
9	Bit4	16	AGND
10	Bit 3	15	V_{OUT}
11	Bit 2	14	I_{IN}
12	Bit 1 (MSB)	13	I_{OUT}

INPUT CODING/OUTPUT VALUE

ANALOG OUTPUT	DIGITAL INPUT	
VOLTAGE	UNIPOLAR BINARY	BIPOLAR OFFSET BINARY
+FS	n/a	000...000
+1/2 FS	n/a	010...000
+1 LSB	n/a	011...111
0	000...000	100...000
−1 LSB	000...001	100...001
−1/2 LSB	100...000	110...000
−FS +1 LSB	111...111	111...111

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OUTPUT RANGE SELECTION

OUTPUT		PIN PROGRAMMING			
OUTPUT RANGE	OUTPUT PIN	JUMPER PIN 14 TO	JUMPER PIN 18 TO	JUMPER PIN 19 TO	JUMPER PIN 20 TO
0V to −5V	Pin 15	Pin 13	Pin 16 (GND)	Pin 15	Pin13
0V to −10V	Pin 15	Pin 13	Pin 16 (GND)	Pin 15	—
±2.5V	Pin 15	Pin 13	Pin 24	Pin 15	Pin 13
±5.0V	Pin 15	Pin 13	Pin 24	Pin 15	—
±10V	Pin 15	Pin 13	Pin 24	—	Pin 15

APPLICATIONS INFORMATION

Power Supplies and Grounds

High speed systems require extra care in power distribution to obtain optimum performnace. It is recommended that 1µF tantalum capacitors be added externally between each supply input and analog ground. The power gorund (pin 22), which is internally connected to the case, must be externally connected to system analog ground to minimize ground loop errors.

Logic Inputs

Logic inputs are standard TTL/DTL compatible. Unused bits, if any, should be grounded since an "open" bit input line represents a logic "1". However, opening the bit lines should not be used to generate a logic "1" due to the possibilities of noise pickup.

Dynamic Characteristics

To optimize settling time and to make the settling time independent of the digital driver characteristics, 2.2KΩ, 1/8 wall pull–up resistors are recommended on all logic inputs.

Optimal Trim Procedures

Offset and gain errors are trimmed at the factory to within the limits listed in the specifications. These initial errors may be trimmee to zero using external potentiometers as shown in *Figure 1*. Adjustments should be made after sufficient time for warm–up (five minutes) and, to avoid interaction, offset should be adjusted before gain. The fixed resistors should be located close to the connecting pins to reduce noise and the potentiometers should have a tempco of 100ppm/°C or less to minimize drift with temperature.

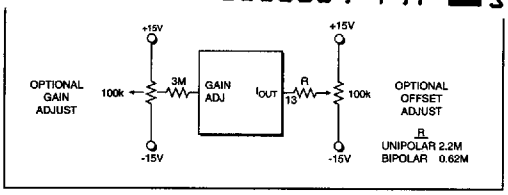


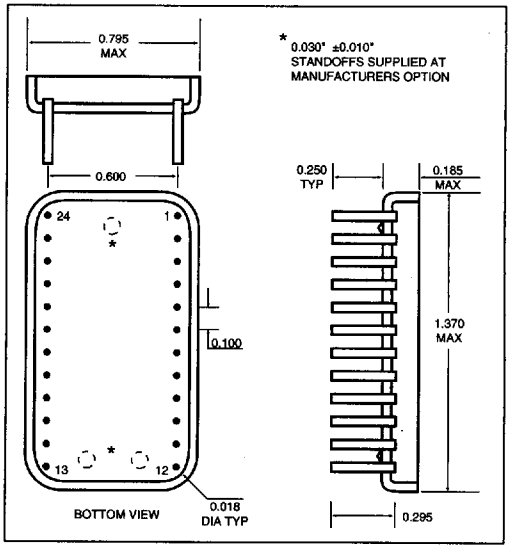
Figure 1. Offset and Gain Adjustment

Offset Adjustment

Set the digital input code to 000...000. Adjust the offset trim potentiometer for zero output voltage (unipolar) or minus full scale output voltage (bipolar).

Gain Adjustment

Set the digital input code to 111...111. Adjust the gain trim potentiometer for plus full scale minus 1LSB output voltage.



ORDERING INFORMATION	
SP9395C	0°C to +70°C
SP9395B	–55°C TO +125°C