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Preview

MATRA M H S

September 1990

DATA SHEET

HM 65688

16 k x 4
ULTIMATE CMOS SRAM

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FEATURES

- **ACCESS TIME**
  MILITARY/INDUSTRIAL : 45/55 ns (max)
  COMMERCIAL : 35/45 ns (max)
- **VERY LOW POWER CONSUMPTION**
  ACTIVE : 175.0 mW (typ)
  STANDBY : 2.0 µW (typ)
  DATA RETENTION : 0.8 µW (typ)
- **WIDE TEMPERATURE RANGE :**
  – 55 TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **SINGLE 5 VOLT SUPPLY**
- **EQUAL CYCLE AND ACCESS TIME**
- **GATED INPUTS : NO PULL-UP/DOWN RESISTORS ARE REQUIRED**

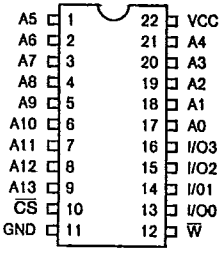
DESCRIPTION

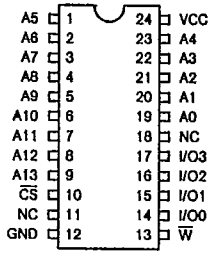
The HM 65688 is a very low power CMOS static RAM organised as 16384 x 4 bits. It is manufactured using the MHS high performance CMOS technology named super CMOS.
With this process, MHS is the first to bring the solution such as aerospace electronics, the portable instruments or PC's.
Utilising an array of six transistors (6T) memory cells, the HM 65688 combines an extremely low standby supply current (typical value = 0.1 µA) with a fast access time at 35 ns over the full temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.
Extra protection against heavy ions is given by the use of an epitaxial layer on a P substrate.
The HM-65688 is processed following the test methods of MIL STD 883C.

PACKAGES

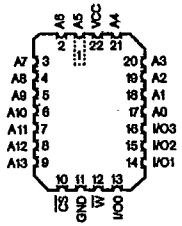
Plastic 300 mils, 22 pins, DIL
Ceramic 300 mils, 22 pins, DIL
SOIC & SOJ* 300 mils, 24 pins
LCC*, 22 pins

Pinout DIL 22/24 pins (top view)





Pinout LCC 22 pins (top view)



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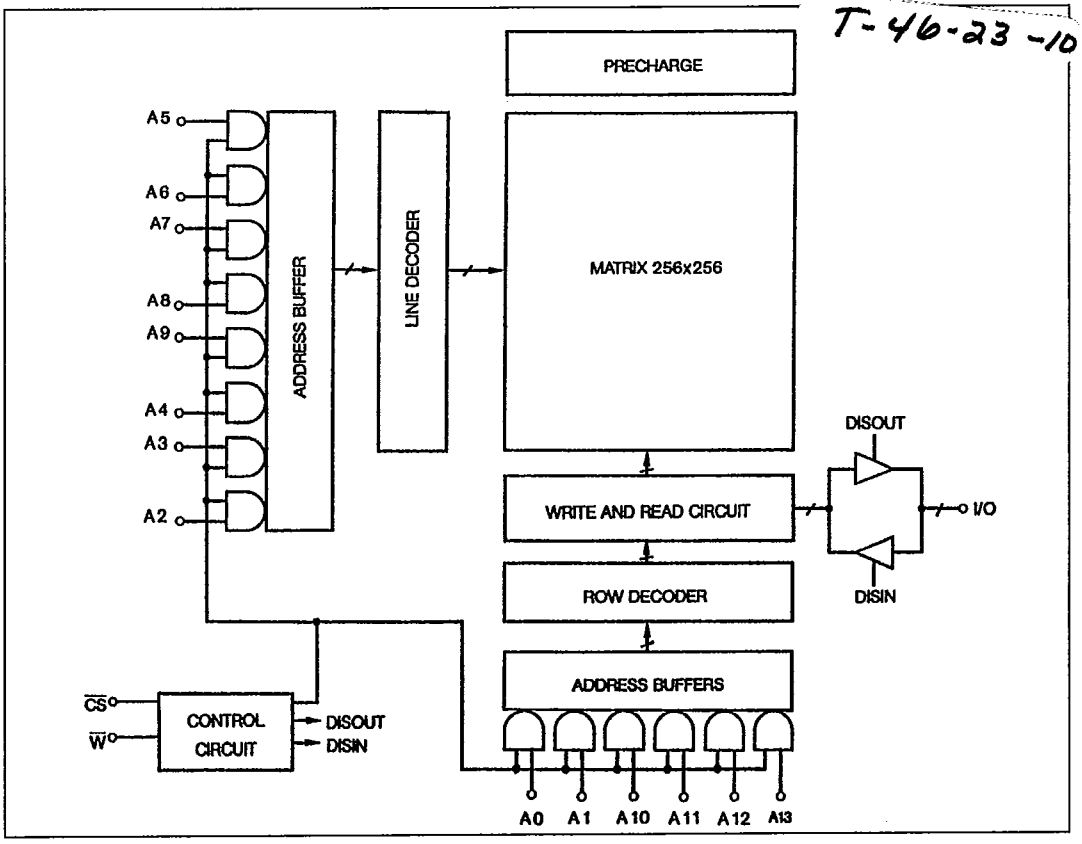
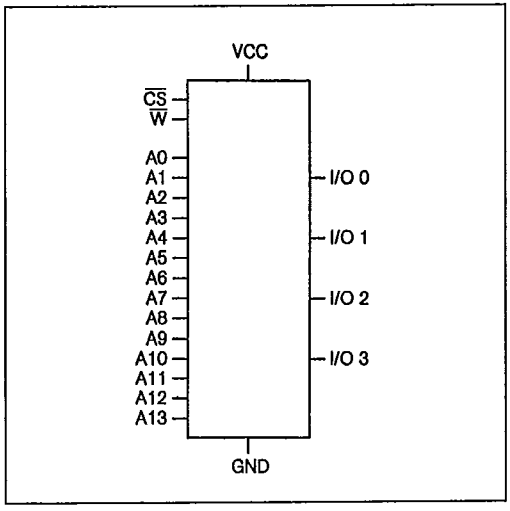
BLOCK DIAGRAM



LOGIC SYMBOL



PIN NAMES

A0-A13 : Address inputs	GND : Ground
I/O0-I/O3 : Inputs/Outputs	$\overline{CS}$: Chip-Select
Vcc : Power	$\overline{W}$: Write Enable

TRUTH TABLE

$\overline{CS}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	Z	Z	Deselect
L	H	Z	Valid	Read
L	L	Valid	Z	Write

L = low, H = high, X = H or L, Z = high impedance

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
Input or Output voltage applied : (Gnd – 0.3 V) to (Vcc + 0.3 V)
Storage temperature : – 65°C to + 150°C

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	Vcc ± 10 %	– 55°C to + 125°C
Industrial	(– 9)	Vcc ± 10 %	– 40°C to + 85°C
Commercial	(– 5)	Vcc ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL (1)	Input low voltage	– 0.3	0.0	0.8	V
VIH	Input high voltage	2.2	–	Vcc + 0.3V	V

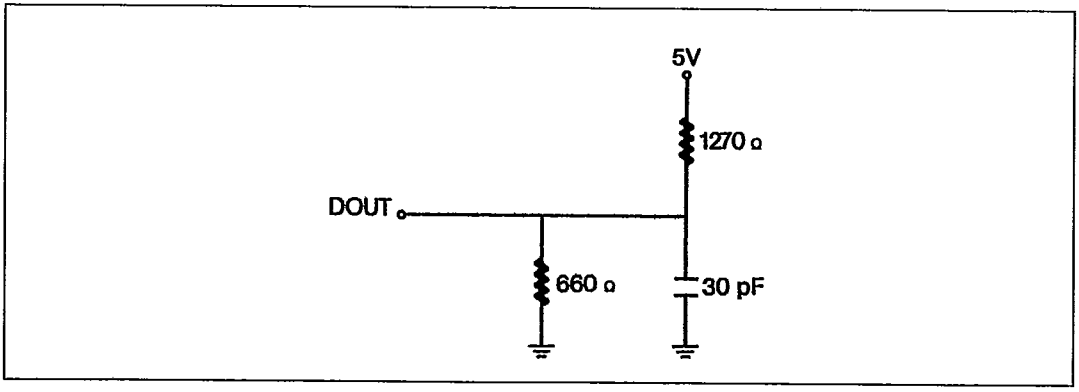
Note : 1. VIL min = – 0.3 V or – 1.0 V pulse width 50 ns.

CAPACITANCE

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin (2)	Input capacitance	–	–	5	pF
Cout (2)	Output capacitance	–	–	7	pF

Note : 2. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not 100 % tested.

OUTPUT LOAD



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ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(3)	Input leakage current	– 1.0	–	1.0	µA
IOZ	(3)	Output leakage current	– 1.0	–	1.0	µA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(4)	Output high voltage	2.4	–	–	V

Notes : 3. Gnd < Vin < Vcc, Gnd < Vout < Vcc output disabled.
4. Vcc min, IOL = 4.0 mA, IOH = – 1.0 mA.

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Consumption for Commercial specification (– 5) :

SYMBOL		PARAMETER	65688 B-5	65688 S-5	65688 -5	65688 C-5	UNIT	VALUE
ICCSB	(5)	Standby supply current	10	15	10	15	mA	max
ICCSB1	(6)	Standby supply current	1.0	75	1.0	75	µA	max
ICC	(7)	Operating supply current	10	15	10	15	mA	max
ICCOP	(8)	Operating supply current	65	75	65	75	mA	max

Consumption for Industrial specification (– 9) :

SYMBOL		PARAMETER	65688 B-9	65688 S-9	65688 -9	65688 C-9	UNIT	VALUE
ICCSB	(5)	Standby supply current	15	20	15	20	mA	max
ICCSB1	(6)	Standby supply current	5.0	100.0	5.0	100.0	µA	max
ICC	(7)	Operating supply current	15	20	15	20	mA	max
ICCOP	(8)	Operating supply current	75	100	75	100	mA	max

Consumption for Military specification (– 2) :

SYMBOL		PARAMETER	65688 B-2	65688 S-2	65688 -2	65688 C-2	UNIT	VALUE
ICCSB	(5)	Standby supply current	15	20	15	20	mA	max
ICCSB1	(6)	Standby supply current	50.0	500.0	50.0	500.0	µA	max
ICC	(7)	Operating supply current	15	20	15	20	mA	max
ICCOP	(8)	Operating supply current	75	100	75	100	mA	max

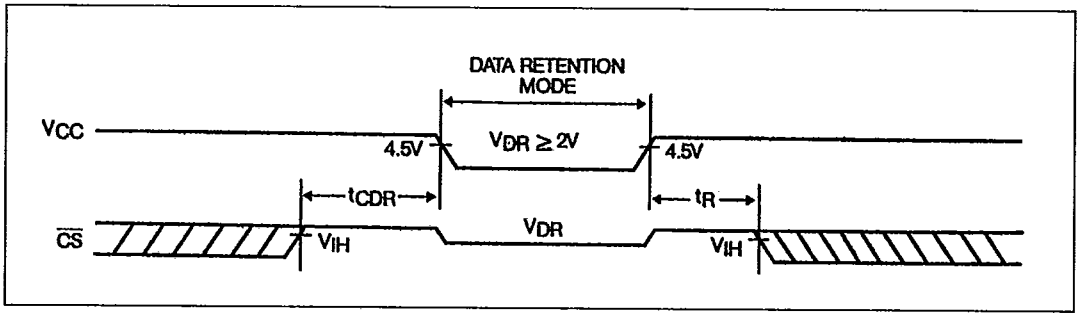
Notes : 5. $\overline{CS} \geq$ VIH.
6. $\overline{CS} \geq$ Vcc – 0.3 V, Iout = 0 mA.
7. $\overline{CS} \leq$ VIL, Iout = 0 mA, Vin = Gnd/Vcc.
8. Vcc max, Iout = 0 mA, f = max, Vin = Gnd/Vcc.

DATA RETENTION MODE

MHS CMOS RAM's are designed with battery backup applications in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ($\overline{CS}$) must be held high during data retention ; within Vcc to Vcc + 0.3V.
2. $\overline{CS}$ must be kept between Vcc + 0.3 V and 70 % of Vcc during the power up and power down transitions.
3. The RAM can begin operation > 35 ns after Vcc reaches the minimum operating voltage (4.5 V).

TIMING



DATA RETENTION CHARACTERISTICS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL (9)	MAXIMUM	UNIT
VCCDR	Vcc for data retention	2.0	–	–	V
TCDR	Chip deselect to data retention time	0.0	–	–	ns
TR	Operation recovery time	TAVAV (10)	–	–	ns
ICCDR1 (11)	Data retention current				
	@ 2.0 V : HM-65664(B)-5	–	0.1	0.5	µA
	HM-65664(B)-9	–	0.1	2.0	µA
	HM-65664(B)-2	–	0.1	20.0	µA
	HM-65664S/C-5	–	0.1	30.0	µA
	HM-65664S/C-9	–	0.1	30.0	µA
	HM-65664S/C-2	–	0.1	200.0	µA
ICCDR2 (11)	Data retention current				
	@ 3.0 V : HM-65664(B)-5	–	0.3	1.0	µA
	HM-65664(B)-9	–	0.3	3.0	µA
	HM-65664(B)-2	–	0.3	30.0	µA
	HM-65664S/C-5	–	0.3	50.0	µA
	HM-65664S/C-9	–	0.3	50.0	µA
	HM-65664S/C-2	–	0.3	300.0	µA

Notes : 9. TA = 25°C.
10. TAVAV = Read cycle time.
11. $\overline{CS}$ = Vcc, Vin = Gnd/Vcc, this parameter is only tested to Vcc = 2 V.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels : 1.5 V
Output load : 1 TTL gate + 30 pF

WRITE CYCLE : Commercial specification

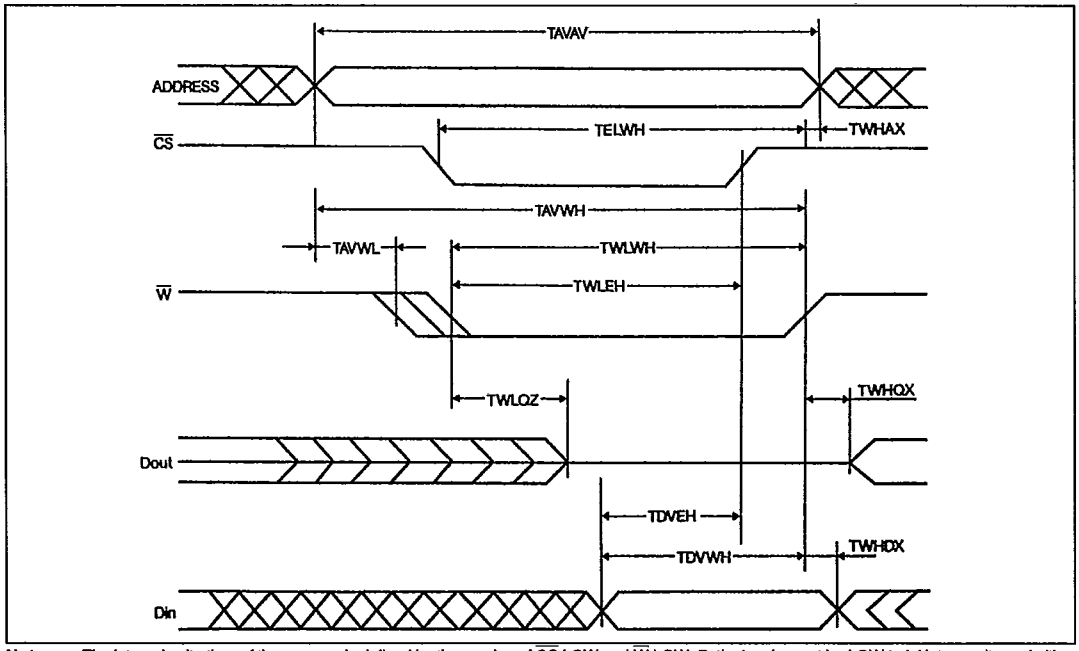
SYMBOL	PARAMETER	65664 B-5	65664 S-5	65664 -5	65664 C-5	UNIT	VALUE
TAVAV	Write cycle time	35	45	45	55	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	35	45	45	55	ns	min
TDVWH	Data set-up time	15	20	20	25	ns	min
TEL1WH	$\overline{CS1}$ low to write end	35	45	45	55	ns	min
TEH2WH	CS2 low to write end	35	45	45	55	ns	min
TWLQZ (12)	Write low to high Z	12	15	15	20	ns	max
TWLWH	Write pulse width	30	40	40	50	ns	min
TWHAX	Address hold to end of write	5	5	5	5	ns	min
TWHDX	Data hold time	3	3	3	3	ns	min
TWHQX (12)	Write high to low Z	0	0	0	0	ns	min

WRITE CYCLE : Industrial and Military specification

SYMBOL	PARAMETER	65664 B-9/2	65664 S-9/2	65664 -9/2	65664 C-9/2	UNIT	VALUE
TAVAV	Write cycle time	45	45	55	55	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	45	45	55	55	ns	min
TDVWH	Data set-up time	20	20	25	25	ns	min
TEL1WH	$\overline{CS1}$ low to write end	45	45	55	55	ns	min
TEH2WH	CS2 low to write end	45	45	55	55	ns	min
TWLQZ (12)	Write low to high Z	15	15	20	20	ns	max
TWLWH	Write pulse width	40	40	50	50	ns	min
TWHAX	Address hold to end of write	5	5	5	5	ns	min
TWHDX	Data hold time	3	3	3	3	ns	min
TWHQX (12)	Write high to low Z	0	0	0	0	ns	min

Note : 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE



Note : The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

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READ CYCLE : Commercial specification

SYMBOL	PARAMETER	65688 B-5	65688 S-5	65688 -5	65688 C-5	UNIT	VALUE
TAVAV	Read cycle time	35	35	45	45	ns	min
TAVQV	Address access time	35	35	45	45	ns	max
TAVQX	Address valid to low Z	5	5	5	5	ns	min
TELQV	Chip-select access time	40	40	50	50	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	5	ns	max
TEHQZ	$\overline{CS}$ high to high Z	35	35	45	45	ns	max

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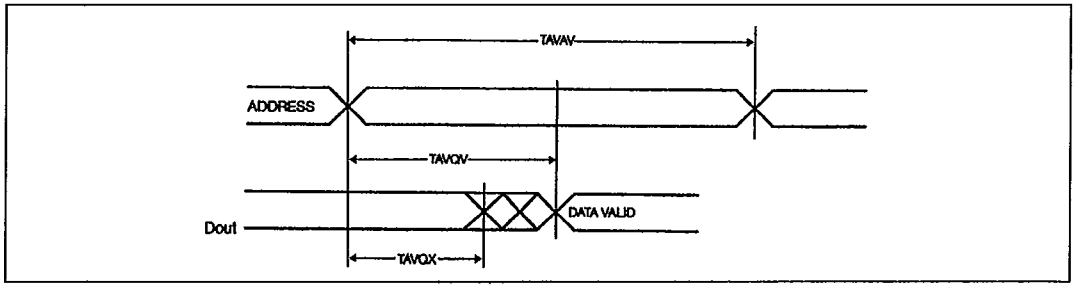
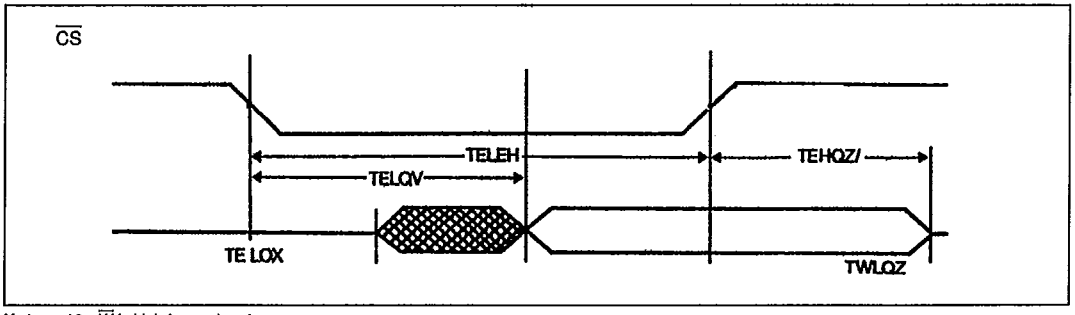
READ CYCLE : Industrial and military specification

SYMBOL	PARAMETER	65688 B-9/2	65688 S-9/2	65688 -9/2	65688 C-9/2	UNIT	VALUE
TAVAV	Read cycle time	45	45	55	55	ns	min
TAVQV	Address access time	45	45	55	55	ns	max
TAVQX	Address Valid to low Z	5	5	5	5	ns	min
TELQV	Chip-select access time	50	50	65	65	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	5	ns	max
TEHQX	$\overline{CS}$ high to high Z	45	45	55	55	ns	max

READ CYCLE nb 1 (notes 13, 14)



READ CYCLE nb 2 (notes 13, 15)



Notes : 13. $\overline{W}$ is high for read cycle.
14. Device is continuously selected, $\overline{CS}$ = VIL.
15. Address valid prior to or coincident with CS transitive low.

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ORDERING INFORMATION

Package	Device Type	Grade	Level
HM1	65688	B	–5
0 - Chip form 1 - Ceramic 22 pins 3 - Plastic 22 pins 300 mils 4* - LCC 22 pins T* - SOIC 24 pins U* - SOJ 24 pins	16 k x 4 Ultimate CMOS static RAM	B - high speed/low current S : high speed/standard current Blank : standard speed/low current C : standard	– 5 : Commercial – 9 : Industrial – 2 : Military – 8 : Military with B.I. (B.I. = Burn-in)

* preliminary

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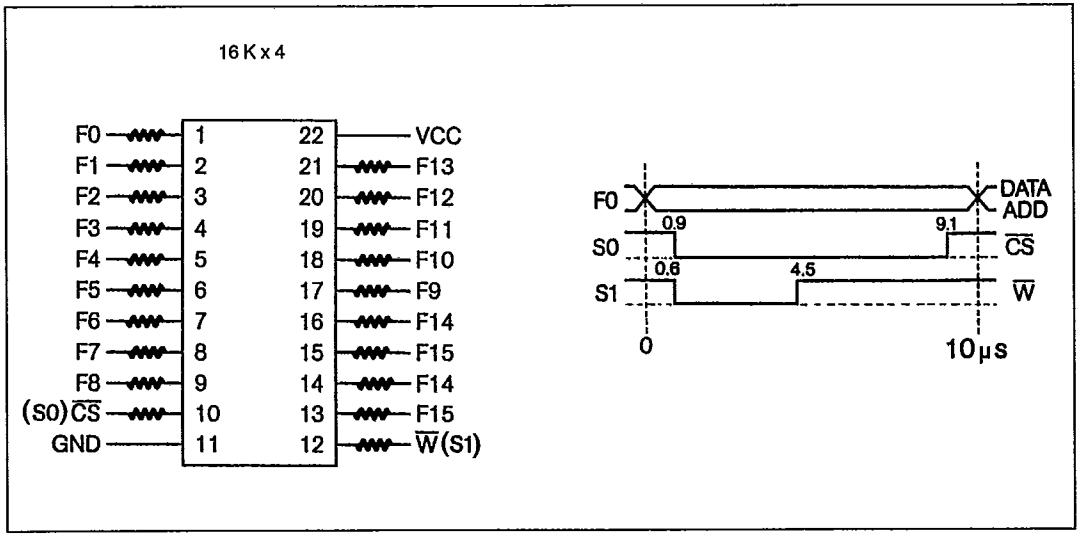
PACKAGE OUTLINE

For the packaging information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 22 pins
Ceramic DIL, 300 mils, 22 pins
SOIC DIL, 300 mils, 24 pins
LCC rectangular, 22 pins

BURN-IN SCHEMATICS



VCC = 5 V (– 0, + 0.5)
R = 1 KΩ per pin

FO = 91.6 KHz ± 20 %
Fn = 1/2 Fn-1

S0 et S1 : programmable signals for write / read cycles