WHITE ELECTRONIC DESIGNS

512Kx32 Static RAM CMOS, High Speed Module

FEATURES

- 512Kx32 bit CMOS Static
- Random Access Memory
  - Access Times: 15, 20, and 25ns
  - Individual Byte Selects
  - Fully Static, No Clocks
  - TTL Compatible I/O
- High Density Package
  - 72 Pin ZIP, No. 173
  - 72 lead SIMM, No. 174 (Gold Option)
  - Common Data Inputs and Outputs
- Single +5V (±10%) Supply Operation

DESCRIPTION

The EDI8F32512C is a high speed 16 megabit Static RAM module organized as 512K words by 32 bits. This module is constructed from four 512Kx8 Static RAMs in SOJ packages on an epoxy laminate (FR4) board.

Four chip enables ($\overline{E0}$-$\overline{E3}$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

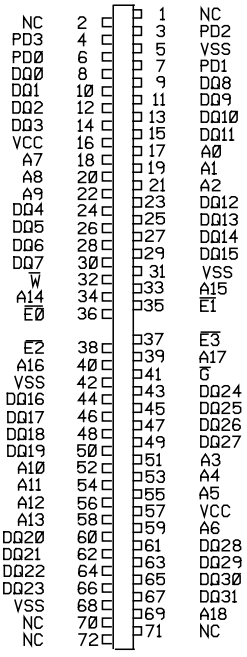
The EDI8F32512C is offered in 72 pin ZIP and 72 lead SIMM packages, which enable 16 megabits of memory to be placed in less than 1.3 square inches of board space.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refreshing for operation and provides equal access and cycle times for ease of use.

Pins PD1- PD4, are used to identify module memory density in applications where alternate modules can be interchanged.

FIG. 1

PIN CONFIGURATIONS AND BLOCK DIAGRAM

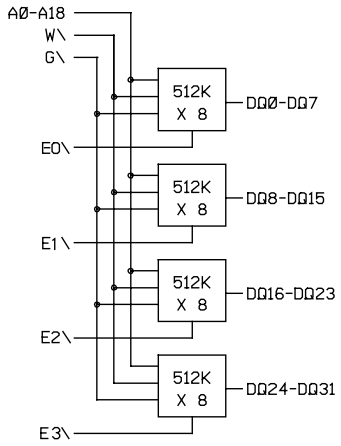


PD0, PD1, PD3= OPEN
PD2= VSS

8G32512C Pin Config.

PIN NAMES

A0-A18	Address Inputs
$\overline{E0}$-$\overline{E3}$	Chip Enables
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0-DQ31	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection



8G32512C Blk Dia.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature, Plastic	-55°C to +125°C
Power Dissipation	5.0 Watts
Output Current	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC TEST CONDITIONS

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL, CL = 30pF

(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC ELECTRICAL CHARACTERISTICS

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle			800	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E} \geq$ VIH, VIN $\leq$ VIL or VIN $\geq$ VIH			300	mA
Full Standby Power Supply Current CMOS	ICC3	$\overline{E} \geq$ VCC-0.2V VIN $\geq$ VCC-0.2V or VIN $\leq$ 0.2V			80	mA
Input Leakage Current	ILI	VIN = 0V to VCC	–	–	±20	µA
Output Leakage Current	ILO	V I/O = 0V to VCC	–	–	±20	µA
Output High Voltage	VOH	IOH = -4.0mA	2.4	–	–	V
Output Low Voltage	VOL	IOL = 8.0mA	–	–	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

TRUTH TABLE

$\overline{E}$	$\overline{W}$	$\overline{G}$	Mode	Output	Power
H	X	X	Standby	HIGH Z	ICC2/ICC3
L	H	L	Read	DOUT	ICC1
L	L	X	Write	DIN	ICC1
L	H	H	Output Deselect	HIGH Z	ICC1

CAPACITANCE

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	45	pF
Data Lines	CD/Q	20	pF
Chip Enable Line	CC	20	pF
Write Line	CN	45	pF

These parameters are sampled, not 100% tested.

AC CHARACTERISTICS READ CYCLE

	Symbol		15ns		20ns		25ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Read Cycle Time	TAVAV	TRC	15		20		25		ns
Address Access Time	TAVQV	TAA		15		20		25	ns
Chip Enable Access	TELQV	TACS		15		20		25	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		6		10		12	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		6		8		10	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		6		8		10	ns

Notes: 1. Parameter guaranteed, but not tested.

FIG. 2

READ CYCLE 1 - $\overline{W}$ HIGH, $\overline{G}$, $\overline{E}$ LOW

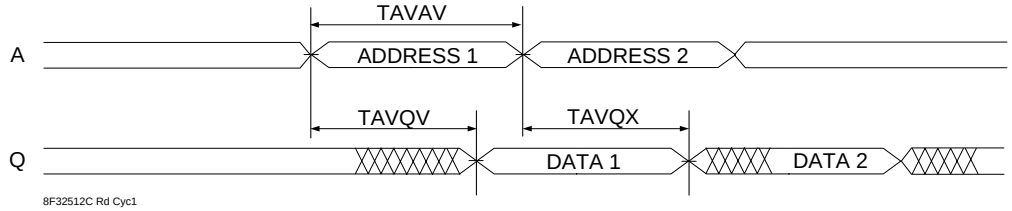
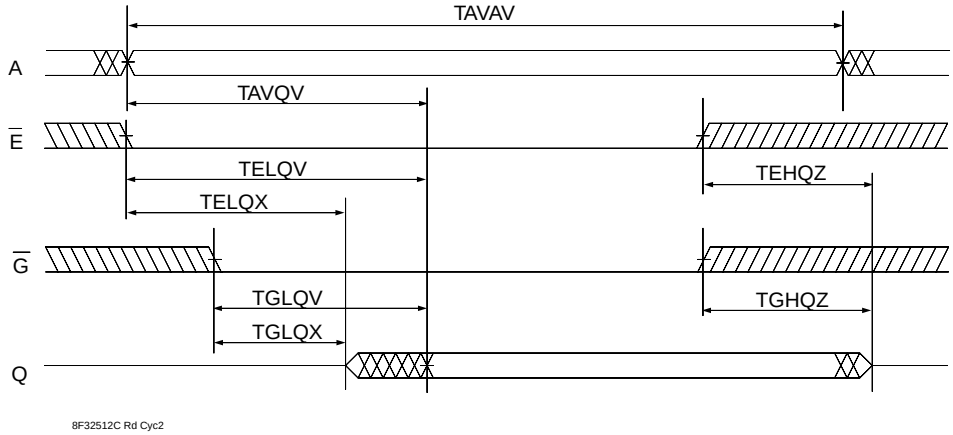


FIG. 3

READ CYCLE 2 - $\overline{W}$ HIGH



AC CHARACTERISTICS WRITE CYCLE

	Symbol		15ns		20ns		25ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Write Cycle Time	TAVAV	TWC	15		20		25		ns
Chip Enable to End of Write	TELWH	TCW	8		15		20		ns
	TWLEH	TCW	8		15		20		ns
Address Setup Time	TAVWL	TAS	0		0		0		ns
	TAVEL	TAS	0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	8		15		15		ns
	TAVEH	TAW	8		15		15		ns
Write Pulse Width	TWLWH	TWP	10		15		15		ns
	TELEH	TWP	10		15		15		ns
Write Recovery Time	TWHAX	TWR	0		0		0		ns
	TEHAX	TWR	0		0		0		ns
Data Hold Time	TWHDX	TDH	0		0		0		ns
	TEHDX	TDH	0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	6	0	8	0	12	ns
Data to Write Time	TDVWH	TDW	7		9		10		ns
	TDVEH	TDW	7		9		10		ns
Output Active from End of Write (1)	TWHQX	TWLZ	3		3		3		ns

Notes: 1. Parameter guaranteed, but not tested.

FIG. 4

WRITE CYCLE 1 - $\overline{W}$ CONTROLLED

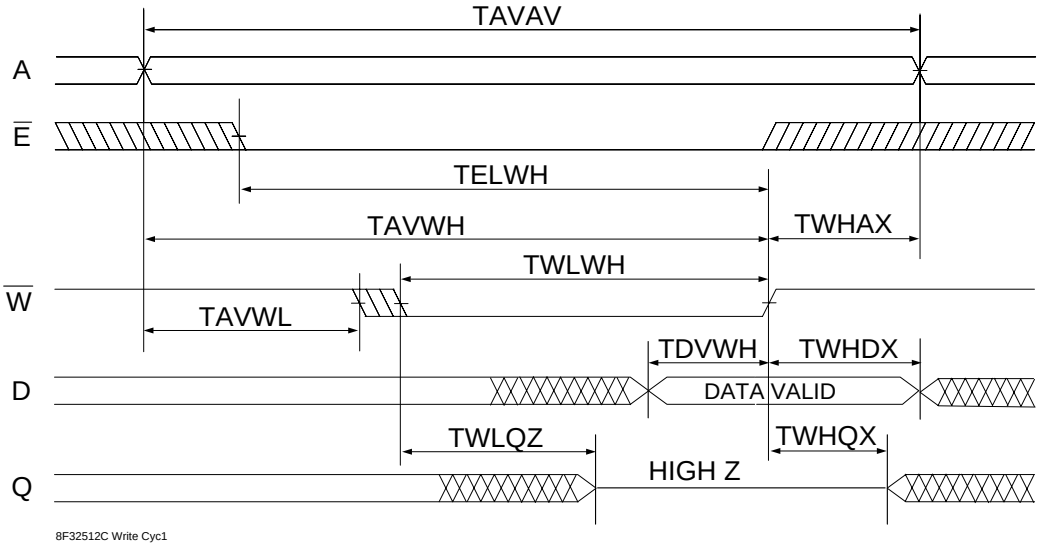
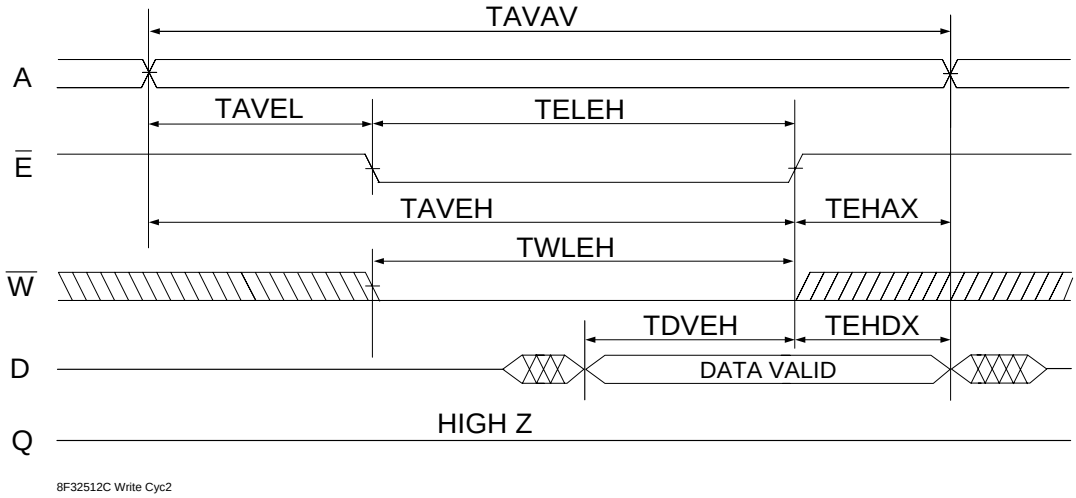


FIG. 5

WRITE CYCLE 2 - $\overline{E}$ CONTROLLED



ORDERING INFORMATION

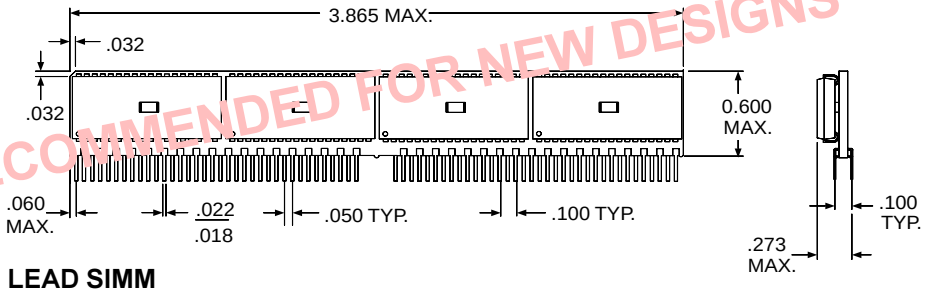
Part Number	Speed (ns)	Package No.
EDI8F32512C15MMC	15	174
EDI8F32512C20MMC	20	174
EDI8F32512C25MMC	25	174

Note: To order gold SIMM option, change from "EDI8F" to "EDI8G".

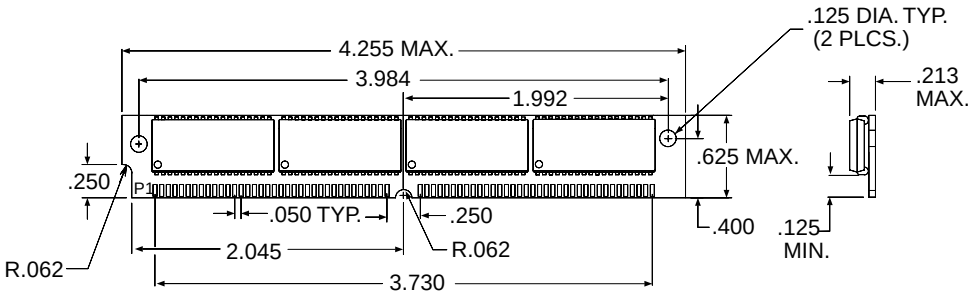
Part Number	Speed (ns)	Package No.
EDI8F32512C15MZC	15	173
EDI8F32512C20MZC	20	173
EDI8F32512C25MZC	25	173

PACKAGE DESCRIPTION

PACKAGE NO. 173: 72 PIN ZIP



PACKAGE NO. 174: 72 LEAD SIMM



ALL DIMENSIONS ARE IN INCHES