



4x1Mx32 FLASH MODULE

DESCRIPTION

The EDI7F4331MV is organized as four banks of 1Mx32. The module is based on AMDs AM29LV008T - 1Mx8 Flash device in TSOP packages which are mounted on an FR4 substrate.

The module offers access times between 80 and 150ns allowing for operation of high-speed microprocessors without wait states.

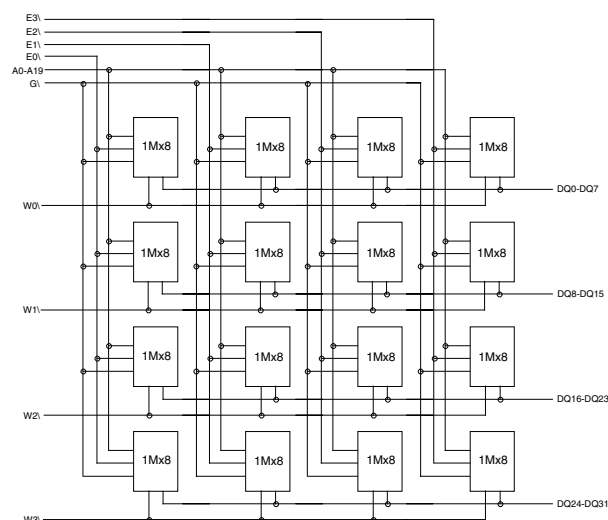
FEATURES

- 4x1Mx32
- Based on AMD - AM29LV008T Flash Device
- Fast Read Access Time - 80ns
- 3.3- Volt-Only Reprogramming
- Flexible, Sector Architecture
 - One 16Kbyte, two 8Kbyte, one 32Kbyte and fifteen 64Kbyte sectors.
 - Any combination of sectors can be erased
 - Also supports full chip erase
- Sector Protection
 - Hardware method that disables any combination of sectors from write or erase operations
- Embedded Erase Algorithms
 - Automatically preprograms and erases the chip or any combination of sectors
- Embedded Program Algorithms
 - Automatically programs and verifies data at specified address
- Data Polling and Toggle Bit feature for detection of program or erase cycle completion
- Low Power Dissipation
 - 30mA per Device Active Current
 - 10µA per Device CMOS Standby Current
- Typical Endurance >100,000 Cycles
- Single 3.3 Volt $\pm 10\%$ Supply
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Range
- Package
 - 80 Pin SIMM (JEDEC)

FIG. 1

BLOCK DIAGRAM

EDI7F4331MV-BNC: 4x1Mx32 80 PIN SIMM





CAPACITANCE

(f=1.0MHz, VIN = VCC or VSS)

4x1Meg			
Parameter	Sym	Max	Unit
Address Lines	CA	140	pF
Data lines	CDQ	60	pF
Chip & Write Enable Lines	CC	60	pF
Output Enable lines	CG	140	pF

PIN CONFIGURATIONS

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	VSS	21	E3\	41	A11	61	DQ9
2	VCC	22	E2\	42	A10	62	DQ8
3	NC	23	E1\	43	A9	63	DQ7
4	G\	24	E0\	44	A8	64	DQ6
5	W0\	25	VSS	45	A7	65	DQ5
6	W1\	26	DQ29	46	A6	66	DQ4
7	NC	27	DQ30	47	A5	67	DQ3
8	DQ16	28	DQ31	48	A4	68	DQ2
9	DQ17	29	W2\	49	A3	69	DQ1
10	DQ18	30	NC	50	A2	70	DQ0
11	DQ19	31	NC	51	A1	71	NC
12	DQ20	32	NC	52	AO	72	VCC
13	DQ21	33	A19	53	W3\	73	PD1
14	DQ22	34	A18	54	VSS	74	PD2
15	DQ23	35	A17	55	DQ15	75	PD3
16	DQ24	36	A16	56	DQ14	76	PD4
17	DQ25	37	A15	57	DQ13	77	PD5
18	DQ26	38	A14	58	DQ12	78	PD6
19	DQ27	39	A13	59	DQ11	79	PD7
20	DQ28	40	A12	60	DQ10	80	VSS

Simm Pin	Density 4x1Meg
21	E3\
22	E2\
23	E1\
24	E0\

Presence Detect Pin Out	
Pin	1Meg
PD1	NC
PD2	NC
PD3	VSS
PD4	VSS

A0-A19 Address input
E0\,E1\,E2\, E3\ Chip Enable
W0\-W3\ Write Enable
G\ Output Enable
DQ0-DQ31 Data Input/Output
PD Presence Detect
VCC Power 3.3V±10%
VSS Ground
NC No Connect

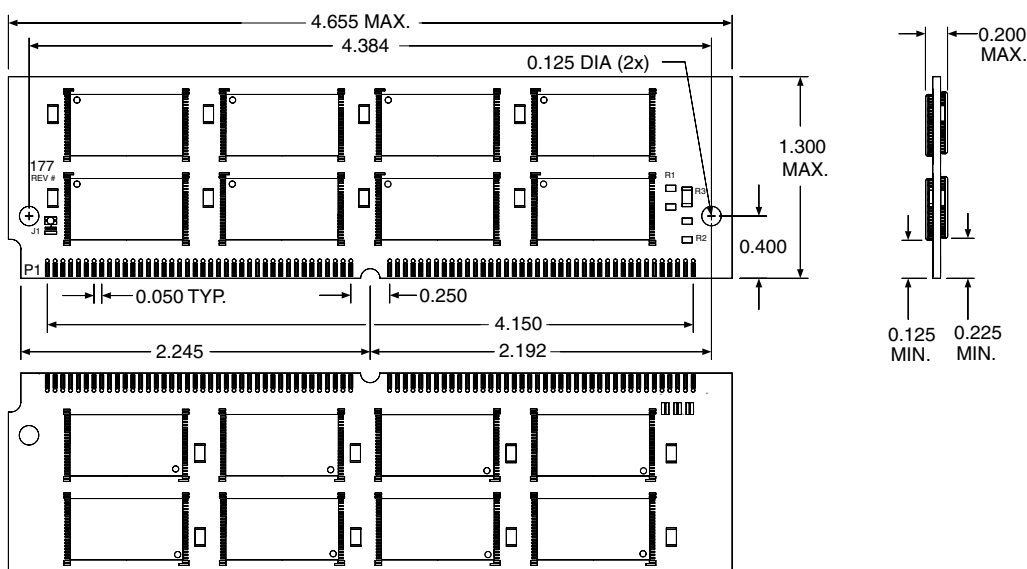


ORDERING INFORMATION

Part Number	Speed (ns)	Package
EDI7F4331MV80BNC	80	394
EDI7F4331MV90BNC	90	394
EDI7F4331MV100BNC	100	394
EDI7F4331MV120BNC	120	394
EDI7F4331MV150BNC	150	394

Note: To order an Industrial grade product substitute the letter C in the Suffix with the letter I.

PACKAGE NO. 394: 80 PIN SIMM (JEDEC)



ALL DIMENSIONS ARE IN INCHES

DATASHEET APPROVALS

EDI PART NO. EDI7F4331MV ECO# 15612 NEW REV 1A DATE 9/30/02

<u>APPROVAL:</u>	<u>INITIAL</u>	<u>DATE</u>	<u>CORRECTION ON PAGES</u>
JUAN GUZMAN L.K.	_____	_____	_____
MUKESH TRIVEDI M.A.	_____	_____	_____
PAUL MARIEN	_____	_____	_____
LARRY WINROTH	_____	_____	_____
DAVE KELLY	_____	_____	_____
MARK DOWNEY	_____	_____	_____
DAVE HARRISON	_____	_____	_____
TONY LEE	_____	_____	_____
BOB KHEDERIAN	_____	_____	_____
LUIS ESTELLA	_____	_____	_____

WILL THIS DATASHEET GO ON THE WEB? YES NO LINE: _____
FAMILY: _____

IS THIS A NEW DATASHEET? PROD.TYPE: _____
ORG: _____
DENSITY: _____
SPEED: _____
PKG: _____
VOLTAGE: _____

WILL THIS DATASHEET REPLACE AN EXISTING
DATASHEET THAT'S ALREADY ON THE WEB?

IF YES, WHAT DATASHEET IS IT REPLACING?

WHAT SECTION SHOULD THIS DATASHEET BE
PLACED IN ON THE WEB? _____

AFTER REVIEWING OR MAKING CORRECTIONS ON THE DATASHEET (S)
**PLEASE SIGN-OFF ON THIS SHEET AND ,MAKE YOUR CORRECTIONS –ON
THE ORIGINAL COPY(S).**

AFTER REVIEWING THE DATA SHEET, TEST ENGINEERING WILL COMPLETE THE SECTION BELOW.

TEST PROGRAM CHANGE REQUIRED:
YES: _____ NO _____ DATE: _____

TEST ENGINEER SIGNATURE _____

IF YES, DO NOT RELEASE DATA SHEET UNTIL TEST PROGRAM CHANGE IS COMPLETED.

TEST PROGRAM CHANGE COMPLETION DATE: _____
TEST PROGRAM NAME AND REVISION _____
TEST ENGINEER SIGNATURE _____