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Fairchild Semiconductor
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Using Fairchild's LVX Low Voltage Dual Supply CMOS Translating Transceivers

INTRODUCTION

The Fairchild CMOS Translating Transceivers: 74LVX3245, 74LVX4245, 74LVXC3245, and 74LVXC4245 are true voltage translating devices. This is accomplished by electrically isolating the A-side from the B-side.

An example of when it is necessary to use a true voltage translator, is in a system translating between 3 volt logic and 5 volt CMOS logic. In this case, the translators will insure a clean, fast and valid V_{IH} (Voltage Input High) signal in both directions. This translation may be problematic with other forms of translation due to the V_{IH} required, typically 3.5V for 5V CMOS.

DEVICE TYPE DESCRIPTIONS

The LVX Translating Transceivers are divided into two types of devices, Dual Supply Translating Transceivers, and Dual Supply Configurable Voltage Interface Transceivers. These devices offer the system designer multiple options for true voltage level translation in a system.

DUAL SUPPLY TRANSLATORS

The Dual Supply Translator devices (74LVX3245 and 74LVX4245) are designed to interface 3 volt to 5 volt signals. The Transmit/Receive control pin controls data direction flow. These devices are designed with the higher voltage V_{CC} able to swing from 4.5V to 5.5V and the lower voltage V_{CC} able to swing from 2.7V to 3.6V. The control pins $\overline{OE}$ (Output Enable) and T/$\overline{R}$ (Transmit/Receive) are powered by the V_{CCA} side of the device.

The 74LVX3245 and 74LVX4245 provide the same 5V to 3V translation function. The difference between the two devices is the side of the device the 5V and 3V V_{CC}'s and their associated I/O (Input/Outputs data) ports are on.

In the case of the 74LVX3245 Figure 1, V_{CCB} and the B I/O port are the 5V side (4.5V to 5.5V) and the V_{CCA} and the A I/O port are the 3V side (2.7V to 3.6V).

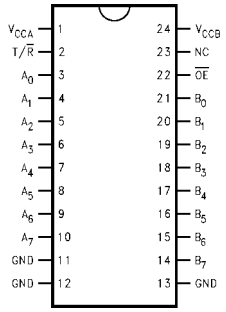

FIGURE 1. 74LVX3245

On the 74LVX4245 Figure 2, V_{CCA} and the A I/O port are the 5V side (4.5V to 5.5V) and the V_{CCB} and the B I/O are the 3V side (2.7V to 3.6V).

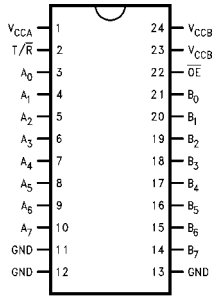

FIGURE 2. 74LVX4245

CONFIGURABLE VOLTAGE INTERFACE TRANSCEIVERS

The Configurable Voltage Interface transceivers (74LVXC3245 and 74LVXC4245) are designed for real time configurable I/O applications such as PCMCIA (Personal Computer Memory Card Interface Association).

Configurability simply means the device is designed with the ability of the "configurable" side of the I/O port, to track, or follow the V_{CCB} voltage level. This is accomplished by tying V_{CCB} of the device to the PCMCIA card voltage supply. The card will always experience full rail data signals, maximizing interface reliability.

The control pins $\overline{OE}$ (Output Enable) and T/$\overline{R}$ (Transmit/Receive) are powered by the V_{CCA} side of the device.

These devices are also designed to allow the configurable side (V_{CCB} and B I/O port) to float, unconnected to any voltage or control source. This is allowed when the $\overline{OE}$ pin is driven to a logic high.

Floating V_{CCB} and the B port is useful in applications where a card or cable may need to be left disconnected. Using a Configurable Voltage Interface device at this point will eliminate false signaling or system damage due to the oscillations that can occur if standard design CMOS inputs and power pins are left floating.

The 74LVXC3245 and 74LVXC4245 are designed for different V_{CCA} and A I/O port voltage levels.

In the case of the 74LVXC3245 Figure 3, the V_{CCA} and the A I/O port are designed for 3V (2.7V to 3.6V). The device B side is the configurable side. V_{CCB} accepts a 3V to 5.5V level, and the B I/O port tracks the V_{CCB} level.

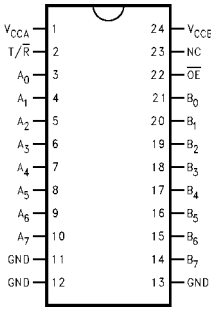

FIGURE 3. 74LVX3245

On the 74LVX4245 Figure 4, V_{CCA} and the A I/O port are designed for 5V (4.5V to 5.5V). The device B side is the configurable side. V_{CCB} accepts a 2.7V to 5.5V level and the B I/O port tracks the V_{CCB} level.

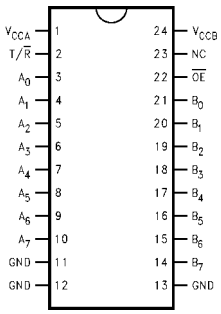

FIGURE 4. 74LVX4245

POWER UP CONSIDERATIONS

These designs give the user a true translating device, however, they also present the system designer with some special considerations during power up to insure the system does not experience unnecessary I_{CC} current draw, bus contention, or oscillations (refer to Table).

To guard against power up problems, some simple guidelines need to be adhered to:

- Power up the control side of the device first. This is the V_{CCA} side on all four devices.
- $\overline{OE}$ should ramp with or ahead of V_{CCA}. This will help guard against bus contention.
- The Transmit/Receive control pin (T/$\overline{R}$) should ramp with or ahead of V_{CCA}, this will ensure that the A port data pins are configured as inputs. WIth V_{CCA} receiving power first, the A I/O port should be configured as inputs to help guard against bus contention and oscillations.
- A side data inputs should be driven to a valid logic level. This will prevent excessive current draw.

The above steps will ensure that no bus contention or oscillations, and therefore no excessive current draw occurs during the power up cycling of these devices. These steps will help prevent possible damage to the translator devices and potential damage to other system components.

Table 1: LOW VOLTAGE TRANSLATOR POWER UP SEQUENCING TABLE

Device Type	V_{CCA}	V_{CCB}	T/$\overline{R}$	$\overline{OE}$	A side I/O	B side I/O	Floatable Pin Allowed
74LVX3245	3V (power up 1st)	5V (power up 2nd)	ramp with V_{CCA}	ramp with V_{CCA}	logic 0V or V_{CCA}	outputs	No
74LVX4245	5V (power up 1st)	3V (power up 2nd)	ramp with V_{CCA}	ramp with V_{CCA}	logic 0V or V_{CCA}	outputs	No
74LVXC3245	3V (power up 1st)	3V to 5.5V configurable	ramp with V_{CCA}	ramp with V_{CCA}	logic 0V or V_{CCA}	outputs	yes, V_{CCB} and B I/O's w/ $\overline{OE}$ HIGH
74LVXC4245	5V (power up 1st)	2.7V to 5.5V configurable	ramp with V_{CCA}	ramp with V_{CCA}	logic 0V or V_{CCA}	outputs	yes, V_{CCB} and B I/O's w/ $\overline{OE}$ HIGH

FLOATING OF PINS

The Dual Supply Configurable Voltage Interface devices (74LVXC3245 and 74LVXC4245) are designed to allow the configurable side of the device (V_{CCB} and the B I/O pins) to float when the V_{CCA} side is powered up and the $\overline{OE}$ pin is driven to a valid logic high.

It is also recommended that the T/$\overline{R}$ pin is set to a logic high (A to B direction) and A side I/O pins are at valid logic levels. This will help prevent oscillations and potential excessive current draw.

Allowing pins to float on the Non-Configurable Dual Supply Translators (74LVX3245 and 74LVX4245) is not recommended. High I_{CC} device currents, signal oscillations, and possible device damage may result.

SUMMARY

Fairchild's Dual Supply CMOS translating transceivers solve mixed voltage design problems by providing translation between 3V logic and 5V CMOS logic. Careful selection of the appropriate configuration and attention to the power up considerations discussed in this applications note can make interfacing in a mixed voltage environment an easy task.