CMOS single-chip 8-bit microcontroller — 87C752/87C752-16

FEATURES

- 80C51 based architecture
- Available in erasable quartz lid or One-Time Programmable ceramic packages
- Inter-Integrated Circuit (I^2C) serial bus interface
- Small package sizes
  - 28-pin DIP
- Wide oscillator frequency range
- Low power consumption:
  - Normal operation: less than 11mA @ 5V, 12MHz
  - Idle mode
  - Power-down mode
- 2K × 8 EPROM, 64 × 8 RAM
- 16-bit auto reloadable counter/timer
- 5 channel 8-bit A/D converter
- 8-bit PWM output/timer
- Fixed-rate timer
- Boolean processor
- CMOS and TTL compatibile
- Well suited for logic replacement applications

DESCRIPTION

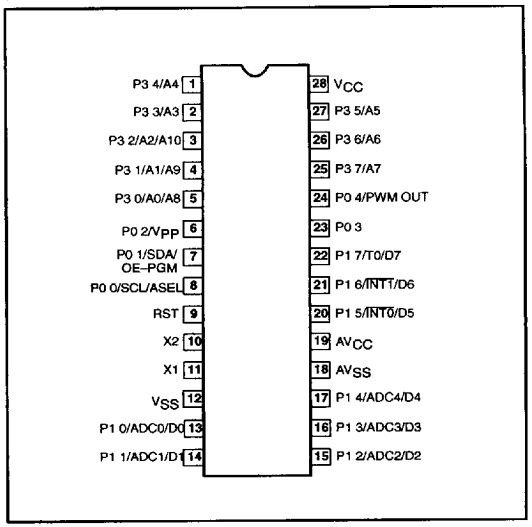
The Philips 87C752 offers many of the advantages of the 80C51 architecture in a small package and at low cost.

The 87C752 Microcontroller is fabricated with Philips high-density CMOS technology. Philips epitaxial substrate minimizes CMOS latch-up sensitivity.

The 87C752 contains a 2K × 8 EPROM, a 64 × 8 RAM, 21 I/O lines, a 16-bit auto- reload counter/timer, a fixed- priority level interrupt structure, a bidirectional inter- integrated circuit (I^2C) serial bus interface, an on-chip oscillator, a five channel multiplexed 8-bit A/D converter, and an 8-bit PWM output.

The onboard inter-integrated circuit (I^2C) bus interface allows the 87C752 to operate as a master or slave device on the I^2C small area network. This capability facilitates I/O and RAM expansion, access to EEPROM, processor-to- processor communication, and efficient interface to a wide variety of dedicated I^2C peripherals.

PIN CONFIGURATION

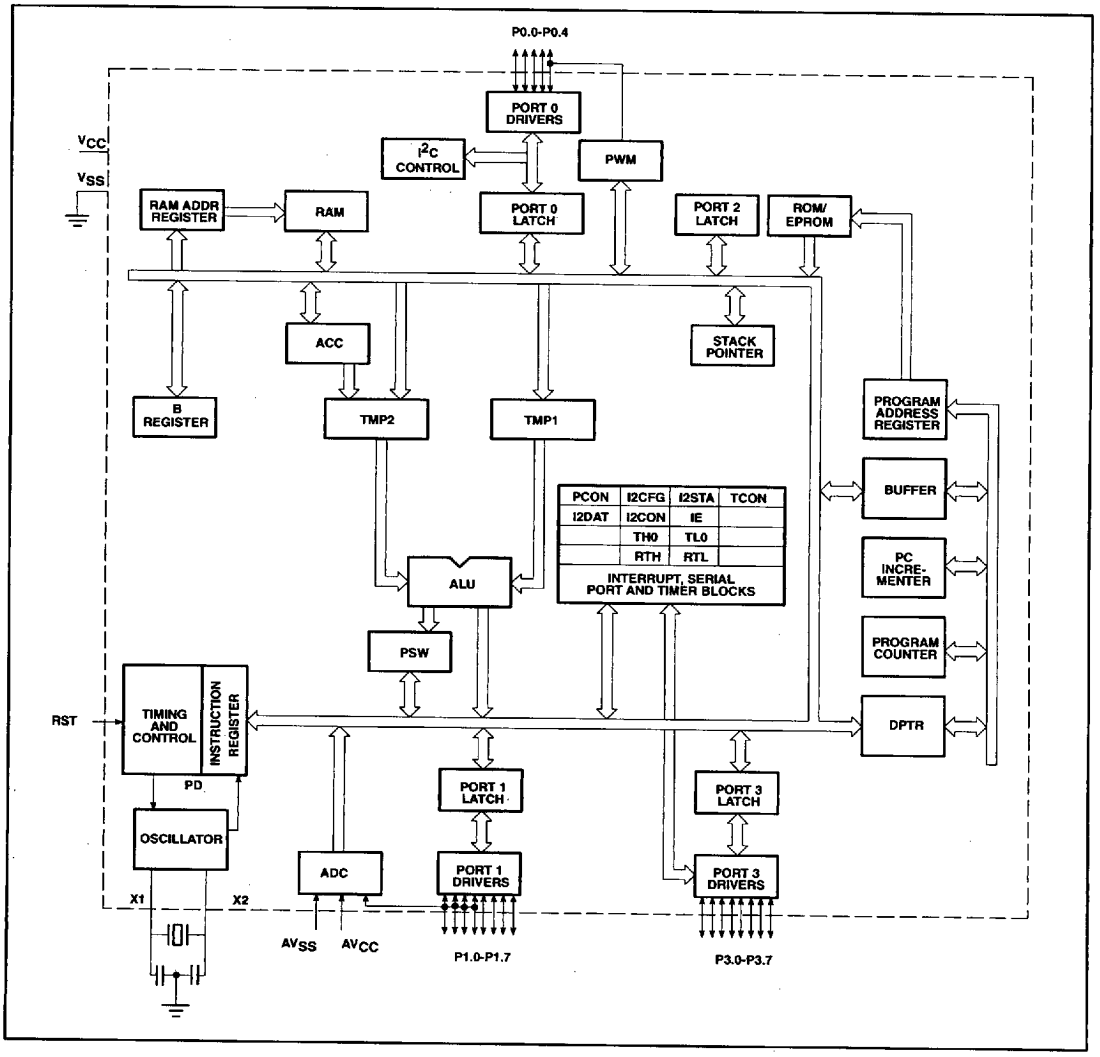


ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PKG DESIGNATOR[2]
28-Pin DIP 600mil-wide	87C752/BXA	GDIP1-T28
28-Pin DIP 600mil-wide (one time programming)	87C752/BXA OT[1]	GDIP1-T28
28-pin DIP 600mil-wide 16MHz	87C752-16/BXA	GDIP1-T28
28-pin DIP 600mil-wide 16MHz (one time programming)	87C752-16/BXA OT[1]	GDIP1-T28

NOTE:
1. Erase characteristics do not apply for one time programming (OT).
2. MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

BLOCK DIAGRAM



PIN CONFIGURATION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
V_{SS}	12	I	**Circuit ground potential.**
V_{CC}	28	I	**Supply voltage during normal, idle, and power-down operation.**
P0.0-P0.4	8-6 23,24	I/O	**Port 0:** Port 0 is a 5-bit bidirectional port. Port 0.0-P0.2 are open drain. Port 0.0-P0.2 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. P0.3-P0.4 are bidirectional I/O port pins with internal pull-ups. Port 0 also serves as the serial I^2C interface. When this feature is activated by software, SCL and SDA are driven low in accordance with the I^2C protocol. These pins are driven low if the port register bit is written with a 0 or if the I^2C subsystem presents a 0. The state of the pin can always be read from the port register by the program. Port 0.3 and 0.4 have internal pull-ups that function identically to Port 3. Pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. To comply with the I^2C specification, P0.0 and P0.1 are open drain bidirectional I/O pins with the electrical characteristics listed in the tables that follow. While these differ from "standard TTL" characteristics they are close enough for the pins to still be used as general-purpose I/O in non-I^2C applications.
	6	I	**V_{CC} (P0.2)** - Programming voltage input.
	7	I	**OE/PGM (P0.1)** - Input which specifies verify mode (output enable) or the program mode. OE/PGM - 1 output enabled (verify mode). OE/PGM - 0 program mode.
	8	O	**ASEL (P0.0)** - Input which indicates which bits of the EPROM address are applied to Port 3. ASEL = 0 low address byte available on Port 3. ASEL = 1 high address byte available on Port 3 (only the three least significant bits are used).
P1.0-P1.7	13-17, 20-22	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. P0.3-P0.4 pins are bidirectional I/O port pins with internal pull-ups. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 1 also serves the special function features of the 80C51 family as listed below:
	20	I	**$\overline{INT0}$ (P1.5):** External interrupt.
	21	I	**$\overline{INT1}$ (P1.6):** External interrupt.
	22	I	**T0 (P1.7):** Timer 0 external input.
	13-17	I	**ADC0 (P1.0)-ADC4 (P1.4):** Port 1 also functions as the inputs to the five channel multiplexed A/D converter. These pins can be used as outputs only if the A/D function has been disabled. These pins can be used as inputs while the A/D converter is enabled. Port 1 serves to output the addressed EPROM contents in the verify mode and accepts as inputs the value to program into the selected address during the program mode.
P3.0-P3.7	5-1, 27-25	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pul-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current because of the pull-ups (See DC Electrical Characteristics: I_{IL}). Port 3 also functions as the address input for the EPROM memory location to be programmed (or verified) . The 11-bit address is multiplexed into this port as specified by P0.0/ASEL.
RST	9	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits a power-on RESET using only an external capacitor to V_{CC}. After the device is reset, a 10-bit serial sequence, sent LSB first, applied to RESET places the device in the programming state allowing programming address, data and V_{PP} to be applied for programming or verification purposes. The RESET serial sequence must be synchronized with the X1 input.
X1	11	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. X1 also serves as the clock to strobe in a serial bit stream into RESET to place the device in the programming state.
X2	10	O	**Crystal 2:** Output from the inverting oscillator amplifier.
AV_{CC}	19	I	**Analog supply voltage and reference input.**
AV_{CC}	18	I	**Analog supply and reference ground.**

OSCILLATOR CHARACTERISTIC

X1 and X2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator.

To drive the device from an external clock source, X1 should be driven while X2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

IDLE MODE

In the idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power- down is the last instruction executed. Only the contents of the on-chip RAM are preserved. A hardware reset is the only way to terminate the power-down mode. The control bits for the reduced power modes are in the special function register PCON.

Table 1. External Pin Status During Idle and Power-Down Modes

Mode	Port 0*	Port 1	Port 2
Idle	Data	Data	Data
Power-down	Data	Data	Data

* Except for PWM output (P0.4).

DIFFERENCES BETWEEN THE 87C752 AND THE 80C51

Program Memory

On the 87C752, program memory is 2048 bytes long and is not externally expandable. Program memory can contain 87C752 instructions and constant data. The only fixed locations in program memory are the addresses at which execution is taken up in response to reset and to interrupts, which are as follows:

Event	Program Memory Address
Reset	000
External $\overline{INT0}$	003
Counter/timer 0	00B
External $\overline{INT1}$	013
Timer I	01B
I^2C serial	023
ADC	02B
PWM	033

Counter/Timer Subsystem

The 87C752 has one counter/timer called timer/counter 0. Its operation is similar to mode 2 operation on the 80C51, but is extended to 16 bits with 16 bits of autoload. The controls for this counter are centralized in a single register called TCON.

A watchdog timer, called Timer I, is for use with the I^2C subsystem. In I^2C applications, this timer is dedicated to time-generation and bus monitoring of the I^2C. In non-I^2C applications, it is available for use as a fixed time-base.

Interrupt Subsytem - Fixed Priority

The IP register and the 2-level interrupt system of the 80C51 are eliminated. Simultaneous interrupt conditions are resolved by a single-level, fixed priority as follows:

Highest priority:	Pin $\overline{INT0}$
	Counter/timer flag 0
	Pin $\overline{INT1}$
	PWM
	Timer I
	Serial I^2C
Lowest priority:	ADC

Serial Communications

The 87C752 contains an I^2C serial communications port instead of the 80C51 UART. The I^2C serial port is a single bit hardware interface with all of the hardware necessary to support multimaster and slave operations. Also included are receiver digital filters and timer (timer I) for communication watch-dog purposes. The I^2C serial port is controlled through four special function registers; I^2C control, I^2C data, I^2C status, and I^2C configuration.

Pulse Width Modulation Output (P0.4)

The PWM outputs pulses of programmable length and interval. the repetition frequency is defined by an 8-bit prescaler which generates the clock for the counter. The prescaler register is PWMP. The prescaler and counter are not associated with any other timer. The 8-bit counter counts modulo 255, that is from 0 to 254 inclusive. The value of the 8-bit counter is compared to the contents of a compare register, PWM. When the counter value matches the contents of this register, the output of the PWM is set high. When the counter reaches zero, the output of the PWM is set low. The pulse width ration (duty cycle) is defined by the contents of the compare register and is in the range of 0 to 1 programmed in increments of 1/255. The PWM output can be set to be continuously high by loading the compare register with 0 and the output can be set to be continuously low by loading the compare register with 255. The PWM output is enabled by a bit in a special function register, PWENA. When enabled, the pin output is driven with a fully active pull-up. That is, when the output is high, a strong pull-up is continuously applied. When disabled, the pin functions as a normal bidirectional I/O pin, however, the counter remains active.

The PWM function is disabled during RESET and remains disabled after reset is removed until re-enabled by software. The PWM output is high during power down and idle. The counter is disabled during idle. The repetition frequency of the PWM is given by:

$f_{PWM} = f_{OSC}/2(1 + PWMP)\ 255$

The low/high ratio of the PWM signal is PWM/(255 - PWM) for PWM not equal to 255. For PWM = 255, the output is always low.

The repetition frequency range is 92Hz to 23.5kHz for an oscillator frequency of 12MHz.

An interrupt will be asserted upon PWM counter overflow if the interrupt is not masked off.

The PWM output is an alternative function of P0.4. In order to use this port as a bidirectional I/O port, the PWM output must be disabled by clearing the enable/disable bit in PWENA. In this case, the PWM subsystem can be used as an interval timer by enabling the PWM interrupt.

A/D Converter

The analog input circuitry consists of a 5-input analog multiplexer and an A to D converter with 8-bit resolution. The conversion takes 40 machine cycles, i.e., 40µs at 12MHz oscillator frequency. The A/D converter is controlled using the ADCON control register. Input channels are selected by the analog multiplexer through ADCON register bits 0-2.

Special Function Register Addresses

Special function registers for the 87C752 are identical to those of the 80C51, except for the changes listed below:

80C51 special function registers not present in the 87C752 are TMOD (89), P2 (A0) and IP (B8). The 80C51 registers TH1, TL1, SCON, and SBUF are replaced with the 87C752 registers RTH, RTL, I2CON, and 12DAT, respectively. Additional special function registers are I2CFG (D8) and I2STA (FB), ADCON (A0), ADAT (84), PWM (8E), PWMP (8F), and PWENA (FE). See Table 2.

Table 2. I^2C Special Function Register Addresses

Register Address			Bit Address							
Name	Symbol	Address	MSB							LSB
I^2C control	I2CON	98	9F	9E	9D	9C	9B	9A	99	98
I^2C data	I2DAT	99	-	-	-	-	-	-	-	-
I^2C configuration	I2CFG	D8	DF	DE	DD	DC	DB	DA	D9	D8
I^2C status	I2STA	F8	FF	FE	FD	FC	FB	FA	F9	F8

ABSOLUTE MAXIMUM RATINGS [1, 2]

SYMBOL	PARAMETER	RATING	UNIT
T_{STG}	Storage temperature range	-65 to + 150	°C
V_{CC}	Voltage from V_{CC} to V_{SS}	-0.5 to +6.5	V
V_S	Voltage from any pin to V_{SS}	-0.5 to V_{CC} +0.5	V
P_D	Power dissipation	1.0	W

DC ELECTRICAL CHARACTERISTICS

$-55°C \le T_{amb} \le 125°C$, $4.5V \le V_{CC} \le 5.5V$, V_{SS} - 0V[3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
I_{CC}	Supply current (see Figure 3)				
Inputs					
V_{IL}	Input Low voltage, except SDA, SCL		-0.5[11]	$0.2V_{CC}$-0.25	V
V_{IH}	Input High voltage, except X1, RST		$0.2V_{CC}$+0.9	V_{CC}+0.5[11]	V
V_{IH1}	Input High voltage, X1, RST		$0.7V_{CC}$	V_{CC}+0.5[11]	V
	SDA, SCL:				
V_{IL1}	Input Low voltage		-0.5[11]	$0.3v_{CC}$	V
V_{IH2}	Input High voltage		$0.7V_{CC}$	V_{CC}+0.5[11]	V
Outputs					
V_{OL}	Output Low voltage, Ports 1, 3, 0.3, and 0.4 (PWM disabled)	I_{OL} = 1.6mA		0.45	V
V_{OL1}	Output Low voltage, Port 0.2	I_{OL} = 3.2mA		0.45	V
V_{OH}	Output High voltage, Ports 1, 3, 0.3, and 0.4 (PWM disabled)	I_{OH} = -60µA	2.4		V
		I_{OH} = -25µA	$0.75V_{CC}$		V
		I_{OH} = -10µA	$0.9V_{CC}$		V
V_{OH2}	Output High voltage, 0.4 (PWM enabled)	I_{OH} = -400µA	2.4		V
		I_{OH} = -40µA	$0.9V_{CC}$		V
	Port 0.0 and 0.1 (I^2C) - Drivers	I_{OL} = 3.2mA			
V_{OL2}	Output low voltage	(over V_{CC} range)		0.45	V
	Driver, receiver combined:				
C	Capacitance[10]			10	pF

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
Outputs (Continued)					
I_{IL} I_{TL} I_{LI}	Logical 0 input current, Ports 1, 3, 0.3, and 0.4 (PWM disabled) Logical 1 to 0 transition current, Ports 1, 3, 0.3 and 0.4 Input leakage current, Port 0.0, 0.1 and 0.2	V_{IN} = 0.45V V_{IN} = 2V 0.45 < V_{IN} < V_{CC}	 -10	-50 -650 10	µA µA µA
R_{RST}	Reset pull-down resistor		25	175	kΩ
C_{IO}	Pin capacitance[11]	Test freq = 1MHz, T_A - 25°C		10	pF
I_{PD}	Power-down current[4]	V_{CC} - 2 to 5.5V		50	µA
V_{PP}	V_{PP} program voltage	V_{SS} = 0V V_{CC} = 5V±10% T_A - 21°C-27°C	12.5	13.0	V
I_{PP}	Program current	V_{PP} - 13.0V		10	mA
Analog inputs (A/D guaranteed only with quartz window covered).					
AV_{CC}	Analog supply voltage[9]	AV_{CC} = V_{CC}±0.2V	4.5	5.5	V
I_{CC}	Supply current (see Figure 3)				
AV_{IN}	Analog input voltage	AV_{CC} = 5.12V	AV_{SS}-0.2	AV_{CC}+0.2	V
C_{IA}	Analog input capacitance[10]			15	pF
t_{ADS}	Sampling time[10]			$8t_{CY}$	s
t_{ADS}	Conversion time[10]			$40t_{CY}$	s
R	Resolution			8	bits
D_{NL}	Differential Non-Linearity10			±1	LSB
OS_e	Zero scale offset			±1	LSB
G_e	Full scale gain error			0.4	%
M_{CTC}	Channel to channel matching[11]			±1	LSB
C_t	Crosstalk[9,10]	0-100kHz		-60	dB

AC ELECTRICAL CHARACTERISTICS

-55°C ≤ T_A ≤ 125°C, 4.0 ≤ V_{CC} ≤ 6.0V_{SS} -0V[3]

SYMBOL	PARAMETER	12MHz		VARIABLE CLOCK		UNIT
		MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	Oscillator frequency			3.5 3.5	12 16	MHz MHz
External clock (Figure 1)						
t_{CHCX}	High time[11]	20		20		ns
t_{CLCX}	Low time[11]	20		20		ns
t_{CLCH}	Rise time[11]		20		20	ns
t_{CHCL}	Fall time[11]		20		20	ns

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying voltages greater than the rated maxima.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages with respect to V^{SS} unless otherwise noted.
4. Power-down I_{CC} is measured with all output pins disconnected; Port 0 = V_{CC}; X2, X1 n.c.; RST =V_{SS}.

Notes continued on following page

NOTES: (Continued)
5. I_{CC} is measured with all output pins disconnected; X1 driven with t_{CLCH}, t_{CHCL} = 5ns, $V_{IL} = V_{SS} + 0.5V$, $V_{IH} = V_{CC} - 0.5V$; X2 n.c.; RST = Port 0 = V_{CC}. I_{CC} will be slightly higher if a crystal oscillator is used.
6. Idle I_{CC} is measured with all output pins disconnected; X1 driven with t_{CLCH}, t_{CHCL} = 5ns, $V_{IL} = V_{SS} + 0.5V$, $V_{IH} = V_{CC} - 0.5V$; X2 n.c; Port 0 = V_{CC}; RST = V_{SS}.
7. Load capacitance for ports = 80pF.
8. The resistor ladder network is not disconnected in the power down or idle modes. Thus, to conserve power the user may remove AV_{CC}.
9. If the A/D function is not required, or if the A/D function is only needed periodically, AV_{CC} may be removed without affecting the operating of the digital circuitry. Contents of ADCON and ADAT are not guaranteed to be valid. Digital inputs on P1.0-P1.4 will not function normally.
10. Tested initially, and after any design changes that affects the parameters.
11. Guaranteed, but not tested.

A/D CONVERTER PARAMETER DEFINITIONS

The following definitions are included to clarify some specifications given and do not represent a complete set of A/D parameter definitions.

Absolute Accuracy Error

Absolute accuracy error of a given output is the difference between the theoretical analog input voltage to produce a given output and the actual analog input voltage required to produce the same code. Since the same output code is produced by a band of input voltages, the "required input voltage" is defined as the midpoint of the band of input voltage that will produce that code. Absolute accuracy error not specified with a code is the maximum over all codes.

Nonlinearity

If a straight line is drawn between the end points of the actual converter characteristics such that zero offset and full scale errors are removed, then non-linearity is the maximum deviation of the code transitions of the actual characteristics from that of the straight line so constructed. This is also referred to as relative accuracy and also integral non-linearity.

Differential Non-Linearity

Differential non-linearity is the maximum difference between the actual and ideal code widths of the converter. The code widths are the differences expressed in LSB between the code transition points, as the input voltage is varied through the range for the complete set of codes.

Gain Error

Gain error is the deviation between the ideal and actual analog input voltage required to cause the final code transition to a full-scale output code after the offset error has been removed. This may sometimes be referred to as full scale error.

Offset Error

Offset error is the difference between the actual input voltage that causes the first code transition and the ideal value to cause the first code transition. This ideal value is 1/2 LSB above V_{ref-}.

Channel to Channel Matching

Channel to channel matching is the maximum difference between the corresponding code transitions of the actual characteristics taken from different channels under the same temperature, voltage and frequency conditions.

Crosstalk

Crosstalk is the measured level of a signal at the output of the converter resulting from a signal applied to one deselected channel.

Total Error

Maximum deviation of any step point from a line connecting the ideal first transition point to the ideal last transition point.

Relative Accuracy

Relative accuracy error is the deviation of the ADC's actual code transition points from the ideal code transition points on a straight line which connects the ideal first code transition point and the final code transition point, after nulling offset error and gain error. It is generally expressed in LSBs or in percent of FSR.

AC SYMBOL DESIGNATIONS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

C - Clock
D - Input data
H - Logic level high
L - Logic level low
Q - Output data
T - Time
V - Valid
X - No longer a valid logic level
Z - Float

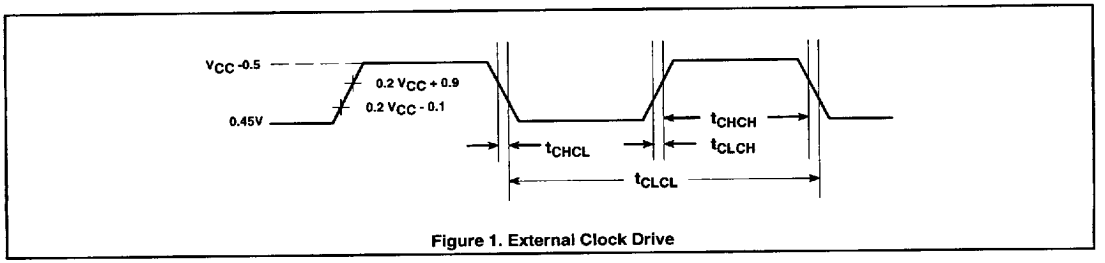


Figure 1. External Clock Drive

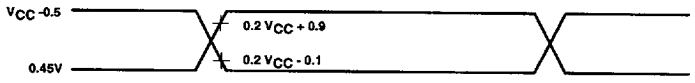


Figure 2. AC Testing Input/Output

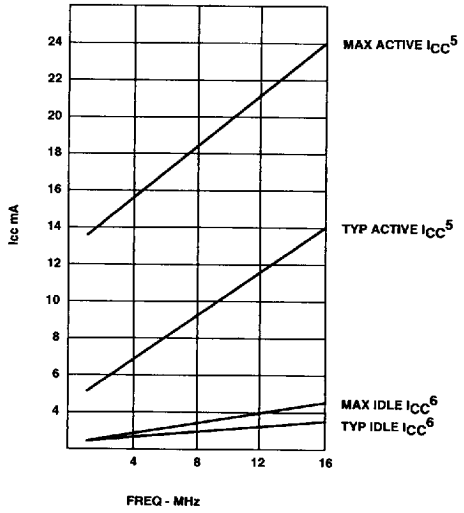


Figure 3. I_{CC} vs. FREQ.
Maximum I_{CC} values taken at V_{CC} = 5.5V and worst case temperature. Typical I_{CC} values taken at V_{CC} = 5.0V and 25°C. Notes 5 and 6 refer to AC Electrical Characteristics.

PROGRAMMING CONSIDERATIONS

EPROM Characteristics

The 87C752 is programmed by using a modified Quick-Pulse Programming algorithm similar to that used for devices such as the 87C451 and 87C51. It differs from these devices in that a serial data stream is used to place the 87C752 in the programming mode.

Figure 4 shows a block diagram of the programming configuration for the 87C752. Port pin P0.2 is used as the programming voltage supply input (V_{PP} signal). Port pin P0.1 is used as the program (PCM/) signal. This pin is used for the 25 programming pulses.

Port 3 is used as the address input for the byte to be programmed and accepts both the high and low components of the eleven bit address. Multiplexing of these address components is performed using the ASEL input. The user should drive the ASEL input high and then drive Port 3 with the high order bits of the address. ASEL should remain high for at least 13 clock cycles ASEL may then be driven low which latches the high order bits of the address internally. The high address should remain on Port 3 for at least two clock cycles after ASEL is driven low. Port 3 may then be driven with the low byte of the address. The low address will be internally stable 13 clock cycles later. The address will remain stable provided that the low byte placed on Port 3 is held stable and ASEL is kept low.
Note: ASEL needs to be pulsed high only to change the high byte of the address.

Port 1 is used as a bidirectional data bus during programming and verify operations. During programming mode, it accepts the byte to be programmed. During verify mode, it provides the contents of the EPROM location specified by the address which has been supplied to Port 3.

The XTAL1 pin is the oscillator input and receives the master system clock. This clock should be between 1.2 and 6MHz.

The RESET pin is used to accept the serial data stream that places the 87C752 into various programming modes. This pattern consists of a 10-bit code with the LSB sent first. Each bit is synchronized to the clock input, X1.

Programming Operation

Figures 5 and 6 show the timing diagrams for the program/verify cycle. RESET should initially be held high for at least two machine cycles. P0.1 (PGM/) and P0.2 (V_{PP}) will be at V_{OH} as a result of the RESET operation. At this point, these pins function as normal quasi-bidirectional I/O ports and the programming equipment may pull these lines low. However, prior to sending the 10-bit code on the RESET pin, the programming equipment should drive these pins high (V_{IH}). The RESET pin may now be used as the serial data input for the data stream which places the 87C752 in the programming mode. Data bits are sampled during the clock high time and thus should only change during the time that the clock is low. Following transmission of the last data bit, the RESET pin should be held low.

Next the address information for the location to be programmed is placed on Port 3 and ASEL is used to perform the address multiplexing, as previously described. At this time, Port 1 functions as an output.

A high voltage V_{PP} level is then applied to the V_{PP} input (P0.2). (This sets Port 1 as an input port.) The data to be programmed into the EPROM array is then placed on Port 1. This is followed by a series of programming pulses applied to the PGM/ pin (P0.1). These pulses are created by driving P0.1 low and then high. This pulse is repeated until a total of twenty-five programming pulses have occurred. At the conclusion of the last pulse, the PGM/ signal should remain high.

The V_{PP} signal may now be driven to the V_{OH} level, placing the 87C752 in the verify mode. (Port 1 is now used as an output port.) After four machine cycles (48 clock periods), the contents of the addressed location in the EPROM array will appear on Port 1.

The next programming cycle may now be initiated by placing the address information at the inputs of the multiplexed buffers, driving the V_{PP} pin to the V_{PP} voltage level, providing the byte to be programmed to Port 1 and issuing the 25 programming pulses on the PGM/ pin, bringing V_{PP} back down to the V_{CC} level and verifying the byte.

Programming Modes

The 87C752 has four programming features incorporated within its EPROM array. These include the USER EPROM for storage of the application's code, a 16-byte encryption key array and two security bits. Programming and verification of the these four elements are selected by a combination of the serial data stream applied to the RESET pin and the voltage levels applied to port pins P0.1 and P0.2. The various combinations are shown in Table 3.

Encryption Key Table

The 87C752 includes a 16-byte EPROM array that is programmable by the end user. The contents of this array can then be used to encrypt the program memory contents during a program memory verify operation. When a program memory verify operation is performed, the contents of the program memory location is XNOR'ed with one of the bytes in the 16-byte encryption table. The resulting data pattern is then provided to Port 1 as the verify data. The encryption mechanism can be disabled, in essence, by leaving the bytes in the encryption table in their erased state (FFH) since the XNOR product of a bit with a logical one will result in the original bit. The encryption bytes are mapped with the code memory in 16-byte groups. The first byte in code memory will be encrypted with the first byte in the encryption table; the second byte in code memory will be encrypted with the second byte in the encryption table and so forth up to and including the 16th byte. The encryption repeats in 16-byte groups; the 17th byte in code memory will be encrypted with the first byte in the encryption table, and so forth.

Security Bits

Two security bits, security bit 1 and security bit 2, are provided to limit access to the USER EPROM and encryption key arrays. Security bit 1 is the program inhibit bit, and once programmed performs the following functions:

1. Additional programming of the USER EPROM is inhibited.
2. Additional programming of the encryption is inhibited.
3. Verification of the encryption key is inhibited.
4. Verification of the USER EPROM and the security bit levels may still be performed.

(If the encryption key array is being used, the security bit should be programmed by the user to prevent unauthorized parties from reprogramming the encryption key to all logical zero bits. Such programming would provide data during a verify cycle that is the logical compliment of he USER EPROM contents.)

Security bit 2, the verify inhibit bit, prevents verification of both the USER EPROM array and the encryption key arrays. The security bit levels may still be verified.

Programming and Verifying Security Bits

Security bits are programmed employing the same techniques used to program the USER EPROM and KEY arrays using serial data streams and logic levels on port pins indicated in Table 3. When programming either security bit, it is not necessary to provide address or data information to the 87C752 on Ports 1 and 3.

Verification occurs in a similar manner using the RESET serial stream shown in Table 3. Port 3 is not required to be driven and the results of the verify operation will appear on ports 1.6 and 1.7.

Port 1.7 contains the security bit 1 data and is a logical one if programmed and logical zero if erased. Likewise, P1.6 contains the security bit 2 data and is a logical one if programmed and a logical zero if erased.

Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. **For this and secondary effects, it is recommended that an opaque label be placed over the window.** For elevated temperature or environments where solvents are being used, use Kapton tape Flourless part number 2345-5 or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose at least 15W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000μW/cm^2 rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

Table 3. Implementing Program/Verify Modes

Operation	Serial Code	P0.1 (PGM/)	P0.2 (V_{PP})
Program user EPROM	296H	-*	V_{PP}
Verify user EPROM	296H	V_{IH}	V_{IH}
Program key EPROM	292H	-*	V_{PP}
Verify key EPROM	292H	V_{IH}	V_{IH}
Program security bit 1	29AH	-*	V_{PP}
Program security bit 2	298H	-*	V_{PP}
Verify security bits	29AH	V_{IH}	V_{IH}

NOTE:
* Pulsed from V_{IH} to V_{IL} and returned to V_{IH}.

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

T_A = 21°C to +27°C, V_{CC} = 5V±10, V_{SS} = 0V

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
$1/t_{CLCL}$	Oscillator/clock frequency	1.2	6	MHz
t_{AVGL}*	Address setup to P0.1 (PROG-) Low	10µs + 24t_{CLCL}		
t_{GHAX}	Address hold after P0.1 (PROG-) High	48t_{CLCL}		
t_{DVGL}	Data setup to P0.1 (PROG-) Low	38t_{CLCL}		
t_{GHDX}	Data hold after P0.1 (PROG-) High	36t_{CLCL}		
t_{SHGL}	V_{PP} setup to P0.1 (PROG-) Low	10		µs
t_{GHSL}	V_{PP} hold after P0.1 (PROG-)	10		µs
t_{GLGH}	P0.1 (PROG-) width	90	110	µs
t_{AVQV}**	V_{PP} Low (V_{CC}) to data valid		48t_{CLCL}	
t_{GHGL}	P0.1 (PROG-) High to P0.1 (PROG-) Low	10		µs
t_{SYNL}	P0.0 (sync pulse) Low	4t_{CLCL}		
t_{SYNH}	P0.0 (sync pulse) High	8t_{CLCL}		
t_{MASEL}	ASEL High time	13t_{CLCL}		
t_{MAHLD}	Address hold time	2t_{CLCL}		
t_{HASET}	Address setup to ASEL	13t_{CLCL}		
t_{ADSTA}	Low address to address stable	13t_{CLCL}		

NOTES:
* Address should be valid at least 24 t_{CLCL} before rising edge of P0.2 (V_{PP}).
** For a pure verify mode, i.e., no program mode in between, t_{AVQV} is 14t_{CLCL} maximum.

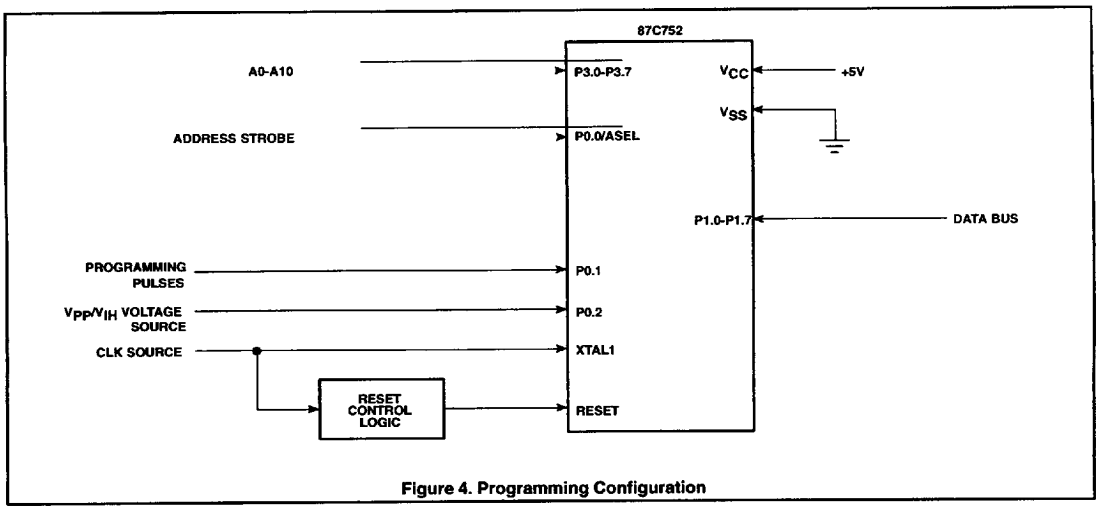


Figure 4. Programming Configuration

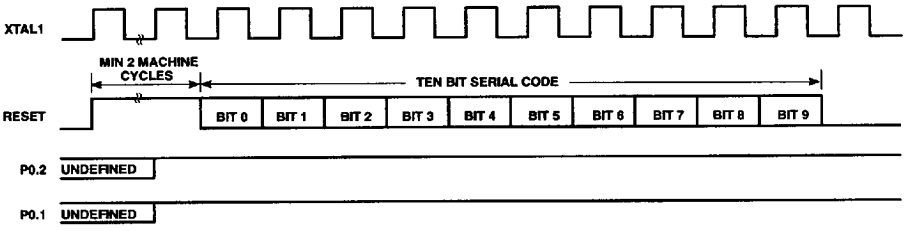


Figure 5. Entry Into Program/Verify Modes

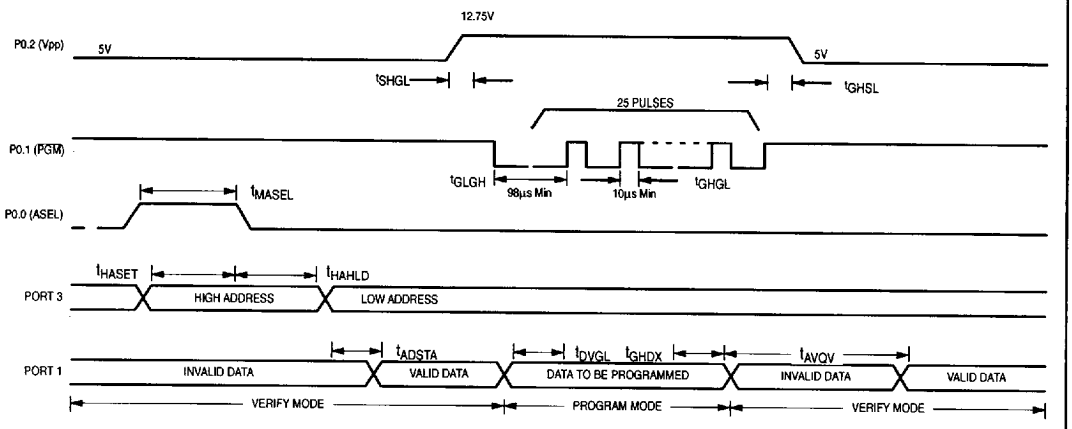


Figure 6. Program/Verify Cycle