NEC

MOS INTEGRATED CIRCUIT

μPD784025,784026

16-/8-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD784026 is 78K/II+ subseries product. The μPD784026 is approximately twice as fast as the μPD78324 subseries, and offers significant improvements over μPD78324 subseries functions, such as 16-bit timer counters, greater on-chip memory capacity, and an enhanced instruction set.

Functions are described in detail in the following user's manuals, which should be read when carrying out design work.

μPD784026 Series User's Manual (Preliminary) Hardware Volume : IEU-850
78K/IV Series User's Manual (Preliminary) Instruction Volume : IEU-844

FEATURES

- 78K/II+ series, 78K/IV series
- The μPD78234 subseries pin compatible
- High-speed instruction execution : 160 ns (at fxx = 25 MHz operation)
- I/O pin : 64 pins
- Timer/counter : 16 bits × 4 channels
- Serial interface : 3 channels
  UART/IOE : 2, CSI : 1
- PWM output : 2 outputs
- Low voltage operation : V_{DD} = 2.7 to 6.0 V
- Standby function ★
  HALT/STOP/IDLE mode
- Clock division function ★
- Watchdog timer: 1 channel ★
- Clock output function ★
  f_{CLK}, $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$ and $f_{CLK}/16$ can be selected.
- A/D converter : Analog 8 inputs
- D/A converter : Analog 2 outputs

APPLICATION FIELD ★

PPC, LBP, AF cameras required for high-speed analog data operation

ORDERING INFORMATION

Ordering Code	Package	On-Chip ROM	On-Chip RAM
μPD784025GC-xxx-3B9	80-pin plastic QFP (□14 mm)	48K	2048
μPD784026GC-xxx-3B9	80-pin plastic QFP (□14 mm)	64K	2048

Remarks "xxx" means the ROM code.

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

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Date Published April 1994 P
Printed in Japan

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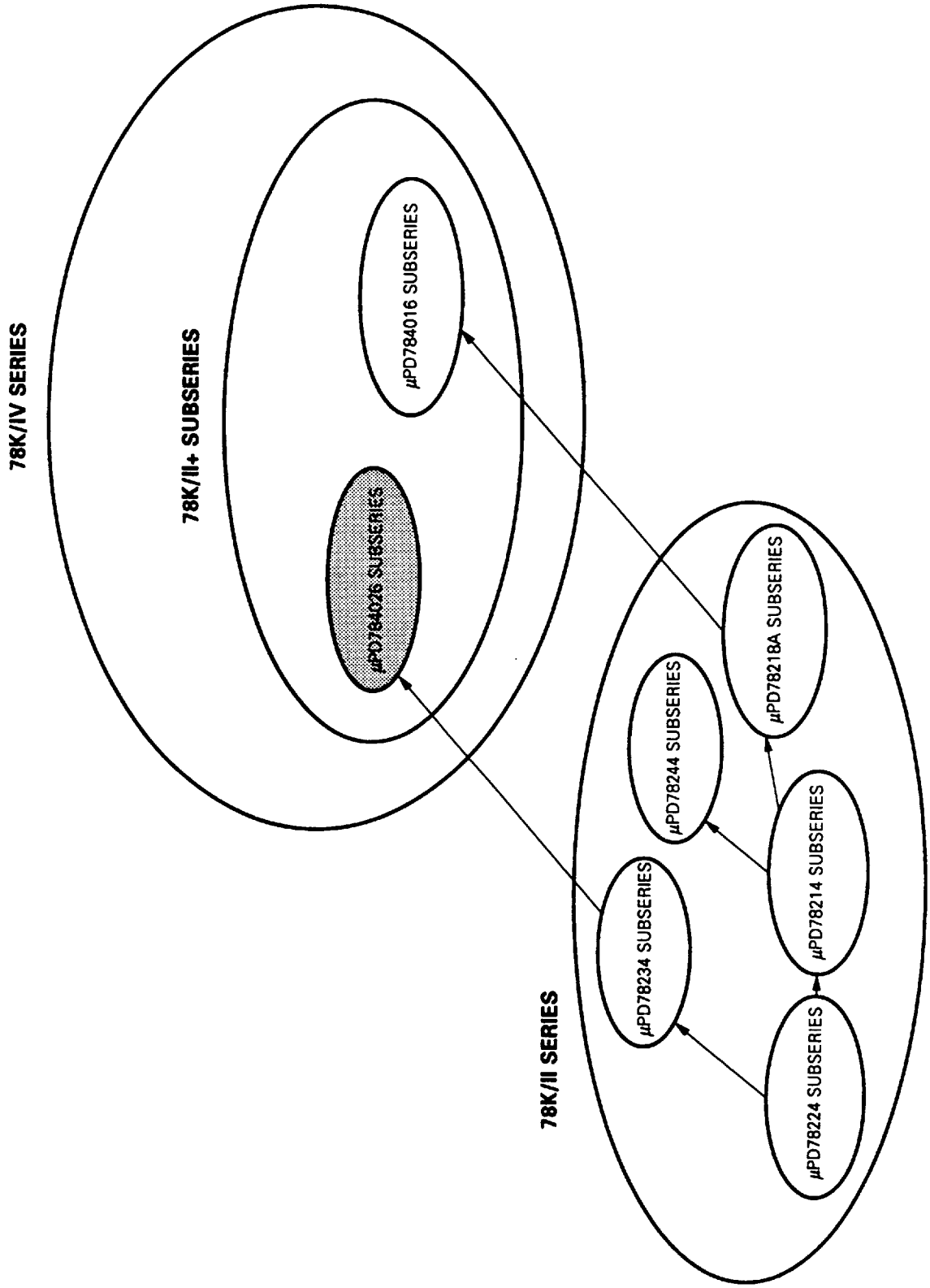
78K/IV SERIES PRODUCTS DEVELOPMENT DIAGRAM

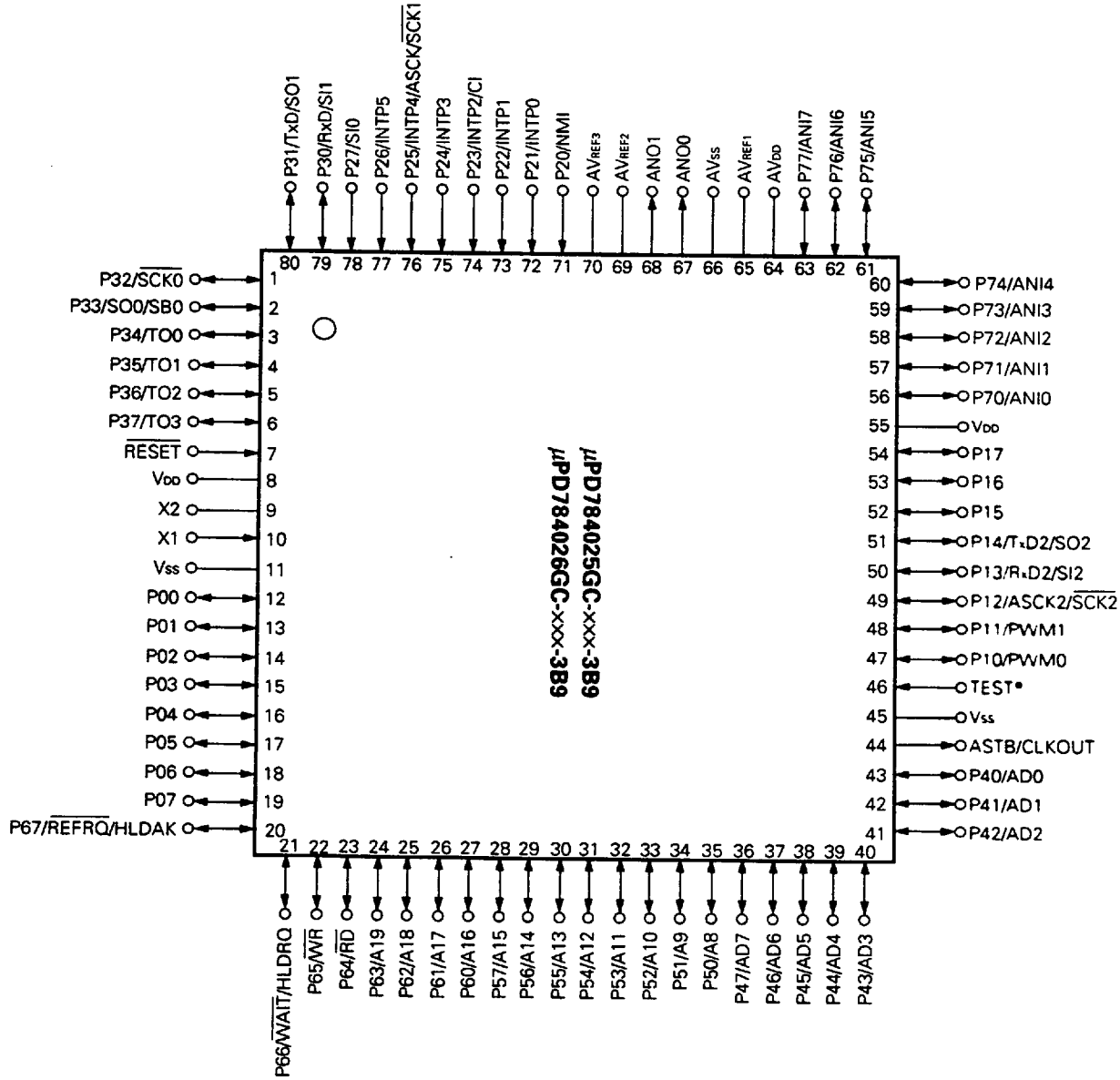


FUNCTION LIST

Item		Function
Number of basic instructions (mnemonics)		113
General registers		8 bits × 16 × 8 banks or 16 bits × 8 × 8 banks (memory mapping)
Minimum instruction execution time		160 ns/320 ns/640 ns/1280 ns (at 25 MHz operation)
Operating voltage range		2.7 to 6.0 V ★
On-chip Memory capacity	ROM	64K bytes (μPD784026), 48K bytes (μPD784025)
	RAM	2048 bytes
Memory space	Program/ data	1M bytes in all ★
I/O pins		Total : 64 — Input port : 8, Input/output port : 56 } On-chip pull-up resistor (pull-up specification by software) : 54 inputs; LED drive possible : 24 outputs; Transistor drive possible : 8 outputs
Real-time output port		4 bits × 2 or 8 bits × 1 ★
Timer/counters		16-bit timer/counter 0 { Timer register × 1, Capture register × 1, Compare register × 2 } Pulse output enable (Toggle output, PWM/PPG output, One-shot pulse output)
		16-bit timer/counter 1 { Timer register × 1, Capture register × 1, Capture/compare register × 1, Compare register × 1 } Pulse output enable (Real-time output : 4 bits × 2)
		16-bits timer/counter 2 { Timer register × 1, Capture register × 1, Capture/compare register × 1, Compare register × 1 } Pulse output enable (Toggle output, PWM/PPG output)
		16-bits timer/counter 3 { Timer register × 1, Compare register × 1 }
PWM output function		12-bit resolution × 2 channels
Serial interface		UART/IOE (3-wire serial I/O) : 2 channels (baud rate generator incorporated) CSI (3-wire serial I/O, SBI) : 1 channel
A/D converter		8-bit resolution × 8 channels
D/A converter		8-bit resolution × 2 channels
Clock output function		f_{CLK}, $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, and $f_{CLK}/16$ can be selected (can also be used as 1-bit output port.) ★
Watchdog timer		1 channel
Standby function		HALT/STOP/IDLE mode ★
Interrupts		23 sources (external 7 (sampling clock variable input : 1), internal 16) + BRK instruction Priority order of 4 levels (programmable) 3 types of servicing (vectored interrupt, macro service, context switching)
Package		80-pin plastic QFP (□ 14 mm)

PIN CONFIGURATION (TOP VIEW)

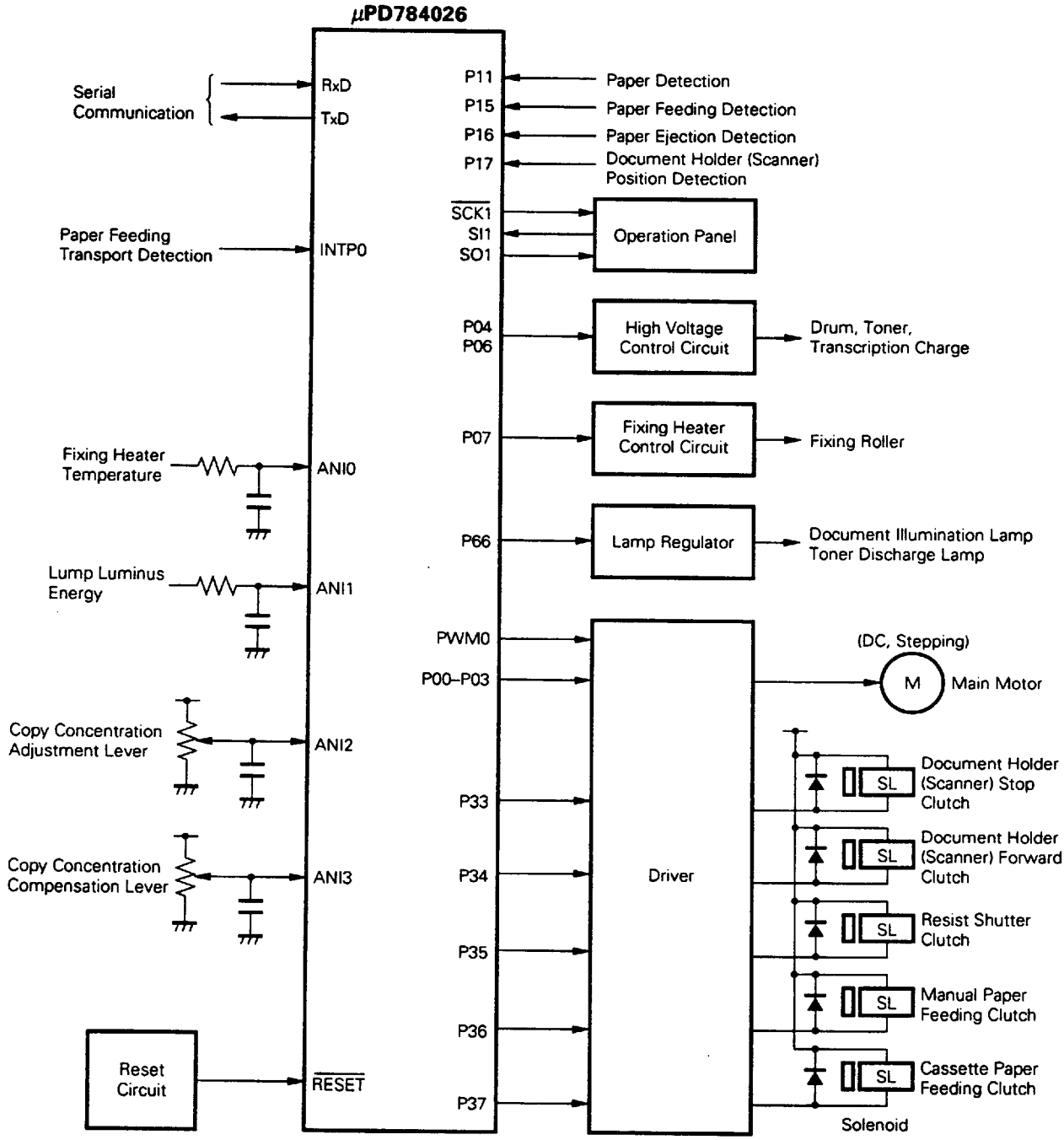
80-Pin Plastic QFP



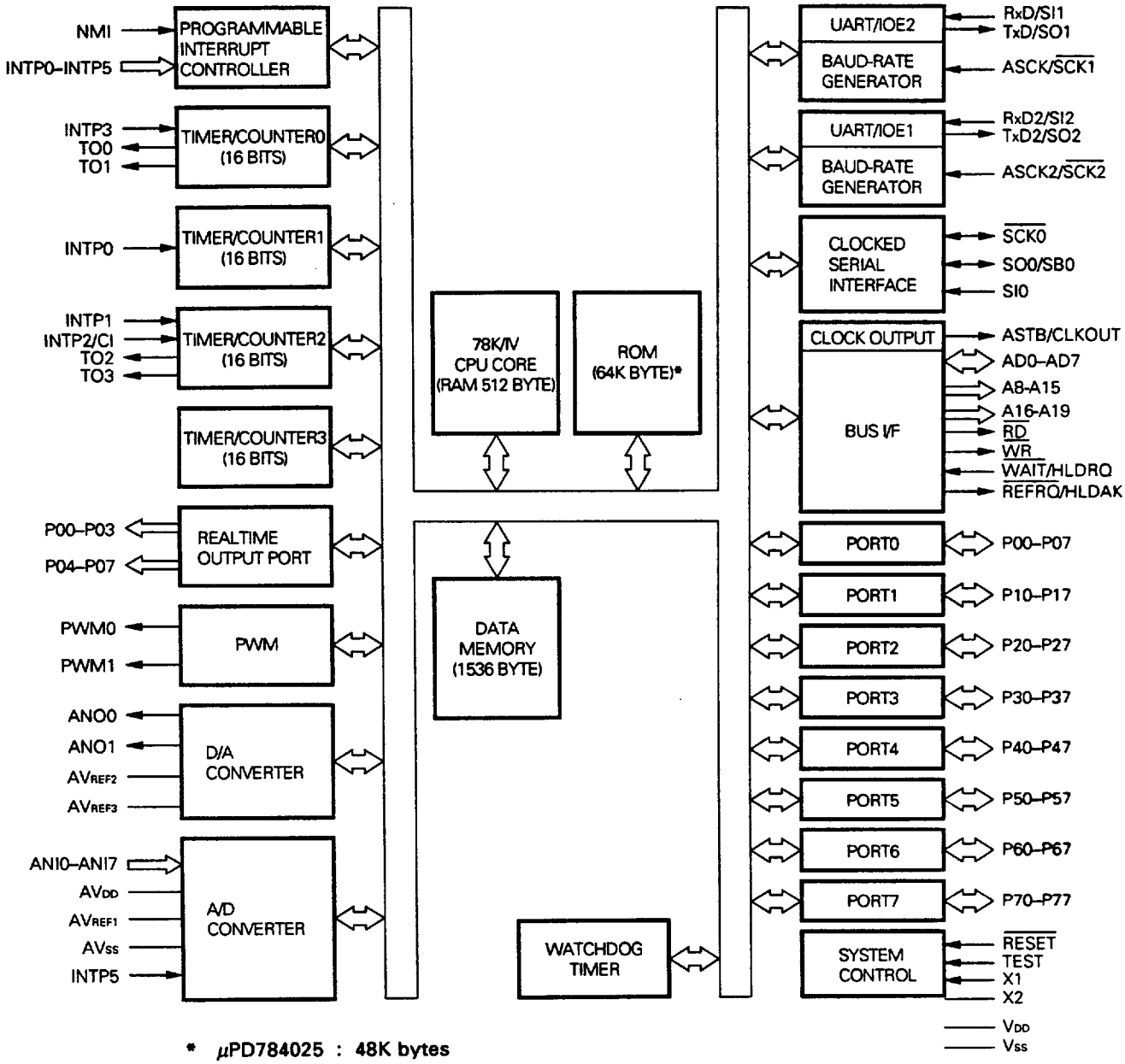
★ * The TEST pin should be connected to Vss directly.

P00 to P07	: Port 0	A8 to A19	: Address Bus
P10 to P17	: Port 1	$\overline{RD}$	: Read Strobe
P20 to P27	: Port 2	$\overline{WR}$	: Write Strobe
P30 to P37	: Port 3	$\overline{WAIT}$	: Wait
P40 to P47	: Port 4	HLDRQ	: Hold Request
P50 to P57	: Port 5	HLDAK	: Hold Acknowledge
P60 to P67	: Port 6	CLKOUT	: Clock Out
P70 to P77	: Port 7	ASTB	: Address Strobe
TO0 to TO3	: Timer Output	$\overline{REFRQ}$	: Refresh Request
CI	: Clock Input	$\overline{RESET}$	: Reset
RxD, RxD2	: Receive Data	X1, X2	: Crystal
TxD, TxD2	: Transmit Data	ANI0 to ANI7	: Analog Input
$\overline{SCK0}$ to $\overline{SCK2}$	: Serial Clock	ANO0, ANO1	: Analog Output
ASCK, ASCK2	: Asynchronous Serial Clock	AV_{REF1} to AV_{REF3}	: Reference Voltage
SB0	: Serial Bus	AV_{DD}	: Analog Power Supply
SI0 to SI2	: Serial Input	AV_{SS}	: Analog Ground
SO0 to SO2	: Serial Output	V_{DD}	: Power Supply
PWM0, PWM1	: Pulse Width Modulation Output	V_{SS}	: Ground
NMI	: Non-maskable Interrupt	TEST	: Test ★
INTP0 to INTP5	: Interrupt From Peripherals		
AD0 to AD7	: Address/Data Bus		

SYSTEM CONFIGURATION EXAMPLE (PPC)



INTERNAL BLOCK DIAGRAM ★



* μPD784025 : 48K bytes

CONTENTS

1. DIFFERENCES BETWEEN μPD784021, 784025, 784026 AND 78P4026

The μPD784021, 784025, and 784026 differ in regard to on-chip memory capacity and some port functions.

★ The μPD78P4026 incorporates one-time PROM or EPROM in place of the mask ROM of the μPD784026. Differences are shown in Table 1-1.

Table 1-1 Differences between μPD784021, 784025, 784026, and 78P4026

Item \ Product Name	μPD784021	μPD784025	μPD784026	μPD78P4026
★ On-chip ROM	None	48K bytes (mask ROM)	64K bytes (mask ROM)	64K bytes (one-time PROM or EPROM)
On-chip RAM	2048 bytes			
P40 to P47	Operation as address/data bus only	Switching between general-purpose port and address/data bus by software		
P50 to P57	Operation as address bus only	Switching between general-purpose port and address bus by software in 2-bit units		
P60 to P63	Switching between output-only port and address bus by software in 2-bit units			
P64, P65	Operation as $\overline{RD}$ and $\overline{WR}$ pins only	Operation as $\overline{RD}$ and $\overline{WR}$ pins when local bys interface is used, and as general-purpose port pins when not used		
★ Package	80-pin plastic QFP (□14 mm)			80-pin ceramic WQFN (□14 mm)

2. PIN FUNCTIONS

2.1 PORTS (1/2)

Pin Name	I/O	Dual-Function Pin	Function
P00 to P07	Input/ output	—	Port 0 (P0): Usable as real-time output port (4 bits × 2) Input/output specifiable bit-wise Internal pull-up resistor connection specifiable as a batch by software for input mode pin Transistor direct drive possible
P10	Input/ output	PWM0	Port 1 (P1): Input/output specifiable bit-wise Internal pull-up resistor connection specifiable as a batch by software for input mode pin LED drive capability
P11		PWM1	
P12		ASCK2/$\overline{SCK2}$	
P13		RxD2/SI2	
P14		TxD2/SO2	
P15 to P17		—	
P20	Input	NMI	Port 2 (P2): P20 cannot be used as a general-purpose port. (Non-maskable interrupt) However, input level can be checked in interrupt routine. Internal pull-up resistor connection specifiable by software for P22 thru P27 as 6-bit unit. The P25/INTP4/ASCK/$\overline{SCK1}$ pin operates as $\overline{SCK1}$ output pin by CSIM1 register setting. ★
P21		INTP0	
P22		INTP1	
P23		INTP2/CI	
P24		INTP3	
P25		INTP4/ASCK/$\overline{SCK1}$	
P26		INTP5	
P27		SI0	
P30	Input/ output	RxD/SI1	Port 3 (P3): Input/output specifiable bit-wise Internal pull-up resistor connection specifiable as a batch by software for input mode pin
P31		TxD/SO1	
P32		$\overline{SCK0}$	
P33		SO0/SB0	
P34 to P37		TO0 to TO3	
P40 to P47	Input/ output	AD0 to AD7	Port 4 (P4): Input/output specifiable bit-wise Internal pull-up resistor connection specifiable as a batch by software for input mode pin LED drive capability
P50 to P57	Input/ output	A8 to A15	Port 5 (P5): Input/output specifiable bit-wise Internal pull-up resistor connection specifiable as a batch by software for input mode pin LED drive capability

2.1 PORTS (2/2)

Pin Name	I/O	Dual-Function Pin	Function
P60 to P63	Input/ output	A16 to A19	Port 6 (P6): Input/output specifiable bit-wise Internal pull-up resistor connection specifiable as a batch by software for input mode pin
P64		$\overline{RD}$	
P65		$\overline{WR}$	
P66		$\overline{WAIT}$/HLDRQ	
P67		$\overline{REFRQ}$/HLDAK	
P70 to P77	Input/ output	ANI0 to ANI7	Port 7 (P7): Input/output specifiable bit-wise

2.2 OTHER PORTS (1/2)

Pin Name	I/O	Function		Dual-Function Pin
TO0 to TO3	Output	Timer output		P34 to P37
CI	Input	Count clock input to 16-bit timer/counter 2		P23 /INTP2
RxD	Input	Serial data input (UART0)		P30/SI1
RxD2		Serial data input (UART2)		P13/SI2
TxD	Output	Serial data output (UART0)		P31/SO1
TxD2		Serial data output (UART2)		P14/SO2
ASCK	Input	Baud rate clock input (UART0)		P25/INTP4/$\overline{SCK1}$
ASCK2		Baud rate clock input (UART2)		P12/$\overline{SCK2}$
SB0	Input /output	Serial data input/output (SBI)		P33/SO0
SI0	Input	Serial data input (3-wire serial I/O0)		P27
SI1		Serial data input (3-wire serial I/O1)		P30/RxD ★
SI2		Serial data input (3-wire serial I/O2)		P13/RxD2 ★
SO0	Output	Serial data output (3-wire serial I/O0)		P33/SB0
SO1		Serial data output (3-wire serial I/O1)		P31/TxD ★
SO2		Serial data output (3-wire serial I/O2)		P14/TxD2 ★
$\overline{SCK0}$	Input /output	Serial clock input/output (SBI, 3-wire serial I/O0)		P32
$\overline{SCK1}$		Serial clock input/output (3-wire serial I/O1)		P25/INTP4/ASCK
$\overline{SCK2}$		Serial clock input/output (3-wire serial I/O2)		P12/ASCK2
NMI	Input	External interrupt request	—	P20
INTP0			Count clock input to 16-bit timer/counter1 CR11 or CR12 capture trigger signal	P21
INTP1			Count clock input to 16-bit timer/counter2 CR22 capture trigger signal	P22
INTP2			Count clock input to 16-bit timer/counter2 CR21 capture trigger signal	P23/CI
INTP3			Count clock input to 16-bit timer/counter0 CR02 capture trigger signal	P24
INTP4			—	P25/ASCK0/$\overline{SCK1}$
INTP5			A/D converter conversion start trigger input	P26
AD0 to AD7	Input /output	Time multiplexing address/data bus (external memory connection)		P40 to P47
A8 to A15	Output	Upper address bus (external memory connection)		P50 to P57
A16 to A19	Output	Upper address when extending address (external memory connection)		P60 to P63
$\overline{RD}$	Output	Read strobe into external memory		P64
$\overline{WR}$	Output	Write strobe into external memory		P65
$\overline{WAIT}$	Input	Wait insertion		P66/HLDRQ
$\overline{REFRQ}$	Output	Refresh pulse output into external pseudo-static memory		P67/HLDAK

2.2 OTHER PORTS (2/2)

Pin Name	I/O	Function	Dual-Function Pin
HLDRQ	Input	Bus hold request input	P66/$\overline{WAIT}$
HLDAK	Output	Bus hold response output	P67/$\overline{REFRQ}$
ASTB	Output	Time multiplexing address (A0 to A7) latch timing output (at external memory accessed)	CLKOUT
CLKOUT	Output	Clock output	ASTB
$\overline{RESET}$	Input	Chip reset	—
X1	Input	Crystal connection for system clock oscillation (capability of clock input to X1)	—
X2	—		
ANI0 to ANI7	Input	Analog voltage input for A/D converter	P70 to P77
ANO0, ANO1	Output	Analog voltage output for D/A converter	—
AV_{REF1}	—	Reference voltage apply for A/D converter	—
AV_{REF2}, AV_{REF3}		Reference voltage apply for D/A converter	
AV_{DD}		Positive power supply for A/D converter	
AV_{SS}		GND for A/D converter	
V_{DD}		Positive power supply	
V_{SS}		GND	
★ TEST		Connect to Vss directly. (IC test pin)	

2.3 PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 2-1. For the input/output circuit configuration of each type, see Fig. 2-1.

Table 2-1 Input/Output Circuit Type of Each Pin and Recommended Connection of Unused Pins (1/2)

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection when not Used
P00 to P07	5-A	Input/output	Input : Connected to V_{DD}. Output : Leave open.
P10/PWM0			
P11/PWM1			
P12/ASCK2/$\overline{SCK2}$	8-A		
P13/RxD2/SI2	5-A		
P14/TxD2/SO2			
P15 to P17			
P20/NMI	2	Input	Connected to V_{DD} or V_{SS}.
P21/INTP0			
P22/INTP1	2-A		Connected to V_{DD}.
P23/INTP2/CI			
P24/INTP3			
P25/INTP4/ASCK/$\overline{SCK1}$	8-A	Input/output	Input : Connected to V_{DD}. Output : Leave open.
P26/INTP5	2-A	Input	Connected to V_{DD}.
P27/SI0			
P30/RxD/SI1	5-A	Input/output	Input : Connected to V_{DD}. Output : Leave open.
P31/TxD/SO1			
P32/$\overline{SCK0}$	8-A		
P33/SB0/SO0	10-A		
P34/TO0 to P37/TO3	5-A		
P40/AD0 to P47/AD7			
P50/A8 to P57/A15			
P60/A16 to P63/A19	5-A	Input/output	Input : Connected to V_{DD}. Output : Leave open.
P64/$\overline{RD}$	5-A	Input/output	Input : Connected to V_{DD}. Output : Leave open.
P65/$\overline{WR}$			
P66/$\overline{WAIT}$/HLDRQ			
P67/$\overline{REFRQ}$/HLDAK			
P70/ANI0 to P77/ANI7	20	Input/output	Input : Connected to V_{DD} or V_{SS}. Output : Leave open.
ANO0, ANO1	12	Output	Leave open.
ASTB/CLKOUT	4		

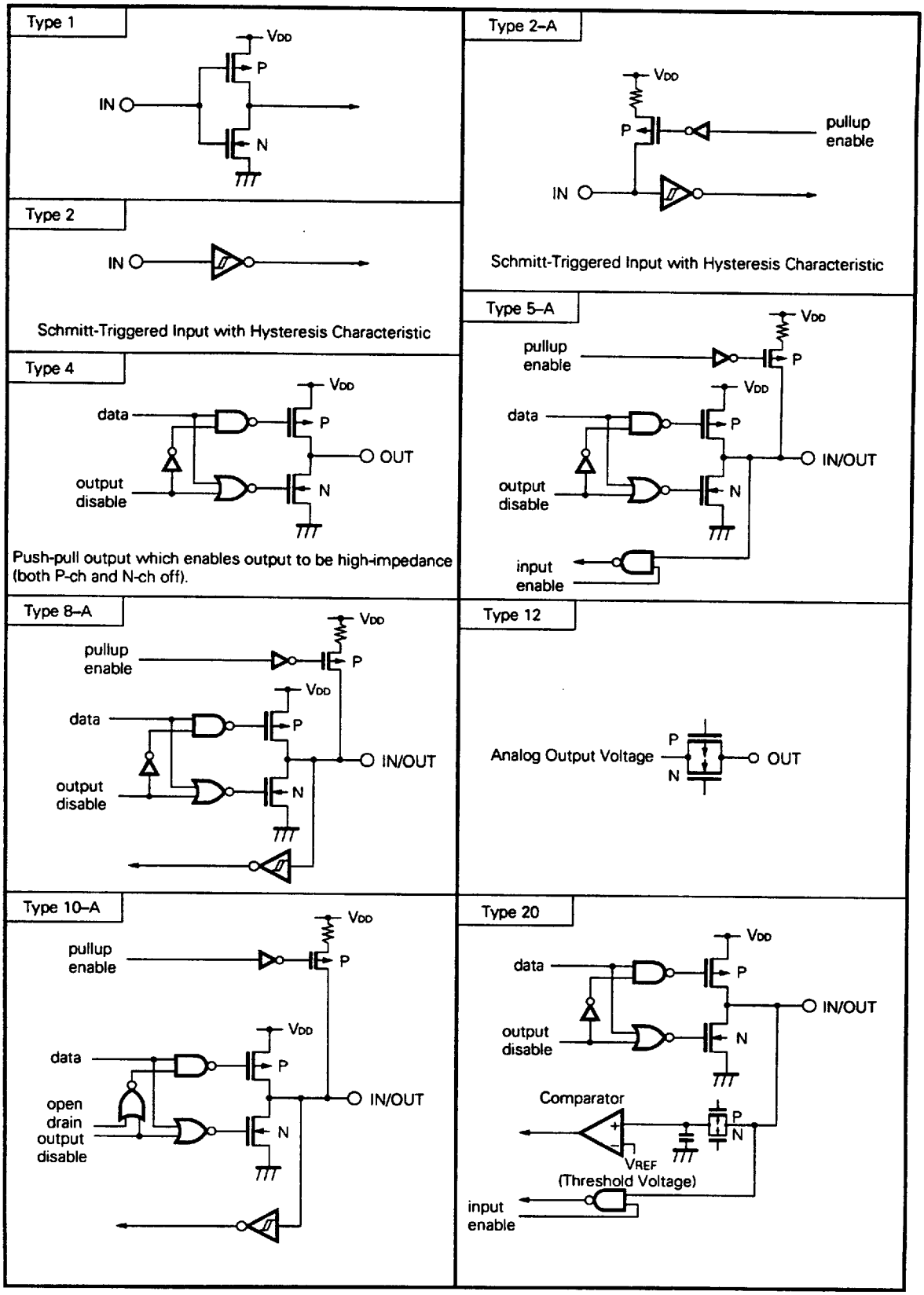
Table 2-1 Input/Output Circuit Type of Each Pin and Recommended Connection of Unused Pins (2/2)

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection when not Used
$\overline{\text{RESET}}$	2	Input	—
★ TEST	1		Connected to Vss directly.
AV_{REF1} to AV_{REF3}	—		Connected to Vss.
AV_{SS}			
AV_{DD}			Connected to V_{DD}

Remarks The type numbers are standardized by 78K series, therefore they are not always consecutive numbers in each product. (Some circuit is not incorporated.)

★ **Note** **With input/output dual-function pins, if input/output mode is indeterminate, the pin should be connected to V_{DD} via a resistor several dozens kΩ (in particular, when the reset input pin exceeds the low level input voltage in a power-on reset, and when input/output is switched by software).**

Fig. 2-1 Pin Input/Output Circuits



3. INTERNAL BLOCK FUNCTION

3.1 CPU REGISTERS

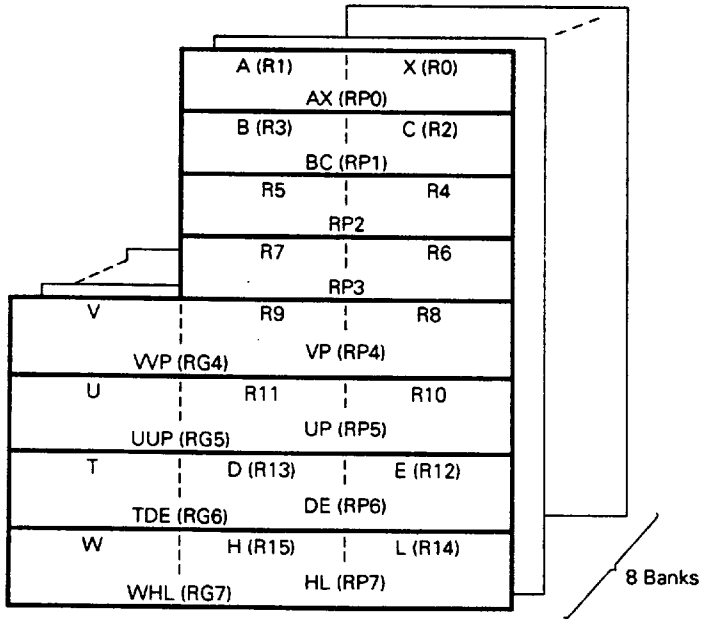
3.1.1 General Registers

There are sixteen 8-bit general registers. In addition, two 8-bit general registers can be combined and used as a 16-bit register. Also, four of the 16-bit registers can be combined with an 8-bit register for address extension, and used as registers for 24-bit address specification.

These register sets are provided in 8 banks, and can be used by switching by means of software or the context switching function.

Except for the V, U, T, and W address extension registers, general registers are mapped in internal RAM.

Fig. 3-1 General Register Format



Items in ( ) are absolute names.

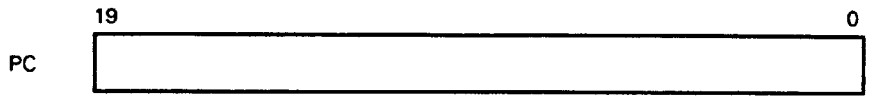
Note **R4, R5, R6, R7, RP2, and RP3 can be used as the X, A, C, B, AX, and BC registers respectively by setting the RSS bit of the PSW to 1, but they should not be used in this way. This function should be used only when utilizing a program for 78K/III series.**

3.1.2 Other CPU Registers

(1) Program counter (PC)

The 20-bit program counter. It is automatically updated by program execution.

Fig. 3-2 Program Counter (PC) Format



(2) Program status word (PSW)

Register which holds various CPU statuses. It is automatically updated by program execution.

Fig. 3-3 Program Status Word (PSW) Format

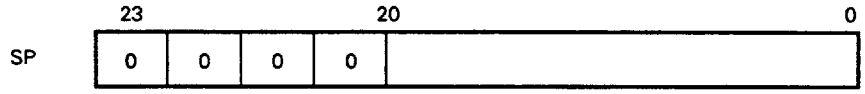
		15	14	13	12	11	10	9	8
PSW	PSWH	UF	RBS2	RBS1	RBS0	—	—	—	—
		7	6	5	4	3	2	1	0
	PSWL	S	Z	RSS*	AC	IE	P/V	0	CY

* This flag is provided for the sake of compatibility with the 78K/III series. It must always be set to 0 except when using 78K/III series software.

(3) Stack pointer (SP)

24-bit pointer which holds the start address of the stack.
0 must be written to the high-order 4 bits.

Fig. 3-4 Stack Pointer (SP) Format



3.2 MEMORY SPACE

It is possible to access a 1M-byte memory space. Internal data area (special function register and internal RAM) mapping differs depending on a LOCATION instruction. The LOCATION instruction should be executed after reset release, and can not be used twice or more.

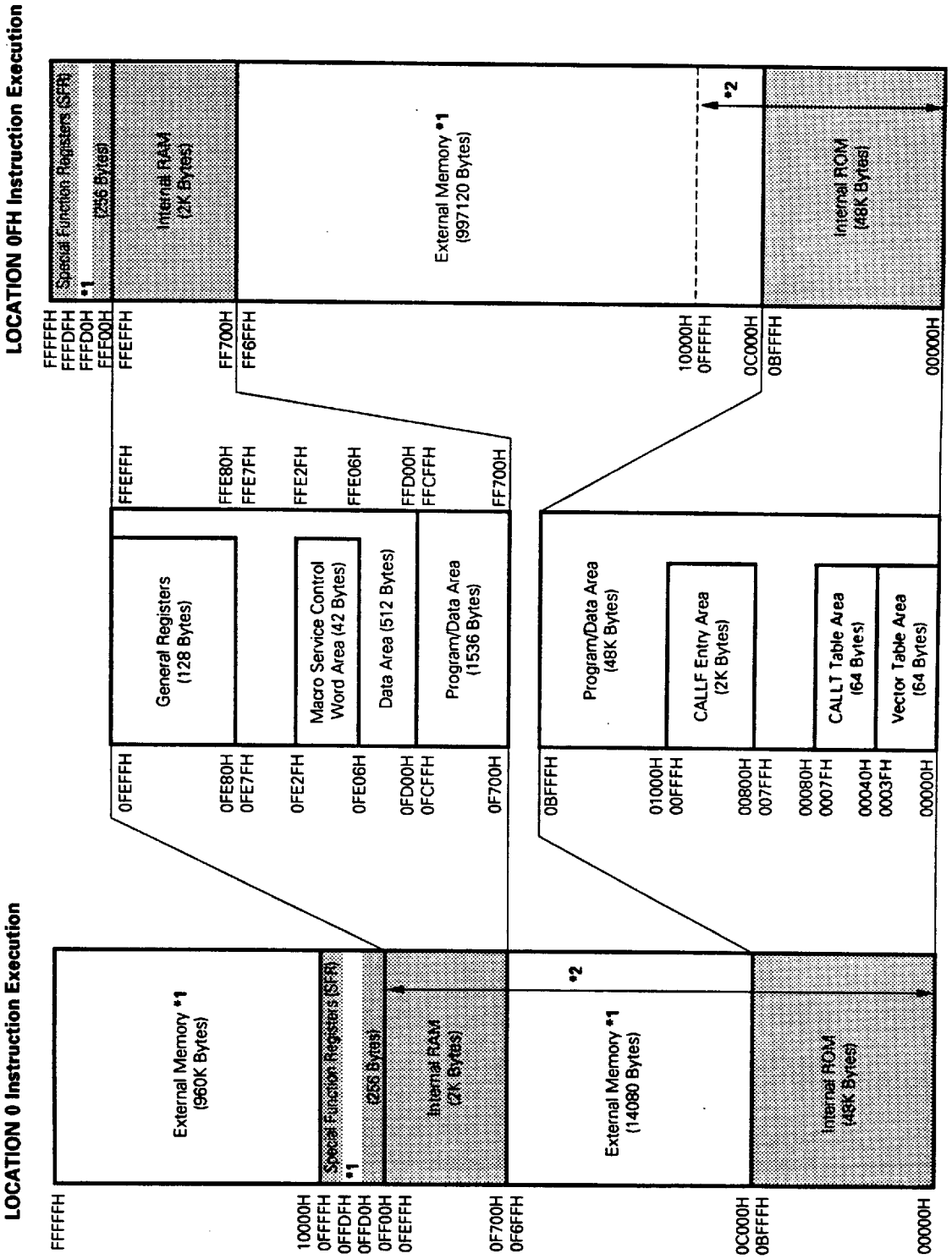
(1) When LOCATION 0 instruction is executed

The internal data area is mapped onto addresses 0F700H to 0FFFFH, and internal ROM is mapped onto addresses
★ 0 to 0F6FFH in the μPD784026, and addresses 0 to 0BFFFH in the μPD784025. In the 64 K-byte ROM which the μPD784026 incorporates, the 2304-byte area which the internal data area overlaps cannot be used after executing the LOCATION 0 instruction. External memory is accessed in the external memory extension mode.

(2) When LOCATION 0FH instruction is executed

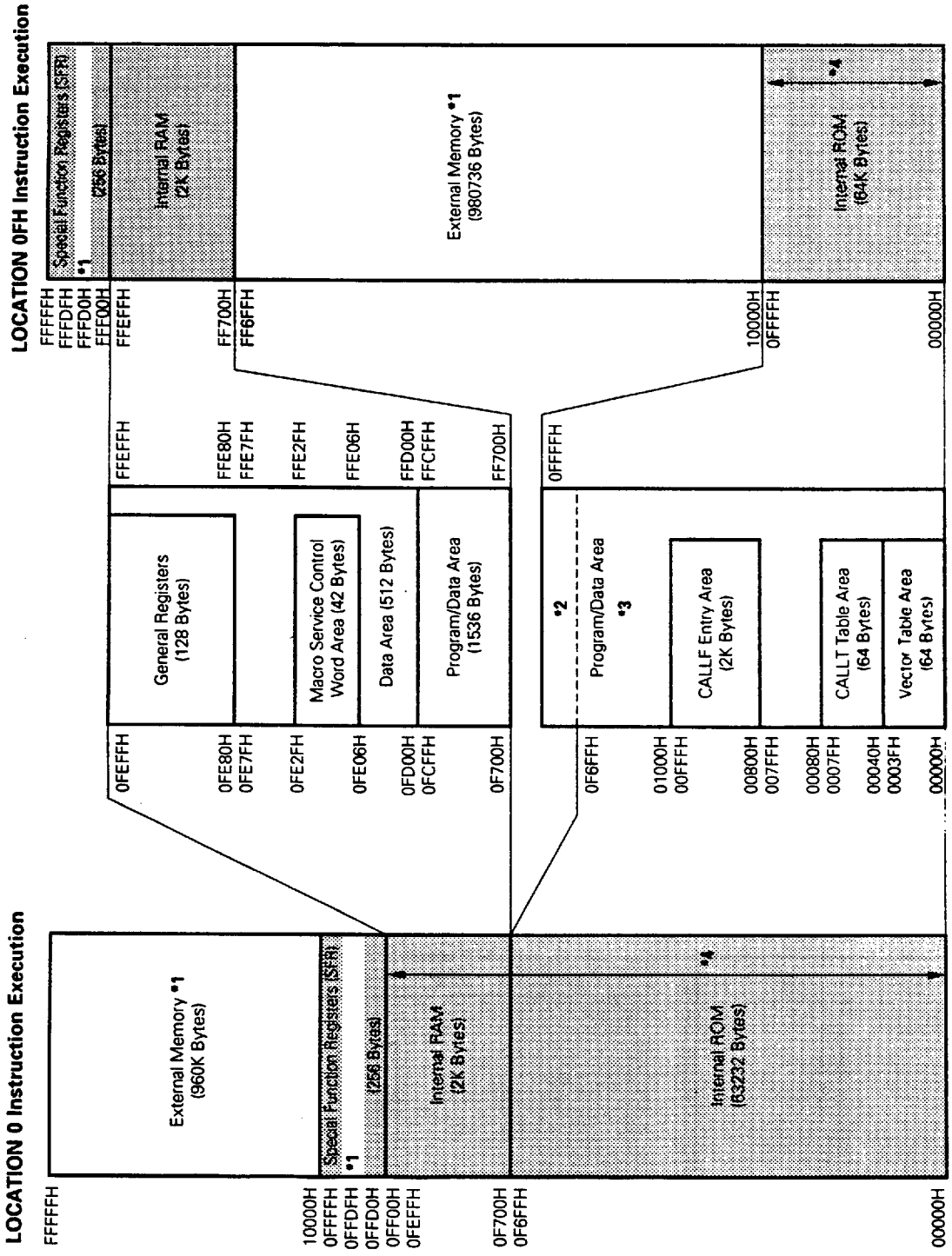
The internal data area is mapped onto addresses FF700H to FFFFFH, and internal ROM is mapped onto addresses 0 to 0FFFFH in the μPD784026, and addresses 0 to 0BFFFH in the μPD784025. External memory is accessed in the external memory extension mode.

Fig. 3-5 μPD784025 Memory Map



* 1. Accessed by external expansion mode.
2. Base area, entry area due to reset or interrupt. However, internal RAM is excluded for reset.

Fig. 3-6 μPD784026 Memory Map



* 1. Accessed by external expansion mode.
2. 2304 bytes of the area can be used as internal ROM only when LOCATION 0FH instruction is executed.
3. LOCATION 0 instruction execution : 63232 bytes, LOCATION 0FH instruction execution : 65536 bytes
4. Base area, entry area due to reset or interrupt. However, internal RAM is excluded for reset.

3.3 PORT

The μPD784025/784026 are equipped with ports as Fig. 3-7, operable for various controls. The function of each port describes Table 3-1. The port 0 to port 6 can be specified to use the internal pull-up resistor by software at input.

Fig. 3-7 Port Configuration

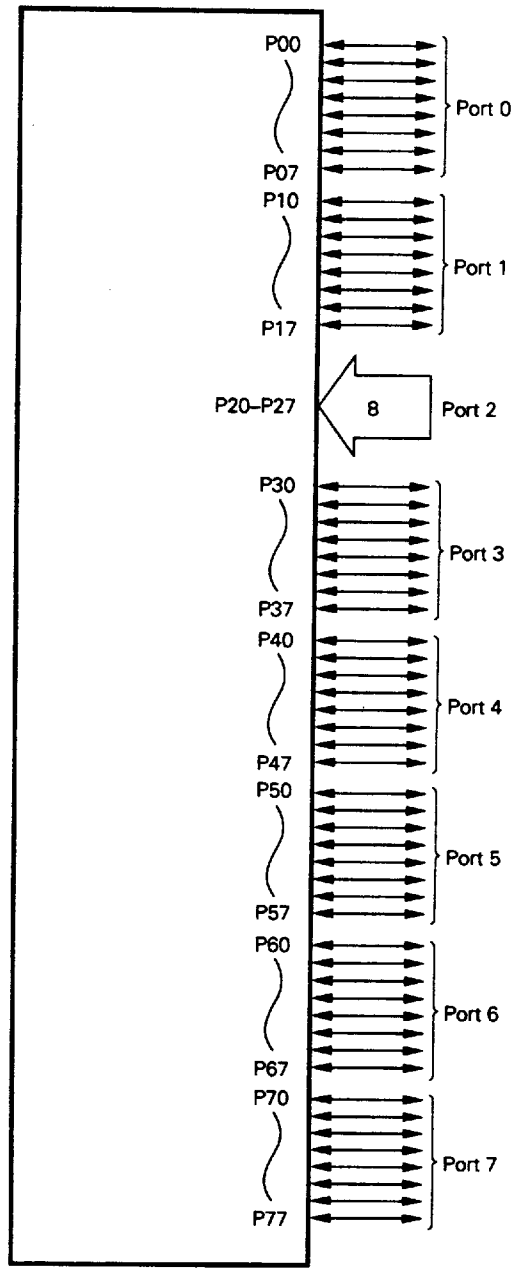


Table 3-1 Port Function

Name	Pin Name	Function	Software Pull-Up Specification
Port 0	P00 to P07	Specifiable as input or output bit-wise. Operable as 4-bit real-time outputs (P00 to P03, P04 to P07). Transistor direct drive possible.	Specify as a batch for input mode pin.
Port 1	P10 to P17	Input or output specifiable bit-wise. LED direct drive possible.	Specify as a batch for input mode pin.
Port 2	P20 to P27	Input port	As 6-bit unit (P22 to P27)
Port 3	P30 to P37	Input or output specifiable bit-wise.	Specify as a batch for input mode pin.
Port 4	P40 to P47	Input or output specifiable as bit-wise. LED direct drive possible.	Specify as a batch for input mode pin.
Port 5	P50 to P57	Input or output specifiable bit-wise. LED direct drive possible.	Specify as a batch for input mode pin.
Port 6	P60 to P67	Input or output specifiable bit-wise.	Specify as a batch for input mode pin.
Port 7	P70 to P77	Input or output specifiable bit-wise.	—

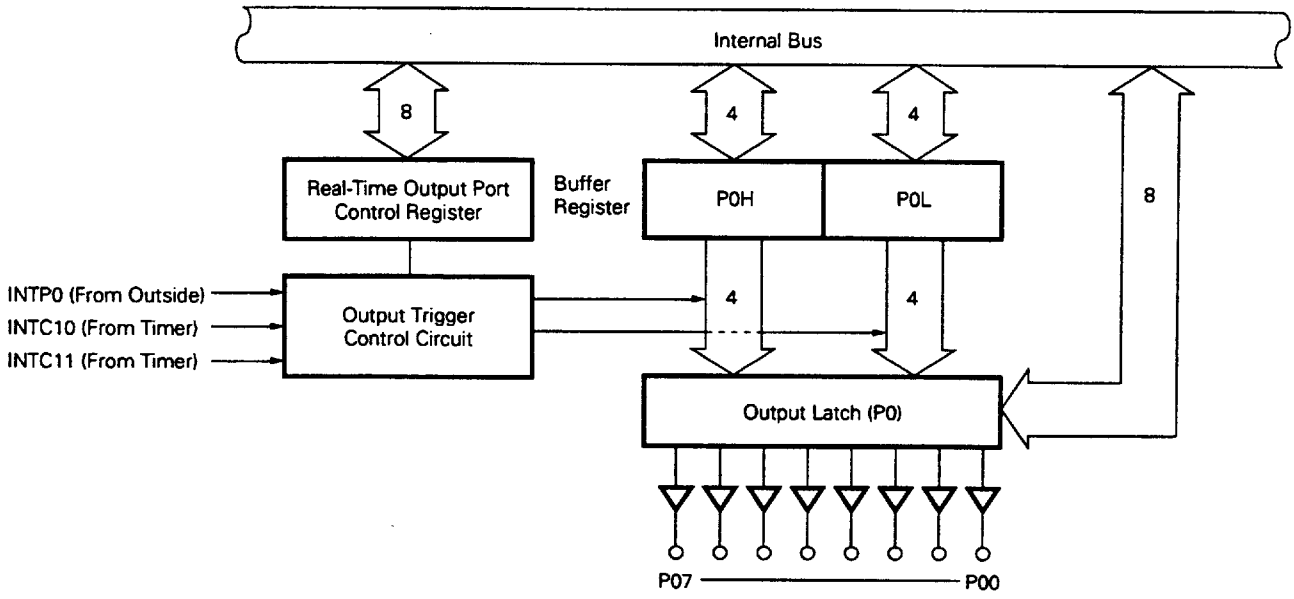
3.4 REAL-TIME OUTPUT PORT

The real-time output port outputs the data stored in the buffer in synchronization with a timer match interrupt or external interrupt. Therefore, a pulse output without jitter can be acquired.

Accordingly, this is suitable for the application (open loop control of a stepping motor etc.) which outputs any pattern at any interval.

As shown in Fig. 3-8, the port 0 and buffer register are the core of the configuration.

Fig. 3-8 Real-Time Output Port Block Diagram



Differences from μPD78234 Subseries

Items \ Series Name	μPD784026 Subseries	μPD78234 Subseries
Output trigger	• INTC10 • INTC11 • INTC10 or INTP0 • INTP0	• INTC10 • INTC11 • INTC10 or INTP0

3.5 TIMER/COUNTER UNIT

The μPD784025/784026 incorporate 4 channels of a 16-bit timer/ counter unit.

Table 3-2 Types and Functions for Timer/Counter

Type & Function \ Unit		16-Bit Timer/ Counter 0	16-Bit Timer/ Counter 1	16-Bit Timer/ Counter 2	16-Bit Timer/ Counter 3
Type	Interval timer	2ch	2ch	2ch	1ch
	External event counter	○	○	○	—
	One-shot timer	—	—	○	—
Function	8-bit operating mode	—	○	○	○
	Timer output	2ch	—	2ch	—
	Toggle output	○	—	○	—
	PWM/PPG output	○	—	○	—
	One-shot pulse output*	○	—	—	—
	Real-time output	—	○	—	—
	Pulse amplitude measurement	1 input	1 input	2 inputs	—
	Number of interrupt requests	2	2	2	1

* One-shot pulse output function is a function to activate the pulse output level by software and to inactivate it by hardware (interrupt request signal).
This function is characteristically different from the 16-bit timer/counter 2 one-shot timer function.

As 7 interrupt requests are supported in total, this functions as the timer of the 7 channels.

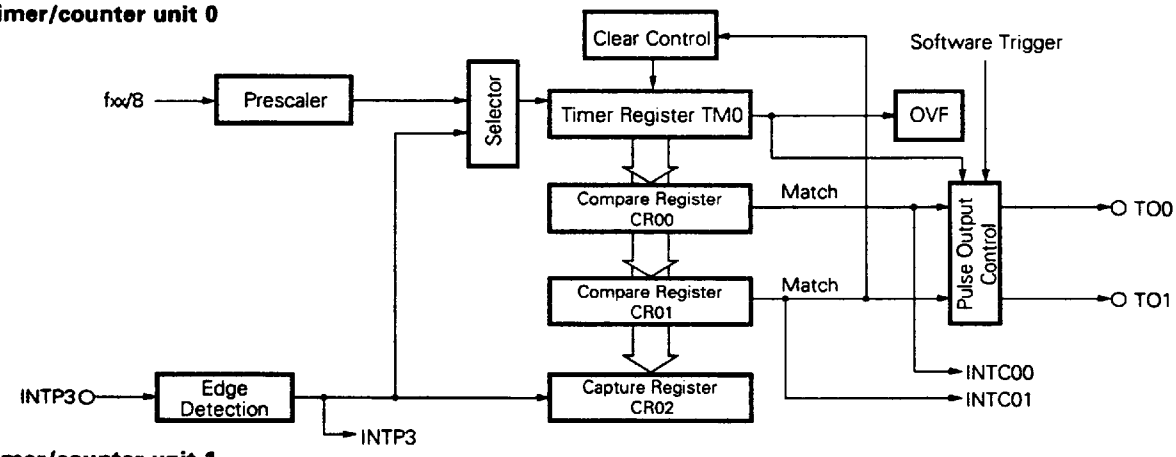
Differences from μPD78234 Subseries

Items \ Series Name	μPD784026 Subseries	μPD78234 Subseries
Count clock	$f_{XX}/8$ is the fastest	$f_{CLK}/8$ is the fastest
External event counter	3 timer/counter, 16-bit timer/counter 0 to 2, is possible.	Only 8-bit timer/counter 2 is possible.
Number of counter bit	16-bit timer/counter × 1 8, 16-bit switchable timer/counter ×3	16-bit timer/counter × 1 8-bit timer/counter × 3
Timer/counter 0 prescaler	Available	None
Timer/counter 1 capture register	A register with dual-function for capture/compare and a dedicated register for capture. However, capture trigger is common.	A register with dual-function for capture/compare only.
Timer counter 2 capture register	A dedicated register for capture and a register dual-function for capture/compare. Separated capture trigger input is available. The dedicated register for capture retains the capture value even after read.	A dedicated register for capture only. The value of the dedicated register for capture after read is undefined.
Timer/counter 3 interrupt	Separated interrupt	Shared with INTP4.

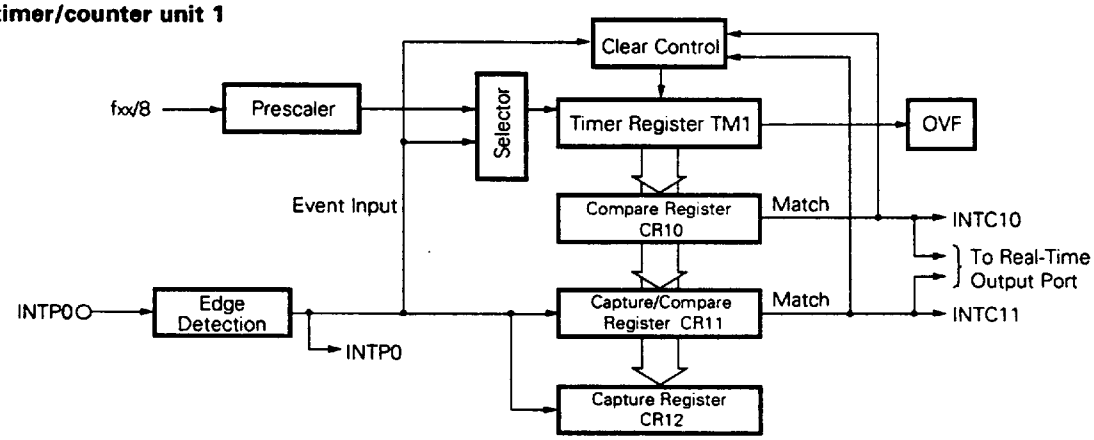
★

★ **Fig. 3-9 Timer/Counter Unit Block Diagram**

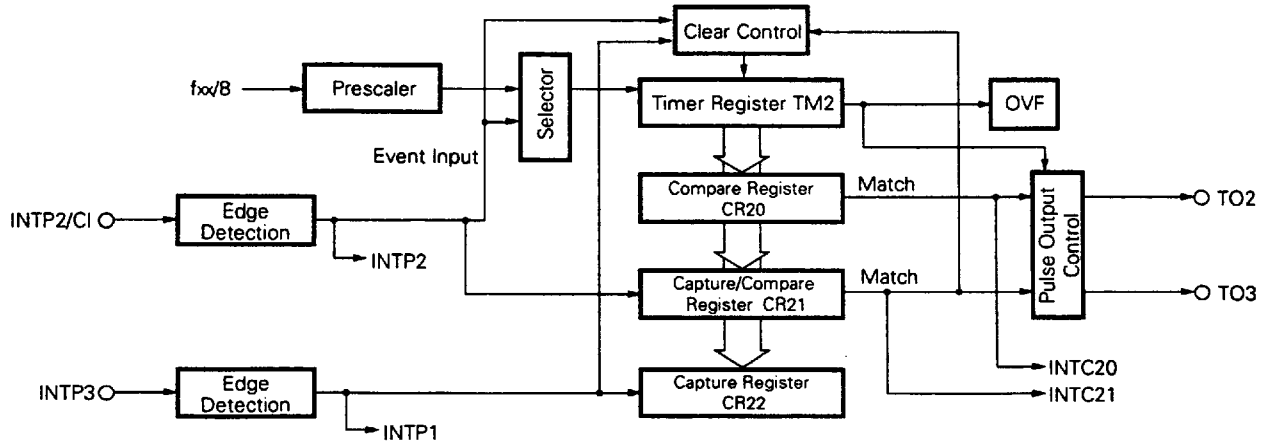
16-bit timer/counter unit 0



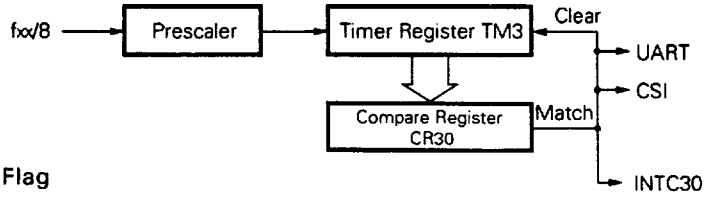
16-bit timer/counter unit 1



16-bit timer/counter unit 2



16-bit timer/counter unit 3

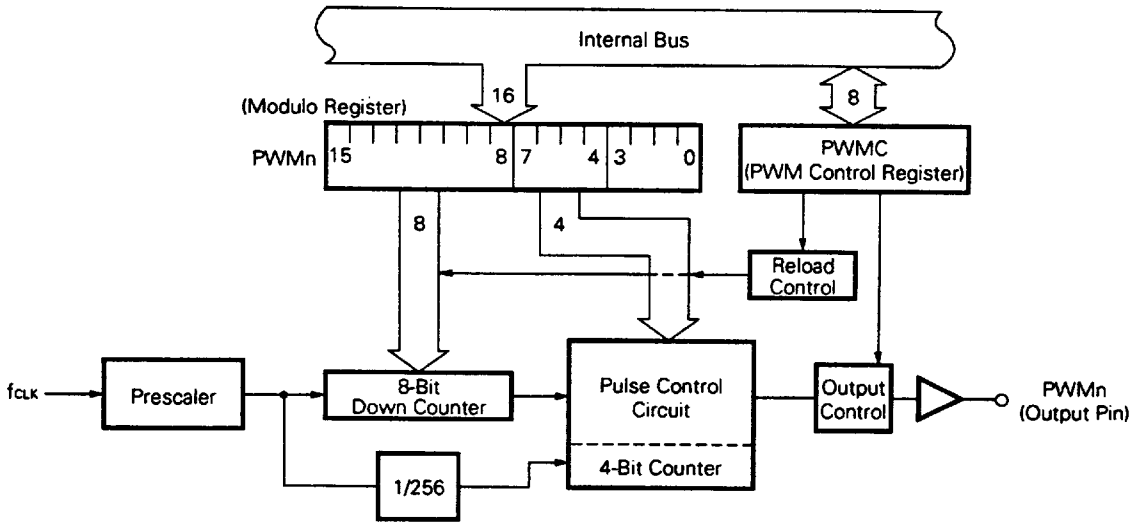


Remarks OVF : Overflow Flag

3.6 PWM OUTPUT (PWM0, PWM1)

The μPD784025/784026 have an on-chip 12-bit resolution PWM (Pulse Width Modulation) with 48.8 kHz repeat frequency (f_{CLK} = 12.5 MHz) output circuit for two channels. The active level of these channels can be selected independently as high or low level. This output is perfect for DC motor speed control.

Fig. 3-10 PWM Output Unit Block Diagram (n = 0, 1)



Differences from μPD78234 Subseries

Items \ Series Name	μPD784026 Subseries	μPD78234 Subseries
Prescaler	Available	None

3.7 A/D CONVERTER

The μPD784025/784026 incorporate an analog/digital (A/D) converter with 8 multiplexed analog inputs (ANI0 to ANI7).

The conversion is a successive approximation and the conversion result is stored in the 8-bit A/D conversion result register (ADCR). Therefore, the conversion can be executed at high speed and accuracy (converting time 10 μs approximately: At f_{CLK} = 12.5 MHz operation).

This prepares the following modes to start the A/D converting operation.

- Hardware start: Starts the conversion with a trigger input (INTP5).
- Software start: Starts the conversion by setting a bit of A/D converter mode register (ADM).

Also, the following modes are prepared for the operation after started.

- Scan mode : Selects analog inputs one after another and acquires the converted data from all pins.
- Select mode : Fixes analog inputs to one pin and acquires the continuous conversion value.

When stopping the above modes and the converting operation, all of them are specified by ADM.

The interrupt request (INTAD) occurs when the converted result is sent to ADCR (except for software start select mode). Using this, by a macro service, the converted values can be sent into the memory continuously.

Differences from μPD78234 Subseries

Items \ Series Name	μPD784026 Subseries	μPD78234 Subseries
INTAD	Separated	Shared with INTP5
INTAD at software start select mode	Generated	Not generated
A/D conversion start mode after ADCR read	Available	None

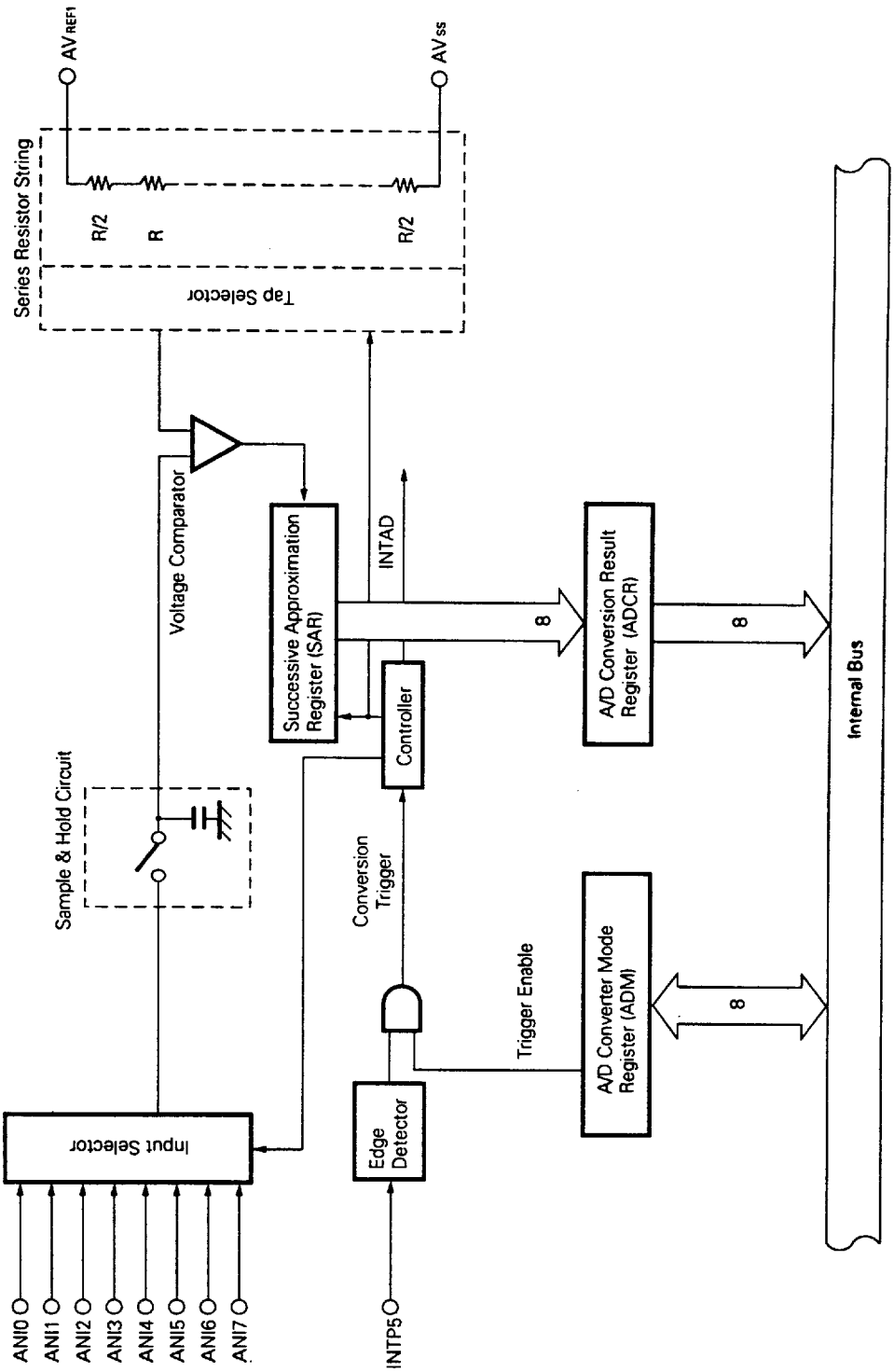


Fig. 3-11 A/D Converter Block Diagram

3.8 D/A CONVERTER

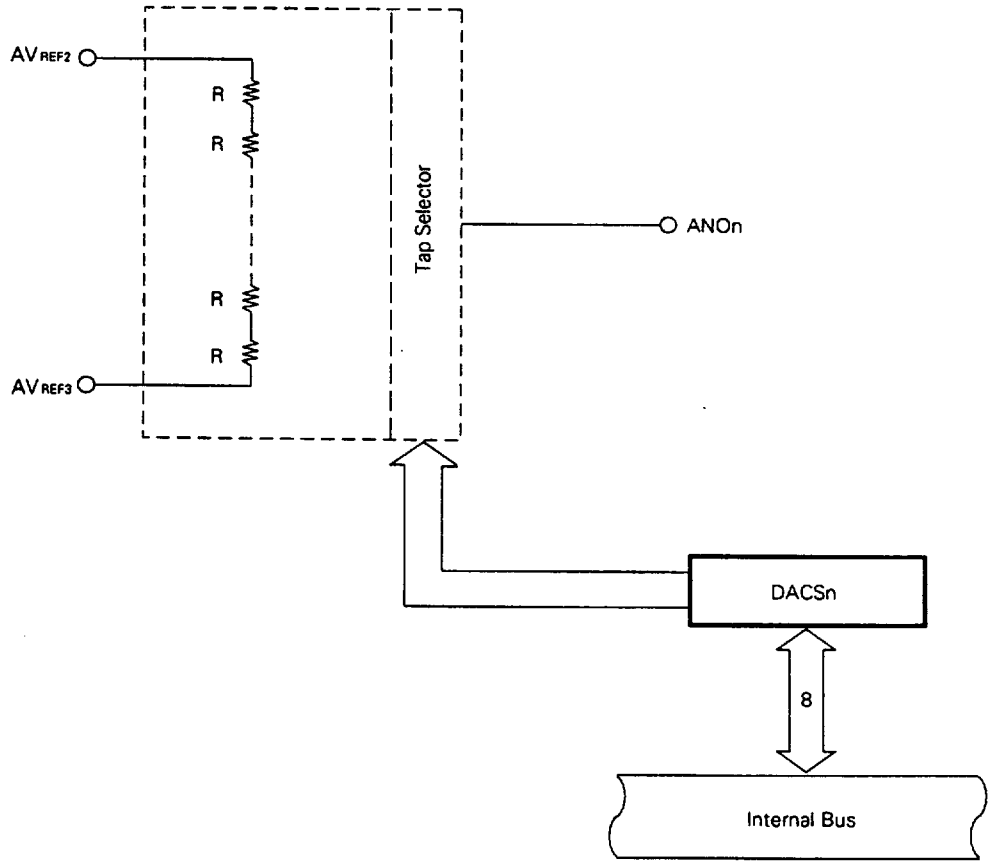
Two 8-bit resolution voltage output type digital/analog (D/A) converters are incorporated.

The conversion method is resistance string. The value to be output is written in 8-bit D/A conversion value setting register DACSn and the analog value is output to the ANOn pin. The voltage applied to the AV_{REF2} pin and AV_{REF3} pin determines the output voltage range.

Since the output impedance is high, a current cannot be taken from the output. When the load impedance is low, use by inserting a buffer amp between the output and the load.

The ANOn pin becomes high impedance during the period the $\overline{RESET}$ signal is low level. After reset is cleared, the DACSn register becomes 0.

Fig. 3-12 D/A Converter Block Diagram (n = 0, 1)



3.9 SERIAL INTERFACE

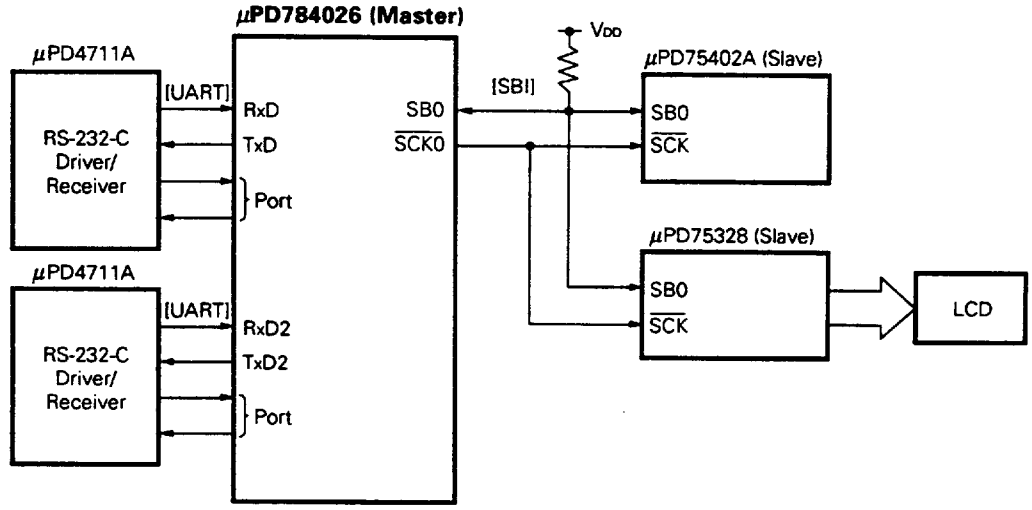
The μPD784025/784026 are equipped with 3 independent channels for serial interfaces.

- Asynchronous serial interface (UART)/3-wired serial I/O (IOE) × 2
- Clock synchronous serial interface (CSI)
  - 3-wire serial I/O (IOE)
  - Serial bus interface (SBI)

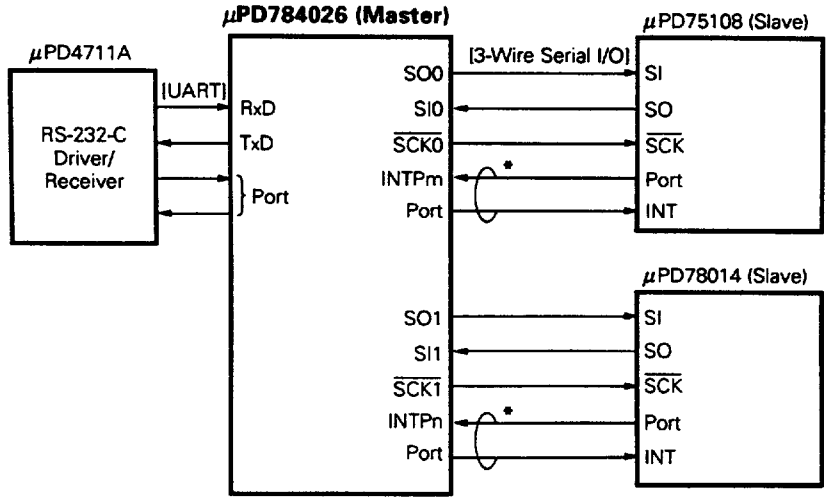
This enables both a communication with the external system and a local communication in the system simultaneously (see **Fig. 3-13**).

Fig. 3-13 Example of Serial Interface

(a) UART + SBI



(b) UART + 3-wire serial I/O



* Handshake line

3.9.1 Asynchronous Serial Interface/3-Wired Serial I/O (UART/IOE)

Two channels of serial interface in which asynchronous serial interface mode and 3-wired serial I/O mode can be selected.

(1) Asynchronous serial interface mode

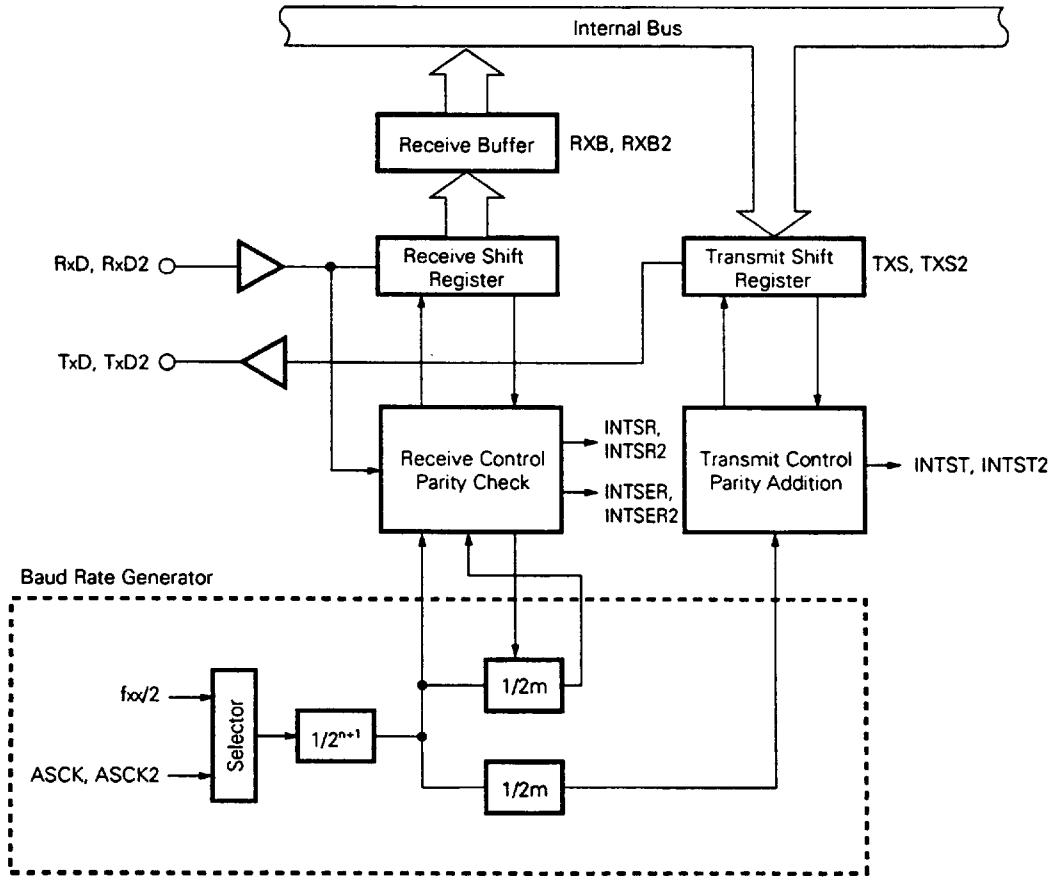
This is the method to transmit the one byte data following the start bit.

As the baud rate generator is incorporated, communications are possible with a wide range of any baud rate.

Also, the baud rate can be defined by dividing the input clock for the ASCK pin.

If the baud rate generator is used, the baud rate (31.25 kbps) of the MIDI specification can be acquired.

Fig. 3-14 Asynchronous Serial Interface Mode Block Diagram



Remarks fxx : Oscillator frequency or external clock input
n = 0 to 11
m = 16 to 30

Differences from μPD78234 Subseries

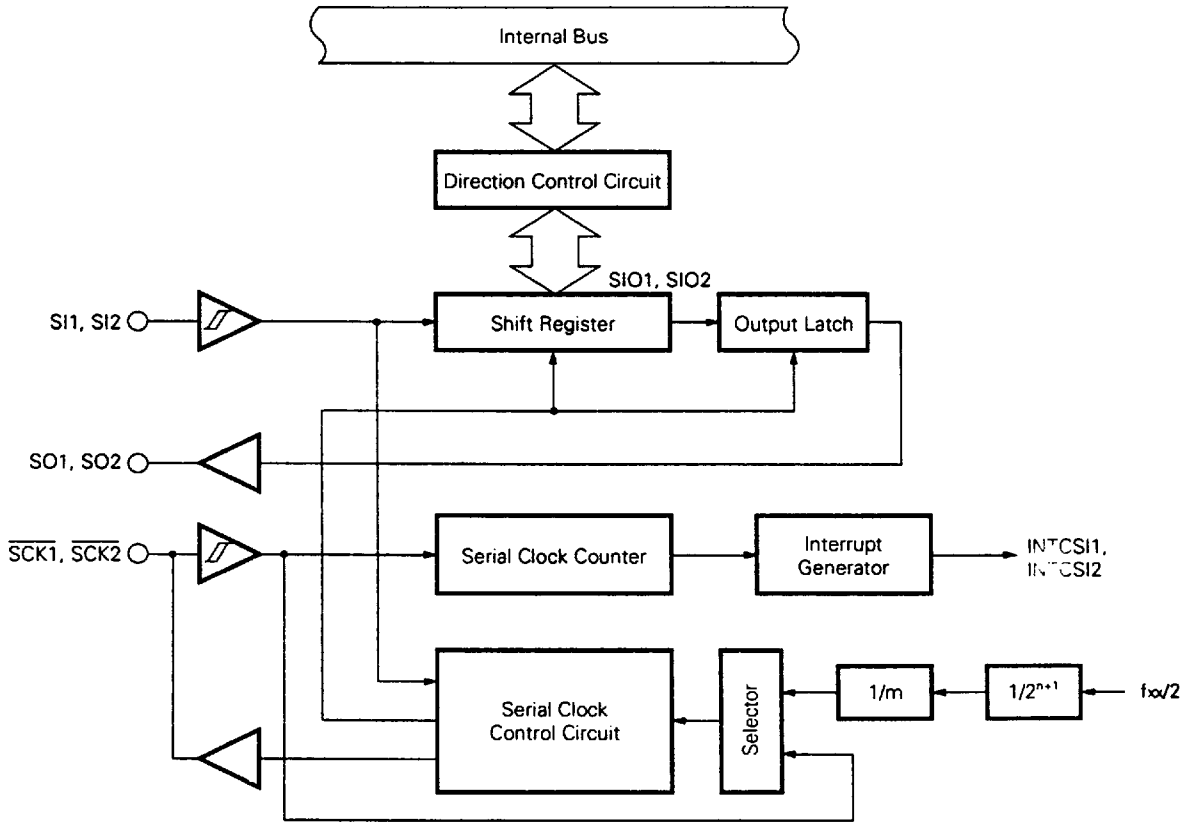
Items \ Series Name	μPD784026 Subseries	μPD78234 Subseries	
Number of channels	2	1	
3-wired serial I/O mode switching	Possible	Impossible	
Reception completion interrupt disable function at reception error generation	Available	None	
Baud rate expression by the baud rate generator	$\frac{fxx}{2^{n+3} \cdot m}$ n = 0 to 11 m = 16 to 30	$\frac{fxx}{2} \cdot \frac{1}{n} \cdot \frac{1}{2^m} \cdot \frac{1}{16}$ n = 1 to 15 m = 1 to 7	★
Transmission enable bit in UART mode (TXE0, TXE1)	Available	None	
Start bit sampling clock	2m times clock of baud rate (m= 16 to 30)	16 times clock of baud rate	★
Baud rate generation by timer/counter 3	Impossible	Possible	
External baud rate input	$\frac{f_{ASCK}}{2^{n+6}}$ n = 0 to 11	$\frac{f_{ASCK}}{2^{n+4} \times 16}$ n = 1 to 15	★

(2) 3-wire serial I/O mode

With this method, the master device starts transmission by activating the serial clock, and one-byte data is transferred in synchronization with this clock.

This interface is used to communicate with devices which incorporate a conventional clocked serial interface. Basically, communication is carried out using 3 lines : the serial clock line ($\overline{SCK}$) and serial data lines (SI, SO). If multiple devices are connected, a handshake line is required.

Fig. 3-15 3-Wired Serial I/O Mode Block Diagram



Remarks fxx : Oscillator frequency or external clock input
n = 0 to 11
m = 1, 16 to 30

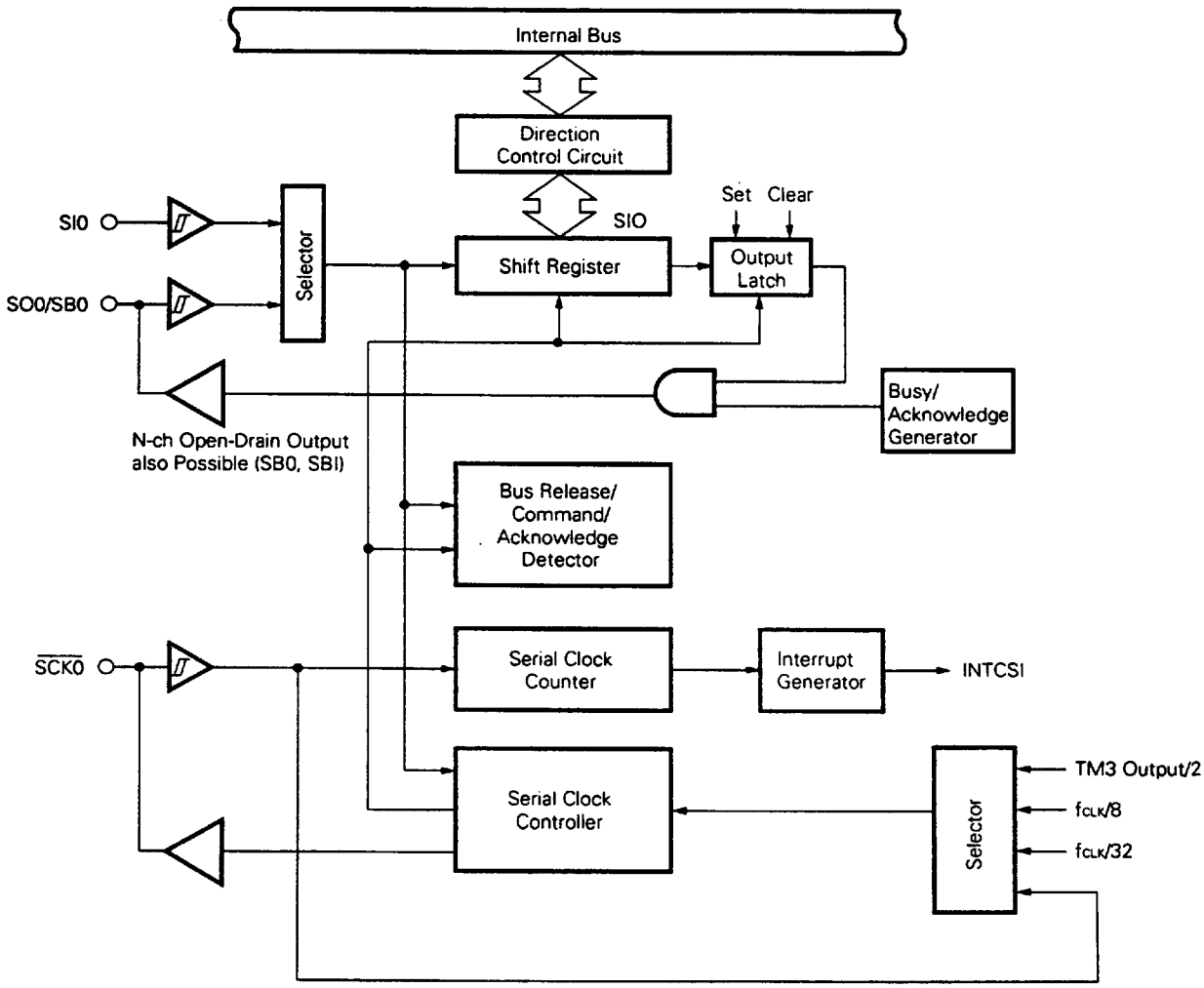
Differences from 3-Wired Serial I/O Mode of μPD78234 Subseries Clocked Serial Interface

Items \ Series Name	μPD784026 Subseries	μPD78234 Subseries
Dual function mode	Asynchronous serial interface mode	SBI mode
Transfer order	MSB first and LSB first switchable	MSB first only
Internal serial clock	$\frac{fxx}{2} \cdot \frac{1}{2^{n+3}} \cdot \frac{1}{m}$ n = 0 to 11 m = 1, 16 to 30	TM3 output, $f_{CLK}/8$, $f_{CLK}/16$ switchable ★

3.9.2 Clocked Serial Interface (CSI)

This is a method to communicate one byte data in synchronization with the serial clock which is activated by master device and starts to transmit.

Fig. 3-16 Clocked Serial Interface Block Diagram



Remarks f_{CLK} : Internal system clock frequency (system clock frequency / 2)

(1) 3-wire serial I/O

This is a interface to communicate with a device which incorporates a conventional clocked serial interface.

Basically, the communication is made through 3 wires of serial clock ($\overline{SCK0}$) and serial data (SI0, SO0). In case of connecting with multiple device, the handshake line is required.

(2) SBI

This can communicate with a multiple device through 2 wires of serial clock ($\overline{SCK0}$) and serial bus (SB0) and this is a NEC standard serial interface.

The master device outputs "address" from the SB0 pin and selects the communicated slave device. Then, "command" and "data" are transmitted and received between the master and slave.

Differences from μPD78234 Subseries

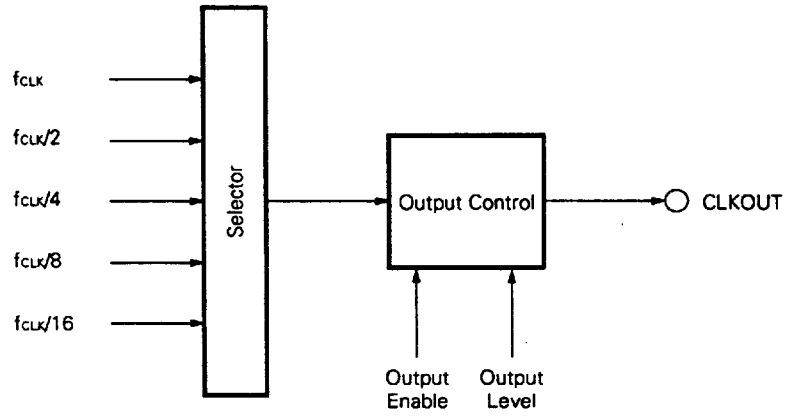
Items \ Series Name	μPD784026 Subseries	μPD78234 Subseries
Transfer order in 3-wired serial I/O mode	MBS first and LSB first switchable	MBS first only
SO0 pin level control in 3-wired serial I/O mode	Possible	Impossible

3.10 CLOCK OUTPUT FUNCTION

The μPD784025/784026 can output externally a clock derived by scaling the CPU operating clock. This can also be used as a 1-bit port.

When this function is used, the ASTB pin and CLKOUT pin have a dual function, and therefore the local bus interface cannot be used.

Fig. 3-17 Clock Output Function Block Diagram



3.11 EDGE DETECTION FUNCTION

The interrupt input pins (NMI, INTP0 to INTP5) are used not only to input interrupt requests, but also as input pins for various on-chip hardware trigger signals, etc. As these all operate on the edge of the input signal, a function for detecting the edge is incorporated. A noise elimination function is also provided to prevent erroneous edge detection due to noise.

Pins	Detectable Edge	Noise Elimination Method
NMI	Either of rising or falling	By analog delay
INTP0 to INTP3	Either of rising or falling, or both	By clock sampling*
INTP4, INTP5		By analog delay

* For INTP0, sampling clock can be selected.

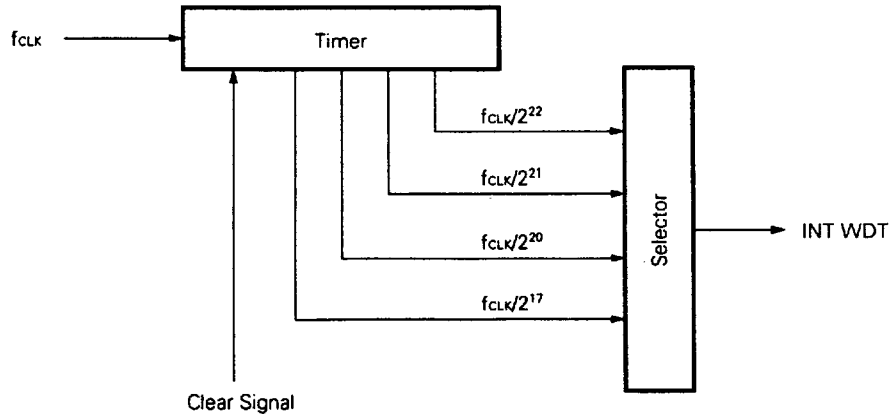
Differences from μPD78234 Subseries

Items \ Series Name	μPD784026 Subseries	μPD78234 Subseries
Noise elimination method of INTP4 and INTP5	By analog delay	By clock sampling
INTP0 noise elimination sampling clock	Selectable	Fixed
INTP4 and INTP5 interrupt	No dual-functions	INTP4 has dual-function as INTC30, and INTP5 has a dual-function as INTAD

3.12 WATCHDOG TIMER

The μPD784025/784026 incorporate a watchdog timer to detect CPU runaway. If this watchdog timer is not cleared by software within the previously specified interval, a non-maskable interrupt is generated. Once operation of the watchdog timer is enable, it cannot be stopped by software. It is possible to specify whether an interrupt generated by the watchdog timer or an interrupt from the NMI pin has priority.

★ **Fig. 3-18 Watchdog Timer Block Diagram**



4. INTERNAL/EXTERNAL CONTROL FUNCTION

4.1 INTERRUPT

The interrupt request servicing can be selected from 3 mode in the following table.

Table 4-1 Interrupt Request Servicing

Servicing Mode	Servicing Means	Servicing	PC, PSW Contents
Vectored interrupt	Software	Branch to and execution of service routine (any service contents)	Saved/restored to/from stack
Context Switching		Switched automatically be register bank, branch to and execution of service routine (any service contents)	Saved/restored to/from fixed area in register bank ★
Macro service	Firmware	Execution of memory-I/O data transfer, etc. (fixed service contents)	Retained

4.1.1 Interrupt Source

The interrupt source includes the 23 types and a BRK instruction execution and operand error as shown in Table 4-2.

The priority of the interrupt servicing can be set to 4 levels (high and low priority levels). Therefore, it can separate the levels of the nest control which the interrupt is in progress and the interrupt request which occurs simultaneously. But the nesting advances certainly in the macro service (not held).

The default priority is the priority level (fixed) to service the interrupt requests which occur at the same level simultaneously (see **Fig. 4-2**).

Table 4-2 Interrupt Source

Type	Default Priority	Source		Internal/ External	Macro Service
		Name	Trigger		
Software	—	BRK instruction	Instruction execution	—	—
		Operand error	When the result of the exclusive-OR of operand byte and byte is not FFH at "MOV STBC, #byte" and "MOV WDM, #byte" instruction execution.		
Non-maskable	—	NMI	Pin input edge detection	External	—
		WDT	At watchdog timer overflow		
Maskable	0 (highest)	INTP0	Pin input edge detection (TM1 capture trigger)	External	○
	1	INTP1	Pin input edge detection (TM2 capture trigger)		
	2	INTP2	Pin input edge detection (TM2 event counter input)		
	3	INTP3	Pin input edge detection (TM0 capture trigger)		
	4	INTC00	TM0 to CR00 match signal generation	Internal	
	5	INTC01	TM0 to CR01 match signal generation		
	6	INTC10	TM1 to CR10 match signal generation		
	7	INTC11	TM1 to CR11 match signal generation		
	8	INTC20	TM2 to CR20 match signal generation		
	9	INTC21	TM2 to CR21 match signal generation		
	10	INTC30	TM3 to CR30 match signal generation		
	11	INTP4	Pin input edge detection	External	
	12	INTP5	Pin input edge detection		
	13	INTAD	A/D converter conversion termination (transfer to ADCR)	Internal	
	14	INTSER	ASI0 receive error generation		—
	15	INTSR	ASI0 receive termination or CSI1 transfer termination		○
		INTCSI1			
	16	INTST	ASI0 transmit termination		
	17	INTCSI	CSI0 transfer termination		
	18	INTSER2	ASI2 receive error generation		—
	19	INTSR2	ASI2 receive termination or CSI2 transfer termination		○
		INTCSI2			
	20 (lowest)	INTST2	ASI2 transmit termination		

Remarks TM0 : 16-bit timer
TM1 to TM3 : 8-bit timer or 16-bit timer
ASI : Asynchronous serial interface
CSI : Clocked serial interface

4.1.2 Vectored Interrupt

The memory contents of the vector table address, which corresponds to the interrupt source, is branched into the processing routine as a destination address.

As the CPU executes the interrupt servicing, the following operations occur.

- When branch: Saving the CPU status (PC, PSW contents) to the stack.
- When return: Returning the CPU status (PC, PSW contents) from the stack.

The RETI instruction executes returning to the main routine from the processing routine.
Also, destination address is limited to 0 to FFFFH.

Table 4-3 Vector Table Address

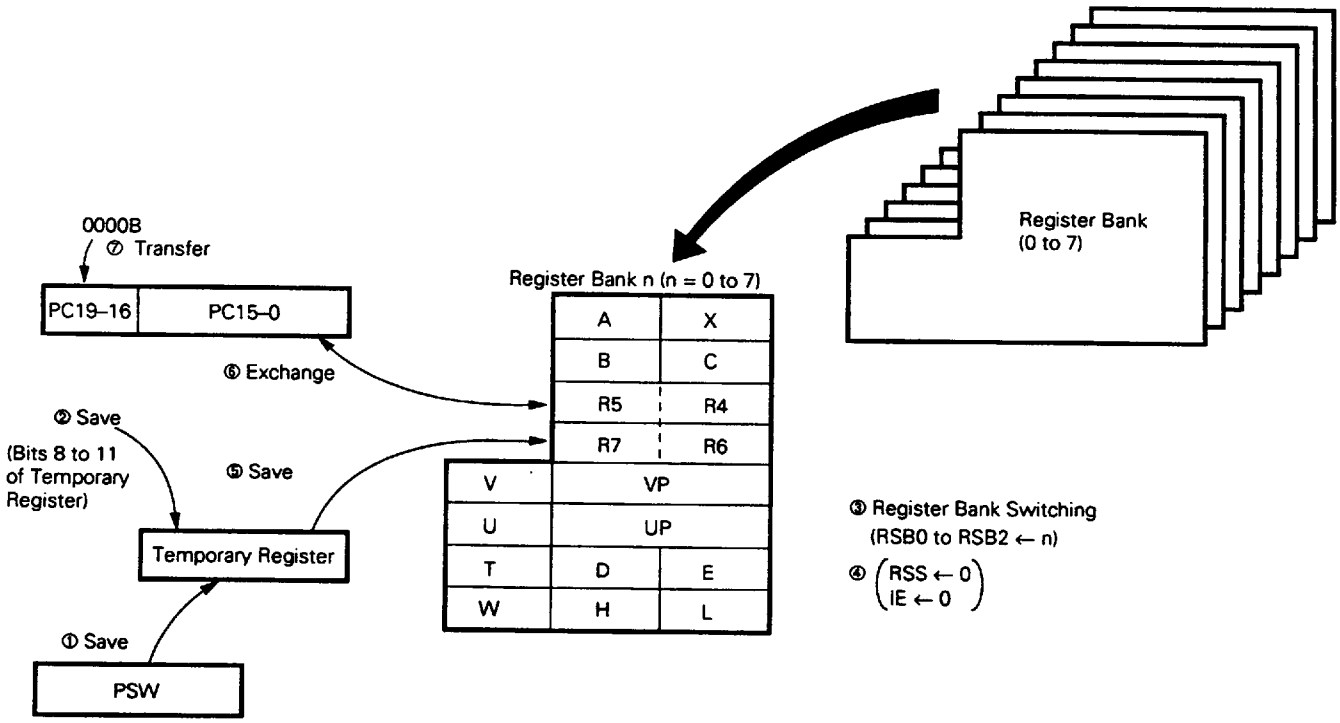
Interrupt Source	Vector Table Address
BRK instruction	003EH
Operand error	003CH
NMI	0002H
WDT	0004H
INTP0	0006H
INTP1	0008H
INTP2	000AH
INTP3	000CH
INTC00	000EH
INTC01	0010H
INTC10	0012H
INTC11	0014H
INTC20	0016H
INTC21	0018H
INTC30	001AH
INTP4	001CH
INTP5	001EH
INTAD	0020H
INTSER	0022H
INTSR	0024H
INTCSI1	
INTST	0026H
INTCSI	0028H
INTSER2	002AH
INTSR2	002CH
INTCSI2	
INTST2	002EH

4.1.3 Context Switching

A specific register bank is selected by hardware by generating an interrupt request or executing a BRKCS instruction. This function branches to the vector address stored beforehand in the register bank, and at the same time stacks the current program counter (PC) and program status word (PSW) contents in the register bank.

The branch destination address range is 0 to FFFFH.

★ **Fig. 4-1 Context Switching Operation by Interrupt Request**

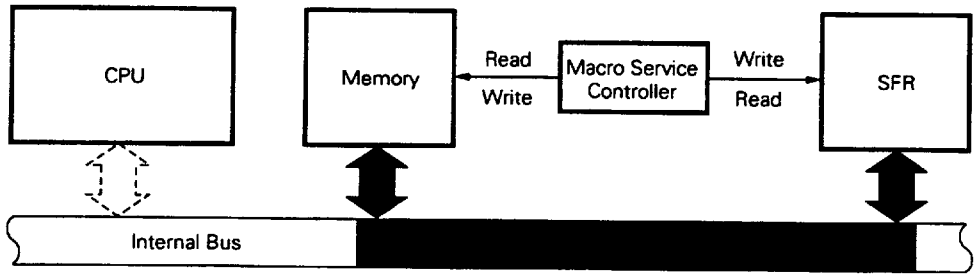


4.1.4 Macro Service

This is a function to transfer the data between the memory special functional registers (SFR) not through the CPU. The macro service controller accesses the memory and SFR during the same transfer cycle, and transfers directly without collecting data.

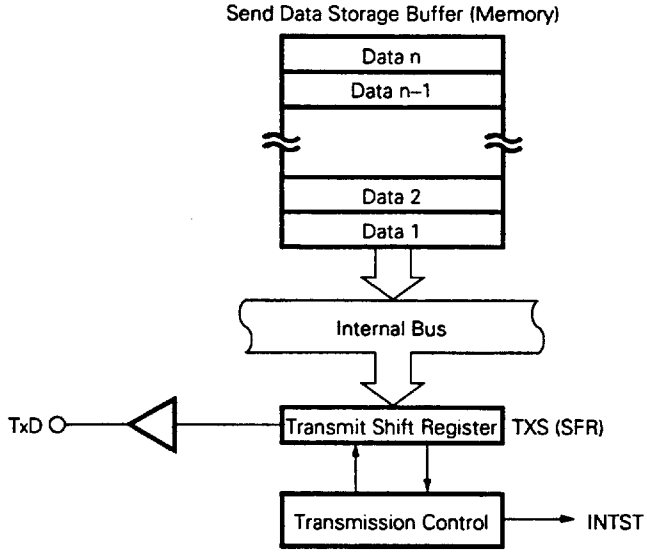
The high-speed data transfer is enabled because no CPU status data is saved, returned nor fetched.

Fig. 4-2 Macro Service



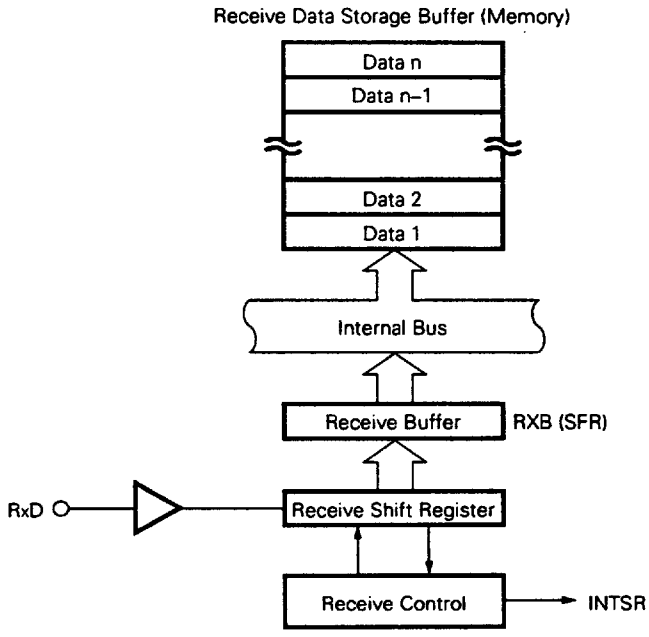
4.1.5 Macro Service Application Example

(1) Transmit operation of serial interface



Whenever the macro service request INTST is generated, the next send data is transferred to TXS from the memory. When the data n (last byte) is transferred to TXS (The send data storage buffer becomes empty.), a vectored interrupt request INTST is generated.

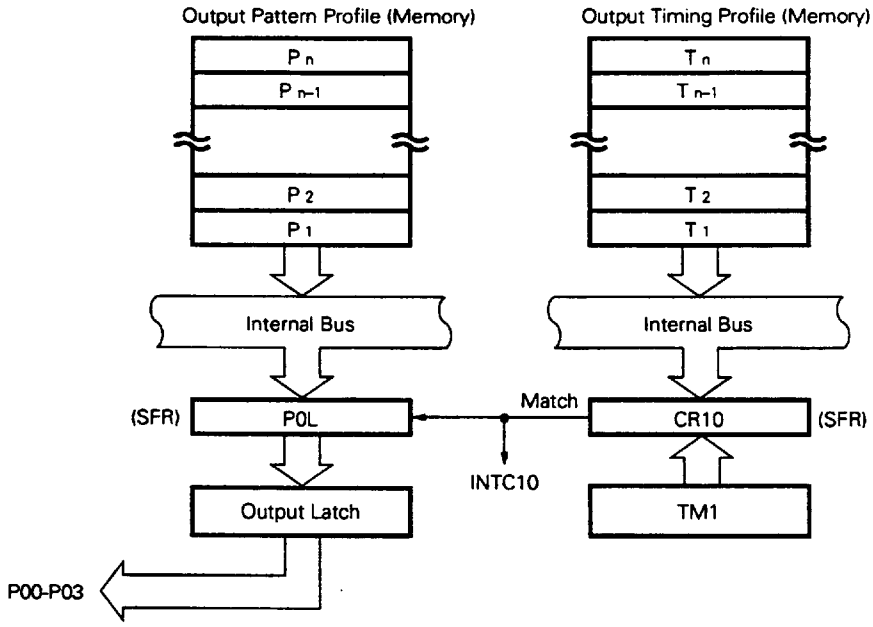
(2) Receive operation of serial interface



Whenever the macro service request INTSR is generated, the receive data is transferred to the memory from RXB. When the data n (last byte) is transferred to the memory (The receive data storage buffer becomes empty.), the vectored interrupt request INTSR is generated.

(3) Real-time output port

The INTC10 and INTC11 become output triggers of the real-time output port. In the macro service to them, the next output pattern and interval can be set simultaneously. Therefore, the INTC10 and INTC11 can control 2 system stepping motor independently. Also, it can be applied to control a PWM or DC motor, etc.



Whenever the macro service request INTC10 is generated, the pattern and timing are transferred to P0L and CR10 respectively. When the contents of the TM1 match with the contents of the CR10, the next INTC10 is generated and the contents of the P0L is sent to the output latch. If T_n (last byte) is sent to CR10, a vectored interrupt request INTC10 is generated.

The same operation is available for INTC11.

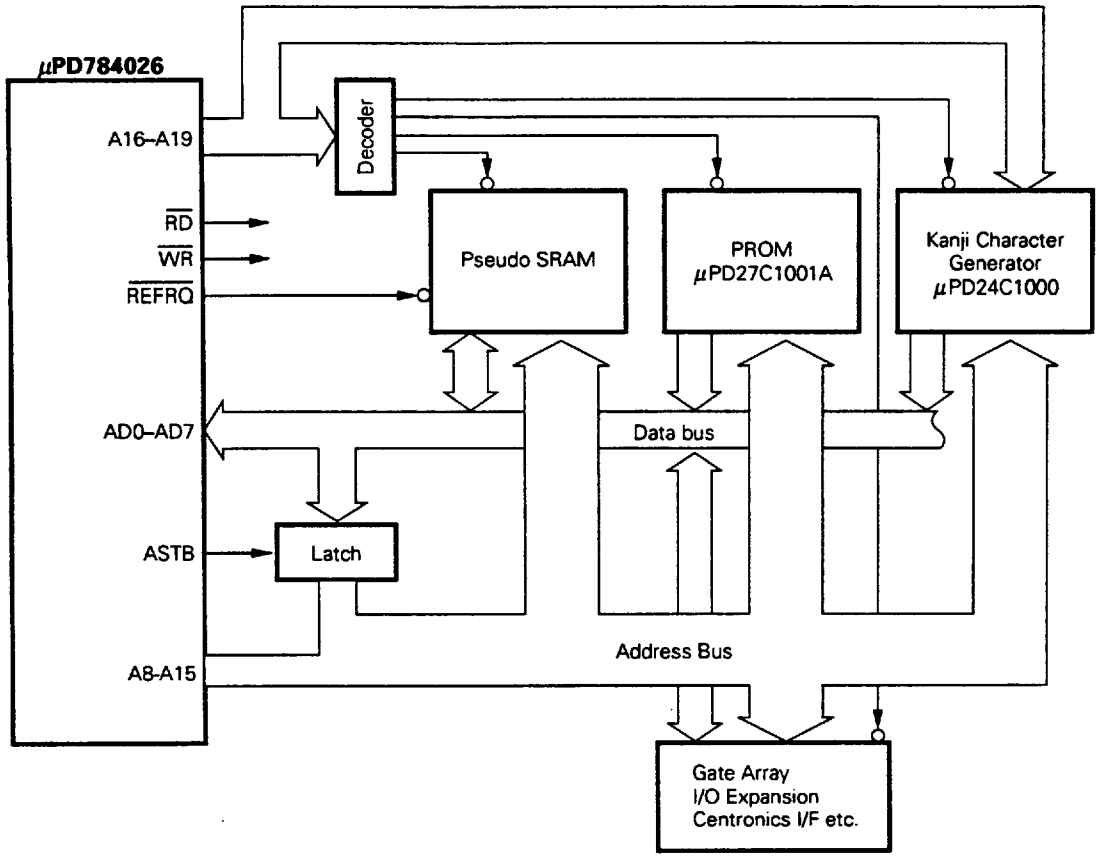
Differences from μPD78234 Subseries

Items \ Series Name		μPD784026 Subseries	μPD78234 Subseries
Interrupt source		BRK instruction, operand error interrupt and 23 types of hardware interrupt	BRK instruction and 19 types of hardware interrupt
Context switching function		Available	None
Multiple processing priority		4 levels	2 levels
Control register for each interrupt request source		A register is available for each interrupt request source.	A register is available in units of function.
Vector table and macro service control word address		Different. Compare them for details using user's manuals of devices.	
Macro Service function	SFR address when type A or type C is used	Programmable	Fixed for each interrupt request source
	Decrement of type C MPD	Possible	Impossible
	16-bit data transfer of type A, type B, and type C timing data	Possible	Impossible
	Operation when macro service counter becomes 0	Whether vectored interrupt request is generated is selectable.	Vectored interrupt request is always generated.

4.2 LOCAL BUS INTERFACE

The μPD784025/784026 can be connected a memory and an I/O (memory mapped I/O) externally and supports the 1M-byte memory space (see **Fig. 4-3**).

Fig. 4-3 Local Bus Interface Example



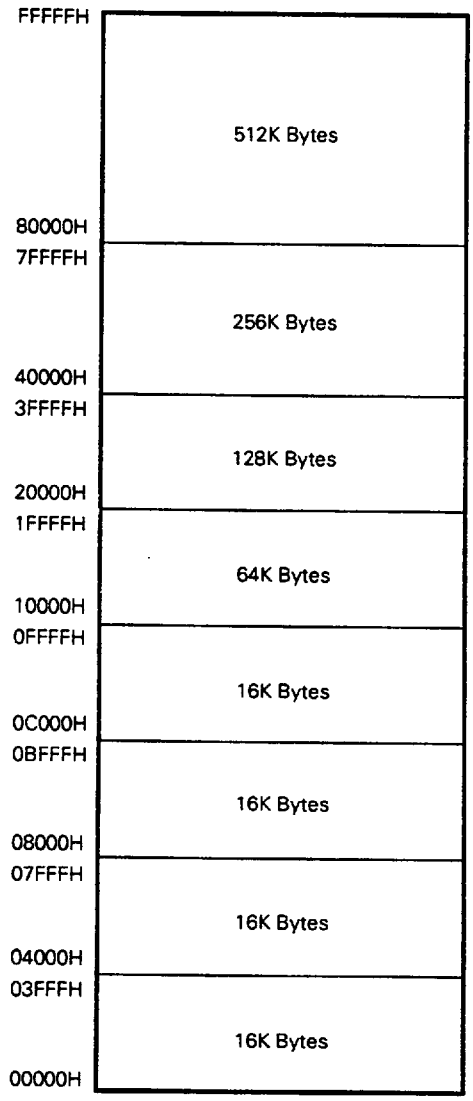
4.2.1 Memory Expansion

Program memory or data memory can externally expanded from 256 bytes up to approximately 1 M bytes in 7 stages.

4.2.2 Memory Space

The 1M-byte memory space is divided into 8 spaces by logical addresses. Control by means of the programmable wait function and pseudo-static RAM refresh function can be performed for each of these spaces.

Fig. 4-4 Memory Space



4.2.3 Programmable Wait

The memory space is divided into 8, and waits can be inserted independently for each memory space while the $\overline{RD}$ or $\overline{WR}$ signal is active. As a result, overall system efficiency is not reduced when memories with different access times are connected.

Also, to gain the address decoding time, an address wait function is provided which increases the active period of the ASTB signal (set for all spaces).

4.2.4 Pseudo-Static RAM Refresh Function

The refresh operations are as follows.

- Pulse refresh : A pulse cycle is inserted which outputs a refresh pulse to the $\overline{REFRQ}$ pin at fixed intervals. The memory space is divided into 8, and when the specified area is accessed it is possible to output a refresh pulse from the $\overline{REFRQ}$ pin at the same time as the memory access. It is thus is possible to prevent ordinary memory accesses from being kept waiting by a refresh cycle.
- Power-down self refresh : Outputs a low-level to the $\overline{REFRQ}$ pin in the standby mode and holds the contents of the pseudo-static RAM.

4.2.5 Bus Hold Function

A bus hold function is provided to facilitate connection of a DMA controller, etc. When a bus hold request signal (HLDRQ) from an external bus master is acknowledged, as soon as the bus cycle being performed at that time finishes, the address bus, address/data bus, and ASTB, $\overline{RD}$ and $\overline{WR}$ pins are set to high impedance, the bus hold acknowledge signal (HLDAK) is activated, and the bus is released to the external bus master.

The external wait function and pseudo-static RAM refresh function cannot be used when this function is used.

4.2.6 Differences from μPD78234 Subseries

Items \ Series Name	μPD784026 Subseries	μPD78234 Subseries
External expansion function	Switchable in 7 steps from 256 bytes to 1M bytes	Switchable in 2 steps of 64K bytes and 1M bytes
Programmable wait memory space division	Specifiable divided into 8	Specifiable divided into 2
Address wait function	Available	No
Refresh operation and memory access operation	Performed simultaneously for specified space otherwise performed exclusively	Performed exclusively
Bus hold function	Available	No

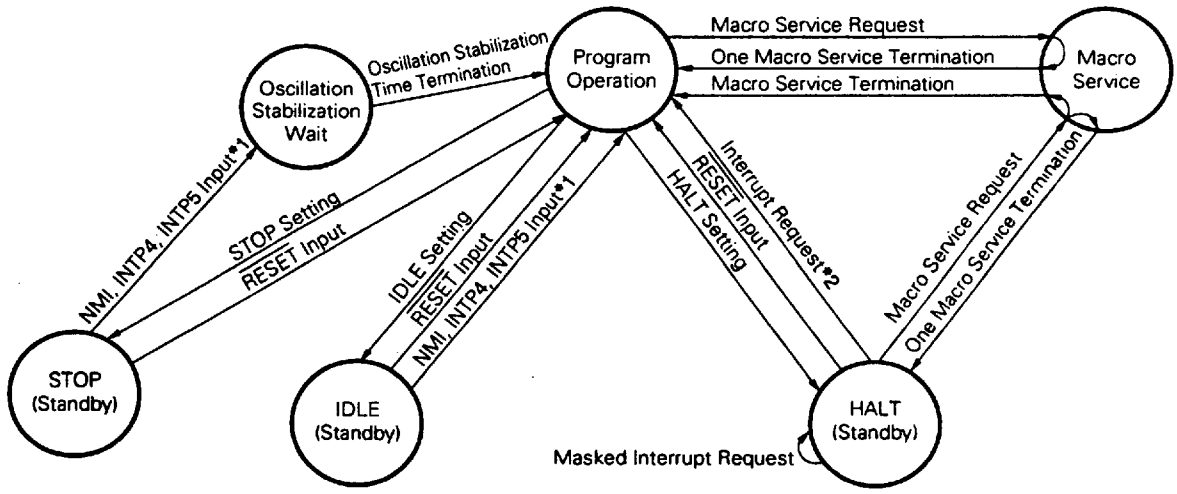
4.3 STANDBY FUNCTION

This is a function to reduce the power consumption of the chip. The following modes have been prepared.

- HALT mode : Stops the operation clock of the CPU. The average power consumption is reduced by the normal operation and the intermittent operation during normal operations.
- ★ IDLE mode : Except that the oscillation circuit continues to operate, in this mode the entire system stops. In the same low power dissipation as with the STOP mode, and for the same time as with the HALT mode, the CPU can return to a normal program operation.
- STOP mode : Stops the oscillator. This stops all operation in the chip and makes the minute power consumption status only with leakage current.

These modes are programmable.
Also, the macro service is started from the HALT mode.

★ **Fig. 4-5 Standby Status Transitions**



* 1. For INTP4 and INTP5, when they are not masked.
2. Only unmasked interrupt request.

Differences from μPD78234 Subseries

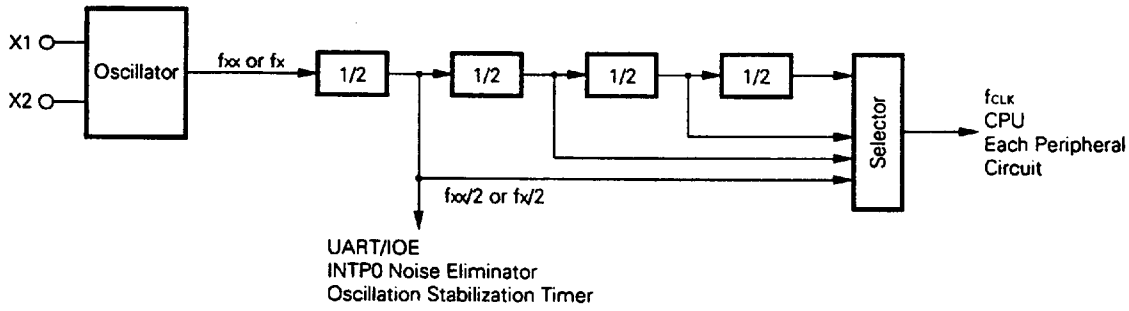
Items \ Series Name	μPD784026 Subseries	μPD78234 Subseries
STOP mode release signal	$\overline{\text{RESET}}$/$\overline{\text{NMI}}$ input and INTP4/INTP5 which is not masked.	$\overline{\text{RESET}}$ and $\overline{\text{NMI}}$ input
HALT mode release by maskable interrupt	Released by interrupt which is not masked.	Released by accessible interrupt.
The oscillation stabilization time at STOP mode release by NMI	The count time for 16 to 19 bits of the oscillation stabilization timer. 16 to 19 are selectable.	The NMI active level time the count time for 16 bits of the oscillation stabilization timer, or the count time for 15 bits of the oscillation stabilization timer.
IDLE mode	Available	None

★

4.4 CLOCK GENERATOR

The μPD784025/784026 are equipped with a clock generator necessary for its operation. Also, the clock generator contains a frequency divider, and if fast operation is not necessary, low current consumption can be achieved by lowering the internal operation frequency.

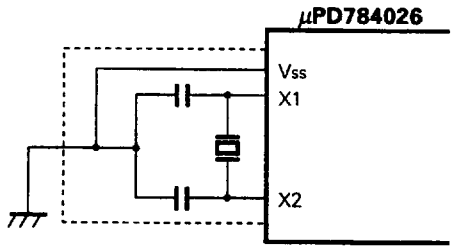
Fig. 4-6 Clock Generator Block Diagram



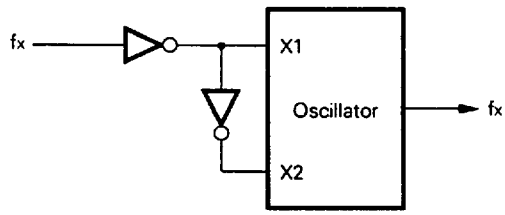
Remarks fx : External clock frequency
fxx : Oscillator frequency
fCLK : Internal operation frequency

Fig. 4-7 Example of Oscillator Use

★ **(1) Crystal/ceramic oscillation**



(2) External clock input



Note When the clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by a dotted line to prevent the influence of wiring capacitance, etc.

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed.**
- **Keep away from lines carrying a high fluctuating current.**
- **The oscillator capacitor grounding point should always be at the same potential as Vss. Do not connect to a ground pattern carrying a high current.**
- **A signal should not be taken from the oscillator.**

Differences from μPD78234 Subseries

Items \ Series Name	μPD784026 Subseries	μPD78234 Subseries
Clock frequency divider	1/2, 1/4, 1/8 and 1/16 division is selectable	1/2 division only

4.5 RESET FUNCTION

When a low level is input to the $\overline{\text{RESET}}$ pin, the internal hardware is initialized (reset state).

When the $\overline{\text{RESET}}$ input becomes from a low level to a high level, the following data is set in the program counter (PC).

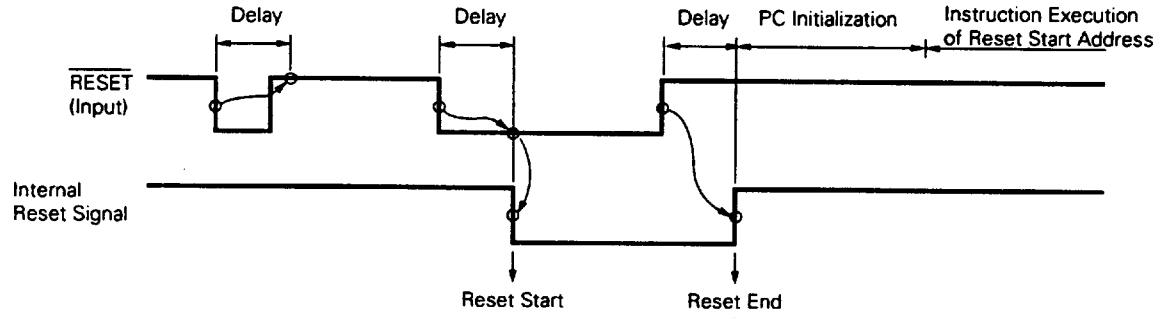
- Lower 8 bits of PC : Contents of 0000H address
- Middle 8 bits of PC : Contents of 0001H address
- Upper 4 bits of PC : 0

The contents of the PC set the destination address and the program starts to be executed from the address. Therefore, it can start from any address by reset start.

Please set the program for the contents of each register as required.

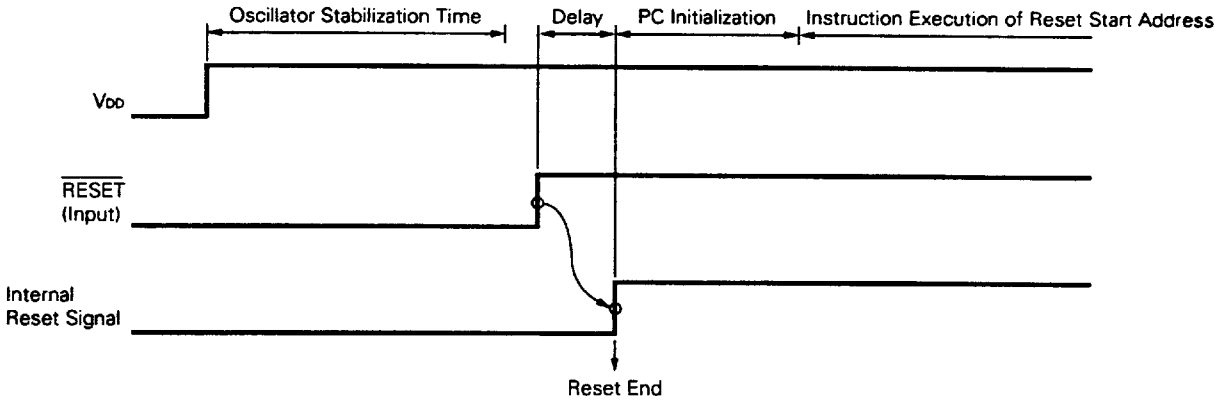
A noise eliminator has been incorporated the $\overline{\text{RESET}}$ input circuit to prevent any error from noise. This noise eliminator circuit is a sampling circuit based on analog delay.

Fig. 4-8 Reset Acknowledge



Set the $\overline{\text{RESET}}$ signal active in the reset operation at power-on until oscillator stabilization time (approx. 40 ms) elapses.

Fig. 4-9 Reset Operation at Power-On



★ 5. INSTRUCTION SET

(1) 8-bit instructions (Combinations expressed by writing "A" as "r" are shown in parentheses)

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, SHR, SHL, ROR4, ROL4, DBNZ, PUSH, POP, MOVM, XCHM, CMPME, CMPMNE, CMPMNC, CMPMC, MOVBK, XCHBK, CMPBKE, CMPBKNE, CMPBKNC, CMPBKC, CHKL, CHKLA

Table 5-1 List of Instructions Classified by 8-Bit Addressing

1st Operand \ 2nd Operand	#byte	A	r r'	saddr saddr'	sfr	!addr16 !!addr24	mem [saddrp] [%saddrg]	r3 PSWL PSWH	[WHL+]	[WHL−]	n	None*2
A	(MOV) ADD*1	(MOV) (XCH) (ADD)*1	MOV XCH (ADD)*1	(MOV)*6 (XCH)*6 (ADD)*1,6	MOV (XCH) (ADD)*1	(MOV) (XCH) ADD*1	MOV XCH ADD*1	MOV	(MOV) (XCH) (ADD)*1	(MOV) (XCH) (ADD)*1		
r	MOV ADD*1	(MOV) (XCH) (ADD)*1	MOV XCH ADD*1	MOV XCH ADD*1	MOV XCH ADD*1	MOV XCH					ROR*3	MULU DIVUW INC DEC
saddr	MOV ADD*1	(MOV)*6 (ADD)*1	MOV ADD*1	MOV XCH ADD*1								INC DEC DBNZ
sfr	MOV ADD*1	MOV (ADD)*1	MOV ADD*1									PUSH POP CHKL CHKLA
!addr16 !!addr24	MOV	(MOV) ADD*1	MOV									
mem [saddrp] [%saddrg]		MOV ADD*1										
mem3												ROR4 ROL4
r3 PSWL PSWH	MOV	MOV										
B, C												DBNZ
STBC, WDM	MOV											
[TDE+]		(MOV) (ADD)*1 MOVM*4							MOVBK*5			
[TDE−]		(MOV) (ADD)*1 MOVM*4								MOVBK*5		

* 1. ADDC, SUB, SUBC, AND, OR, XOR and CMP are equivalent to ADD.
2. There is no 2nd operand, or the 2nd operand is not an operand address.
3. ROL, RORC, ROLC, SHR and SHL are equivalent to ROR.
4. XCHM, CMPME, CMPMNE, CMPMNC and CMPMC are equivament to MOVM.
5. XCHBK, CMPBKE, CMPBKNE, CMPBKNC and CMPBKC are equivalent to MOVBK.
6. When saddr is saddr2 in this combination, there is a short code length instruction.

(2) 16-bit instructions (Combinations expressed by writing "AX" as "rp" are shown in parentheses)

MOVW, XCHW, ADDW, SUBW, CMPW, MULUW, MULW, DIVUX, INCW, DECW, SHRW, SHLW, PUSH, POP, ADDWG, SUBWG, PUSHU, POPU, MOVTBLW, MACW, MACSW, SACW

Table 5-2 List of Instructions Classified by 16-Bit Addressing

1st Operand \ 2nd Operand	#word	AX	rp rp'	saddrp saddrp'	sfrp	!addr16 !!addr24	mem [saddrp] [%saddrg]	[WHL+]	byte	n	None*2
AX	(MOVW) ADDW*1	(MOVW) (XCHW) (ADD)*1	(MOVW) (XCHW) (ADDW)*1	(MOVW)*3 (XCHW)*3 (ADDW)*1,3	MOVW (XCHW) (ADDW)*1	(MOVW) XCHW	MOV XCH	MOVW XCHW	(MOVW) (XCHW)		
rp	MOVW ADDW*1	(MOVW) (XCHW) (ADDW)*1	MOVW XCHW ADDW*1	MOVW XCHW ADDW*1	MOVW XCHW ADDW*1	MOVW				SHRW SHLW	MULW*4 INCW DECW
saddrp	MOVW ADDW*1	(MOVW)*3 (ADDW)*1	MOVW ADDW*1	MOVW XCHW ADDW*1							INC DECW
sfrp	MOVW ADDW*1	MOVW (ADDW)*1	MOVW ADDW*1								PUSH POP
!addr16 !!addr24	MOVW	(MOVW)	MOVW						MOVTBLW		
mem [saddrp] [%saddrg]		MOVW									
PSW											PUSH POP
SP	ADDWG SUBWG										
post											PUSH POP PUSHU POPU
[TDE+]		(MOVW)						SACW			
byte											MACW MACSW

* 1. SUBW and CMPW are equivalent to ADDW.
2. There is no 2nd operand, or the 2nd operand is not an operand address.
3. When saddr is saddr2 in this combination, there is a short code length instruction.
4. MULUW and DIVUX are equivalent to MULW.

(3) 24-bit instructions (Combinations expressed by writing "WHL" as "rg" are shown in parentheses)
MOVG, ADDG, SUBG, INCG, DECG, PUSH, POP

Table 5-3 List of Instructions Classified by 24-Bit Addressing

1st Operand \ 2nd Operand	#imm24	WHL	rg rg'	saddrg	!!addr24	mem1	[%saddrg]	SP	None*
WHL	(MOVG) (ADDG) (SUBG)	(MOVG) (ADDG) (SUBG)	(MOVG) (ADDG) (SUBG)	(MOVG) ADDG SUBG	(MOVG)	MOVG	MOVG	MOVG	
rg	MOVG ADDG SUBG	(MOVG) (ADDG) (SUBG)	MOVG ADDG SUBG	MOVG	MOVG				INCG DECG PUSH POP
saddrg		(MOVG)	MOVG						
!!addr24		(MOVG)	MOVG						
mem1		MOVG							
[%saddrg]		MOVG							
SP	MOVG	MOVG							INCG DECG

* There is no 2nd operand, or the 2nd operand is not an operand address.

(4) Bit manipulation instructions
MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR, BFSET

Table 5-4 List of Bit Manipualtion Instructions Classified by Addressing

1st Operand \ 2nd Operand	CY	saddr.bit sfr.bit A.bit X.bit PSWL.bit PSWH.bit mem2.bit !addr16.bit !!addr24.bit	/saddr.bit /sfr.bit /A.bit /X.bit /PSWL.bit /PSWH.bit /mem2.bit /!addr16.bit /!!addr24.bit	None*
CY		MOV1 AND1 OR1 XOR1	AND1 OR1	NOT1 SET1 CLR1
saddr.bit sfr.bit A.bit X.bit PSWL.bit PSWH.bit mem2.bit !addr16.bit !!addr24.bit	MOV1			NOT1 SET1 CLR1 BF BT BTCLR BFSET

* There is no 2nd operand, or the 2nd operand is not an operand address.

(5) Call return instructions/branch instructions

CALL, CALLF, CALLT, BRK, RET, RETI, RETB, RETCS, RETCSB, BRKCS, BR, BNZ, BNE, BZ, BE, BNC, BNL, BC, BL, BNV, BPO, BV, BPE, BP, BN, BLT, BGE, BLE, BGT, BNH, BH, BF, BT, BTCLR, BFSET, DBNZ

Table 5-5 List of Call Return Instructions/Branch Instructions Classified by Addressing

Instruction Address operand	$addr20	$!addr20	!addr16	!!addr20	rp	rg	[rp]	[rg]	!addr11	[addr5]	RBn	None
Basic instructions	BC* BR	CALL BR	CALL BR RETCS RETCSB	CALL BR	CALL BR	CALL BR	CALL BR	CALL BR	CALLF	CALLF	BRKCS	BRK RET RETI RETB
Compound instructions	BF BT BTCLR BFSET DBNZ											

* BNZ, BNE, BZ, BE, BNC, BNL, BL, BNV, BPO, BV, BPE, BP, BN, BLT, BGE, BLE, BGT, BNH and BH are equivalent to BC.

(6) Other instructions

ADJBA, ADJBS, CVTBW, LOCATION, SEL, NOT, EI, DI, SWRS

6. ELECTRICAL SPECIFICATIONS (DESIRED VALUE)

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATING	UNIT
Supply voltage	V_{DD}		−0.5 to +7.0	V
	AV_{DD}		AVss to V_{DD}+0.5	V
	AVss		−0.5 to +0.5	V
Input voltage	V_I		−0.5 to V_{DD}+0.5	V
Output voltage	V_O		−0.5 to V_{DD}+0.5	V
Output current low	I_{OL}	One pin	15	mA
		Total of all output pins	150	mA
Output current high	I_{OH}	One pin	−10	mA
		Total of all output pins	−100	mA
A/D converter reference input voltage	AV_{REF1}		−0.5 to V_{DD}+0.3	V
D/A converter reference input voltage	AV_{REF2}		−0.5 to V_{DD}+0.3	V
	AV_{REF3}		−0.5 to V_{DD}+0.3	V
Operating temperature	T_{opt}		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

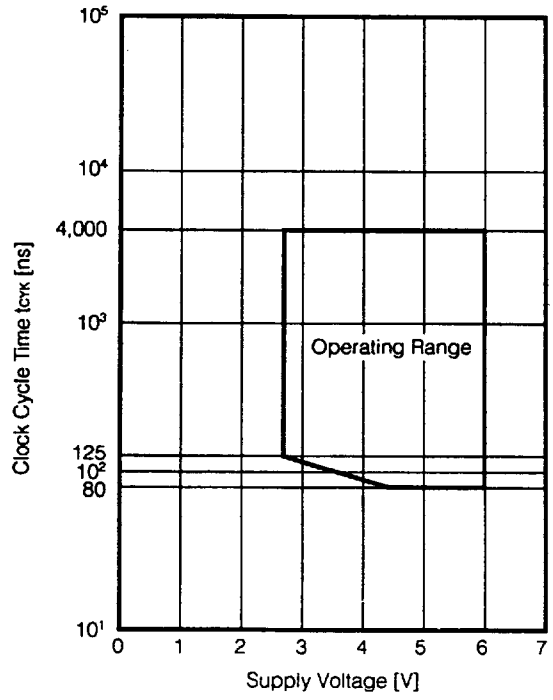
OPERATING CONDITION

Operating temperature (T_{opt}) : −40 to +85°C

Supply voltage and clock cycle time: **See Fig. 6-1.**

Rise/fall time (t_r, t_f) (Unspecified pin): 0 to 200 μs

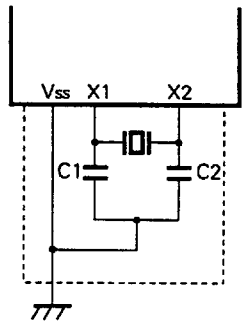
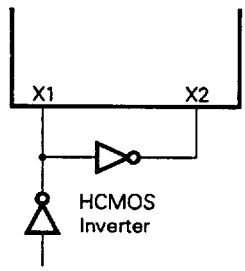
Fig. 6-1 Supply Voltage and Clock Cycle Time



CAPACITANCE (T_a = 25°C, V_{DD} = V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_I	f = 1 MHz Unmeasured pins returned to 0 V.			10	pF
Output capacitance	C_O				10	pF
I/O capacitance	C_{IO}				10	pF

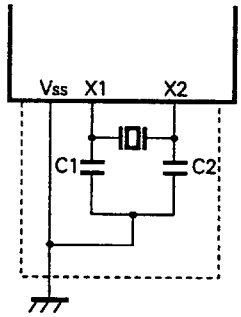
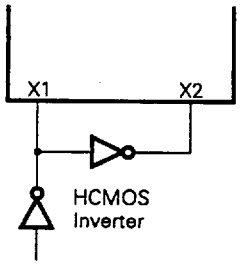
OSCILLATOR CHARACTERISTICS (T_a = −40 to +85°C, V_{DD} = +4.5 to +6.0 V, V_{SS} = 0 V)

RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	MIN.	MAX.	UNIT
Ceramic resonator or crystal resonator		Oscillator frequency (f_{XX})	4	25	MHz
External clock		X1 input frequency (f_X)	4	25	MHz
		X1 input rise/fall time (t_{XR}, t_{XF})	0	5	ns
		X1 input high/low-level width (t_{WXH}, t_{WXL})	20	130	ns

Note **When the clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by a dotted line to prevent the influence of wiring capacitance, etc.**

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed.**
- **Keep away from lines carrying a high fluctuating current.**
- **The oscillator capacitor grounding point should always be at the same potential as V_{SS}. Do not connect to a ground pattern carrying a high current.**
- **A signal should not be taken from the oscillator.**

OSCILLATOR CHARACTERISTICS (T_a = −40 to +85°C, V_{DD} = +2.7 to 6.0 V, V_{SS} = 0 V)

RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	MIN.	MAX.	UNIT
Ceramic resonator or crystal resonator		Oscillator frequency (f_{XX})	4	16	MHz
External clock		X1 input frequency (f_X)	4	16	MHz
		X1 input rise/fall time (t_{XR}, t_{XF})	0	10	ns
		X1 input high/low-level width (t_{WXH}, t_{WXL})	20	130	ns

Note **When the clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by a dotted line to prevent the influence of wiring capacitance, etc.**

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed.**
- **Keep away from lines carrying a high fluctuating current.**
- **The oscillator capacitor grounding point should always be at the same potential as V_{SS}. Do not connect to a ground pattern carrying a high current.**
- **A signal should not be taken from the oscillator.**

DC CHARACTERISTICS (T_a = −40 to +85°C, V_{DD} = 2.7 to 6.0 V) (1/2)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input voltage low	V_{IL1}	Except pins of *1, *2, *3 and *4	−0.3		0.3V_{DD}	V
	V_{IL2}	Pins of *1, *2, *3 and *4	−0.3		0.2V_{DD}	V
	V_{IL3}	V_{DD} = +5.0 V ±10% Pins of *2, *3 and *4	−0.3		+0.8	V
Input voltage high	V_{IH1}	Except pins of *1	0.7V_{DD}		V_{DD}+0.3	V
	V_{IH2}	Pins of *1	0.8V_{DD}		V_{DD}+0.3	V
	V_{IH3}	V_{DD} = +5.0 V ±10% Pins of *2, *3 and *4	2.2		V_{DD}+0.3	V
Output voltage low	V_{OL1}	I_{OL} = 20 μA			0.1	V
	V_{OL2}	I_{OL} = 100 μA			0.2	V
	V_{OL3}	I_{OL} = 2 mA			0.4	V
	V_{OL4}	V_{DD} = 4.5 to 6.0 V I_{OL} = 8.0 mA Pins of *2 and *5			1.0	V
Output voltage high	V_{OH1}	I_{OH} = 20 μA	V_{DD}−0.1			V
	V_{OH2}	I_{OH} = 100 μA	V_{DD}−0.2			V
	V_{OH3}	I_{OH} = −2 mA	V_{DD}−0.4			V
	V_{OH4}	V_{DD} = 4.5 to 6.0 V I_{OH} = −5.0 mA Pins of *4	V_{DD}−1.0			V
X1 input current low	I_{IL}	When EXTC = 0 0 V ≤ V_I ≤ V_{IL2}			−100	μA
X1 input current high	I_{IH}	When EXTC = 0 V_{IH2} ≤ V_I ≤ V_{DD}			+100	μA

* 1. X1, X2 $\overline{\text{RESET}}$, P12/ASCK2/$\overline{\text{SCK2}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK/$\overline{\text{SCK1}}$, P26/INTP5, P27/SIO, P32/$\overline{\text{SCK0}}$, P33/SO/SB0, TEST

2. P40/AD0-P47/AD7, P50/A8-P57/A15
3. P60/A16-P63/A19, P64/$\overline{\text{RD}}$, P65/$\overline{\text{WR}}$, P66/$\overline{\text{WAIT}}$/HLDRQ, P67/$\overline{\text{REFRQ}}$/HLDAK
4. P00-P07
5. P10-P17

DC CHARACTERISTICS (T_a = −40 to +85°C, V_{DD} = 2.7 to 6.0 V) (2/2)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input leak current	I_{LI}	0 V ≤ V_I ≤ V_{DD} (Except X1 pin when EXTC = 0)				± 5	μA
Output leak current	I_{LO}	0 V ≤ V_O ≤ V_{DD}				± 5	μA
V_{DD} supply current	I_{DD1}	Operating mode	f_{XX} = 25 MHz		30	60	mA
			f_{XX} = 16 MHz V_{DD} = 2.7 to 3.3 V		12	25	mA
	I_{DD2}	HALT mode	f_{XX} = 25 MHz		12	30	mA
			f_{XX} = 16 MHz V_{DD} = 2.7 to 3.3 V		5	12	mA
	I_{DD3}	IDLE mode (EXTC=0)	f_{XX} = 25 MHz		1.5	3	mA
			f_{XX} = 16 MHz V_{DD} = 2.7 to 3.3 V		0.6	1.2	mA
Data retention voltage	V_{DDDR}	STOP mode, IDLE mode		2.0		6.0	V
Data retention current	I_{DDDR1}	STOP mode IDLE mode (EXTC=1)	V_{DD} = 2.5 V		2	10	μA
			V_{DD} = 4.5 to 6.0 V		10	50	μA
Pull-up resistance	R_L	V_I = 0 V V_{DD} = 4.5 to 6.0 V		15	40	80	kΩ
		V_I = 0 V V_{DD} = 2.7 to 4.5 V		20		500	kΩ

AC CHARACTERISTICS (T_a = −40 to +85°C, V_{DD} = 2.7 to 6.0 V)

(1) Read/write operation

PARAMETER	SYMBOL	CONDITIONS, FORMULA	MIN.	MAX.	UNIT
Address setup time	t_{SAST}	(0.5 + a) T−24	16		ns
Address hold time (from ASTB↓)	t_{HSTLA}	0.5T−14	26		ns
Address hold time (from ASTB↑)	t_{HSTHA}		0		ns
ASTB high-level width	t_{WSTH}	(0.5 + a) T−17	23		ns
Address hold time (from $\overline{RD}$↑)	t_{HRA}	0.5T−14	26		ns
$\overline{RD}$↓ delay time from address	t_{DAR}	T−30	50		ns
$\overline{RD}$↓ address float time	t_{FRA}			24	ns
Data input time from address	t_{DAID}	(2.5 + a + n) T−44		156	ns
Data input time from ASTB↓	t_{DSTID}	(2 + n) T−20		140	ns
Data input time from $\overline{RD}$↓	t_{DRID}	(1.5 + n) T−40		80	ns
$\overline{RD}$↓ delay time from ASTB↓	t_{DSTR}	0.5T−16	24		ns
Data hold time (from $\overline{RD}$↑)	t_{HRID}		0		ns
Address active time from $\overline{RD}$↑	t_{DRA}	0.5T−14	26		ns
ASTB↑ delay time from $\overline{RD}$↑	t_{DRST}	0.5T−14	26		ns
$\overline{RD}$ low-level width	t_{WRL}	(1.5 + n) T−15	105		ns
$\overline{WR}$↓ delay time from address	t_{DAW}	T−30	50		ns
Address hold time (from $\overline{WR}$↑)	t_{HWA}	0.5T−14	26		ns
Data output delay from ASTB↓	t_{DSTOD}	T+30		120	ns
Data output delay from $\overline{WR}$↓	t_{DWOD}	0.5T−11		29	ns
$\overline{WR}$↓ output delay time from ASTB↓	t_{DSTW}	0.5T−16	24		ns
Data setup time (to $\overline{WR}$↑)	t_{SODW}	(1 + n) T−5	75		ns
Data hold time (from $\overline{WR}$↑)	t_{HWOD}	*	26		ns
ASTB↑ delay time from $\overline{WR}$↑	t_{DWST}	0.5T−14	26		ns
$\overline{WR}$ low-level width	t_{WWL}	(1.5 + n) T−15	105		ns

* The hold time includes a time when V_{OH1} and V_{OL1} are retained in the load condition of C_L = 50 pF and R_L = 4.7 kΩ.

Remarks T : t_{CYK} (System clock cycle time)
a : Address wait is 1, otherwise 0.
n : Number of waits (n ≥ 1)

(2) External wait/bus hold/refresh timing

PARAMETER	SYMBOL	CONDITIONS, FORMULA	MIN.	MAX.	UNIT
$\overline{WAIT}$↓ input time from address	t_{DAWT}	1.5T–50		70	ns
$\overline{WAIT}$↓ input time from ASTB↓	t_{DSTWT}	T–40		40	ns
$\overline{WAIT}$ hold time from ASTB↓	t_{HSTWT}	nT + 10	90		ns
$\overline{WAIT}$↑ delay time from ASTB↓	t_{DSTWTH}	(1 + n) T–30		130	ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{DRWTL}	0.5T–40		0	ns
$\overline{WAIT}$ hold time from $\overline{RD}$↓	t_{HRWT}	(n – 0.5) T+5	45		ns
$\overline{WAIT}$↑ delay time from $\overline{RD}$↓	t_{DRWTH}	(n + 0.5) T–60		60	ns
Data input time from $\overline{WAIT}$↑	t_{DWTID}	T–20		60	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑	t_{DWTW}	T–10	70		ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑	t_{DWTR}	T–10	70		ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{DWWTL}	0.5T–40		0	ns
$\overline{WAIT}$ hold time from $\overline{WR}$↓	t_{HWWT}	(n – 0.5) T+5	45		ns
$\overline{WAIT}$↑ delay time from $\overline{WR}$↓	t_{DWWTH}	(n + 0.5) T–60		60	ns
Float delay time from HLDRQ↑	t_{FHQC}	To be decided			ns
HLDAK↑ delay time from HLDRQ↑	$t_{DHQHHAH}$	To be decided			ns
HLDAK↑ delay time from float	t_{DCFHA}	To be decided			ns
HLDAK↓ delay time from HLDRQ↓	$t_{DHQLHAL}$	To be decided			ns
Active delay time from HLDAK↓	t_{DHAC}	To be decided			ns
Random read/write cycle time	t_{RC}	3T	240		ns
$\overline{REFRQ}$ low-level pulse width	t_{WRFQL}	1.5T–15	105		ns
$\overline{REFRQ}$ delay time from ASTB↓	t_{DSTRFQ}	0.5T–14	26		ns
$\overline{REFRQ}$ delay time from $\overline{RD}$↑	t_{DRRFQ}	To be decided			ns
$\overline{REFRQ}$ delay time from $\overline{WR}$↑	t_{DWRFQ}	To be decided			ns
ASTB delay time from $\overline{REFRQ}$↑	t_{DRFQST}	0.5T–14	26		ns
$\overline{REFRQ}$ high-level pulse width	t_{WRFQH}	1.5T–15	105		ns

Remarks T : t_{CYK} (System clock cycle time)
n : Number of waits (n ≥ 1)

SERIAL OPERATION (CSI)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	MAX.	UNIT
Serial clock cycle time ($\overline{SCK}$)	t_{CYSK0}	Input	External clock	500		ns
		Output		T		μs
Serial clock low-level width ($\overline{SCK}$)	t_{WSKL0}	Input	External clock	210		ns
		Output		0.5T–40		ns
Serial clock high-level width ($\overline{SCK}$)	t_{WSKH0}	Input	External clock	210		ns
		Output		0.5T–40		ns
SI, SB0 setup time (to $\overline{SCK}$↑)	t_{SSSK0}			80		ns
SI, SB0 hold time (from $\overline{SCK}$↑)	t_{HSK0}			80		ns
SO, SB0 output delay time (from $\overline{SCK}$↓)	t_{DSBSK1}	CMOS push-pull output (3-wire serial I/O mode)		0	150	ns
	t_{DSBSK2}	Open-drain output (SBI mode), R_L = 1 kΩ		0	400	ns
SO, SB0 output hold time (from $\overline{SCK}$↑)	t_{HSBSK1}	Data transfer		$0.5t_{CYSK0}$–80		ns
SB0 high hold time (from $\overline{SCK}$↑)	t_{HSBSK2}	SBI mode		4		t_{CYX}
SB0 low setup time (to $\overline{SCK}$↓)	t_{SSBSK}			4		t_{CYX}
SB0 low-level width	t_{WSBL}			4		t_{CYX}
SB0 high-level width	t_{WSBH}			4		t_{CYX}

Remarks
1. Values in the table apply when f_{XX} = 25 MHz and C_L = 100 pF.
2. t_{CYX} = 1/fxx
3. T : Serial clock cycle set by software, the minimum is 16/fxx.

SERIAL OPERATION (IOE1, IOE2)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	MAX.	UNIT
Serial clock cycle time ($\overline{SCK1}$, $\overline{SCK2}$)	t_{CYSK1}	Input	External clock	320		ns
		Output	Internal division by 16	T		μs
Serial clock low-level width ($\overline{SCK1}$, $\overline{SCK2}$)	t_{WSKL1}	Input	External clock	120		ns
		Output	Internal division by 16	0.5T–40		ns
Serial clock high-level width ($\overline{SCK1}$, $\overline{SCK2}$)	t_{WSKH1}	Input	External clock	120		ns
		Output	Internal division by 16	0.5T–40		ns
SI1, SI2 setup time (to $\overline{SCK}$↑)	t_{SSSK1}			80		ns
SI1, SI2 hold time (from $\overline{SCK}$↑)	t_{HSSK1}			80		ns
SI1, SI2 output delay time (from $\overline{SCK}$↓)	t_{DSOSK}			0	150	ns
SO, SO2 output hold time (from $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{HSOSK}	Data transfer		$0.5t_{CYSK1}$–80		ns

Remarks
1. Values in the table apply when C_L = 100 pF.
2. t_{CYX} = 1/fxx
3. T : Serial clock cycle set by software, the minimum is 16/fxx.

SERIAL OPERATION (UART, UART2)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
ASCK clock input cycle time	t_{CYASK}		200		ns
ASCK clock low-level width	t_{WASKL}		60		ns
ASCK clock high-level width	t_{WASKH}		60		ns

OTHER OPERATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
NMI low-level width	t_{WNIL}		10		μs
NMI high-level width	t_{WNIH}		10		μs
INTP0 low-level width	t_{WIT0L}		3		t_{CYSMP}
INTP0 high-level width	t_{WIT0H}		3		t_{CYSMP}
INTP1-INTP3, CI low-level width	t_{WIT1L}		3		t_{CYCPU}
INTP1-INTP3, CI high-level width	t_{WIT1H}		3		t_{CYCPU}
INTP4, INTP5 low-level width	t_{WIT2L}		10		μs
INTP4, INTP5 high-level width	t_{WIT2H}		10		μs
$\overline{\text{RESET}}$ low-level width	t_{WRSL}		10		μs
$\overline{\text{RESET}}$ high-level width	t_{WRSH}		10		μs

Remarks 1. t_{CYSMP} : Sampling clock set by software
2. t_{CYCPU} : CPU operating clock set by CPU software

CLOCK OUTPUT OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
CLKOUT cycle time	t_{CYCL}	nT	80	1280	ns
CLKOUT low-level width	t_{CLL}	V_{DD} = 4.5 to 6.0 V 0.5T–10	30	630	ns
		0.5T–20	20	620	ns
CLKOUT high-level width	t_{CLH}	V_{DD} = 4.5 to 6.0 V 0.5T–10	30	630	ns
		0.5T–20	20	620	ns
CLKOUT rise time	t_{CLR}	V_{DD} = 4.5 to 6.0 V		10	ns
				20	ns
CLKOUT fall time	t_{CLF}	V_{DD} = 4.5 to 6.0 V		10	ns
				20	ns

Remarks n : Scaling factor set by CPU software
T : t_{CYK} (System clock cycle time)

A/D CONVERTER CHARACTERISTICS (T_a = 40 to +85°C, AV_{DD} = V_{DD} = 2.7 to 6.0 V, 3.4 V ≤ AV_{REF1} ≤ AVss, AVss = Vss = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Resolution			8			bit
Overall error *		4.0 V ≤ AV_{REF1} ≤ AVss T_a = −40 to +85°C			0.6	%
		2.7 V ≤ AV_{REF1} ≤ AVss T_a = −40 to +85°C			0.8	%
		4.0 V ≤ AV_{REF1} ≤ AVss T_a = −10 to +70°C			0.4	%
Quantization error					±1/2	LSB
Conversion time	t_{CONV}	V_{DD} = 4.5 to 6.0 V 80 ns ≤ t_{CYK} ≤250 ns, FR = 1	120			t_{CYK}
		80 ns ≤ t_{CYK} ≤ 250 ns, FR = 0	180			t_{CYK}
Sampling time	t_{SAMP}	V_{DD} = 4.5 to 6.0 V 80 ns ≤ t_{CYK} ≤ 250 ns, FR = 1	24			t_{CYK}
		80 ns ≤ t_{CYK} ≤250 ns, FR = 0	36			t_{CYK}
Analog input voltage	V_{IAN}		−0.3		AV_{REF1}+0.3	V
Analog input impedance	R_{AN}			1000		MΩ
Reference voltage	AV_{REF1}		2.7		AV_{DD}	V
AV_{REF1} current	AI_{REF1}	CS = 1, V_{DD} = +5.0 V		0.5	1.5	mA
		STOP mode or CS = 0 V_{DD} = +5.0 V		0.2	0.7	mA
AV_{DD} supply current	AI_{DD1}	fxx = 25 MHz		1.5	3.0	mA
	AI_{DD2}	STOP mode, CS = 0		10	20	μA

* Quantization error is not included. Represented by the ratio to full-scale value.

D/A CONVERTER CHARACTERISTICS (T_a = −40 to +85°C, AV_{REF2} = AV_{DD} = V_{DD} = 2.7 to 6.0 V, AV_{REF3} = AV_{SS} = V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Resolution				8			bit
Overall error		Load condition 4 MΩ, 30 pF	V_{DD} = 4.5 to 6.0 V			0.4	%
						0.6	%
			V_{DD} = 4.5 to 6.0 V AV_{REF2} = 0.75 V_{DD} AV_{REF3} = 0.25 V_{DD}			0.6	%
			AV_{REF2} = 0.75 V_{DD} AV_{REF3} = 0.25 V_{DD}			0.8	%
		Load condition 2 MΩ, 30 pF	V_{DD} = 4.5 to 6.0 V			0.6	%
						0.8	%
			V_{DD} = 4.5 to 6.0 V AV_{REF2} = 0.75 V_{DD} AV_{REF3} = 0.25 V_{DD}			0.8	%
			AV_{REF2} = 0.75 V_{DD} AV_{REF3} = 0.25 V_{DD}			1.0	%
Settling time		Load condition 2 MΩ, 30 pF				10	μs
Output resistance	R_O	*			20		kΩ
Analog reference voltage	AV_{REF2}				0.75 V_{DD}	V_{DD}	V
Analog reference voltage	AV_{REF3}					0.25 V_{DD}	V
Reference power supply input current	AI_{REF2}				0	5	mA
Reference power supply input current	AI_{REF3}				−5	0	mA

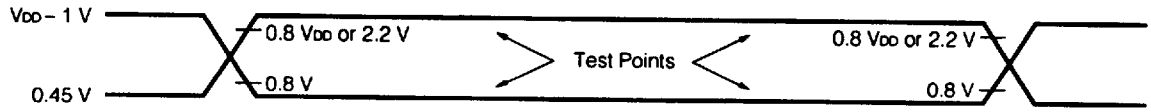
* DACS0, DACS1 = 7FH

DATA RETENTION CHARACTERISTICS (T_a = –40 to +85°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention voltage	V_{DDDR}	STOP mode	2.0		6.0	V
Data retention current	I_{DDDR}	V_{DDDR} = 2.5 V		2	10	μA
		V_{DDDR} = 5 V ±10%		5	20	μA
V_{DD} rise time	t_{RVD}		200			μs
V_{DD} fall time	t_{FVD}		200			μs
V_{DD} retention time (from STOP mode setting)	t_{HVD}		0			ms
STOP release signal input time	t_{DREL}		0			ms
Oscillation stabilization wait time	t_{WAIT}	Crystal resonator	30			ms
		Ceramic resonator	5			ms
Input voltage low	V_{IL}	Specific pin *	0		0.1V_{DDDR}	V
Input voltage high	V_{IH}		0.9V_{DDDR}		V_{DDDR}	V

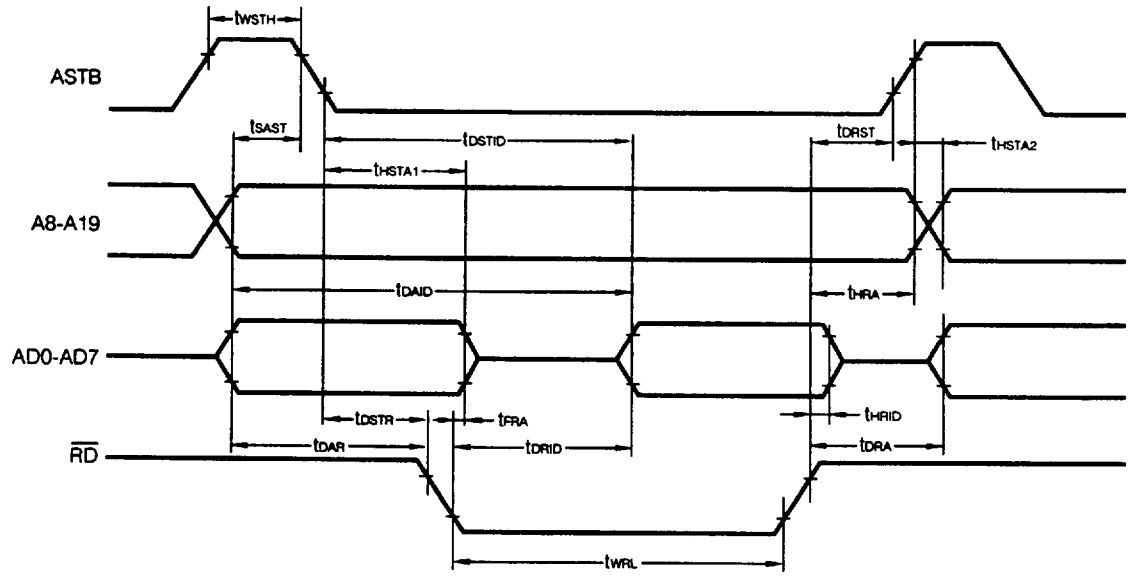
* $\overline{\text{RESET}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK/$\overline{\text{SCK1}}$, P26/INTP5, P27/SIO, P32/$\overline{\text{SCK0}}$, P33/SO0/SB0 pins

AC Timing Test Points

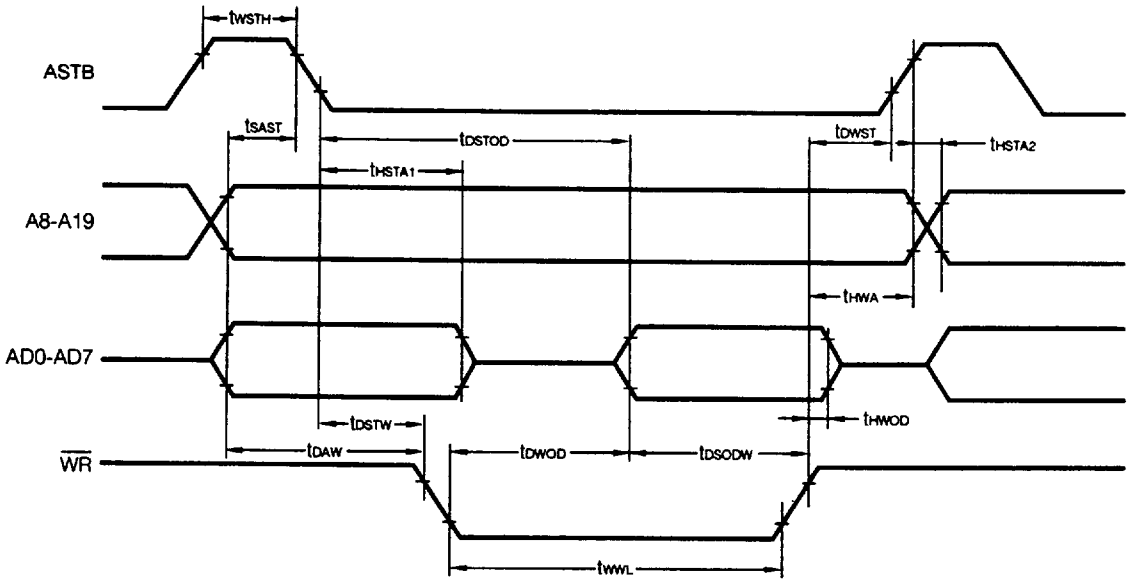


Timing Waveform

Read operation

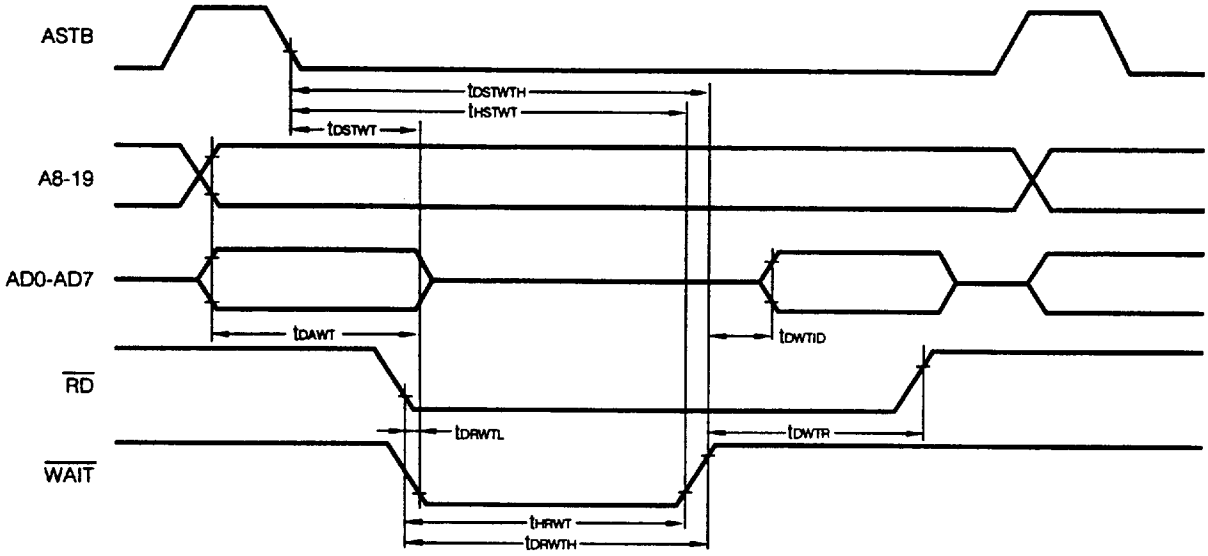


Write operation

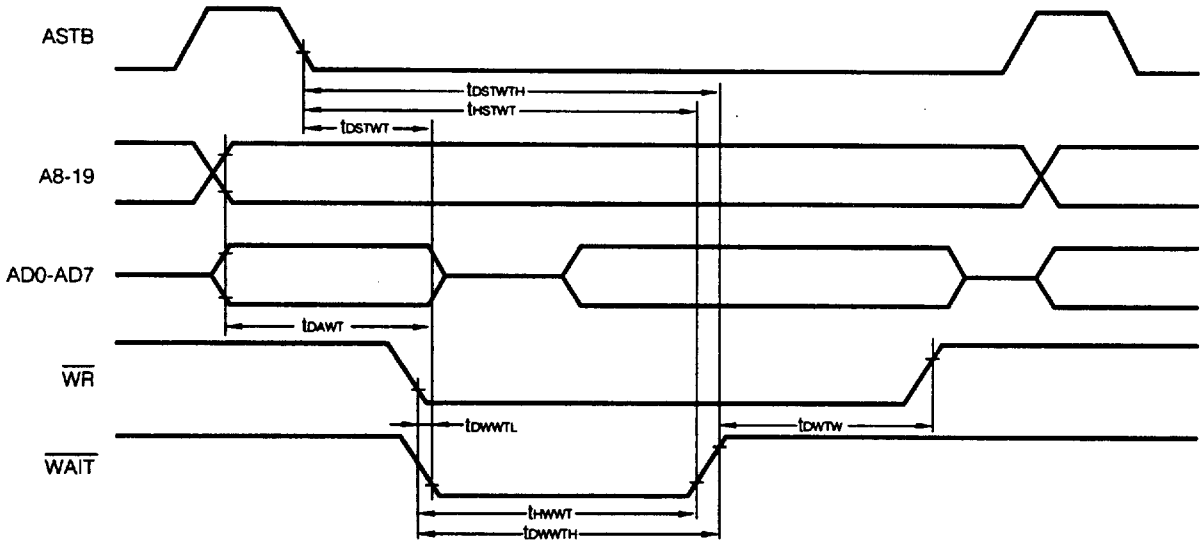


External WAIT Signal Input Timing

Read operation

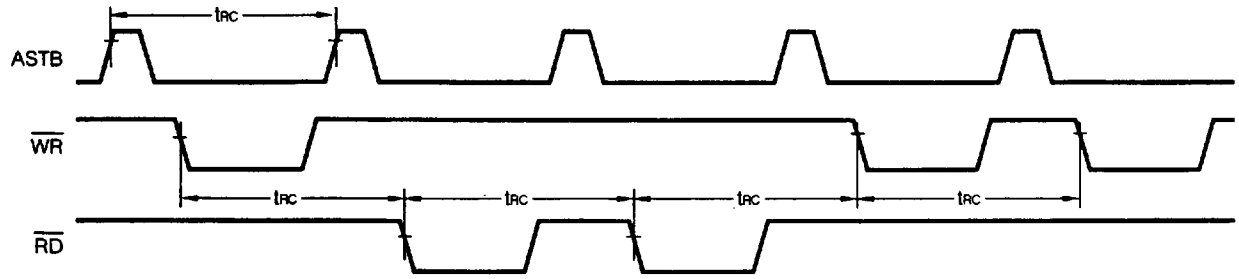


Write operation

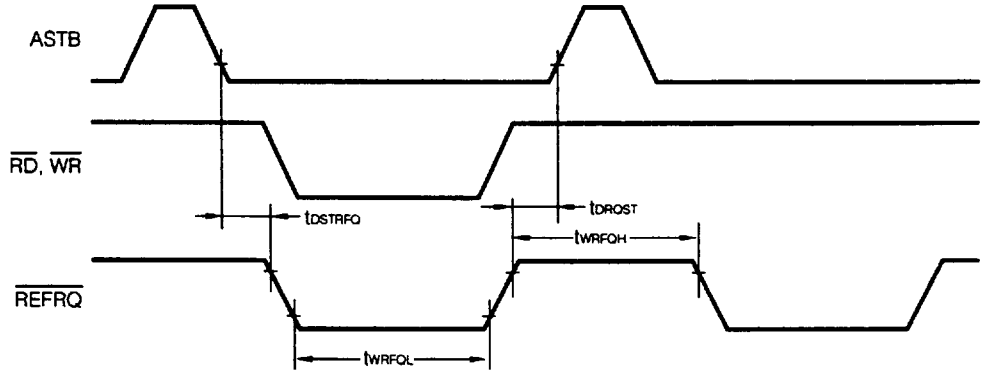


Refresh Timing Waveform

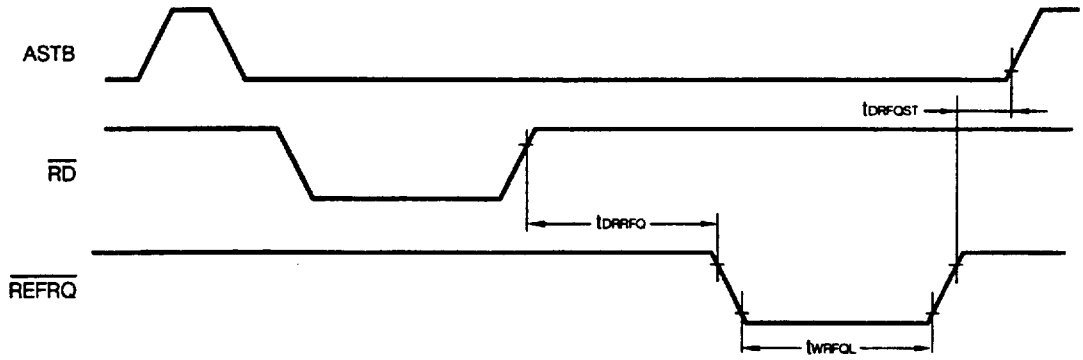
Random read/write cycle



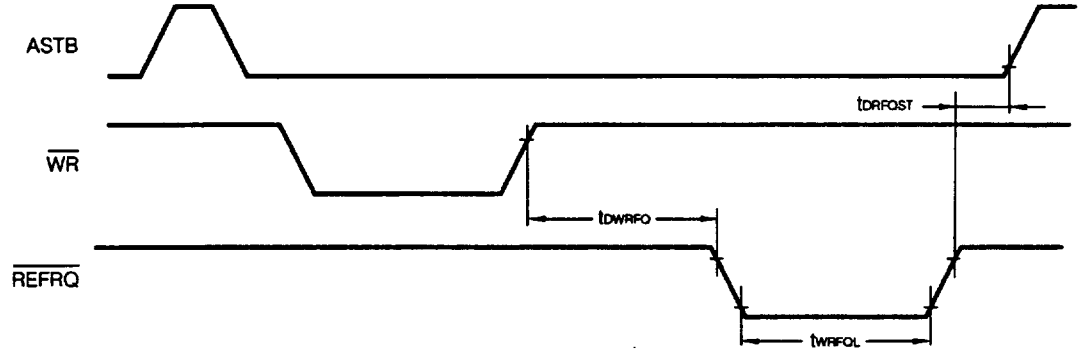
When refresh memory is accessed simultaneously



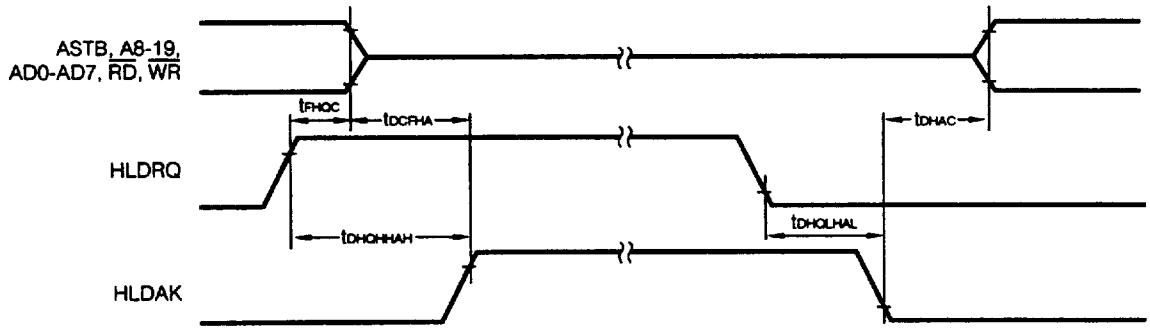
Refreshing after read



Refreshing after write

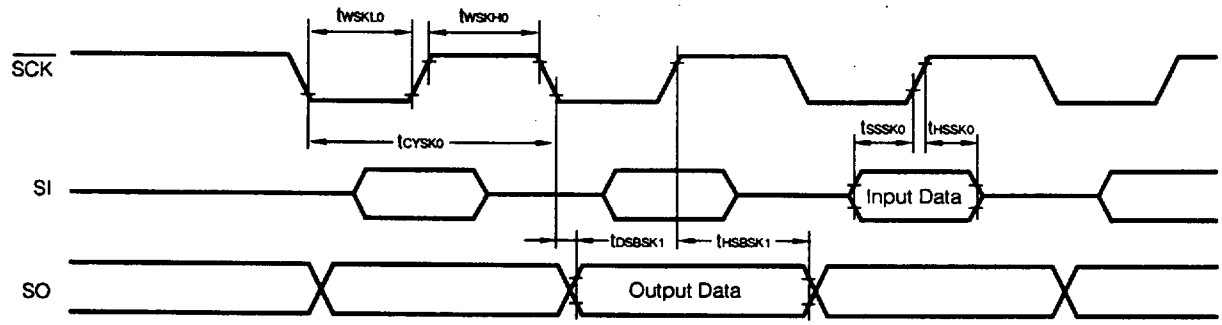


Hold timing



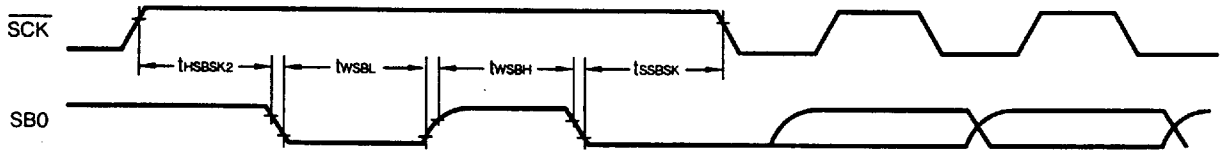
Serial operation (CSI)

3-wire serial I/O mode

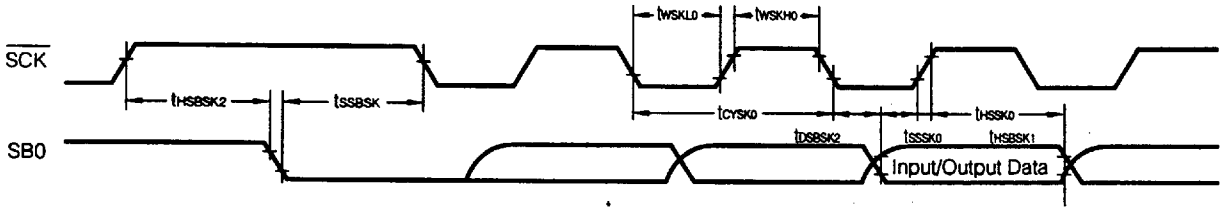


SBI mode

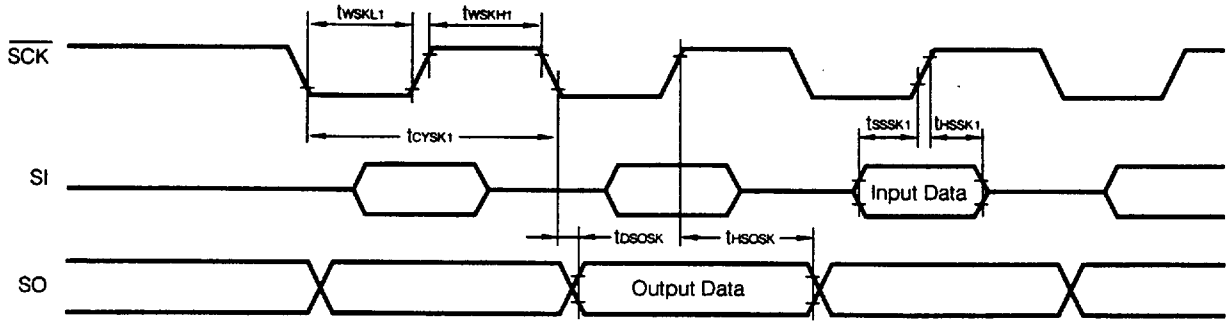
Bus release signal transfer



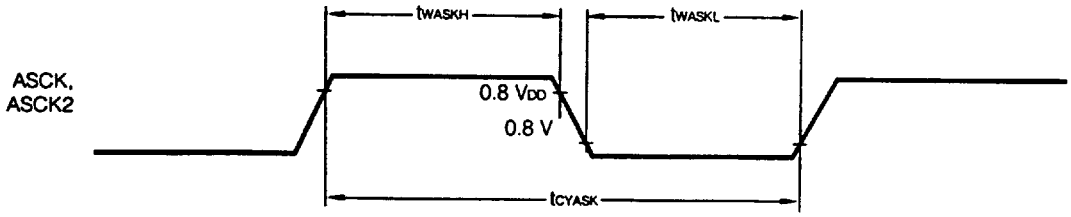
Command signal transfer



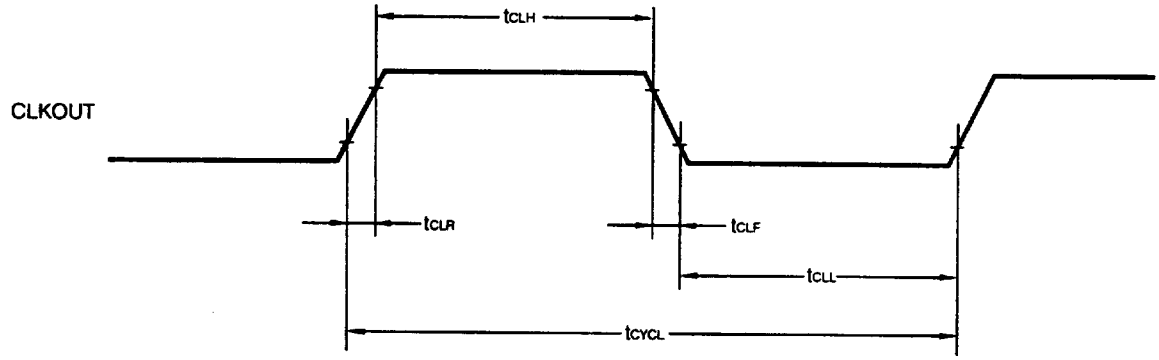
Serial operation (IOE1, IOE2)



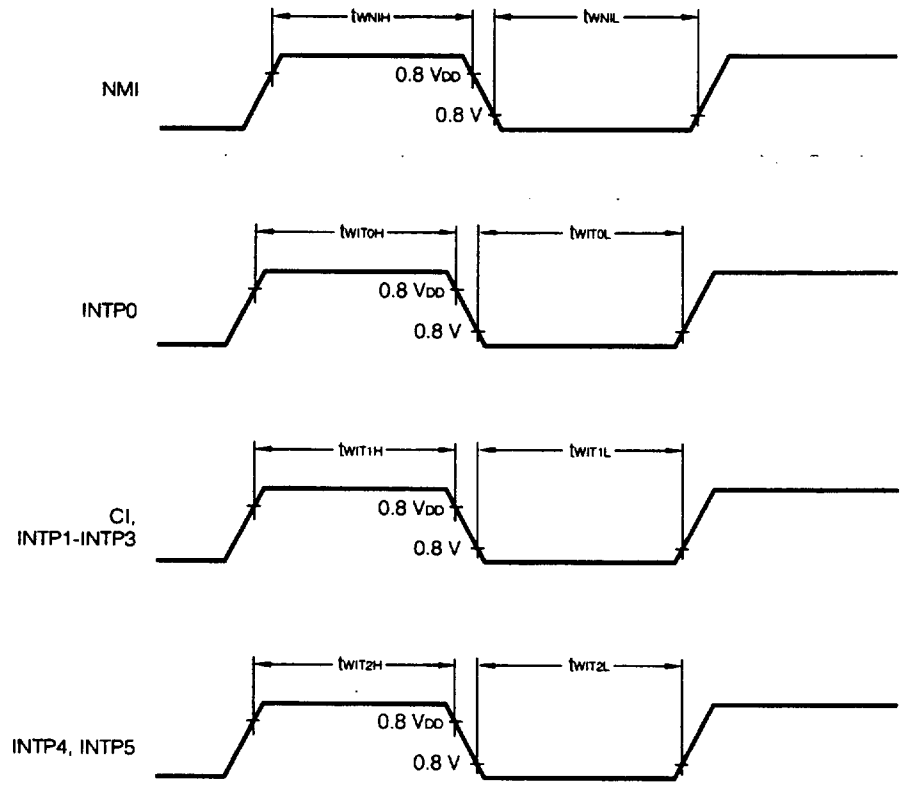
Serial Operation (UART, UART2)



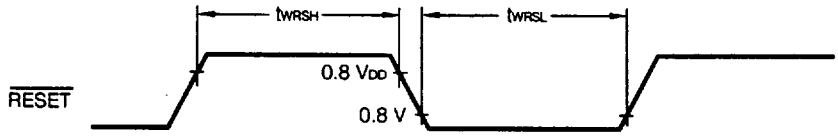
Clock Output Timing



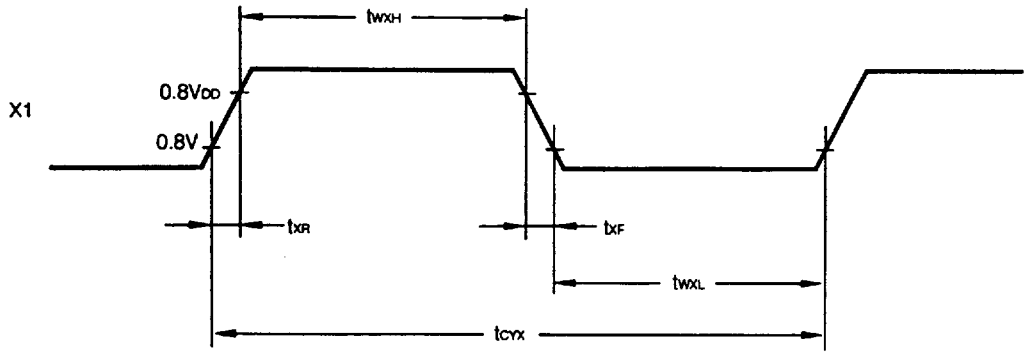
Interrupt Input Timing



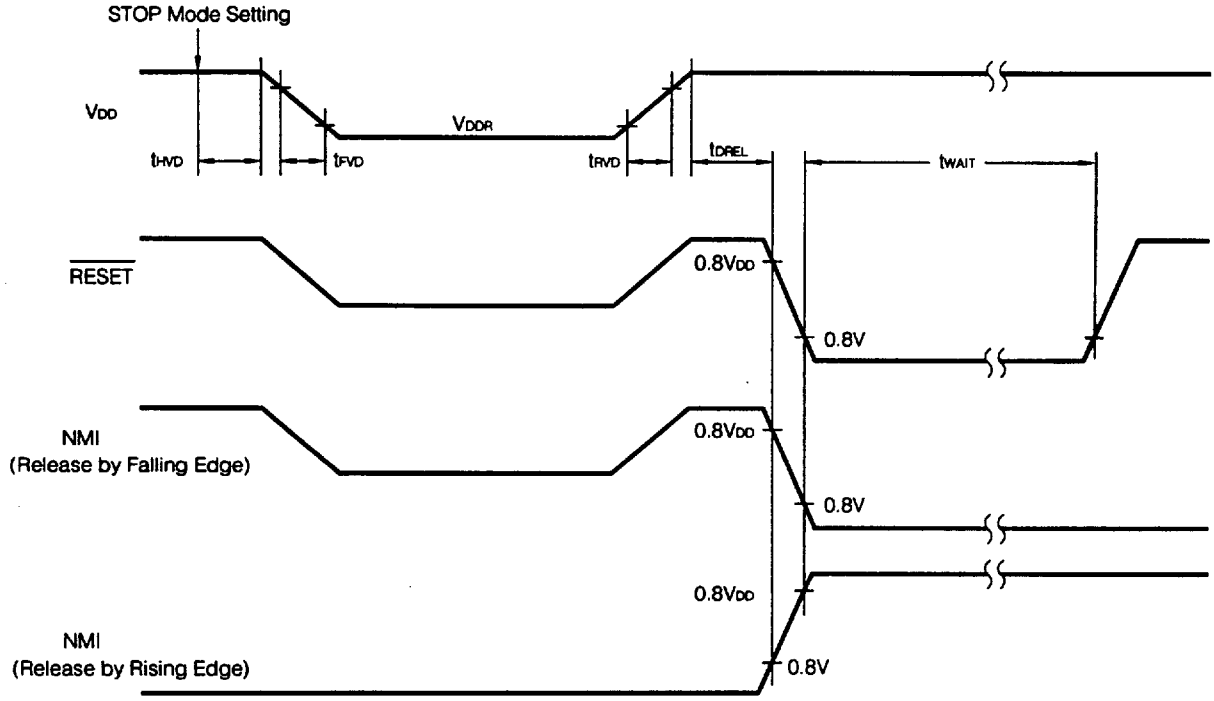
Reset Input Timing



External Clock Timing

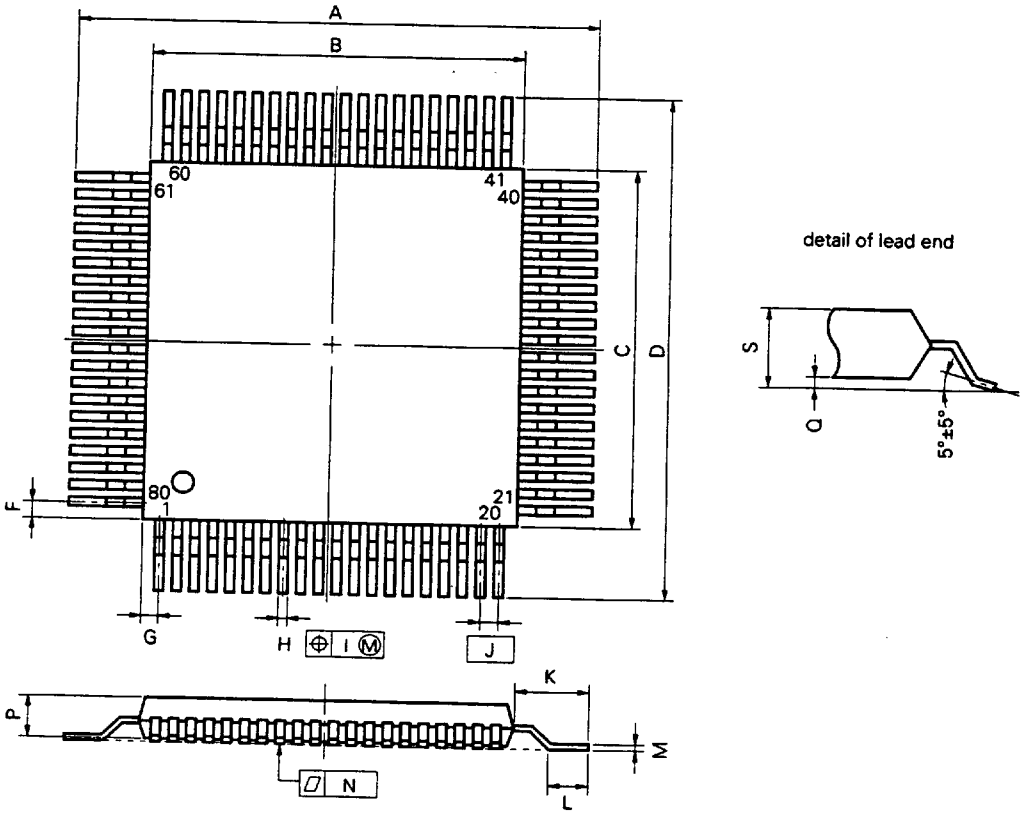


Data Retention Characteristics



7. PACKAGE INFORMATION

80 PIN PLASTIC QFP (□14)



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S80GC-65-3B9-3

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.8	0.031
G	0.8	0.031
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

8. RECOMMENDED SOLDERING CONDITIONS

Undefined

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using μPD784025/784026.

Language Processing Software

RA78K/IV*	78K/IV series common assembler package
CC78K/IV*	78K/IV series common C compiler package
CC78K/IV-L*	78K/IV series common C compiler library source file

PROM Writing Tools

PG-1500	PROM programmer
PA-78P4026GC PA-78P4026KK-T	Programmer adapters connected to PG-1500
PG-1500 Controller *	PG-1500 control program

Debugging Tools

IE-784000-R	μPD784026 subseries common in-circuit emulator
IE-784000-R-BK	78K/IV series common break board
IE-784000-R-SV (Provisional name) IE-784026-R-EM1 IE-784000-R-EM	μPD784026 subseries evaluation emulation boards
IE-70000-98-IF-A	Interface adapter and cable when using PC-9800 series (except notebook size personal computers) as a host machine
IE-780000-98N-IF	Interface adapter and cable when using a PC-9800 series notebook size personal computer as a host machine
IE-70000-PC-IF-A	Interface adapter and cable when using IBM PC/AT™ as a host machine
EP-78230GC-R	μPD784026 subseries common emulation probe
EV-9200GC-80	Socket to be mounted on a target system board made for 80-pin plastic QFP
EV-9900	Tool used when removing μPD78P4026KK-T from EV-9200GC-80
SD78K/IV*	IE-78400-R screen debugger
DF784026*	μPD784026 subseries device file

Real-Time OS

RX78K/IV*	78K/IV series common real-time OS

* PC-9800 series (MS-DOS™) based, IBM PC/AT (PC DOS™) based

APPENDIX B. RELATED DOCUMENTS ★

Device Related Documents

Document Name	Document No. (Japanese)	Document No. (English)
μPD784026 Series User's Manual (Preliminary) Hardware Volume	IEU-850	–
78K/IV Series User's Manual (Preliminary) Instruction Volume	IEU-844	IEU-1291
78K/IV Series Instruction Application Table	IEM-5580	–
78K/IV Series Instruction Set	IEM-5572	–
μPD784026 Series Special Function Register Application Table	IEM-5579	–

Development Tool Related Documents (User's Manuals)

Document Name		Document No. (Japanese)	Document No. (English)
RA78K Series Assembler Package	Operation Volume	In preparation	In preparation
	Language Volume	In preparation	In preparation
RA78K Series Structured Assembler Preprocessor		In preparation	In preparation
CC78K Series C Compiler	Operation Volume	In preparation	In preparation
	Language Volume	In preparation	In preparation
CC78K Series Library Source File		In preparation	In preparation
PG-1500 PROM Programmer		EEU-651	EEU-1335
PG-1500 Controller		EEI-704	EEU-1291
IE-784000-R In-Circuit Emulator		In preparation	In preparation
IE-784000-R-EM		In preparation	In preparation
IE-784026-R-EM1		In preparation	In preparation
EB-784026		In preparation	In preparation
SD78K/IV Screen Debugger	Primer	In preparation	In preparation
	Reference	In preparation	In preparation

Real-Time OS

RX78K/IV Real-Time OS	In preparation	In preparation

Other Related Documents

Document Name	Document No. (Japanese)	Document No. (English)
QTOP Microcomputer Brochure	IB-5040	–
Package Manual	IEI-635	IEI-1213
Surface Mount Technology Manual	IEI-616	IEI-1207
Quality Grades on Semiconductor Devices	IEI-620	IEI-1209
NEC Semiconductor Device Reliability & Quality Control	IEM-5068	–
Electrostatic Discharge (ESD) Test	MEM-539	–
Semiconductor Devices Quality Control Guarantee Guide	MEI-603	MEI-1202
Microcomputer Related Products Guide Other Manufacturers Volume	MEI-604	–

Note **The information in these related documents is subject to change without notice. For design purposes, etc., be sure to use the latest documents.**