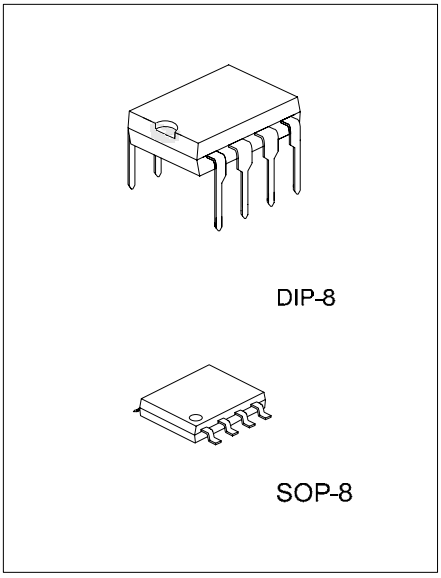
UC3848

LINEAR INTEGRATED CIRCUIT

HIGH PERFORMANCE CURRENT MODE CONTROLLERS



*Pb-free plating product number: UC3848L

■ DESCRIPTION

The UTC **UC3848** is designed to provide several special enhancements to satisfy the needs: Power-Saving mode for low standby power, Over Current Protection (OCP), Over Voltage Protection (OVP), Over Load Protection (OLP), Over Temperature Protection (OTP) etc protection features. IC will be shutdown when either protection arise and can auto-restart. UVLO featuring typical start-up current 20μA, and $V_{CC(ON)}$ 12.6V, $V_{CC(OFF)}$ 8.1V. Lower typical operation current Icc 3.7mA at inactive output. The output stage, suitable for driving N-Channel MOSFETs, can operate to duty cycles approach 70%. The **UC3848** are fully pin-to-pin compatible with UC3842 except V_{REF}-pin and NC-pin. V_{REF}-pin's application as application circuits. Pin FB with an 4kΩ pull up resistor to internal reference voltage. The **UC3848** also have soft-start function avoiding overshoot, and controlled driver output rise edge time t_R for low EMI.

■ FEATURES

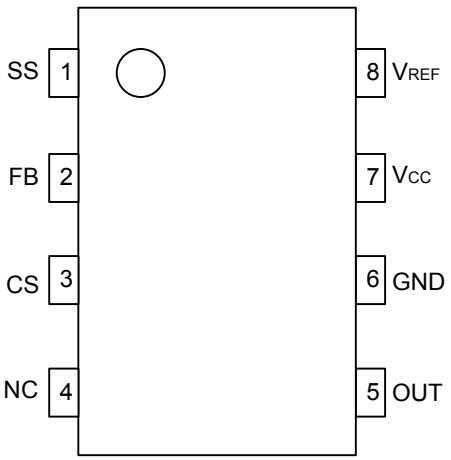
* Low startup and operation current
* 68kHz switching frequency
* Max duty cycle 70%
* Power-saving mode for low power
* Under voltage lockout with hysteresis
* Over temperature protection
* Overload protection
* Over voltage protection
* Leading edge blanking
* Soft start

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Normal	Lead Free Plating		
UC3848-D08-T	UC3848L-D08-T	DIP-8	Tube
UC3848-S08-R	UC3848L-S08-R	SOP-8	Tape Reel
UC3848-S08-T	UC3848L-S08-T	SOP-8	Tube

UC3848L-D08-T (1)Packing Type (2)Package Type (3)Lead Plating	(1) R: Tape Reel, T: Tube (2) D08: DIP-8, S08: SOP-8 (3) L: Lead Free Plating, Blank: Pb/Sn

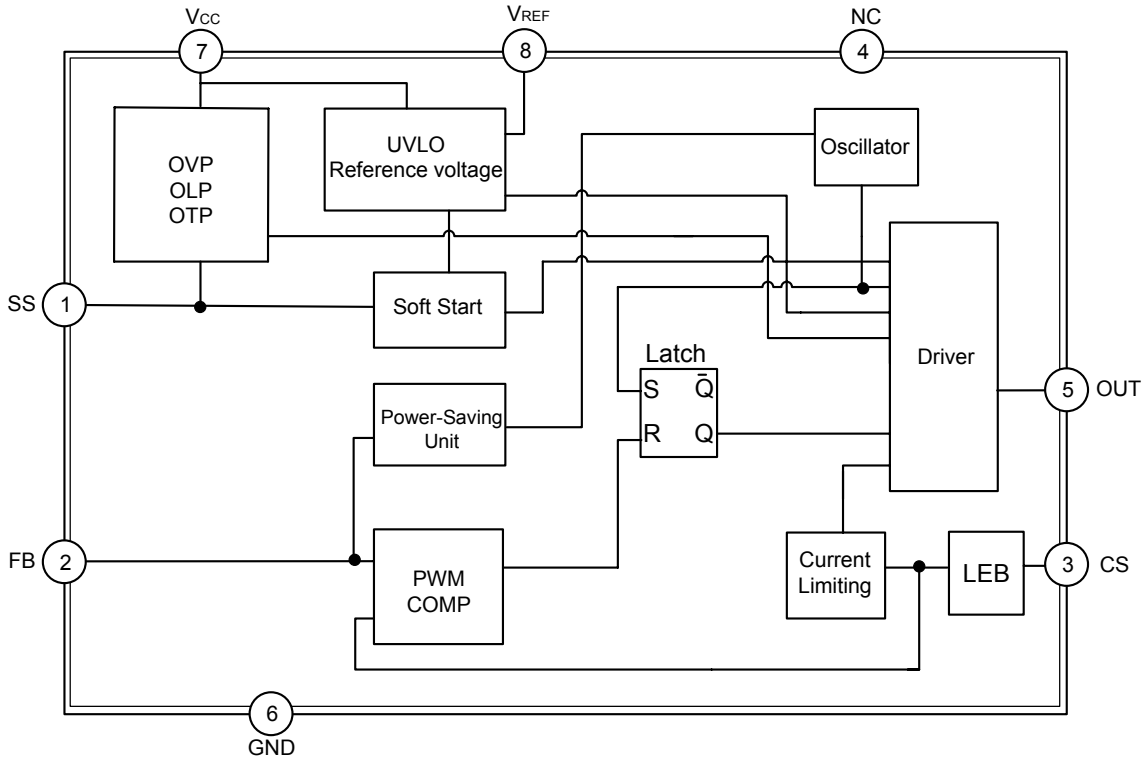
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	SYMBOL	FUNCTION
1	SS	Soft-start
2	FB	Feedback
3	CS	Controller current sense input
4	NC	
5	OUT	Ground
6	GND	Output to the gate of external power MOS
7	V_{CC}	Supply voltage
8	V_{REF}	Inter 6.3V reference voltage, connected with the filter capacitor

■ BLOCK DIAGRAM



Explain:OLP(Over Load Protection)
OVP(Over Voltage Protection)
OTP(Over Temperature Protection)
UVLO(Under Voltage Latch-Out
LEB(Led Edge Blanking)
SS(Soft Start)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C, V_{CC}=15V, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	26	V
Input Voltage to FB Pin	V_{FB}	-0.3 ~ 6.2	V
Input Voltage to CS Pin	V_{CS}	-0.3 ~ 2.8	V
Junction Temperature	T_J	+150	°C
Operating Temperature	T_{OPR}	-40 ~ +125	°C
Storage Temperature	T_{STG}	-50 ~ +150	°C

Note Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	8.2 ~ 21	V

■ ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=15V, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY SECTION							
Start Up Current		I_{STR}	V_{CC}=12.5V		27	45	μA
Supply Current with switch	OFF	I_{OFF}	V_{SS} = 0, I_{FB} = 0		3.7	5.5	mA
	ON	I_{ON}	V_{SS} = 5V, I_{FB} = 0		4.0	6.0	mA
UNDER-VOLTAGE LOCKOUT SECTION							
Start Threshold Voltage		$V_{THD(ON)}$		11.8	12.6	13.4	V
Min. Operating Voltage		$V_{CC(MIN)}$		7.6	8.1	8.6	V
Hysteresis		$V_{CC(HY)}$			4.5		V
INTERNAL VOLTAGE REFERENCE							
Reference Voltage		V_{REF}	measured at pin V_{REF}	6.1	6.3	6.6	V
CONTROL SECTION							
Switch Frequency	Normal	$F_{(SW)}$	V_{FB} = 4V	61	68	75	kHz
	Power-Saving		V_{FB} = 1V	17	20	**24**	kHz
Duty Cycle	MAX	D_{MAX}		65	70	75	%
	MIN	D_{MIN}	V_{FB} < 0.5V	0			%
V_{FB} Operating Level	MIN	V_{MIN}		0.5			V
	MAX	V_{MAX}				4.4	V
Feedback Resistor		R_{FB}		2.6	3.8	5.0	kΩ
Soft-Start Time		T_{SS}	C_{SS}=0.05uF		6		ms
			C_{SS}=0.1uF		12		ms
			C_{SS}=1uF		120		ms
PROTECTION SECTION							
OVP threshold		$V_{(OVP)}$	V_{SS} < 3.5V, V_{FB} > 5V	15.2	16	16.8	V
OLP threshold		$V_{FB(OLP)}$	V_{SS} > 5.4V	4.4	4.6	4.9	V
OTP threshold		$T_{(THR)}$		120	135	150	°C
OVP Disable threshold		$V_{SS(DEACT)}$	V_{FB} > 5V, V_{CC} > 17V	3.7	3.9	4.2	V
OLP Enable threshold		$V_{SS(ACT)}$	V_{FB} > 5V	4.9	5.1	5.4	V
Spike Blanking time		T_{SB}			7.2		μs
CURRENT LIMITING SECTION							
LEB		t_{LEB}			220		ns
DRIVER OUTPUT SECTION							
Output Voltage Low State		V_{OL}	I_{SOURCE} = 200 mA			2.5	V
Output Voltage High State		V_{OH}	I_{SINK} = 200 mA	12.2			V
Output Voltage Rise Time		t_R	C_L = 1.0 nF		300	400	ns
Output Voltage Fall Time		t_F	C_L = 1.0 nF		50	90	ns

■ FUNCTIONAL DESCRIPTION

The internal reference voltages and bias circuit work at V_{CC}>12.6V, and shutdown at V_{CC}< 8.1V.

(1) Soft-Start

When every IC power on, driver output duty cycle will be decided by voltage V_{SS} on soft-start capacitor and V_{CS} on current sense resistor at beginning. After V_{SS} reach 5.1V, the whole soft-start phase end, and driver duty cycle depend on V_{FB} and V_{CS}. The relation among V_{SS}, V_{FB} and V_{OUT} as followed FIG.3, here soft-start phase $T_{soft-start}$ should more than V_{OUT} start-up phase $T_{start-up}$, otherwise, IC will enter false OLP protection state. Because after the soft-start phase end, if V_{OUT} remain in lower voltage, V_{FB} more than 4.6V, then IC enter false OLP state.

Furthermore, soft-start phase should end before V_{CC} reach $V_{CC(MIN)}$ during V_{CC} power on. Otherwise, if soft-start phase remain not end before V_{CC} reach $V_{CC(MIN)}$ during V_{CC} power on, IC will enter auto-restart phase and not set up V_{OUT}.

Finally soft-start also set OVP active phase. OVP active phase between V_{SS}=0 and V_{SS}=3.8V, OVP will not be sensed after V_{SS} reach 3.8V.The Soft-start phase T_{SS}：

$$T_{SS} = \begin{cases} 6\ ms & (C_{SS}=0.05uF) \\ 12\ ms & (C_{SS}=0.1uF) \\ 120\ ms & (C_{SS}=1uF) \end{cases}$$

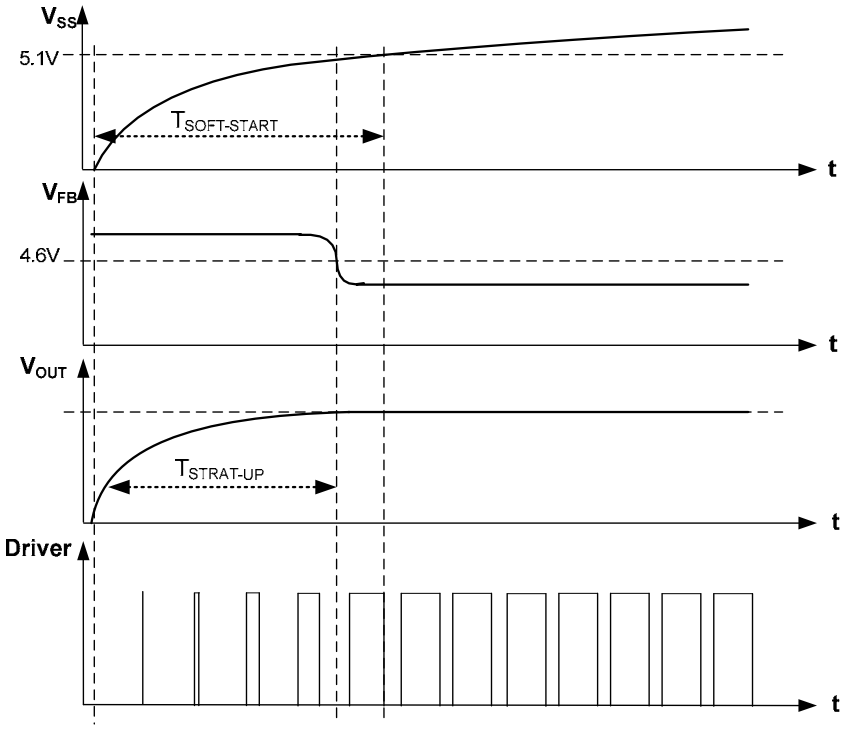


FIG.3 Soft-start phase

■ FUNCTIONAL DESCRIPTION(Cont.)

(2) Switch Frequency Set

The maximum switch frequency is 68KHz. The switch frequency is also modulated by output power P_{OUT} during IC operating. Lower switch frequency at lower load can improve IC's standby efficiency. Switch frequency is decreased minimum at no load, then the **UC3848** will operate at Power-Saving mode for Lower standby power. The relation curve between f_{SW} and P_{OUT} as followed FIG.4.

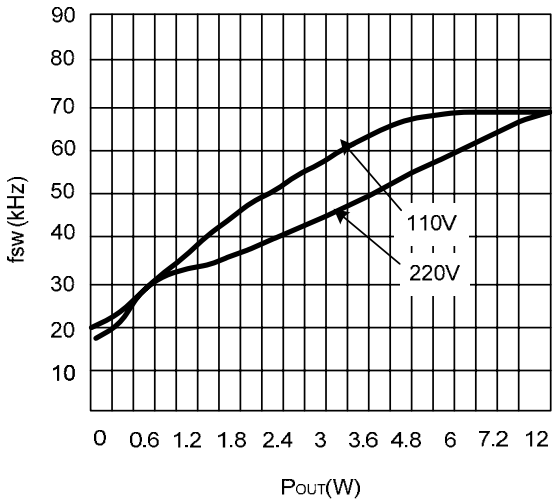


FIG.4 The relation curve between f_{SW} and output power P_{OUT}

■ FUNCTIONAL DESCRIPTION(Cont.)

(3) Protection section

UC3848 takes on more protection functions such as OLP, OVP and OTP etc. In case of those failure modes for continual 7.2μs (blanking time), the driver is shut down. At the same time, IC enters auto-restart, V_{CC} power on and driver is reset after V_{CC} power on again.

OLP

After soft-start phase end (V_{SS}>5.1V), IC will shutdown driver if over load state occurs (corresponding to V_{FB}>4.6V) for continual 7.2μs. OLP function will not inactive during soft-start phase. OLP case as followed **FIG.6**. The test circuit as followed FIG.8.

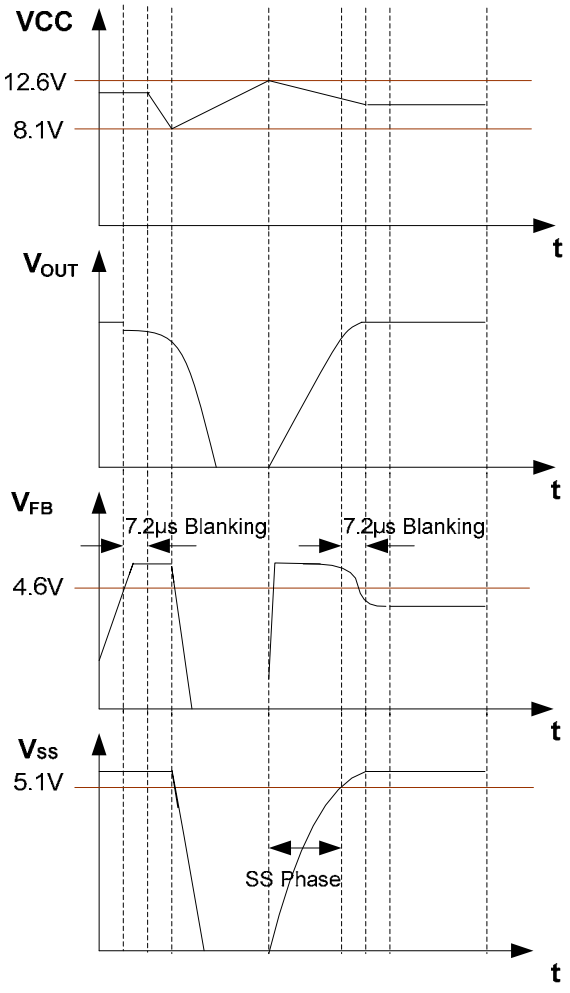


FIG.6 OLP case

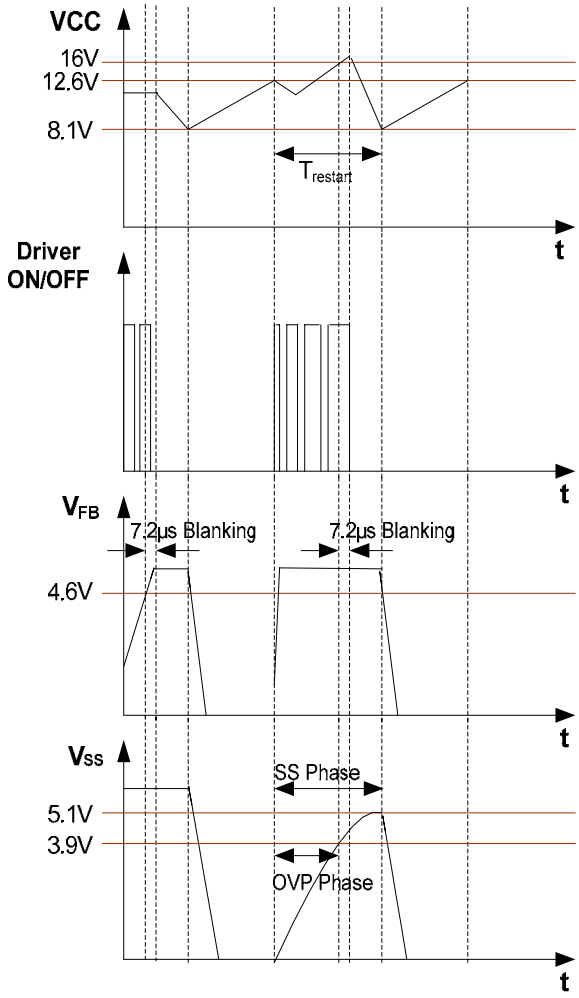


FIG.7 OVP case

OVP

Power supply V_{CC}'s OVP function are enabled only when V_{SS}<3.9V & V_{FB}>4.6V during soft-start phase. During above condition, driver will be shutdown if over voltage state occurs (V_{CC}>16V) for continual 7.2μs. OVP function will not inactive after soft-start phase. OLP case as followed **FIG.7**. The test circuit as followed FIG.9.

OTP

OTP will shut down driver when junction temperature T_J of internal circuits is more than threshold 135°C for continual 7.2μs.

■ FUNCTIONAL DESCRIPTION(Cont.)

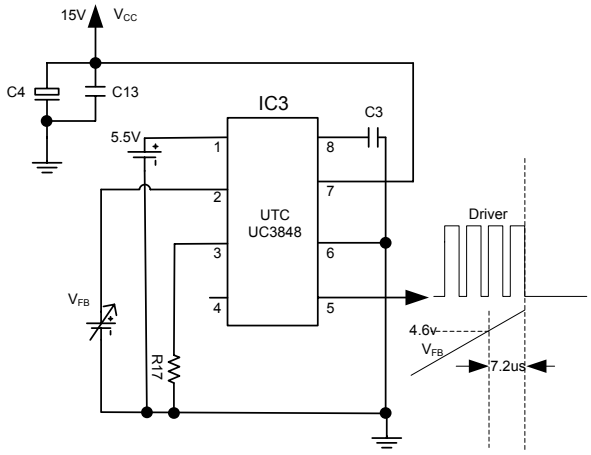


FIG.8 OLP test circuit

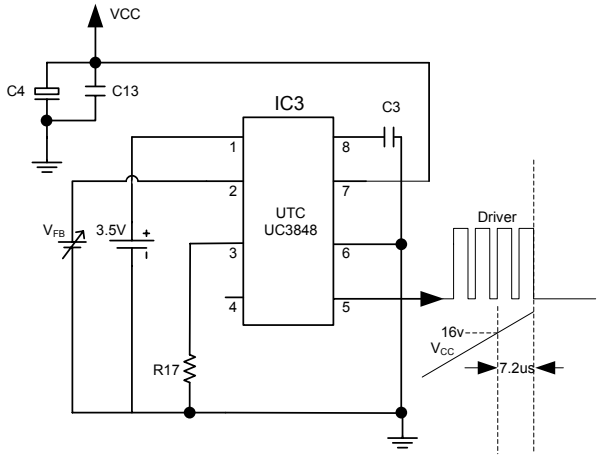


FIG.9 OVP test circuit

(4) Driver Output Section

Rise edge time of driver output is about 200ns for avoiding Low EMI. When driver output $V_{OL(MAX)}$ is less than 2.5V with 200mA source current, and $V_{OH(MIN)}$ is more than 12.2V with 200mA sink current.

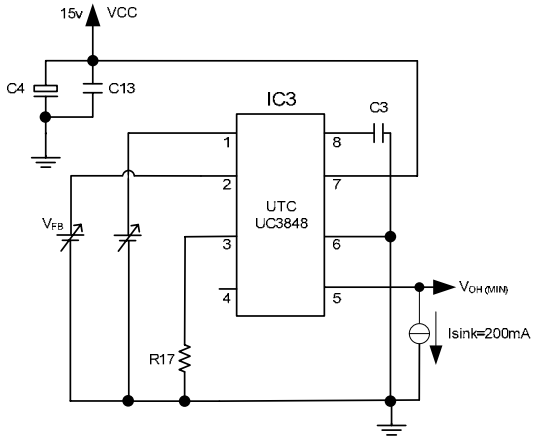


FIG.10 driver test circuit with sink current

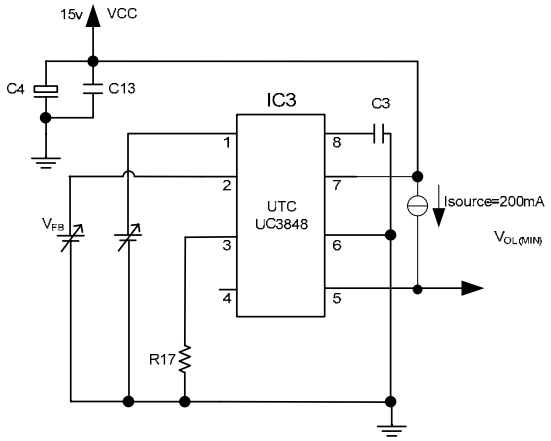


FIG.11 driver test circuit with source current

(5) External power switch MOS transistor

Because UC3848 driver output voltage Low level threshold is about 2.5V, User may apply power MOS transistors with bigger threshold. 4N60 is recommended normally.

■ TYPICAL APPLICATION CIRCUIT

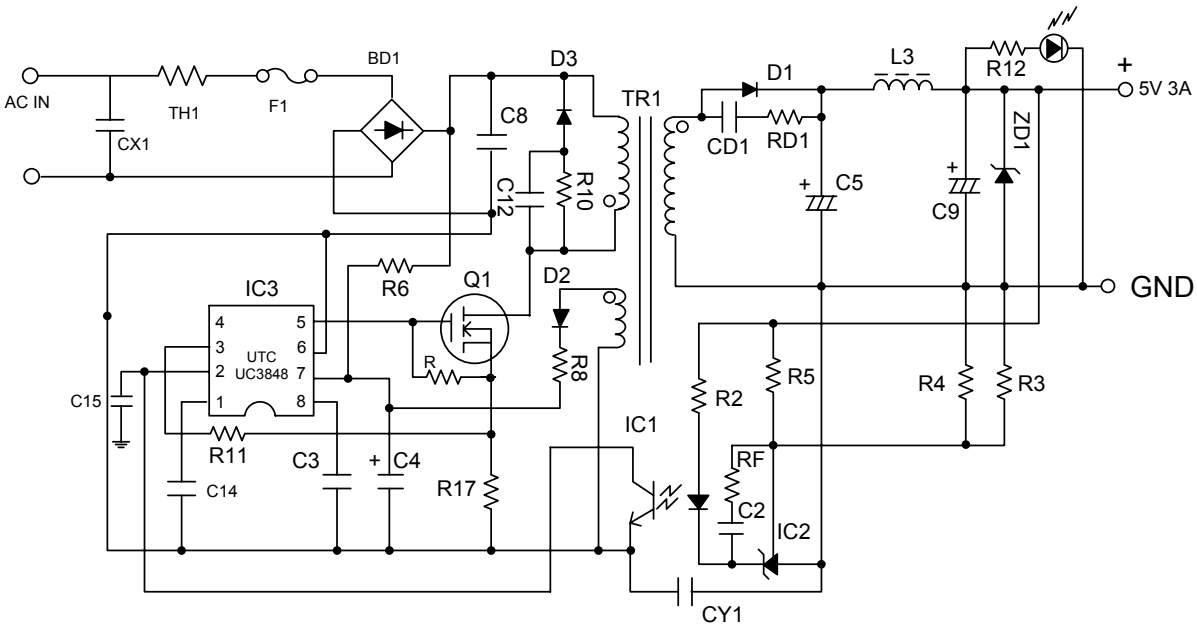


FIG.12 UC3848 Typical Application Circuit

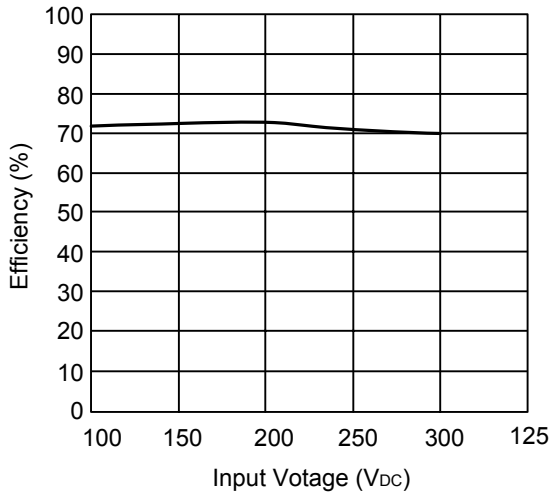
Table1 Components Reference description for UC3848 application circuit

C12	CC	10nF/1000V		D3	Diode	UF1007			R	R	470KΩ	1/8W
C14	CC	100nF/50V		IC1	IC	PC817			TH1		SCK-103	
C2	CC	33nF/50V		IC2	IC	TL431CLP			BD1	R	KBP-208	
CX1		104/275V		IC3	IC	UC3848			RD1	R	10Ω	1/8W
C5	EC	1000uF/15V		L3	L	1.2uH			R12	R	3.3kΩ	1/8W
C4	CC	22uF/50V		Q1	MOS	4N60			TR1		optional	
C8	EC	68uF/400V							RF	R	4.7kΩ	1/8W
C9	EC	1000uF/16V		R17	R	1.2Ω/1W	1/8W		C15	CC	0.1μF/50V	
CD1	CC	1nF/1KV		R2	R	680Ω	1/8W					
CY1	CC	4.7nF/250V		R3	R	ADJ	1/8W					
D1	Diode	C63-004		R4	R	5.6KΩ	1/8W					
D2	Diode	1N4148		R5	R	5.6KΩ	1/8W					

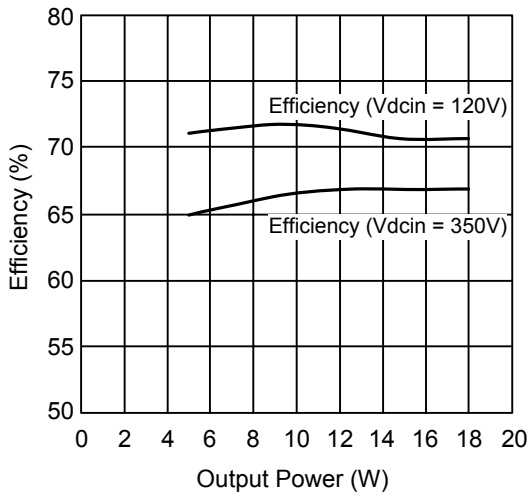
Note：C5 and C9 are lower ESR capacitors.

■ TYPICAL CHARACTERISTICS

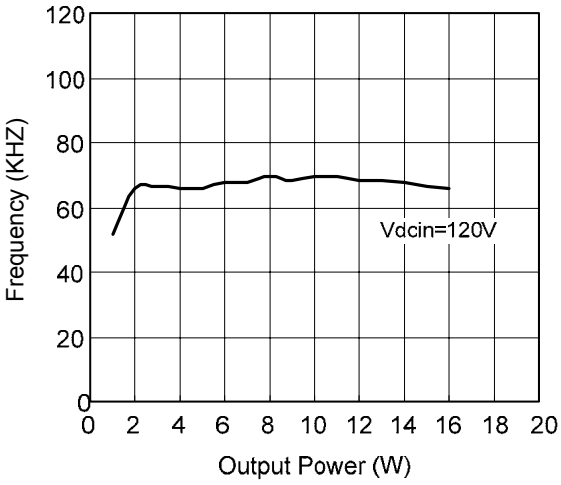
Efficiency vs. Input Voltage at Nominal Load



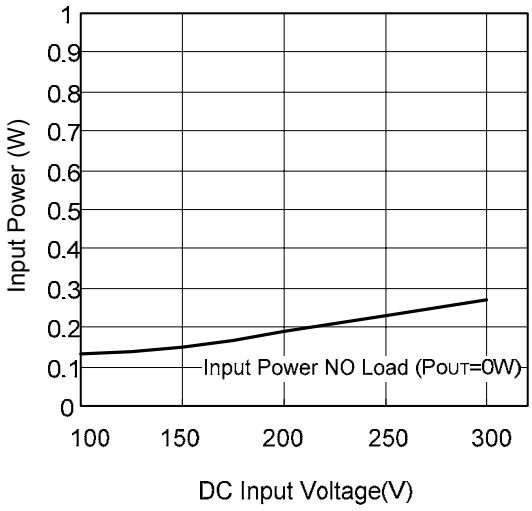
Efficiency vs. Output Power



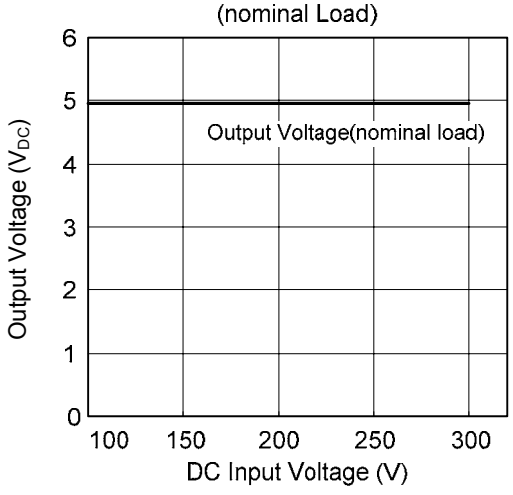
Frequency vs. Output Power



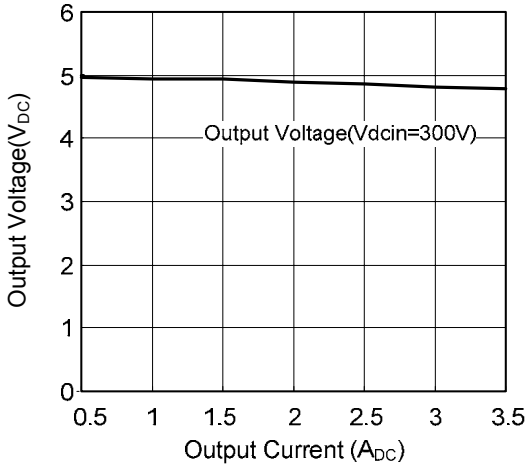
NO Load Input Power vs. Line Voltage (Normal Mode)



Output Voltage vs. Line Input Voltage (nominal Load)

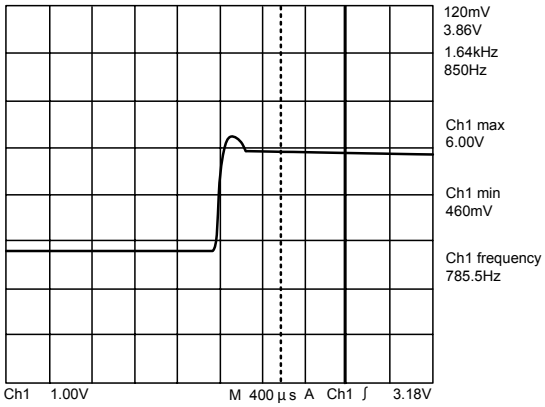


Load Regulation

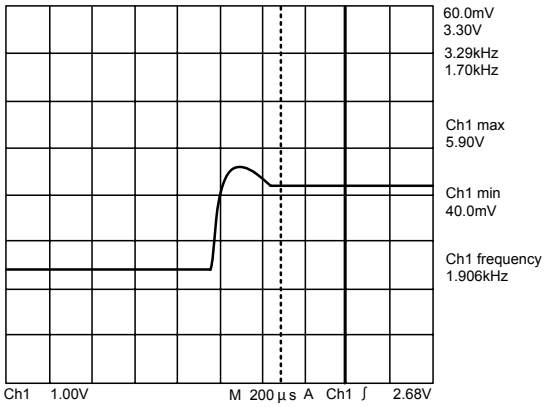


■ TYPICAL CHARACTERISTICS(Cont.)

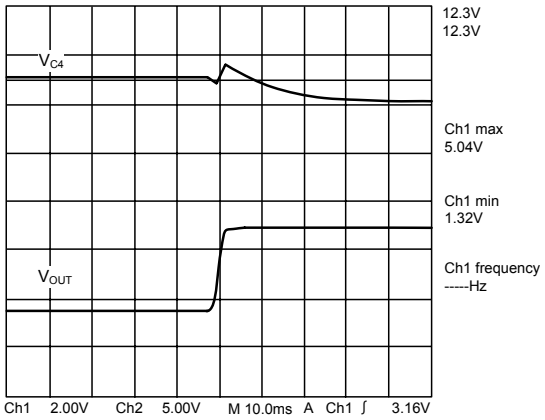
Feedback Voltage During Loadjump From 10% Up To 100% Load (V_{DCIN}=120V)



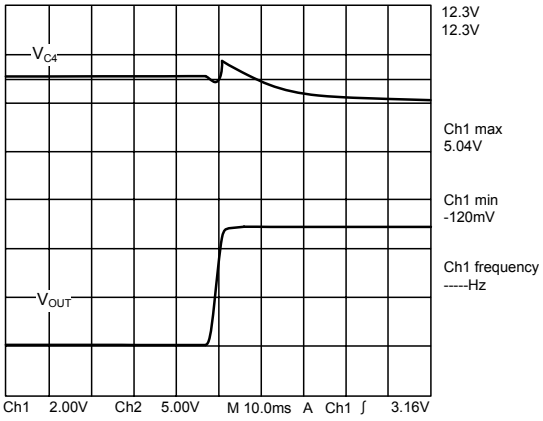
Feedback Voltage During Loadjump From 10% Up To 100% Load (V_{DCIN}=350V)



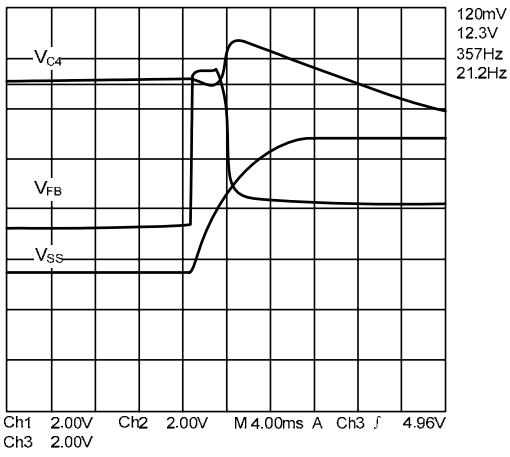
Startup With Full Load Condition At V_{DCIN}=120V, Vc4 and Vout



Startup With Full Load Condition At V_{DCIN}=350V, Vc4 and Vout



Startup Behavior At Nominal Load Condition V_{DCIN}=120V



Startup Behavior At Nominal Load Condition V_{DCIN}=350V