TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC9318AFAG,TC9318AFBG

Single Chip DTS Microcontroller (DTS-21)

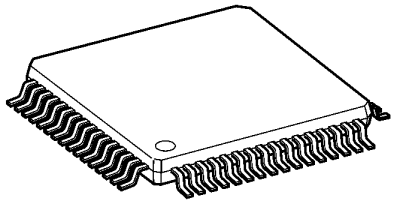
The TC9318AFAG and TC9318AFBG are a 4 bit CMOS microcontroller for signal chip digital tuning systems. It is capable of functioning at a low voltage of 3 V and features a built-in prescaler of operating 230 MHz, PLL and LCD drivers.

The CPU has 4 bit parallel addition and subtraction instructions (e.g., AI, SI), logic operation instructions (e.g., OR, AN), composite judging and compare instructions (e.g., TM, SL), and time-base functions.

The package is an pin 64, 0.5/0.65-mm-pitch quad flat pack package. In addition to various input/output ports and a dedicated key-input port, which are controlled by powerful input/output instructions (IN 1, 2, OUT 1, 2), there are many dedicated LCD pins, a buzzer port, a 6 bit A/D converter, an IF counter, and other pins.

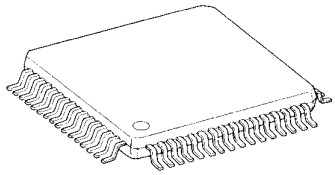
Low-voltage and low-current consumption make this microcontroller suitable for portable DTS equipment.

TC9318AFAG



P-LQFP64-1010-0.50E

TC9318AFBG



P-LQFP64-1212-0.65A

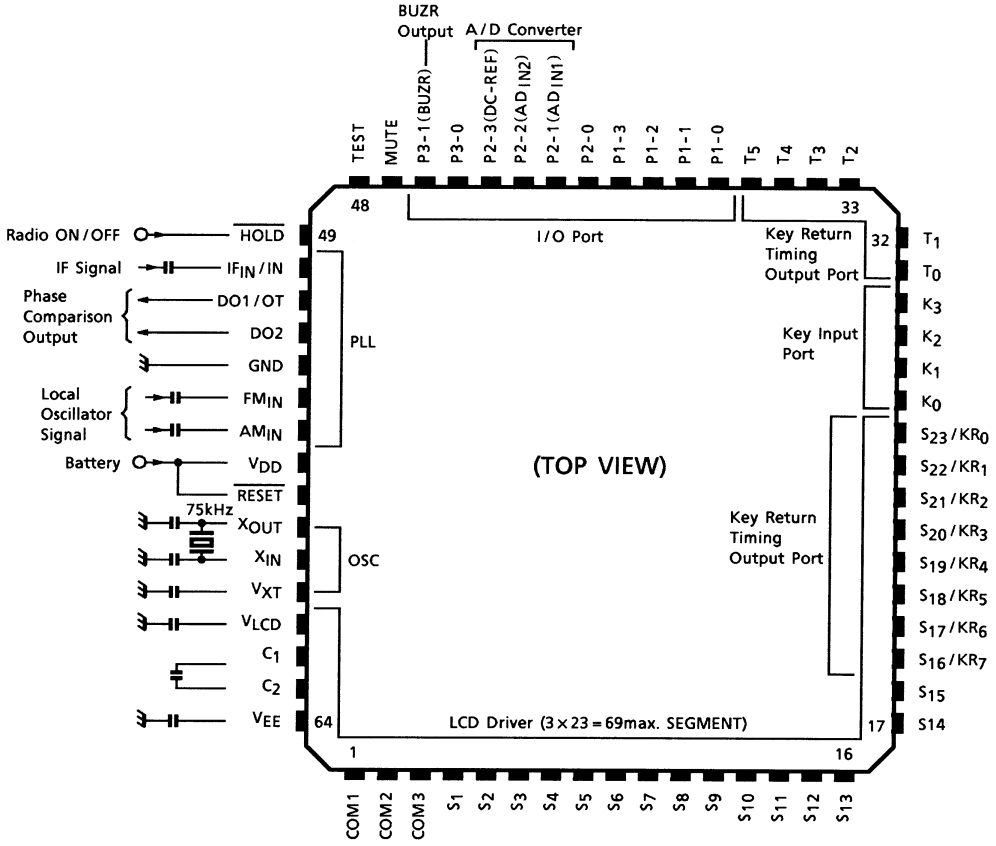
Weight
P-LQFP64-1010-0.50E: 0.32 g (typ.)
P-LQFP64-1212-0.65A: 0.45 g (typ.)

## Features

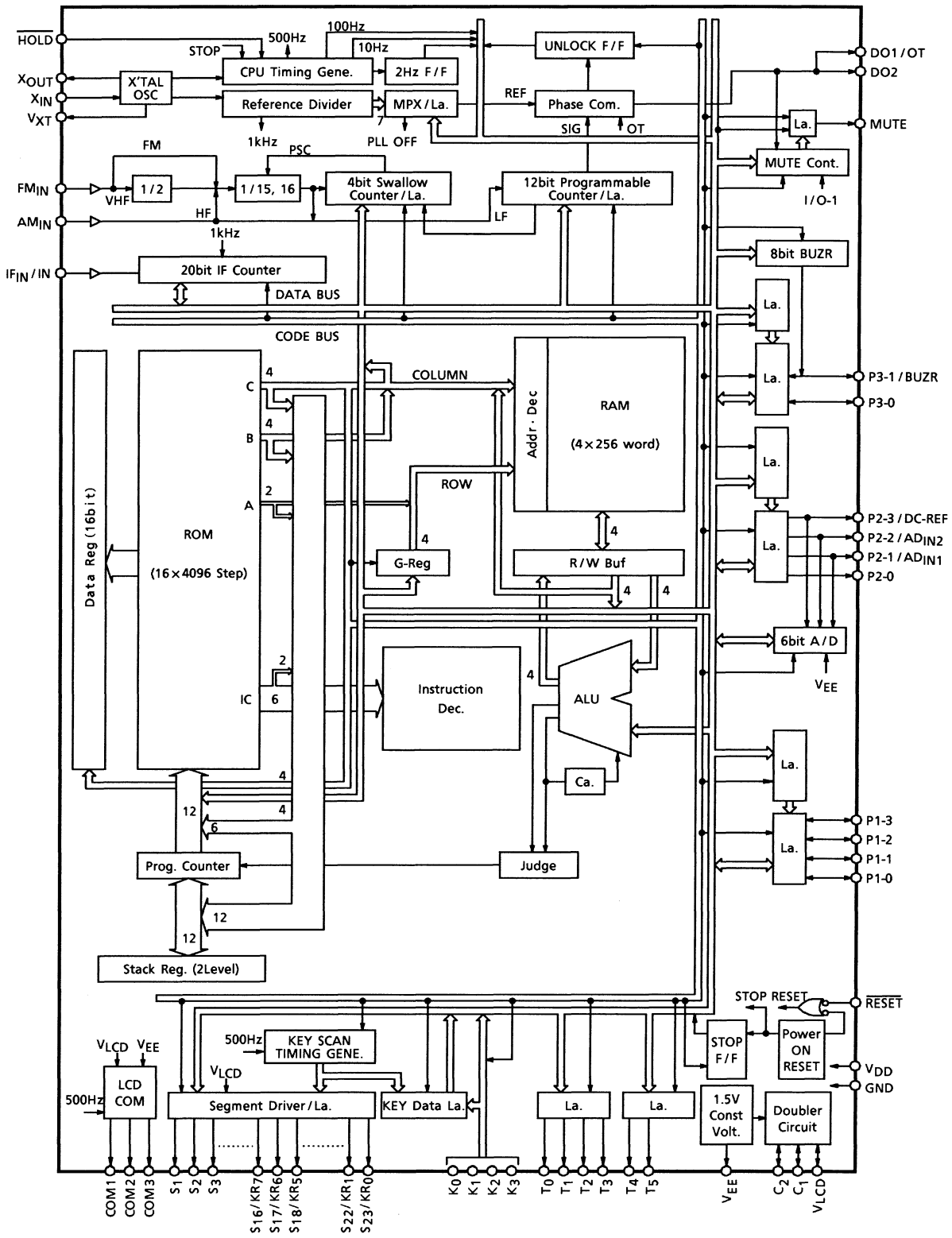
- 4 bit microcontroller for digital tuning systems.
- Operating voltage $V_{DD}$ = 1.8~3.6 V, with low current consumption because of CMOS circuitry (with only CPU operating, when $V_{DD}$ = 3 V, $I_{DD}$ = 80 μA max)
- Built-in prescaler (1/2 fixed divider +2 modulus prescaler: fmax ≥ 230 MHz)
- Features built-in 1/3-duty, 1/2-bias LCD drivers and a built-in 3 V booster circuit for the display.
- Data memory (RAM) and ports are easily backed up.
- Program memory (ROM): 16 bit × 4096 steps
- Data memory (RAM): 4 bit × 256 words
- 60-instruction set (all one-word instructions)
- Instruction execution time: 40 μs (with 75 kHz crystal) (MVGS, DAL instructions: 80 μs)
- Many addition and subtraction instructions (12 types addition, 12 types subtraction)
- Powerful composite judging instructions (TMTR, TMFR, TMT, TMF, TMTN, TMFN)
- Data can be transmitted between addresses on the same row. (MVSR instruction)
- Register indirect transfer available (MVGD, MVGS instruction).
- 16 powerful general registers (located in RAM)
- Stack levels: 2
- JUMP or CAL instruction can be used anywhere in the 4096 steps of program memory (ROM) as there are no pages or fields.
- 16 bit of any address in the 1024 steps in program memory (ROM) can be referenced (DAL instruction).
- Features independent frequency input pins ($FM_{IN}$ and $AM_{IN}$) and two (DO1 and DO2) phase comparison outputs for FM/VHF and AM.
- Seven reference frequencies can be selected by program.
- Powerful input/output instructions (IN 1, 2, OUT 1, 2)
- Dedicated input ports ($K_0$~$K_3$) for key input. 26 LCD drive pins (69 segments maximum) available.
- 17 I/O ports: 10 with input/output programmable in 1 bit units, and 7 output-only port. The 2 $IF_{IN}$, and DO1 pins can be switched by instruction to IN (input-only) or OT (output-only).
- Three back-up modes available by instruction: Only CPU operation, crystal oscillation only, clock stop.

- Features a built-in 2 Hz timer F/F and a built-in 10/100 Hz interval pulse output (internal port for time base).
- Allows PLL lock status detection.
- 8 of the LCD segment outputs ($S_{16}$~$S_{23}$) can also operate as key return timing outputs ($KR_0$~$KR_7$). The I/O ports are not dedicated key return timing outputs but can have other uses as well.
- Built-in 20 bit, general-purpose IF counter can detect stations during auto-tuning by counting the intermediate frequencies of each band.
- Built-in 8 bit buzzer output circuit can produce 254 different tone signals.
- Features a built-in 2-channel, 6 bit A/D converter.
- To prevent CPU malfunctions, a built-in supply voltage drop detection circuit shuts down the CPU when voltage falls below 1.5 V.

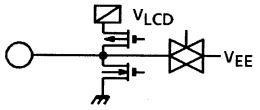
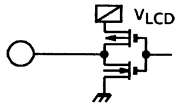
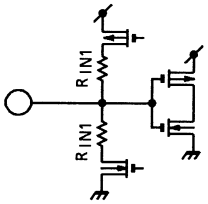
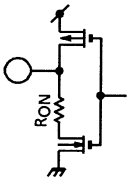
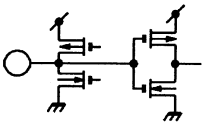
## Pin Assignment (top view)

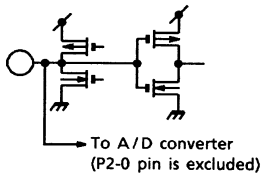
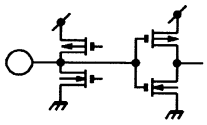
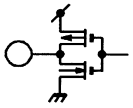
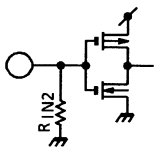


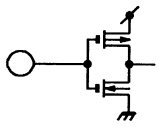
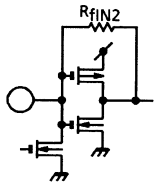
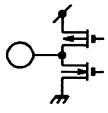
## Block Diagram

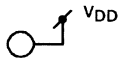
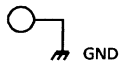
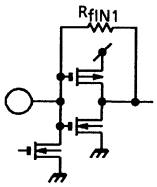
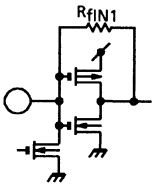
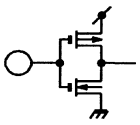


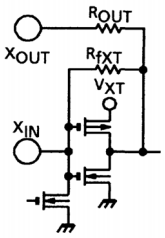
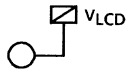
## Explanation of Function

| Pin No. | Symbol | Pin Name | Function and Operation | Remarks |
|---|---|---|---|---|
| 1 | COM1 | LCD common output | Output common signals to the LCD panel. Through a matrix with pins $S_1$~$S_{23}$, a maximum of 69 segments can be displayed.<br>Three levels, $V_{LCD}$, $V_{EE}$, and GND, are output at 83 Hz every 2 ms.<br>$V_{EE}$ is output after SYSTEM RESET and CLOCK STOP are released, and a common signal is output after the DISP OFF bit is set to "0". |  |
| 2 | COM2 | | | |
| 3 | COM3 | | | |
| 4~18 | $S_1$~$S_{15}$ | LCD segment output | Segment signal output pins for the LCD panel. Together with COM1, COM2, and COM3, a matrix is formed that can display a maximum of 69 segments.<br>The signals for the key matrix and the segment signals from pins $S_{16}/KR_7$~$S_{23}/KR_0$ are output on a time division basis. $4 \times 8 = 32$ key matrix can be created in conjunction with key input ports $K_0$~$K_3$. |  |
| 19~26 | $S_{16}/KR_7$~<br>$S_{23}/KR_0$ | LCD segment output/Key return timing output | | |
| 27~30 | $K_0$~$K_3$ | Key input ports | 4 bit input ports for key matrix input.<br>Combined in a matrix with key return timing outputs of the LCD segment pins, data from a maximum of $4 \times 8 = 32$ keys can be input and pins are pulled up. On the key seteutining output pins, data from $4 \times 6 = 24$ keys can be input and pins are pulled down. The WAIT mode is released when high level is applied to key input ports set to pull-down. |  |
| 31~36 | $T_0$~$T_5$ | Key return timing output port | These ports output the timing signal for key matrix. To form the key matrix, load resistance has been built-in the N-channel side. When the key matrix combined with push-key, that does not need a key matrix diode. |  |
| 37~40 | P1-0~P1-3 | I/O port 1 | The input and output of these 4 bit I/O ports can be programmed in 1 bit units.<br>By altering the input to I/O ports set to input, the CLOCK STOP and WAIT modes can be released, and the MUTE bit of the MUTE pin can be set to "1". |  |

| Pin No. | Symbol | Pin Name | Function and Operation | Remarks |
|---|---|---|---|---|
| 41~44 | P2-0<br>P2-1/$AD_{IN1}$<br>P2-2/$AD_{IN2}$<br>P2-3/ DC-REF | I/O port 2<br>/AD analog voltage input<br>/AD analog voltage input<br>/Reference voltage input | 4 bit I/O ports.<br>Input and output may be programmed in 1 bit units.<br>Pins P2-1 through P2-2 can also be used for analog input to the built-in 6 bit, 2-channel A/D converter.<br>Conversion time of the built-in A/D converter using the successive comparison method is 280 μs. The necessary pin can be programmed to AD analog input in 1 bit units, and P2-3 can be set to the reference voltage input. Internal power supply ($V_{DD}$) or constant voltage ($V_{EE}$) can be used as the reference voltage. In addition, constant voltage ($V_{EE}$) can be input to the AD analog input so battery voltage, etc., can be easily detected. The reference voltage input, for which a built-in operational amp is used, has high impedance.<br>The A/D converter, and their control are all executed by program. |  |
| 45~46 | P3-0<br>P3-1/BUZR | I/O port 3<br>/Buzzer output | 2 bit I/O ports, whose input/output can be programmed in 1 bit units.<br>The P3-1 pin also functions as the output for the built-in buzzer circuit. The buzzer sound can be output in 254 different tones between 18.75 kHz and 147 Hz, and at a duty of 50%.<br>The buzzer output, and all associated controls can be programmed. |  |
| 47 | MUTE | Muting output port | 1 bit output port. Normally, this port is used for muting control signal output.<br>This pin can set the internal MUTE bit to “1” according to a change in the input of I/O port 1. MUTE bit output logic can be changed; PLL phase difference can also be output using this pin. |  |
| 48 | TEST | TEST mode control input | Input pin used for controlling TEST mode. High level indicates TEST mode, while low level indicates normal operation. The pin is normally used at low level or no-connection (NC). (a pull-down resistor is built-in). |  |

| Pin No. | Symbol | Pin Name | Function and Operation | Remarks |
|---|---|---|---|---|
| 49 | $\overline{\text{HOLD}}$ | HOLD mode control input | Input pin for request/release HOLD mode.<br>Normally, this pin is used to input radio mode selection signals or battery detection signals.<br>HOLD mode includes CLOCK STOP mode (stops crystal oscillation) and WAIT mode (halts CPU). Setting is implemented with the CKSTP instruction or the WAIT instruction. When the CKSTP instruction is executed, request/release of the HOLD mode depends on the internal MODE bit. If the MODE bit is "0" (MODE-0), executing the CKSTP instruction while the $\overline{\text{HOLD}}$ pin is at low level stops the clock generator and the CPU and changes to memory back-up mode. If the MODE bit is "1" (MODE-1), executing the CKSTP instruction enters memory back-up mode regardless of the level of the $\overline{\text{HOLD}}$ pin. Memory back-up is released when the $\overline{\text{HOLD}}$ pin goes high in MODE-0, or when the level of the $\overline{\text{HOLD}}$ pin level in MODE-1.<br>When memory back-up mode is entered by executing a WAIT instruction, any change in the $\overline{\text{HOLD}}$ pin input releases the mode.<br>In memory back-up mode, current consumption is low (below 10 μA), and all the output pins (e.g., display output, output ports) are automatically set to low level. |  |
| 50 | $IF_{IN}$/IN | IF signal input/Input port | IF counter's IF signal input pin for counting the IF signals of the FM and AM bands and detecting the automatic stop position.<br>The input frequency is between 0.35~12 MHz (0.2 $V_{p-p}$ (min)). A built-in input amp and C coupling allow operation at low-level input.<br>The IF counter is a 20 bit counter with optional gate times of 1, 4, 16, and 64 ms. 20 bits of data can be readily stored in memory.<br>This input pin can be programmed for use as an input port (IN port). CMOS input is used when the pin is set as an IN port. |  |
| 51<br>52 | DO1/OT<br>DO2 | Phase comparison output/Output port<br>Phase comparison output | PLL's phase comparison tri-state output pins.<br>When the programmable counter's prescaler output is higher than the reference frequency, output is at high level. When output is lower than the reference frequency, output is at low level. When output equals the reference frequency, high impedance output is obtained.<br>Because DO1 and DO2 are output in parallel, optimal filter constants can be designed for the FM/VHF and AM bands.<br>Pin DO1 can be programmed to high impedance or programmed as an output port (OT). Thus, the pins can be used to improve lock-up time or used as output ports. |  |

| Pin No. | Symbol | Pin Name | Function and Operation | Remarks |
|---|---|---|---|---|
| 56 | $V_{DD}$ | Power-supply pins | Pins to which power is applied.<br>Normally, $V_{DD}$ = 1.8~3.6 V (3.0 V typ.) is applied.<br>In back-up mode (when CKSTP instructions are being executed), voltage can be lowered to 1.0 V. If voltage falls below 1.5 V while the CPU is operating, the CPU stops to prevent malfunction (STOP mode). When the voltage rises above 1.5 V, the CPU restarts.<br>STOP mode can be detected by checking the STOP F/F bit. If necessary, execute initialization or adjust clock by program. When detecting or preventing CPU malfunctions using an external circuit, STOP mode can be invalidated and rendered non-operative by program. In that case, all four bits of the internal TEST port should be set to "1".<br>If more than 1.8 V is applied when the pin voltage is 0, the device's system is reset and the program starts from address "0". (power on reset)<br>Note: To operate the power on reset, the power supply should start up in 10~100 ms. |  |
| 53 | GND | | |  |
| 54 | $FM_{IN}$ | FM programmable counter input | Programmable counter input pin for FM, VHF band.<br>The 1/2 + pulse swallow system (VHF mode) and the pulse swallow system (FM mode) are selectable freely by program.<br>At the VHF mode, local oscillation output (VCO output) of 50~230 MHz (0.2$V_{p-p}$ (min)) is input and FM mode, 40~130 MHz (0.2$V_{p-p}$ (min)) is input.<br>A built-in input amp and C coupling allow operation at low-level input.<br>Note: When in the PLL OFF mode or when set to $AM_{IN}$ input, the input is pulled down. |  |
| 55 | $AM_{IN}$ | AM local oscillator signal input | Programmable counter input pin for AM band.<br>The pulse swallow system (HF mode) and direct dividing system (LF mode) are freely selectable by program. At the HF mode, local oscillation output (VCO output) of 1~45 MHz (0.2 $V_{p-p}$ (min)) is input and LF mode, 0.5~12 MHz (0.2 $V_{p-p}$ (min)) is input.<br>Built-in input amp operates with low-level input using a C coupling.<br>Note: When in PLL OFF mode or when set to $FM_{IN}$ input, the input is pulled down. |  |
| 57 | $\overline{\text{RESET}}$ | Reset input | Input pin for system reset signals.<br>$\overline{\text{RESET}}$ takes place while at low level; at high level, the program starts from address "0".<br>Normally, if more than 1.8 V is supplied to $V_{DD}$ when the voltage is 0, the system is reset (power on reset).<br>Accordingly, this pin should be set to high level during operation. |  |

| Pin No. | Symbol | Pin Name | Function and Operation | Remarks |
|---|---|---|---|---|
| 58 | $X_{OUT}$ | Crystal oscillator pins | Crystal oscillator pins.<br>A reference 75 kHz crystal oscillator is connected to the $X_{IN}$ and $X_{OUT}$ pins.<br>The oscillator stops oscillating during CKSTP instruction execution.<br>The $V_{XT}$ pin is the power supply for the crystal oscillator. A stabilizing capacitor (0.47 μF typ.) is connected. |  |
| 59 | $X_{IN}$ | | | |
| 60 | $V_{XT}$ | | | |
| 61 | $V_{LCD}$ | Voltage doubler boosting pin | Voltage doubler boosting pin for driving the LCD.<br>A capacitor (0.1 μF typ.) is connected to boost the voltage.<br>The $V_{LCD}$ pin outputs voltage (3.0 V), which has been doubled from the constant voltage ($V_{EE}$: 1.5 V) using the capacitors connected between $C_1$ and $C_2$. That potential is supplied to the LCD drivers. If the internal $V_{LCD}$ OFF bit is set to "1" by program, an external power supply can be input through the $V_{LCD}$ pin to drive the LCD.<br>At this time, the $V_{LCD}/2$ potential, whose $V_{LCD}$ voltage is divided using registers, is output from the $C_2$ pin. |  |
| 62 | $C_1$ | | | |
| 63 | $C_2$ | | | |
| 64 | $V_{EE}$ | Constant voltage supply pin | 1.5 V constant voltage supply pin for driving the LCD.<br>A stabilizing capacitor (0.1 μF typ.) is connected. This is a reference voltage for the A/D converter, key input, and the LCD common output's bias potential. | — |

Note 1: When the device is reset (voltage higher than 1.8 V, or when $\overline{\text{RESET}}$ = low → high) I/O ports are set to input, the pins for I/O ports and additional functions (e.g., A/D converter) are set to I/O port input pins, while the $IF_{IN}$/IN pins become IF input pins.

Note 2: When in PLL OFF mode (when the three bits in the internal reference ports all show "1"), the $IF_{IN}$ and $FM_{IN}$, $AM_{IN}$ pins are pulled down, and DO1 and DO2 are at high impedance.

Note 3: When in CLOCK STOP mode (during execution of CKSTP instruction), the output ports and the LCD output pins are all at low level, while the constant voltage circuit ($V_{EE}$), the voltage doubler circuit ($V_{LCD}$), and the power supply for the crystal oscillator ($V_{XT}$) are all off.

Note 4: When the device is being reset, the contents of the output ports and internal ports are undefined and initialization by program is necessary.

## Explanation of Operation

### CPU

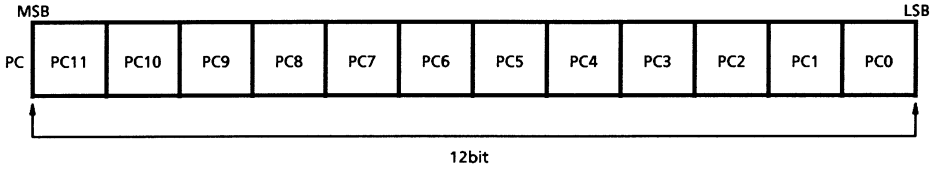
CPU is composed of program counter, stack register, ALU, program memory, data memory, G-register, carry F/F and judging circuit.

### 1. Program Counter (PC)

Program Counter is a block to designate the address of program memory (ROM), and is composed of 12 bits binary up counter. This is cleared by system reset, and the program starts from zero address.

Usually, it's increment is made one by one everytime the one instruction is executed, but when JUMP instruction or CAL instruction is executed, the address designated at operand part of that instruction is loaded.

Further, when the instruction (AIS, SLTI, TMT, RNS instructions, etc.) having skip function is executed, two increments of program counter is made if the result is the condition to be skipped, and the succeeding instruction is skipped.




### 2. Stack Register (STACK)

This is a register composed of 2 × 12 bits during the execution of subroutine call instruction, the value obtained by adding +1 to the content of program counter, namely return address, is housed. The content of stack register is loaded on the program counter by the execution of return instruction. (RN, RNS instructions)

This stack level is 2 level, and nesting is 2 level.

### 3. ALU

ALU has binary 4 bits parallel addition and subtraction, logical operation, comparison and plural bit judge functions.

This CPU has no accumulator, and all operations directly treat the contents of data memory.

### 4. Program Memory (ROM)

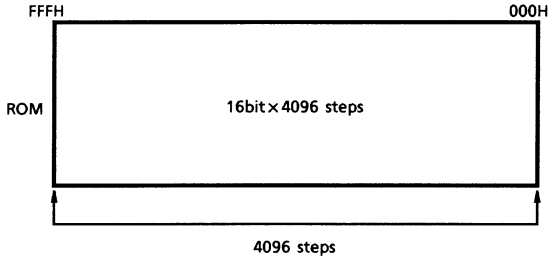
Program memory is composed of 16 bit × 4096 steps and is the address of 000H~FFFH.

Program memory has no concept of page or field, so JUMP instruction and CAL instruction can be freely used among 4096 steps.

Further, it is possible to use optional address of program memory as data area, and its content, 16 bits, can be loaded to the data register by executing DAL instruction.

Note 5: Provide the data area at the address outside the program loop in the program memory.

Note 6: In DAL instruction, the address of program memory can be designated as the data area becomes 1024 steps of 000H~3FFH.



## 5. Data Memory (RAM)

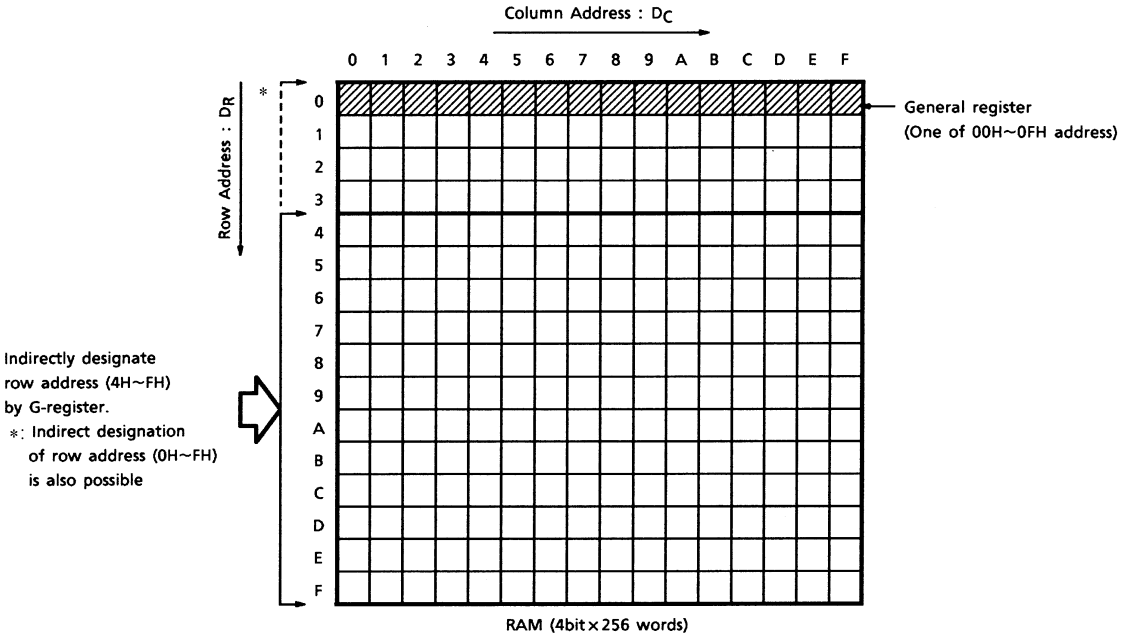
Data memory is composed of 4 bit × 256 words and used for storing data.

This 256 words are expressed with row address (4 bits) and column address (4 bits).

192 words (row address = 4H~FH) among the data memory are indirect addressing by G-register. For this reason, when carrying out data processing within this territory, it is necessary to designate row address by G-register beforehand Area of 00H~0FH address in data memory is called general register, and can be used only by designating column address (4 bits). These 16 general registers can be used for operation and transfer between data memories. Further, it can also be used as ordinary data memory.

Note 7: The column address (4 bits) to designate general register becomes register number of the general register.

Note 8: It is also possible to indirectly designate all of row address (= 0H~FH) by G-register.




## 6. G-Register (G-REG.)

G-register is a 4 bits register for addressing row address ($D_R$ = 4H~FH) of 192 words in data memory.

Content of this register is effective during executing MVGD instruction, MVGS instruction, and is not related with the execution of other instructions.

This register is treated as one of the port, and its content is set by the execution of OUT1 instruction among input and output instructions.

(refer to register port item 1)

## 7. Data Register (DATA REG.)

This is a register composed of 1 × 16 bits. In this register, 16 bits data of optional address among the program memory in 000H~3FFH is loaded during executing of DAL instruction. This register is treated as one of the port, and when IN1 instruction among input and output instruction is executed, it's content is read in the data memory in 4 bits unit.

(refer to register port item 2)

## 8. Carry F/F (C・F/F)

This is set when carry or borrow is produced as a result of executing operational instruction, and is reset when it is not produced. Content of carry F/F changes only when addition and subtraction instruction is executed, and does not change during the execution of other instructions.

## 9. Judging Circuit (J)

When a instruction with skip function is executed, this circuit judges it's skip condition. When skip condition is satisfied, this circuit makes two increments of program counter, and skips the succeeding instruction.

It is provided with 29 kinds of instructions having abundant skip function.

(refer to item 11, explanation list of function and operation of instructions, * marked instruction)

## 10. List of Instruction Set

60 kinds of instruction set are included, all of which consisting of one word instruction.

These instructions are expressed with 6 bits instruction code.

| Higher Rank 2 Bits / Lower Rank 4 Bits | | 00 | | 01 | | 10 | | 11 | |
|---|---|---|---|---|---|---|---|---|---|
| | | 0 | | 1 | | 2 | | 3 | |
| 0000 | 0 | AI | M, I | AD | r, M | TMTR | r, M | SLTI | M, I |
| 0001 | 1 | AIS | M, I | ADS | r, M | TMFR | r, M | SGEI | M, I |
| 0010 | 2 | AIN | M, I | ADN | r, M | SEQ | r, M | SEQI | M, I |
| 0011 | 3 | AIC | M, I | AC | r, M | SNE | r, M | SNEI | M, I |
| 0100 | 4 | AICS | M, I | ACS | r, M | LD | r, M | TMTN | M, N |
| 0101 | 5 | AICN | M, I | ACN | r, M | ST | M, r | TMT | M, N |
| 0110 | 6 | ORIM | M, I | ORR | r, M | MVGD | r, M | TMFN | M, N |
| 0111 | 7 | ANIM | M, I | ANDR | r, M | MVGS | M, r | TMF | M, N |
| 1000 | 8 | SI | M, I | SU | r, M | CALL $ADDR_1$ | | IN1 | M, C |
| 1001 | 9 | SIS | M, I | SUS | r, M | | | IN2 | M, C |
| 1010 | A | SIN | M, I | SUN | r, M | | | — | |
| 1011 | B | SIB | M, I | SB | r, M | | | OUT1 | C, M |
| 1100 | C | SIBS | M, I | SBS | r, M | JUMP $ADDR_1$ | | OUT2 | C, M |
| 1101 | D | SIBN | M, I | SBN | r, M | | | — | |
| 1110 | E | XORI | M, I | XORR | r, M | | | DAL $ADDR_2$, r | |
| 1111 | F | MVIM | M, I | MVSR | $M_1$, $M_2$ | | | RN, RNS, WAIT CKSTP, NOOP | |

## 11. Explanation List of Function and Operation of Instructions (explanation of symbols)

M: Data memory address
Normally, one of 00H~3FH address of data memory.
r: General register
One of 00H~0FH address of data memory.
PC: Program counter (12 bit)
STACK: Stack register (12 bit)
G: G-register (4 bit)
DATA: Data register (16 bit)
I: Immediate data (4 bit)
N: Bit position (4 bit)
—: All "0"
C: Code No. of port (4 bit)
$C_N$: Code No. of port (4 bit)
$R_N$: General register No. (4 bit)
$ADDR_1$: Program memory address in page 0 or 1 (12 bit)
$ADDR_2$: Higher rank 6 bit of program memory address in page 0
Ca: Carry
b: Borrow
IN1~IN2: Port treated during the execution of IN1~IN2 instruction
OUT1~OUT2: Port treated during the execution of OUT1~OUT2 instruction
( ): Register or data memory content
[ ] C: Content of port indicated by code No. C (4 bit)
[ ]: Content of data memory indicated by the content of register or data memory
[ ] P: Content of program memory (16 bit)
IC: Instruction code (6 bit)
*: Instruction having skip function
$D_C$: Data memory column address (4 bit)
$D_R$: Data memory row address (2 bit)
P: Wait condition

| Inst. Gr. | Mnemonic | | Skip Function | Explanation of Function | Explanation of Operation | Machine Language (16 bit) | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | IC (6 bit) | A (2 bit) | B (4 bit) | C (4 bit) |
| ADDITION INSTRUCTION | AI | M, I | | Add immediate data to memory | M ← (M) + I | 000000 | $D_R$ | $D_C$ | I |
| | AIS | M, I | * | Add immediate data to memory, then skip if carry | M ← (M) + I<br>Skip if carry | 000001 | $D_R$ | $D_C$ | I |
| | AIN | M, I | * | Add immediate data to memory, then skip if not carry | M ← (M) + I<br>Skip if not carry | 000010 | $D_R$ | $D_C$ | I |
| | AIC | M, I | | Add immediate data to memory with carry | M ← (M) + I + ca | 000011 | $D_R$ | $D_C$ | I |
| | AICS | M, I | * | Add immediate data to memory with carry, then skip if carry | M ← (M) + I + ca<br>Skip if carry | 000100 | $D_R$ | $D_C$ | I |
| | AICN | M, I | * | Add immediate data to memory with carry, then skip if not carry | M ← (M) + I + ca<br>Skip if not carry | 000101 | $D_R$ | $D_C$ | I |
| | AD | r, M | | Add memory to general register | r ← (r) + (M) | 010000 | $D_R$ | $D_C$ | $R_N$ |
| | ADS | r, M | * | Add memory to general register, then skip if carry | r ← (r) + (M)<br>Skip if carry | 010001 | $D_R$ | $D_C$ | $R_N$ |
| | ADN | r, M | * | Add memory to general register, then skip if not carry | r ← (r) + (M)<br>Skip if not carry | 010010 | $D_R$ | $D_C$ | $R_N$ |
| | AC | r, M | | Add memory to general register with carry | r ← (r) + (M) + ca | 010011 | $D_R$ | $D_C$ | $R_N$ |
| | ACS | r, M | * | Add memory to general register with carry, then skip if carry | r ← (r) + (M) + ca<br>Skip if carry | 010100 | $D_R$ | $D_C$ | $R_N$ |
| | ACN | r, M | * | Add memory to general register with carry, then skip if not carry | r ← (r) + (M) + ca<br>Skip if not carry | 010101 | $D_R$ | $D_C$ | $R_N$ |

| Inst. Gr. | Mnemonic | | Skip Function | Explanation of Function | Explanation of Operation | Machine Language (16 bit) | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | IC (6 bit) | A (2 bit) | B (4 bit) | C (4 bit) |
| SUBTRACTION INSTRUCTION | SI | M, I | | Subtract immediate data from memory | M ← (M) – I | 001000 | $D_R$ | $D_C$ | I |
| | SIS | M, I | * | Subtract immediate data from memory, then skip if borrow | M ← (M) – I<br>Skip if borrow | 001001 | $D_R$ | $D_C$ | I |
| | SIN | M, I | * | Subtract immediate data from memory, then skip if not borrow | M ← (M) – I<br>Skip if not borrow | 001010 | $D_R$ | $D_C$ | I |
| | SIB | M, I | | Subtract immediate data from memory with borrow | M ← (M) – I – b | 001011 | $D_R$ | $D_C$ | I |
| | SIBS | M, I | * | Subtract immediate data from memory with borrow, then skip if borrow | M ← (M) – I – b<br>Skip if borrow | 001100 | $D_R$ | $D_C$ | I |
| | SIBN | M, I | * | Subtract immediate data from memory with borrow, then skip if not borrow | M ← (M) – I – b<br>Skip if not borrow | 001101 | $D_R$ | $D_C$ | I |
| | SU | r, M | | Subtract memory from general register | r ← (r) – (M) | 011000 | $D_R$ | $D_C$ | $R_N$ |
| | SUS | r, M | * | Subtract memory from general register, then skip if borrow | r ← (r) – (M)<br>Skip if borrow | 011001 | $D_R$ | $D_C$ | $R_N$ |
| | SUN | r, M | * | Subtract memory from general register, then skip if not borrow | r ← (r) – (M)<br>Skip if not borrow | 011010 | $D_R$ | $D_C$ | $R_N$ |
| | SB | r, M | | Subtract memory from general register with borrow | r ← (r) – (M) – b | 011011 | $D_R$ | $D_C$ | $R_N$ |
| | SBS | r, M | * | Subtract memory from general register with borrow, then skip if borrow | r ← (r) – (M) – b<br>Skip if borrow | 011100 | $D_R$ | $D_C$ | $R_N$ |
| | SBN | r, M | * | Subtract memory from general register with borrow, then skip if not borrow | r ← (r) – (M) – b<br>Skip if not borrow | 011101 | $D_R$ | $D_C$ | $R_N$ |
| COMPARISON INSTRUCTION | SLTI | M, I | * | Skip if memory is less than immediate data | Skip if (M) < I | 110000 | $D_R$ | $D_C$ | I |
| | SGEI | M, I | * | Skip if memory is greater than or equal to immediate data | Skip if (M) ≧ I | 110001 | $D_R$ | $D_C$ | I |
| | SEQI | M, I | * | Skip if memory is equal to immediate data | Skip if (M) = I | 110010 | $D_R$ | $D_C$ | I |
| | SNEI | M, I | * | Skip if memory is not equal to immediate data | Skip if (M) ≠ I | 110011 | $D_R$ | $D_C$ | I |
| | SEQ | r, M | * | Skip if general register is equal to memory | Skip if (r) = (M) | 100010 | $D_R$ | $D_C$ | $R_N$ |
| | SNE | r, M | * | Skip if general register is not equal to memory | Skip if (r) ≠ (M) | 100011 | $D_R$ | $D_C$ | $R_N$ |

| Inst. Gr. | Mnemonic | | Skip Function | Explanation of Function | Explanation of Operation | Machine Language (16 bit) | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | IC (6 bit) | A (2 bit) | B (4 bit) | C (4 bit) |
| TRANSFER INSTRUCTION | LD | r, M | | Load memory to general register | r ← (M) | 100100 | $D_R$ | $D_C$ | $R_N$ |
| | ST | M, r | | Store general register to memory | M ← (r) | 100101 | $D_R$ | $D_C$ | $R_N$ |
| | MVSR | $M_1$, $M_2$ | | Move memory to memory in the same row | ($D_R$, $D_{C1}$) ← ($D_R$, $D_{C2}$) | 011111 | $D_R$ | $D_{C1}$ | $D_{C2}$ |
| | MVIM | M, I | | Move immediate data to memory | M ← I | 001111 | $D_R$ | $D_C$ | I |
| | MVGD | r, M | | Move memory to destination memory referring to G-register and general register | [(G), (r)] ← (M) | 100110 | $D_R$ | $D_C$ | $R_N$ |
| | MVGS | M, r | | Move source memory referring to G-register and general register to memory | M ← [(G), (r)] | 100111 | $D_R$ | $D_C$ | $R_N$ |
| INPUT AND OUTPUT INSTRUCTION | IN1 | M, C | | Input IN1 port data to memory | M ← [IN1] $_C$ | 111000 | $D_R$ | $D_C$ | $C_N$ |
| | OUT1 | C, M | | Output contents of memory to OUT1 port | [OUT1] $_C$ ← (M) | 111011 | $D_R$ | $D_C$ | $C_N$ |
| | IN2 | M, C | | Input IN2 port data to memory | M ← [IN2] $_C$ | 111001 | $D_R$ | $D_C$ | $C_N$ |
| | OUT2 | C, M | | Output contents of memory to OUT2 port | [OUT2] $_C$ ← (M) | 111100 | $D_R$ | $D_C$ | $C_N$ |
| LOGICAL OPERATION INSTRUCTION | ORR | r, M | | Logical OR of general register and memory | r ← (r) ∨ (M) | 010110 | $D_R$ | $D_C$ | $R_N$ |
| | ANDR | r, M | | Logical AND of general register and memory | r ← (r) ∧ (M) | 010111 | $D_R$ | $D_C$ | $R_N$ |
| | ORIM | M, I | | Logical OR of memory and immediate data | M ← (M) ∨ I | 000110 | $D_R$ | $D_C$ | I |
| | ANIM | M, I | | Logical AND of memory and immediate data | M ← (M) ∧ I | 000111 | $D_R$ | $D_C$ | I |
| | XORIM | M, I | | Logical exclusive OR of memory and immediate data | M ← (M) ⊕ I | 001110 | $D_R$ | $D_C$ | I |
| | XORR | r, M | | Logical exclusive OR of general register and memory | r ← (r) ⊕ (M) | 011110 | $D_R$ | $D_C$ | $R_N$ |
| BIT JUDGE INSTRUCTION | TMTR | r, M | * | Test general register bits by memory bits, then skip if all bits specified are true | Skip if r [N (M)] = all “1” | 100000 | $D_R$ | $D_C$ | $R_N$ |
| | TMFR | r, M | * | Test general register bits by memory bits, then skip if all bits specified are false | Skip if r [N (M)] = all “0” | 100001 | $D_R$ | $D_C$ | $R_N$ |
| | TMT | M, N | * | Test memory bits, then skip if all bits specified are true | Skip if M (N) = all “1" | 110101 | $D_R$ | $D_C$ | N |
| | TMF | M, N | * | Test memory bits, then skip if all bits specified are false | Skip if M (N) = all “0” | 110111 | $D_R$ | $D_C$ | N |
| | TMTN | M, N | * | Test memory bits, then not skip if all bits specified are true | Skip if M (N) = not all “1" | 110100 | $D_R$ | $D_C$ | N |
| | TMFN | M, N | * | Test memory bits, then not skip if all bits specified are false | Skip if M (N) = not all “0” | 110110 | $D_R$ | $D_C$ | N |

| Inst. Gr. | Mnemonic | Skip Function | Explanation of Function | Explanation of Operation | Machine Language (16 bit) | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | IC (6 bit) | A (2 bit) | B (4 bit) | C (4 bit) |
| SUBROUTINE INSTRUCTION | CALL $ADDR_1$ | | Call subroutine | STACK ← (PC) + 1 and PC ← $ADDR_1$ | 1010 | $ADDR_1$ (12 bit) | | |
| | RN | | Return to main routine | PC ← (STACK) | 111111 | 00 | — | — |
| | RNS | * | Return to main routine and skip unconditionally | PC ← (STACK) and skip | 111111 | 01 | — | — |
| JUMP INST. | JUMP $ADDR_1$ | | Jump to the address specified | PC ← $ADDR_1$ | 1011 | $ADDR_1$ (12 bit) | | |
| OTHER INSTRUCTION | DAL $ADDR_2$, r | | Load program memory in page 0 to DATA register | DATA ← [$ADDR_2$ + (r)] $_P$ in page 0 | 111110 | | | $R_N$ |
| | WAIT P | | At P = "0" H, the condition is CPU waiting (soft wait mode) | Wait at condition P | 111111 | 10 | 0000 | P |
| | | | At P = "1" H, except for clock generator, all function is waiting (hard wait mode) | | | | | |
| | CKSTP | | Clock generator stop | Stop clock generator at MODE condition | 111111 | 10 | 1000 | — |
| | NOOP | | No operation | — | 111111 | 11 | — | — |

Note 9: Among 10 bits of the program memory address assigned by DAL instruction, the lower rank of 4 bits become indirect addressing based on the content of general register.

DAL instruction executing time is 80 μs (2 machine cycles).

Note 10: MVGS instruction executing time is 80 μs (2 machine cycles).

### I/O Map

All ports in the device are expressed by matrix of four input and output instruction (OUT1~2 instructions, IN1~2 instructions) and 4 bits of code No. C. Assignment of these ports is indicated previously as I/O map. In the I/O map, port names treated in the execution of each input and output instruction are assigned horizontally, while code No. of port are assigned vertically. G-register and data register are also treated as port.

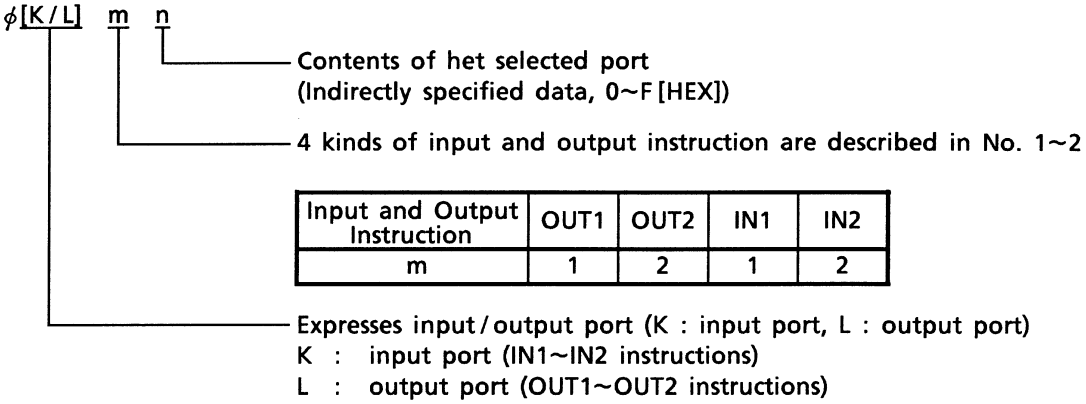
The OUT1~2 instructions are assigned to output port, and IN1~2 instructions are assigned to input port.

Note 11: The port indicated with oblique line on I/O map is a port not existing in the device. In the execution of output instruction, when data is output to the non-existing output port, no effect is given to the content of other port or data memory. When non-existing input port is designated during the execution of input instruction, the content read into the data memory becomes "1".

Note 12: Among the output ports on I/O map, * marked port is unused port. The data output here becomes "don't care".

Note 13: Regarding the content of port expressed in 4 bits, Y1 corresponds to the least significant of the data of data memory, and Y8 to the most significant bit.

Each port assigned by four input and output instruction and code No. C is coded as follows:




(example) The G-register is set by OUT1 instruction wite code "F".
Therefore, the notation is "ϕL1F".

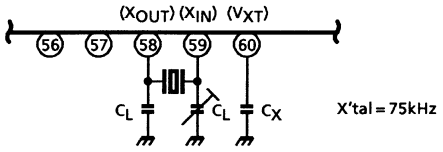
**I/O Map**

| | I/O | ϕL1 | | | | ϕL2 | | | | ϕK1 | | | | ϕK2 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | OUT1 | | | | OUT2 | | | | IN1 | | | | IN2 | | | |
| | Code | Y1 | Y2 | Y4 | Y8 | Y1 | Y2 | Y4 | Y8 | Y1 | Y2 | Y4 | Y8 | Y1 | Y2 | Y4 | Y8 |
| CN | 0 | HF | IF OFFSET | | FM | A/D CONTROL | | | | IF CONTROL | | | 1 | A/D DATA | | | |
| | | | +1 | −1 | | AD SEL0 | AD SEL1 | REF SEL0 | REF SEL1 | BUSY | MANUAL | OVER | | AD0 | AD1 | AD2 | AD3 |
| | 1 | PROGRAMMABLE COUNTER | | | | A/D CONTROL | | | | IF DATA | | | | A/D DATA | | | 1 |
| | | P0 | P1 | P2 | P3 | STA | DCREF ON | AD1 ON | AD2 ON | F0 | F1 | F2 | F3 | AD4 | AD5 | BUSY | |
| | 2 | PROGRAMMABLE COUNTER | | | | I/O-1 DATA | | | | IF DATA | | | | I/O-1 DATA | | | |
| | | P4 | P5 | P6 | P7 | −0 | −1 | −2 | −3 | F4 | F5 | F6 | F7 | −0 | −1 | −2 | −3 |
| | 3 | PROGRAMMABLE COUNTER | | | | I/O-2 DATA | | | | IF DATA | | | | I/O-2 DATA | | | |
| | | P8 | P9 | P10 | P11 | −0 | −1 | −2 | −3 | F8 | F9 | F10 | F11 | −0 | −1 | −2 | −3 |
| | 4 | PROGRAMMABLE COUNTER | | | | I/O-3 DATA | | * | | IF DATA | | | | I/O-3 DATA | | 1 | |
| | | P12 | P13 | P14 | P15 | −0 | −1 | | | F12 | F13 | F14 | F15 | −0 | −1 | | |
| | 5 | REFERENCE SELECT | | | PROGURAMMABLE COUNTER | I/O-1 CONTROL | | | | IF DATA | | | | | | | |
| | | R0 | R1 | R2 | P16 | −0 | −1 | −2 | −3 | F16 | F17 | F18 | F19 | | | | |
| | 6 | IF COUNTER CONTROL | | | | I/O-2 CONTROL | | | | | | | | KEY INPUT DATA | | | |
| | | IF/IN | * | * | * | −0 | −1 | −2 | −3 | | | | | K0 | K1 | K2 | K3 |
| | 7 | IF COUNTER CONTROL | | | | I/O-3 CONTROL | | | | UNLOCK | | IN PORT | | KEY SCAN DIGIT | | | 1 |
| | | STA/$\overline{\text{STP}}$ | MANUAL | G0 | G1 | −0 | −1 | * | * | F/F | ENABLE | IN | 1 | KS0 | KS1 | KS2 | |
| | 8 | MUTE | MUTE CONTROL | | | KEY RETURN TIMING | | | | | | | | KEY SCAN INPUT DATA-0 | | | |
| | | | I/O | POL | UNLOCK | T0 | T1 | T2 | T3 | | | | | KS00 | KS01 | KS02 | KS03 |
| | 9 | UNLOCK RESET | DO1 CONTROL | | | KEY RETURN TIMING | | * | | | | | | KEY SCAN INPUT DATA-1 | | | |
| | | | OTC | OT | Hz | T4 | T5 | | | | | | | KS10 | KS11 | KS12 | KS13 |
| | A | TIMER RESET | | TEST DATA | | | | | | TIMER | | | STOP F/F | KEY SCAN INPUT DATA-2 | | | |
| | | 2Hz F/F | TIMER | #4 | #5 | | | | | 2Hz F/F | 10 Hz | 100 Hz | | KS20 | KS21 | KS22 | KS23 |
| | B | BUZR DATA | | | | | | | | $\overline{\text{HOLD}}$ | 1 | | | KEY SCAN INPUT DATA-3 | | | |
| | | B0 | B1 | B2 | B3 | | | | | | | | | KS30 | KS31 | KS32 | KS33 |
| | C | BUZR DATA | | | | | | | | DATA-reg | | | | KEY SCAN INPUT DATA-4 | | | |
| | | B4 | B5 | B6 | B7 | | | | | d0 | d1 | d2 | d3 | KS40 | KS41 | KS42 | KS43 |
| | D | TEST DATA | | | | SEG DATA SELECT | | | | DATA-reg | | | | KEY SCAN INPUT DATA-5 | | | |
| | | #0 | #1 | #2 | #3 | S1 | S2 | S4 | S8 | d4 | d5 | d6 | d7 | KS50 | KS51 | KS52 | KS53 |
| | E | * | BUZR ON | * | CKSTP MODE | SEG-1 DATA | | | | DATA-reg | | | | KEY SCAN INPUT DATA-6 | | | |
| | | | | | | COM1 | COM2 | COM3 | * | d8 | d9 | d10 | d11 | KS60 | KS61 | KS62 | KS63 |
| | F | G REGISTER | | | | SEG-2 DATA | | | | DATA-reg | | | | KEY SCAN INPUT DATA-7 | | | |
| | | G0 | G1 | G2 | G3 | COM1 | COM2 | COM3 | * | d12 | d13 | d14 | d15 | KS70 | KS71 | KS72 | KS73 |

### Connecting Crystal Oscillator

The following diagram shows the connection of the 75 kHz crystal oscillator to the device's crystal oscillator pins ($X_{IN}$, $X_{OUT}$).

The oscillation signal is supplied to the clock generator, reference frequency divider, and other sub-systems to generate the various CPU timing signals, reference frequency, and other signals. The power supply for the crystal oscillator circuit is the voltage ($V_{XT}$ = 1.4 V typ.) supplied by the built-in constant voltage circuit. This stabilizes the crystal oscillation and reduces the current consumption.




Note 14: Use a crystal oscillator with a low CI value and with good startup characteristics.

### System Reset

The system is reset when a low level is applied to the $\overline{\text{RESET}}$ pin, or when the voltage supplied to the $V_{DD}$ pin goes from 0 V to 1.8 V or more (a power on reset). Following a system reset, the program starts from address 0 after a standby period of 100 ms.

As the power on reset function is typically used, fix the $\overline{\text{RESET}}$ pin to the high level.

Note 15: During a system reset and during the standby period following the reset, the LCD common and segment outputs are fixed at the low level.

Note 16: After a system reset, the internal ports shown in the following table are fixed at the specified levels. The states of the other ports after a reset are undefined. Therefore, initialize the ports in the program when necessary.

**Fixed Internal Ports**

| Ports Set to "0" | Ports Set to "1" |
|---|---|
| MANUAL bit (ϕL17) | REFERENCE PORT (ϕL15) |
| IO, POL, UNLOCK bit (ϕL18) | MUTE bit (ϕL18) |
| DO1 CONTROL PORT (ϕL19) | IF/$\overline{\text{IN}}$ bit (ϕL16) |
| BUZR ON bit (ϕL1E) | DISP OFF bit (ϕL2FF) |
| TEST PORT (ϕL1A, ϕL1D) | |
| CKSTP MODE bit (ϕL1E) | |
| AD CONTROL PORT (ϕL20, ϕL21) | |
| TIMER PORT (ϕK1A) | |
| KEY RETURN SELECT bit (ϕL2FF) | |
| IO-1~IO-3 IO CONTROL PORT (ϕL25~ϕL27) | |

## Backup Modes

To enter the three backup modes, execute the CKSTP or WAIT instruction.

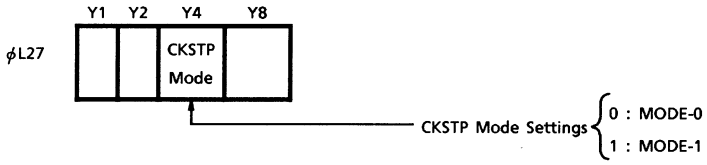
### 1. Clock Stop Mode

Clock stop mode halts the system and maintains the internal state of the system immediately prior to halting. During a halt, the system is maintained with low current consumption (10 μA or below, at $V_{DD}$ = 3.0 V). In clock stop mode, the crystal oscillator halts and the output ports and LCD display output pins are all automatically set to the low level or the off state. The supply voltage can be reduced to 1.0 V.

When the CKSTP instruction is executed, execution halts at the address of the CKSTP instruction. Therefore, execution starts again from the next instruction when clock stop mode is released (after a standby period of around 100 ms).

(1) Setting clock stop mode

Clock stop mode can be set to one of two modes. The CKSTP bit determines which of the two modes is set. Use the OUT2 instruction with the operand [$C_N$ = 7H] to access this bit.




1) MODE-0

In mode 0, executing the CKSTP instruction when the $\overline{HOLD}$ pin is low enters clock stop mode. Executing the CKSTP instruction when the $\overline{HOLD}$ pin is high is equivalent to executing a NOOP instruction.

2) MODE-1

In mode 1, executing the CKSTP instruction enters clock stop mode regardless of the level of the $\overline{HOLD}$ pin.

Note 17: The PLL turns off during execution of the CKSTP instruction.

(2) Releasing clock stop mode

1) MODE-0

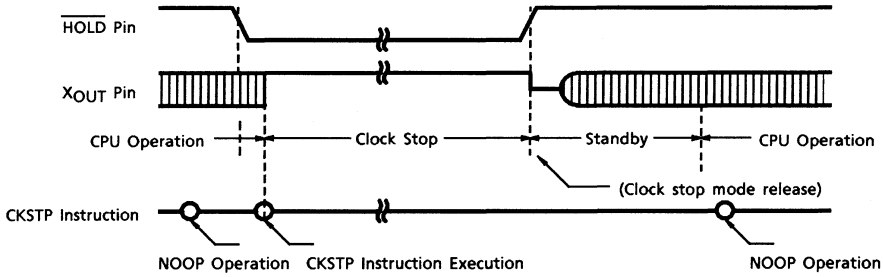
In mode 0, clock stop mode is released when the $\overline{HOLD}$ pin goes to high, or by a change in the input state of any I/O port 1 pin (P1-0~P1-3) set as an input port.

2) MODE-1

In mode 1, clock stop mode is released by a change in the input state of the $\overline{HOLD}$ pin or in the input state of any I/O port 1 pin (P1-0~P1-3) set as an input port.

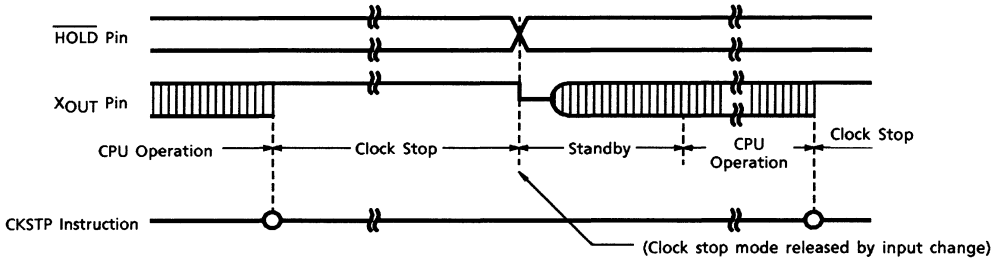
(3) Clock stop mode timing

1) MODE-0



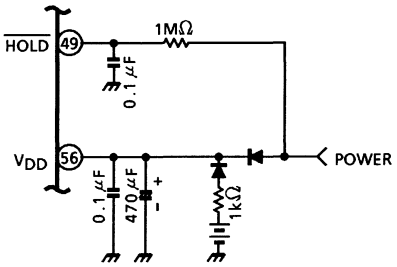

(executing the CKSTP instruction while the $\overline{\text{HOLD}}$ pin input is low sets the device to clock stop mode.)

2) MODE-1

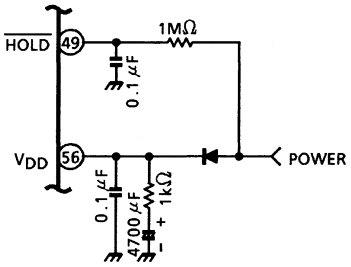



(executing the CKSTP instruction always sets the device to clock stop mode.)

(4) Circuit example (MODE-0)




**Example of Backup Circuit Using Battery**




**Example of Backup Circuit Using Capacitor**

## 2. Wait Mode

Wait mode halts the system and maintains, with reduced current consumption, the internal state of the system immediately prior to halting. Two wait modes are available: "soft wait" and "hard wait". When the WAIT instruction is executed, execution halts at the address of the WAIT instruction. Therefore, when wait mode is released, execution starts again from the next instruction without delaying for the standby time.

(1) Soft wait mode

Executing the WAIT instruction with the operand [P = 0H] stops only the CPU inside the device. In this mode, the crystal oscillator, display circuit, and other circuitry continue to operate normally.

Using soft wait mode in the program for clock functions reduces the current consumed during clock operation.

Note 18: The current consumption depends on the program.

(2) Hard wait mode

Executing the WAIT instruction with the operand [P = 1H] stops all operation other than the crystal oscillator. This reduces current consumption still further than soft wait mode. In this state, the CPU and display circuits are halted, and the LCD display output pins are all automatically fixed at the low level. (15 μA typ. at $V_{DD}$ = 3 V)

(3) Setting wait mode

Executing the WAIT instruction always sets wait mode.

Note 19: In hard wait mode, the PLL turns off, while in soft wait mode, the PLL does not turn off. Accordingly, before setting a soft wait, turn the PLL off by software.

(4) Wait mode release conditions

Wait mode is released by the following conditions.

1) At a change in the input state of the $\overline{\text{HOLD}}$ pin
2) When a high level is input to a key input pin (K0~K3)

(Note 20: depends on the key input mode)

3) When the 2 Hz timer flip-flop is set to "1". (in soft wait mode only)
4) At a change in the input state of an I/O-1 port (P1-0~P1-3) set as an input port

## 3. $\overline{\text{HOLD}}$ Input Port

| | Y1 | Y2 | Y4 | Y8 |
|---|---|---|---|---|
| φK1B | $\overline{\text{HOLD}}$ | 1 | 1 | 1 |

The $\overline{\text{HOLD}}$ pin can be used as an input port. Executing the IN1 instruction with the operand [$C_N$ = BH] reads the data input from this bit to data memory.

When setting clock stop mode, always access this port prior to executing the CKSTP instruction.

Note that if the CKSTP instruction is executed without first accessing this port, the device may not enter clock stop mode.

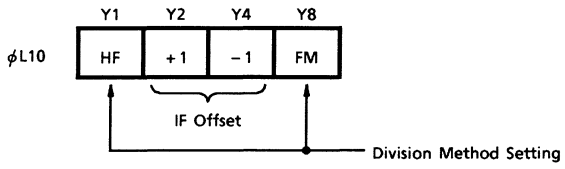
## Programmable Counter

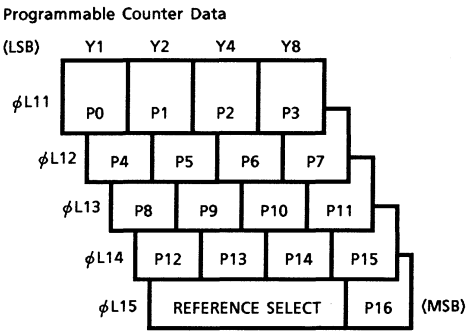
The programmable counter block consists of a 2-modulus prescaler, 4 bit and 13 bit programmable counters, and the ports used to control the block.

The programmable counters can be turned on and off by the contents of the reference ports.

### 1. Programmable Counter Control Ports

These ports control the divisor, division method, and the IF correction (IF offset) for the FM band.




Access the division method and the IF offset using the OUT1 instruction with the operand [$C_N$ = 0H].

Access the divisor settings using the OUT1 instruction with the operands [$C_N$ = 1H~5H]. Set the divisor by writing to bits P0~P16. When the programmable counter data (P16) is set, all the data from P0 to P16 are updated. Therefore, always access P16 to set the data, even when changing only a portion of the data.

And the reference frequency is set at the same time.

### 2. Setting Division Method

The HF and FM bits select the pulse swallow or direct division method.

As the following table shows, there are four methods. Select the appropriate method in accordance with the frequency band used.

| Mode | HF | FM | Division Method | Example of Reception Band | Operating Frequency Range | Input Pin | Divisior (Note 20) |
|---|---|---|---|---|---|---|---|
| LF | 0 | 0 | Direct division method | MW/LW | 0.5~12 MHz | $AM_{IN}$ | n |
| HF | 1 | 0 | (1/15 or 1/16) Pulse swallow method | SW | 1.0~45 MHz | | |
| FM | 0 | 1 | | FM | 40~130 MHz | $FM_{IN}$ | |
| VHF | 1 | 1 | 1/2 × (1/15 or 1/16) Pulse swallow method | VHF | 50~230 MHz | | 2n |

Note 21: n indicates the programmed divisor.

## 3. IF Correction Function for FM Band

When the pulse swallow method is selected, the ΔIF ± 1 ports allow the actual divisor to be varied by ±1 without changing the programmed divisor. This can be used for IF offset in FM.

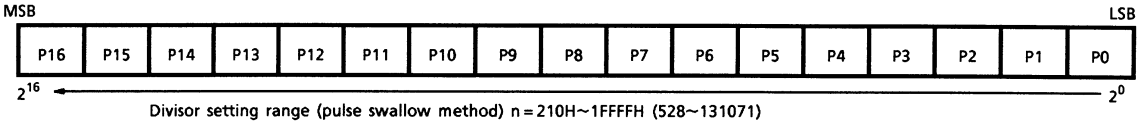
When the direct division method is selected, the IF offset function does not operate.

| ΔIF + 1 | ΔIF – 1 | Divisor (at $FM_H$) | Divisor (at $FM_L$, HF) |
|---|---|---|---|
| 0 | 0 | 2·n | n |
| 0 | 1 | 2·(n – 1) | n – 1 |
| 1 | 0 | 2·(n + 1) | n + 1 |
| 1 | 1 | Prohibited | Prohibited |

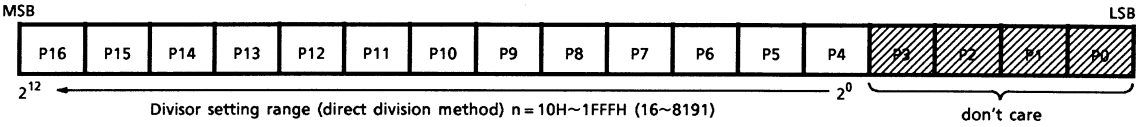
## 4. Setting Divisor

Set the divisor of the programmable counter as a binary value in bits P0~P16.

- Pulse swallow method (17 bits)




- Direct division method (13 bits)



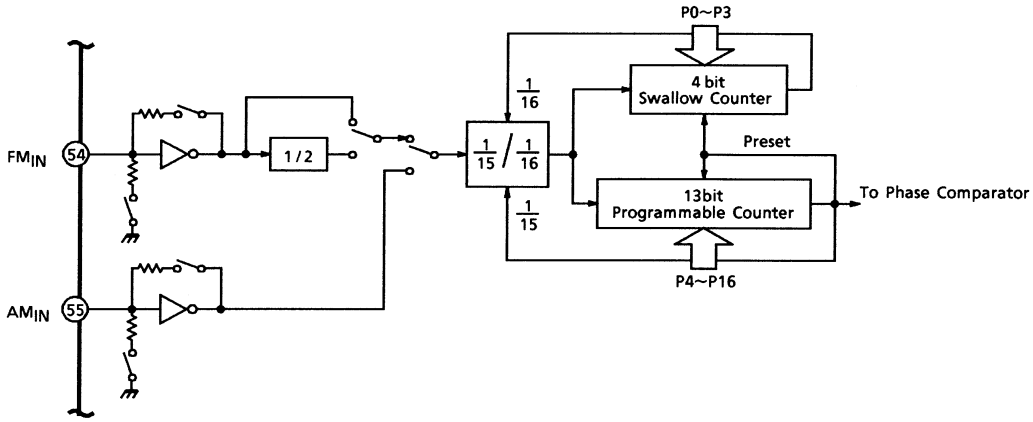

Note 22: In case of direct dividing mode, Pϕ~P3 (ϕL11) data be comes unrelated and P4 port becomes LSB.

Note 23: In VHF mode, the divisor is double the programmed divisor.

## 5. Programmable Counter Circuit Structure

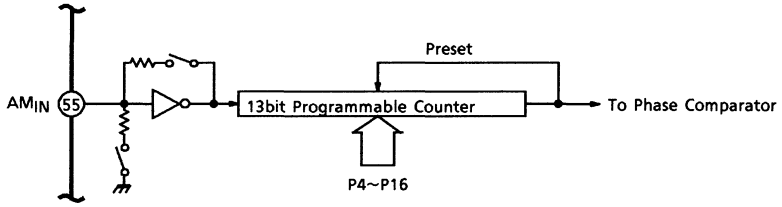
- Pulse swallow method circuit structure

The programmable counter circuit is made up of a 1/15 or 1/16 2-modulus prescaler, a 4 bit swallow counter, and a 13 bit binary programmable counter. In $FM_H$ mode, a 1/2 divider is inserted before the prescaler.



- Direct division method circuit structure

  This circuit bypasses the prescaler and uses the 13 bit programmable counter.




Note 24: The $FM_{IN}$ and $AM_{IN}$ pins incorporate amps. Connecting a capacitor permits low-amplitude operation. The input pins not selected by the division method are pulled down. In PLL off mode (set by the reference port), the inputs are also pulled down.

## Reference Frequency Divider

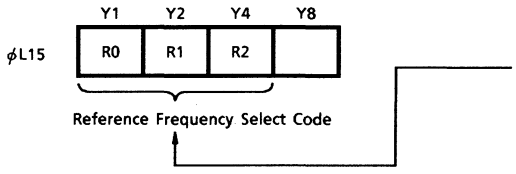
The reference frequency divider divides the frequency of the external 75 kHz crystal oscillator to generate seven PLL reference frequency signals: 1 kHz, 3 kHz, 3.125 kHz, 5 kHz, 6.25 kHz, 12.5 kHz, and 25 kHz. The frequency signal is selected by the reference port data.

The selected signal is supplied as the reference frequency for the phase comparator, which is described next. The PLL is turned on or off by the reference port setting.

### 1. Reference Port

The reference port is an internal port used to select the reference frequency signal (from the seven frequencies). Use the OUT1 instruction with the operand [$C_N$ = 5H] ($\phi$L15) to access this port. When the contents of the reference port are all "1", the programmable counter, IF counter, and reference counter are halted, and the PLL is turned off.

When the reference port are set, the frequency division data of the programmable counter are updated. Therefore, in case of setting reference port, it is neccesary to set the frequency division data of the programmable counter.




| R2 | R1 | R0 | / | REFERENCE FREQUENCY |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1kHz |
| 0 | 0 | 1 | 1 | 3kHz |
| 0 | 1 | 0 | 2 | 3.125kHz |
| 0 | 1 | 1 | 3 | 5kHz |
| 1 | 0 | 0 | 4 | 6.25kHz |
| 1 | 0 | 1 | 5 | 12.5kHz |
| 1 | 1 | 0 | 6 | 25kHz |
| 1 | 1 | 1 | 7 | PLL OFF MODE |

## Phase Comparator, Clock Detection Port

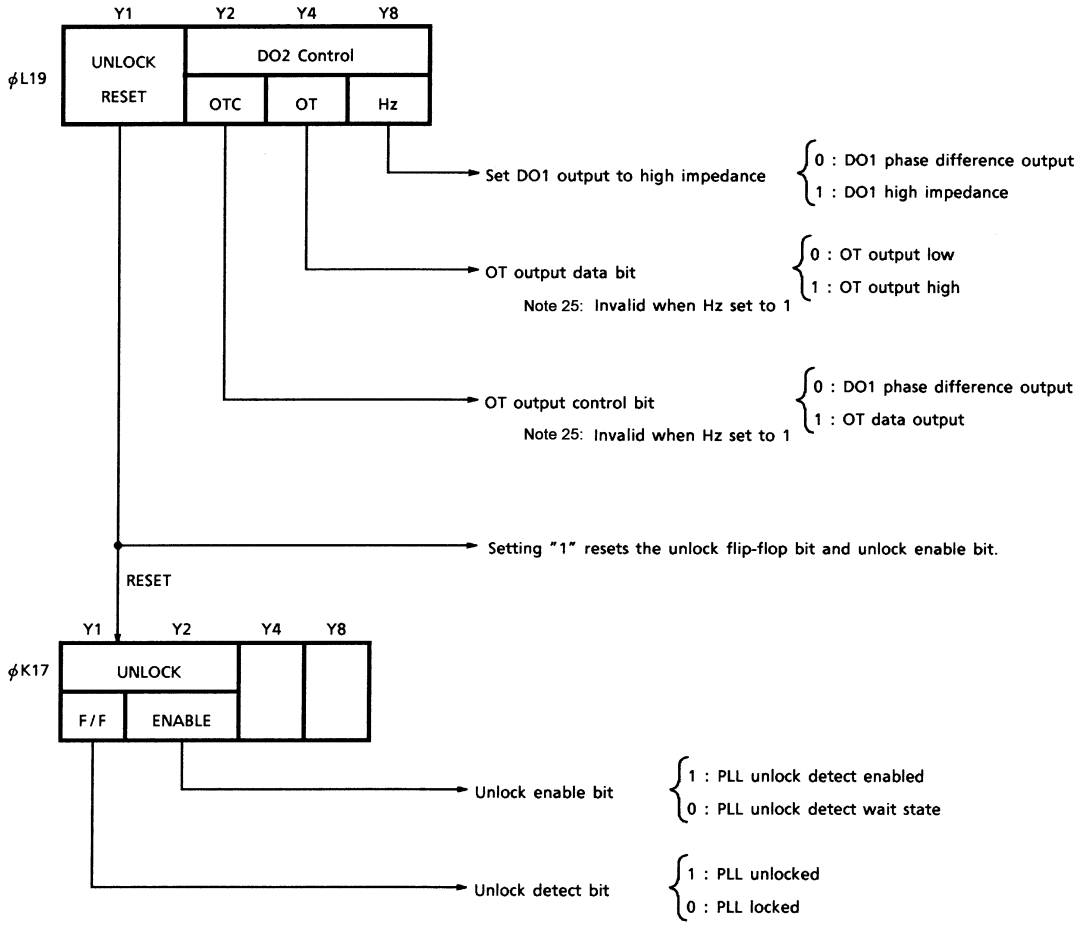
The phase comparator compares the reference frequency signal supplied by the reference frequency divider with the divided signal output by the programmable counter, and outputs the phase difference. The output of the phase comparator is used to control the VCO via the low pass filter so as to eliminate the frequency and phase difference between the two signals.

Data are output from the phase comparator to the tristate buffered DO1 and DO2 pins in parallel. This enables the optimal filter constants to be designed for both FM and AM bands.

Also, the DO1 pin can be set for general-purpose output by the DO1 control port. The DO1 pin can also be set to high impedance. By using the DO1 and DO2 pins, PLL loop characteristics, such as the lockup time, can be improved.

The lock detection port can be used to detect the PLL lock state.

### 1. DO2 Control Port, Unlock Detection Port



The OTC, OT, and Hz control bits of the DO1 control port set the DO1 output pin as a general-purpose output port, and control whether DO1 goes to high impedance instead of outputting the phase difference.

Set these bits to the required values by program.

When the phase is approximately 180°, the unlock flip-flop bit detects the phase difference between the divided output of the programmable counter and the reference frequency. If the phase difference does not match, that is, if the PLL is unlocked, the unlock flip-flop is set. Also, setting the unlock reset bit to "1" resets the unlock flip-flop.

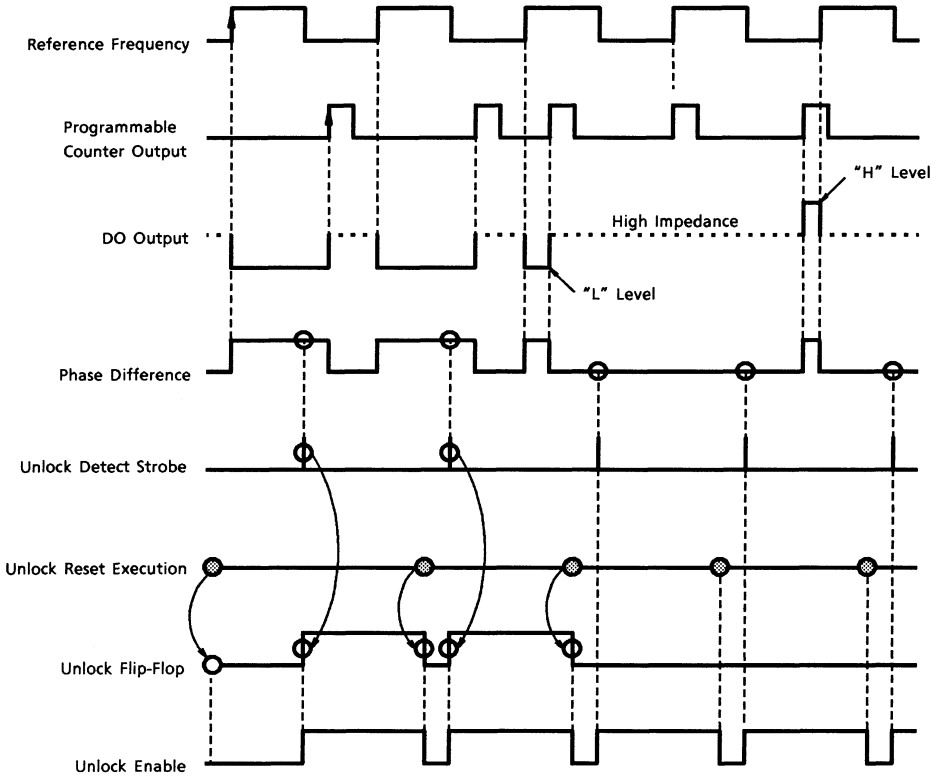
To detect the phase difference during the reference voltage period, reset the unlock flip-flop, then access the unlock flip-flop after waiting for a time longer than the reference frequency period. An enable bit is supplied for this purpose. After confirming that the unlock enable bit is set to "1", access the unlock flip-flop.

Setting the unlock reset bit to "1" resets the unlock enable bit.

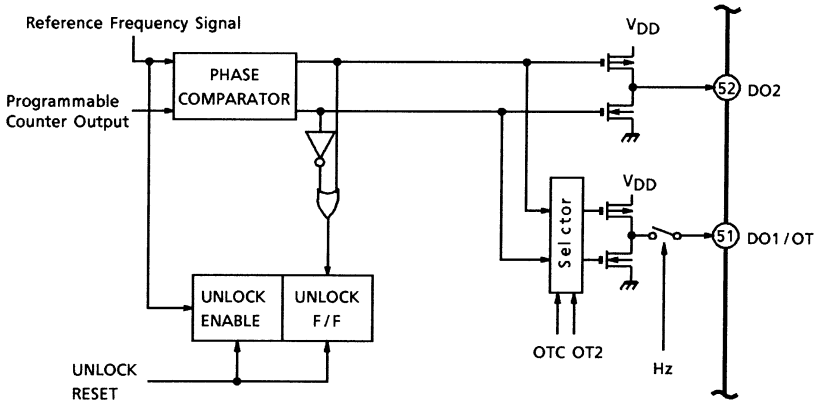
Use the OUT1 and IN1 instructions with the operand [$C_N$ = 7 or 9H] to control these ports, and to load data.

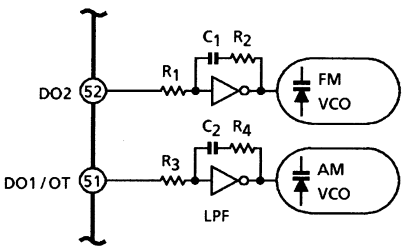
Note 26: When the PLL is off, the DO output is set to high impedance. However, when DO1 is set as an output port (OT output), the data are output from the port without change.

## 2. Phase Comparator, Unlock Port Timing

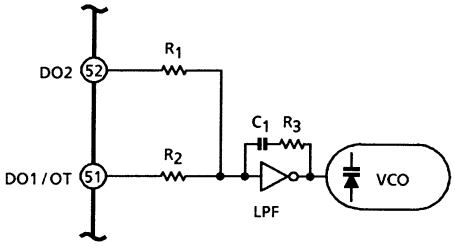


### 3. Phase Comparator, Unlock Port Circuit Structure

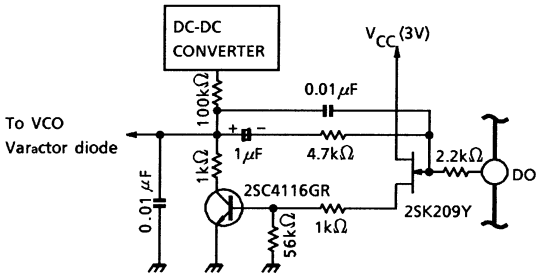



**When Setting Different Filter Constants for Each Band**




**When Using the Same Low Pass Filter for Both Bands (set DO1 to high impedance to switch the filter constant)**



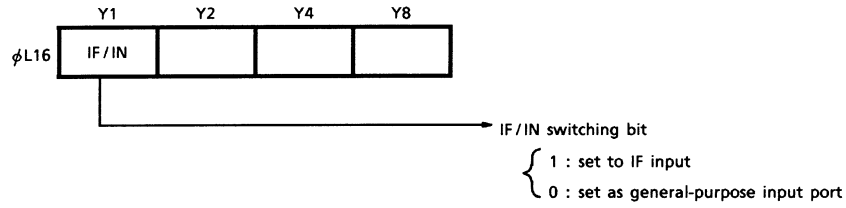

Note 27: The filter circuit shown in the above figure is an example for reference, and the actual circuit should be investigated and designed conforming to the system band construction and the required characteristics.

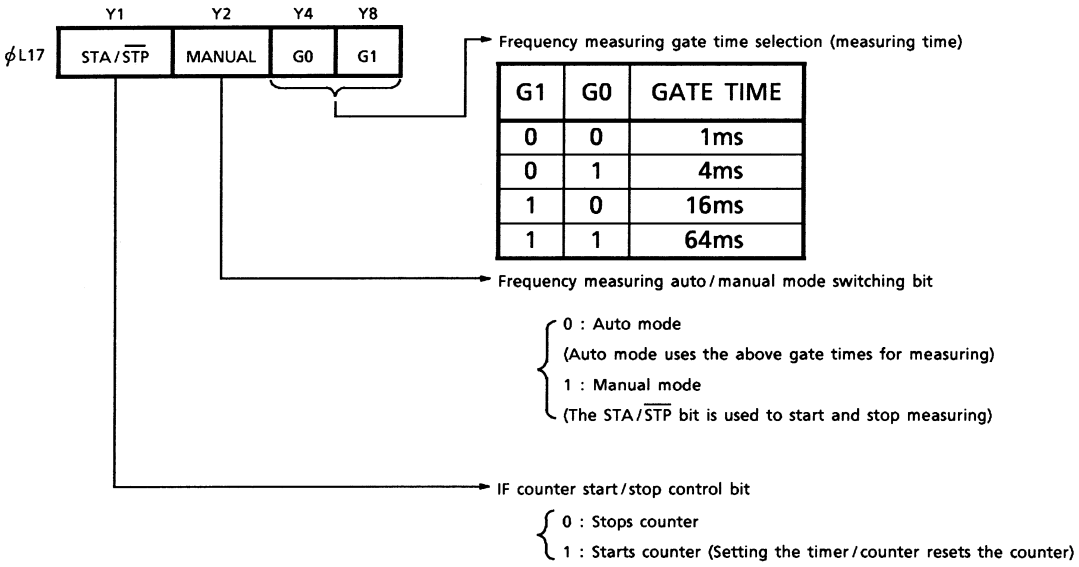
## IF Counter

This is a 20 bit general-purpose intermediate frequency (IF) counter used for such purposes as counting the FM or AM intermediate frequency during auto-tuning or detecting the auto-stop signal.

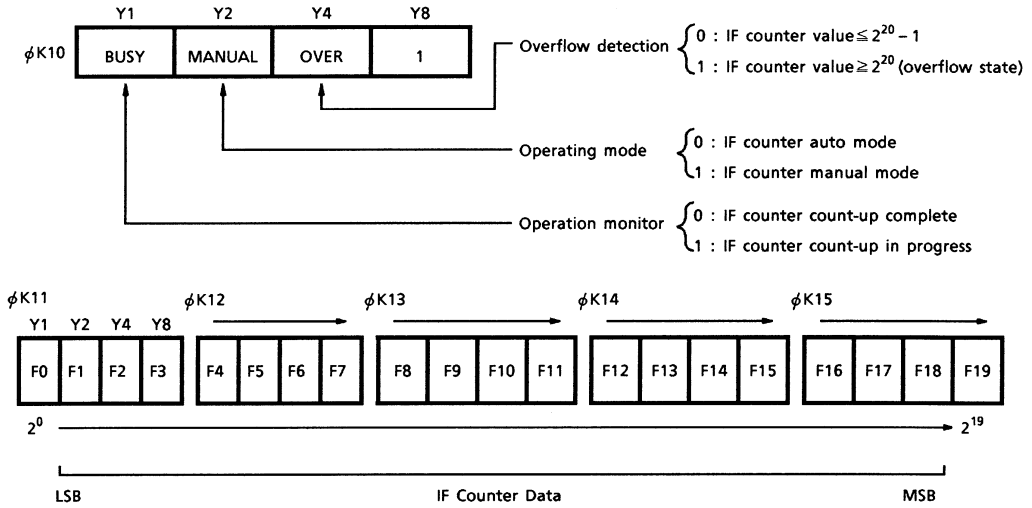
The IF counter block consists of a 20 bit binary counter and a control port.

### 1. IF Counter Control Port, Data Port




| G1 | G0 | GATE TIME |
|---|---|---|
| 0 | 0 | 1ms |
| 0 | 1 | 4ms |
| 1 | 0 | 16ms |
| 1 | 1 | 64ms |




Note 28: When the PLL is off, the IF counter is disabled.

(1) IF counter auto mode (frequency measuring)

To use IF counter auto mode, use the IF/$\overline{\text{IN}}$ switching bit to set the IF pin to IF input.

Set the gate time based on the IF input frequency band. Set the MANUAL bit to "0" and the STA/$\overline{\text{STP}}$ bit to "1" to start the IF counter.

As a result, the clock for the 20 bit binary counter is input from the IF pin for the specified gate time. The IF counter counts the number of input pulses. To determine when the IF counter has finished counting, check the BUSY bit. When the count equals or exceeds $2^{20}$ input pulses, the OVER bit is set to "1".

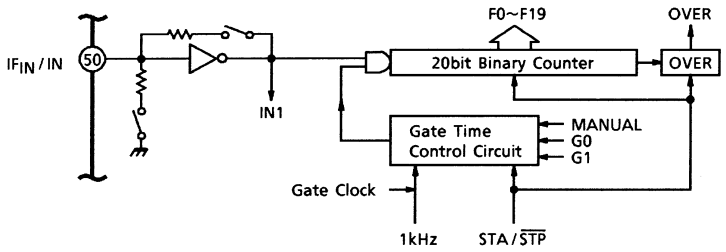
To measure the frequency input to the IF input pin, load the F0~F19 IF data when the BUSY and OVER bits are both "0".

(2) IF counter manual mode (frequency measuring)

Use manual mode to measure the frequency using the IF frequency by controlling the gate time using an internal time base (eg, 10 Hz).

Perform the same IF counter input settings as for auto mode, and set the G0 and G1 bits to other than "1". Set the MANUAL bit to "1" and the STA/$\overline{\text{STP}}$ bit to "1" to start the count. Setting the STA/$\overline{\text{STP}}$ bit to "0" terminates the count and loads the data in binary format.

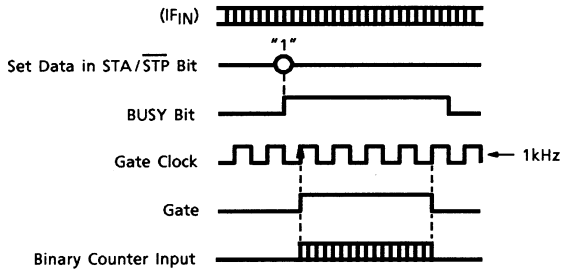
## 2. IF Counter Circuit Structure




The IF counter block consists of an input amp, a gate timer control circuit, and a 20 bit binary counter.

When the PLL is turned off, the IF counter is off. However, the block can still operate when set as a timer/counter.

Note 29: The $IF_{IN1}$ pins incorporate amps. Connecting the pins via a capacitor permits low-amplitude operation.




**Frequency Measuring Auto Mode**

## LCD Driver

The LCD driver has a 1/3 duty and 1/2 bias drive (frame frequency is 83 Hz).

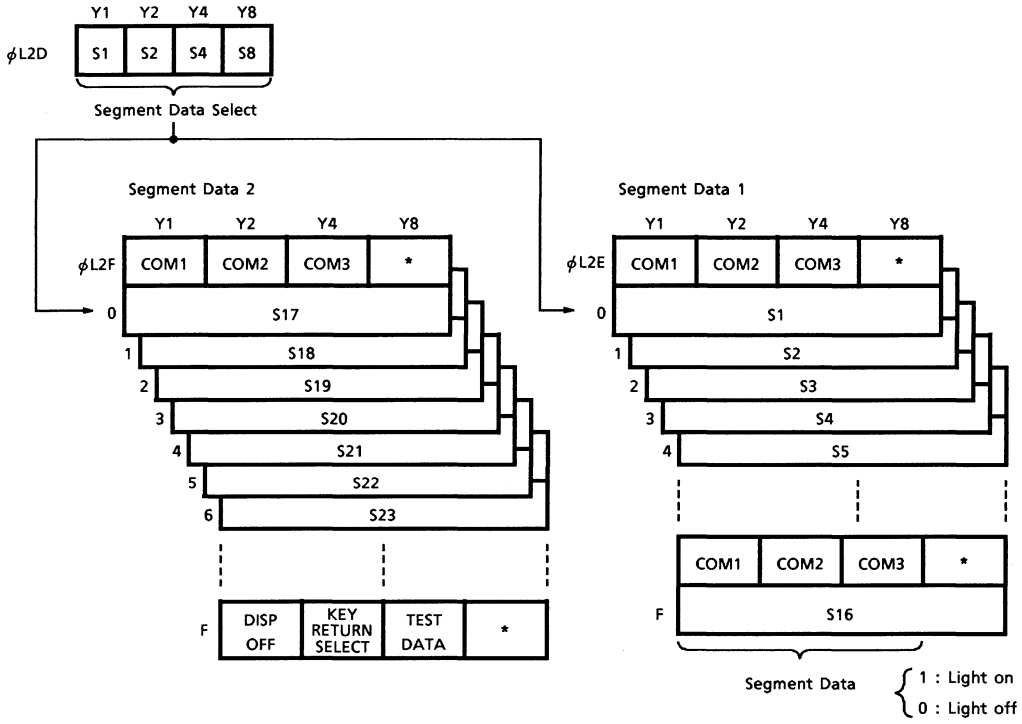
The common outputs are at three voltages: $V_{LCD}$, $V_{LCD}/2V_{EE}$, and GND. The segment outputs are at two voltages: $V_{LCD}$ and GND.

The combination of three common outputs and 23 segment outputs enables the LCD driver to drive a maximum of 69 segments.

LCD driver segment output pins S16~S23 are also used for the key return timing signals for loading key matrix data.

The LCD driver incorporates a constant voltage circuit ($V_{EE}$ = 1.5 V) and voltage double boosting circuit ($V_{LCD}$ = 3.0 V) for the display. This maintains an even LCD contrast regardless of fluctuations in the supply voltage.

### 1. LCD Driver Port




*: Don't care

Note 30: The segment data control whether or not the segments corresponding to the common and segment outputs are lit.

Note 31: The DISP OFF bit is set to "1" at a system reset and at release of clock stop mode.

The LCD driver control ports consist of a segment data selection port and segment data ports. Use the OUT2 instruction with the operand [$C_N$ = DH~FH] to access these ports.

Set the LCD driver segment data using the segment data ports (ϕL2E, ϕL2F). Set the segment data port to "0" to turn the LCD display off and set "1" to turn the LCD display on. When FH is specified for the segment data select port, the DISP OFF and KEY RETURN SELECT bits are selected as segment-2 data (ϕL2FF). The DISP OFF bit can turn the whole LCD display off without setting segment data.

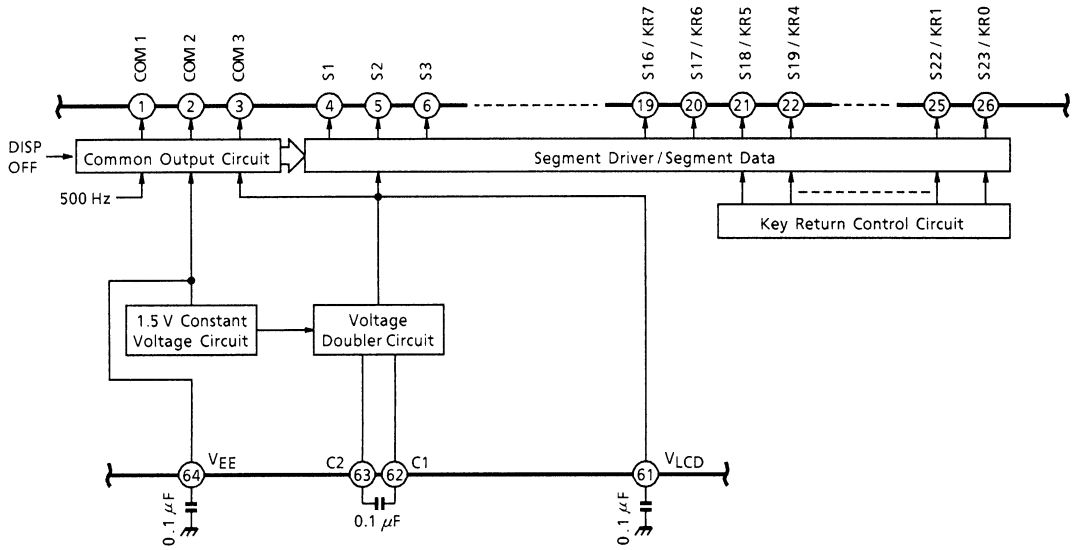
Setting this bit to "1" outputs the de-selected waveform from the common outputs and turns off the entire LCD display. The segment contents are preserved. Setting the DISP OFF bit back to "0" displays the previous LCD screen.

Segment data can be rewritten during DISP OFF. After a reset, and after CKSTP execution, the DISP OFF bit is set to "1".

The KEY RETURN SELECT bit allows an external power supply to be used. This is useful for changing the LCD drive voltage.

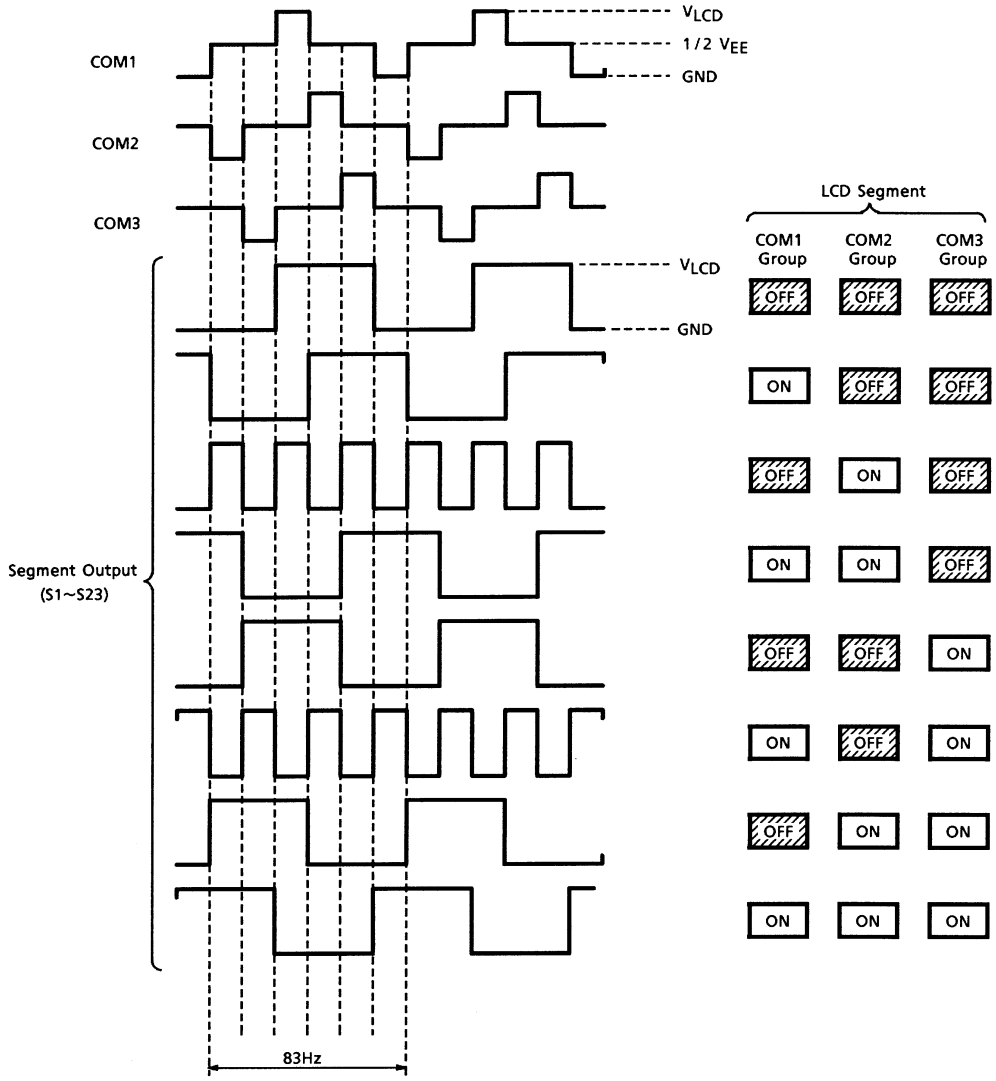
The data are set according to the segment data select port (ϕL2D). Segment output pins S16~S23 are also used for the key return timing signals for loading key matrix data. At the timing for loading the key matrix data, the segment output is set to the GND level.

## 2. LCD Driver Circuit Structure



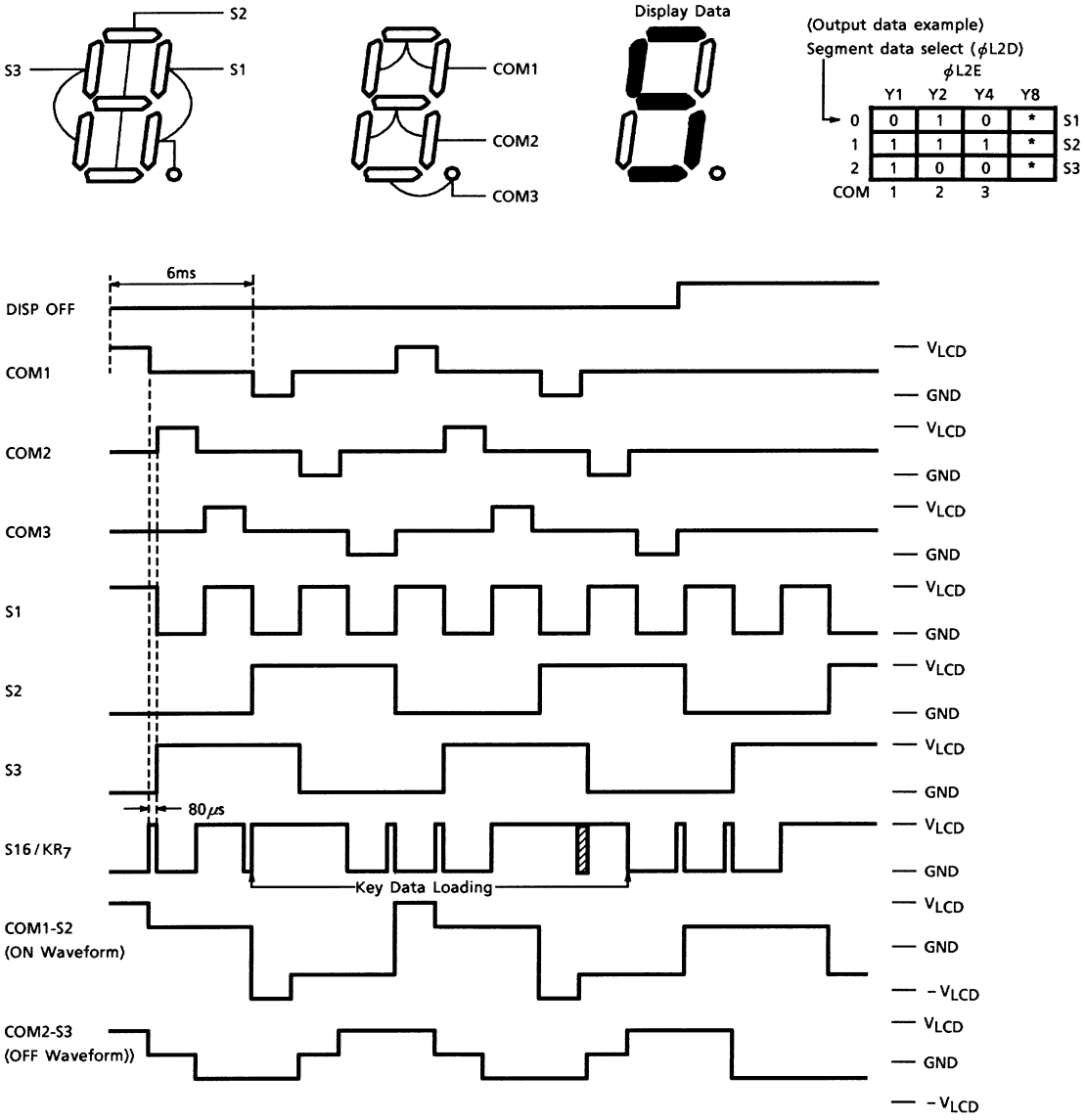
### 3. LCD Driver Timing Chart

The following chart shows the timing for the COM1~COM3 output waveforms and the eight types of segment output waveform.



## 4. Example of Timing Chart for LCD Driver Output Data and Loading Key Data

The following chart shows the output waveform timing and key return data loading timing when the common and segment outputs are allocated as shown.



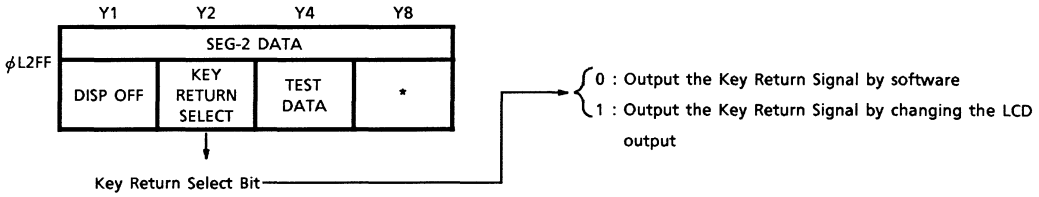

The voltages output in the LCD driver waveform are $V_{LCD}$, GND, and an intermediate voltage halfway between the two. Pins S16~S23 output the key return signals at the timing for switching between these levels. During key return data loading, the segment outputs are at the $V_{LCD}$ level for 80 μs.

Note 32: At CKSTP instruction execution or at a system reset, the common and segment pins go to the low level.

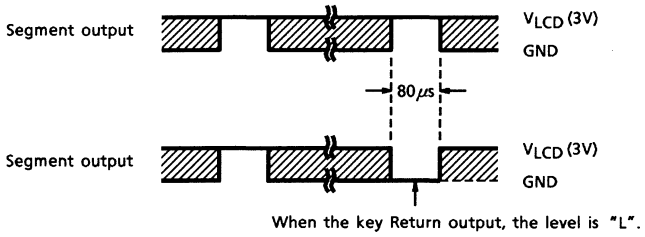
## Key Input, Key Scan Timing

The following are the two basic methods of loading key data.
Select the appropriate method for the system.

### 1. Key Control Port, Key Scan Data




In case of setting data "1" to the key Return Select bit, the segment output is the output timing as shown below.




In case of setting "0" to the bit, The key Return signal don't outputted.

Key Scan Digit Port

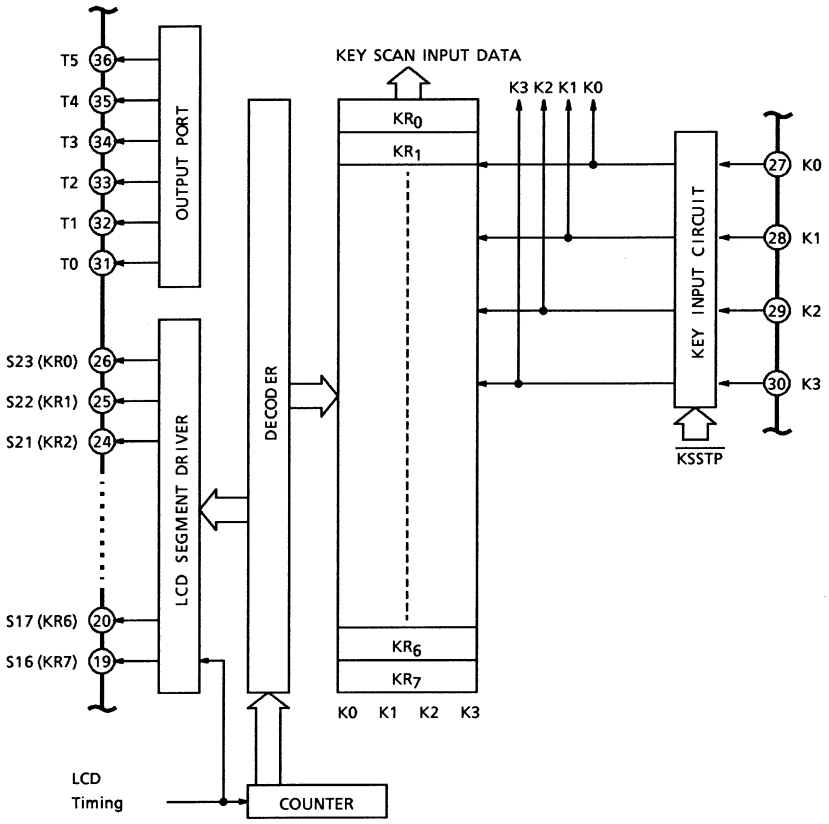
| | Y1 | Y2 | Y3 | Y4 |
|---|---|---|---|---|
| | KEY SCAN DIGIT | | | |
| ϕK27 | KS0 | KS1 | KS2 | 1 |

Key Scan Input Data Port

| | Y1 | Y2 | Y3 | Y4 |
|---|---|---|---|---|
| ϕK28 | KEY SCAN INPUT DATA-0 | | | |
| | KS00 | KS01 | KS02 | KS03 |
| ϕK29 | KEY SCAN INPUT DATA-1 | | | |
| | KS10 | KS11 | KS12 | KS13 |
| ϕK2A | KEY SCAN INPUT DATA-2 | | | |
| | KS20 | KS21 | KS22 | KS23 |
| ϕK2B | KEY SCAN INPUT DATA-3 | | | |
| | KS30 | KS31 | KS32 | KS33 |
| ϕK2C | KEY SCAN INPUT DATA-4 | | | |
| | KS40 | KS41 | KS42 | KS43 |
| ϕK2D | KEY SCAN INPUT DATA-5 | | | |
| | KS50 | KS51 | KS52 | KS53 |
| ϕK2E | KEY SCAN INPUT DATA-6 | | | |
| | KS60 | KS61 | KS62 | KS63 |
| ϕK2F | KEY SCAN INPUT DATA-07 | | | |
| | KS70 | KS71 | KS72 | KS73 |

The key Return Select bit is the bit of setting the loading key method.
The data is loading by the digit timing of the key Return Signals from the key scan digit Port.
The key data by key scan is input to the key scan input data port. By accessing this port, the key data is loading to the data memory.

## 2. Key Scan Circuit Structure

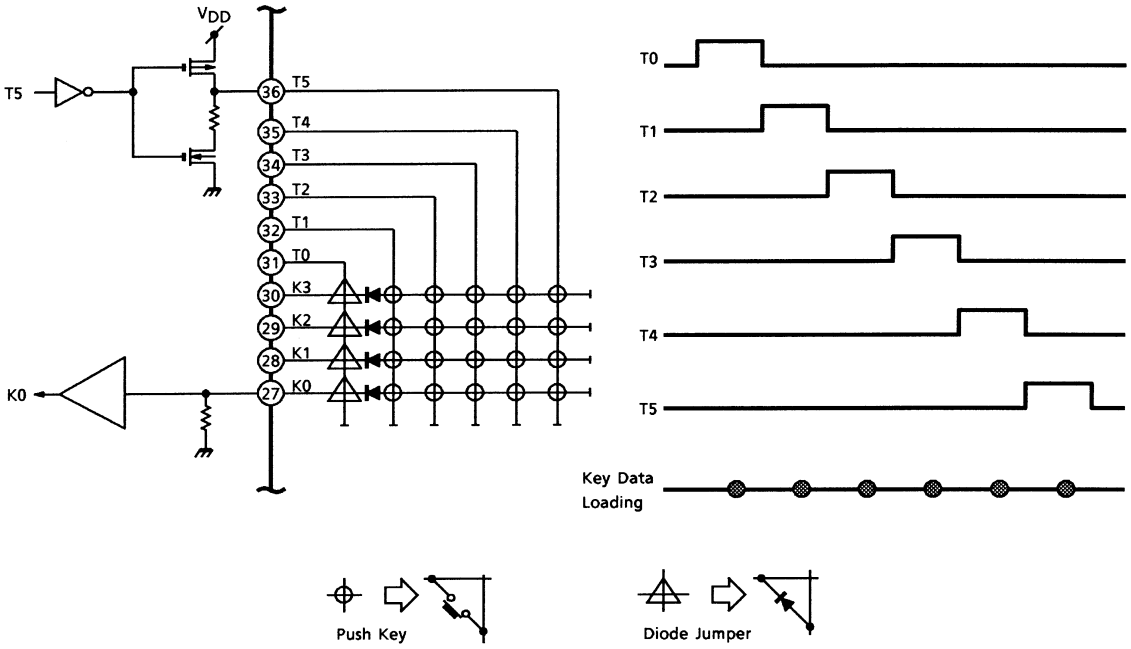



The key input block of the key scan circuit consist of key input circuit, latch circuit for loading key data. The key return timing output block consist of LCD segment driver, decoder and counter block.

### 3. Key Matrix Structure

The key matrix can have one of the following two structures.

(1) Key data loading by software




When loading key data by software, use a key matrix with the above structure. For this method, set to high the key timing output port data (ϕL28, ϕL29) for the key line to be loaded. Then to determine which keys are pressed, load the key input port (ϕK26) data to memory. At this timing, set the other key timing output ports to low. If the corresponding key is pressed, the key input port data are "1"; if not pressed, "0". This structure allows up to 24 (4 × (6)) keys to be used. The key data can be loaded at high speed. Also, as the structure has a high resistance in the N channel FETs of pins T0~T5, there is no need to use a diode to prevent reverse current flow caused by, for example, multiple keys being pressed.

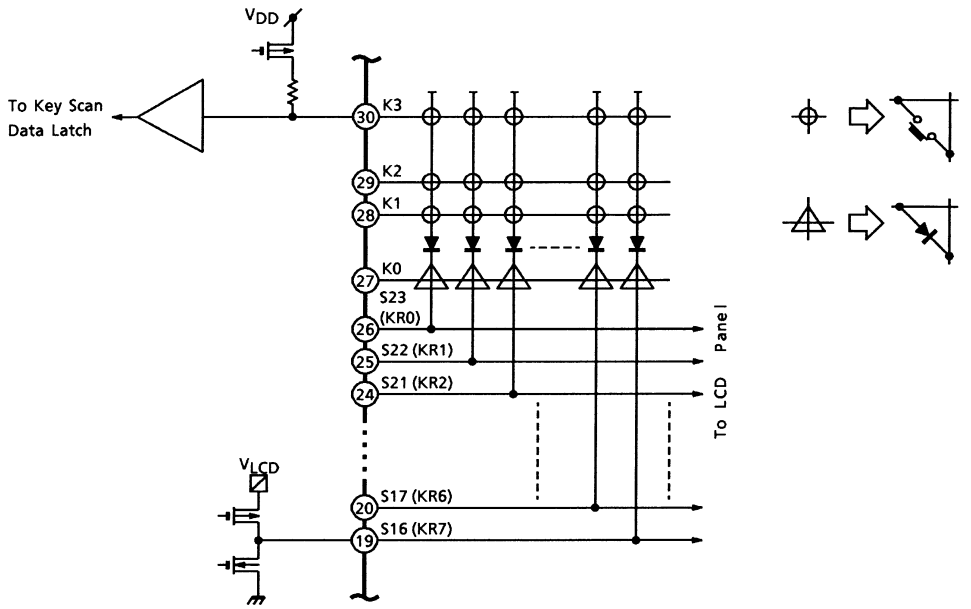
When loading key data by software, set to "0" to the key return select bit.

Note 33: In case of structuring a diode jumper, the key input voltage is input/ow voltage of VF ( ≃ 0.6 V) voltage of diode. It's necessary the diode for diode jumper malfunction prevention to structure of double push of a key.

The diode is unnecessary when there is no diode jumper necessity. Therefore, key input thre-shold level is set up low.

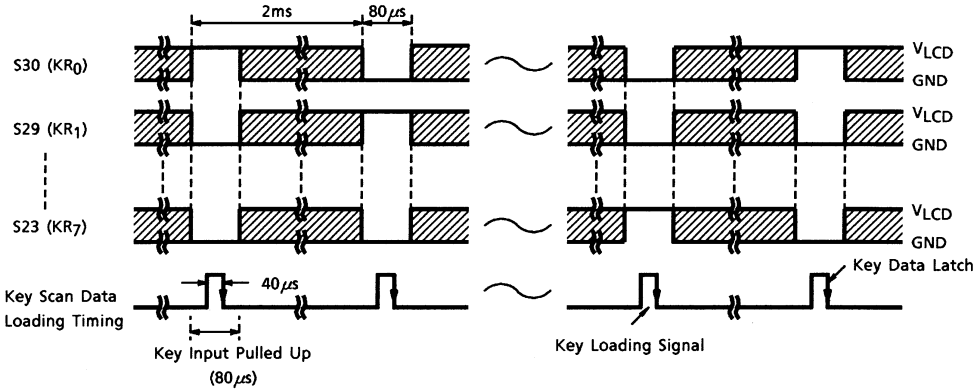
In the mode structure, when executing a wait instruction (in WAIT mode), applying a high level to a key input pin releases WAIT mode and restarts the CPU.

(2) Key data loading by LCD segment output (hardware scan)




Note 34: A key matrix to 4 × 8 = 32 can be created.

Note 35: The same key line cannot contain both push keys and diode jumpers or alternate switches. Place diode jumpers or alternate switches on the key return signal output side.




When loading key data by LCD segment output, use a key matrix with the above structure. In this structure, it's necessary for a diode to prevent reverse current flow and be careful the direction of diode and diode jumper.

The $V_{LCD}$ and GND potential are outputted from a segment pin at the timing of changing LCD output.

When loading key data, loading of segment signal becomes to the GND potential and key input pin is pulled up to the $V_{DD}$ potential at changing LCD output.

At this timing, if key is not pressed (or without diode jumper), key input pin is inputted $V_{DD}$ potential; if key is pressed (or with diode jumper), key input pin is inputted one diode potential ( ≃ 0.6 V) from GND potential.

Therefore, key input threshold level is set up high.

Inputted key data is load key scan data port corresponding to segment output line of loading the key. If a key is pressed, the key data is "1"; if not pressed, "0".

The key data loading time for each one line is 2 ms. Referring the key scan action monitor, key scan data (ϕK26) is loaded to the data memory.

### Key Return Timing Output Port (T0~T5)

T0~T5 are exclusive output port of 6 bits with N-channel load resostors. Normally, T0~T5 is used as output of key return timing Signal for Key matrix.

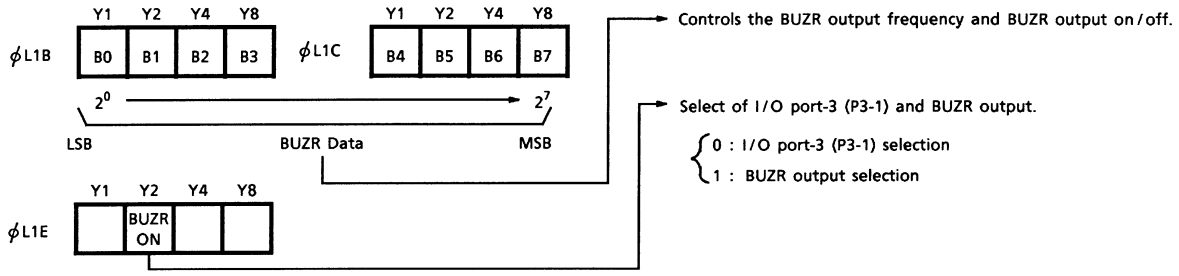
This output port is made access by OUT2 instruction designated the operand part [$C_N$ = 8 or 9] ($\phi$L28 or $\phi$L29).

Note 36: During the clock stop mode (excusing CKSTP instruction), T0~T3 and OT0, OT1 output is fixed at "L" level automatically, but the content of port is held on the previous data.


### Buzzer Output (BUZR)

The buzzer output is used for such purposes as audible alarms or to issue confirmation beeps for key-presses or tuning scan mode. The buzzer frequency can be set as desired. 50% duty waveform is output.

### 1. BUZR Data Port




The BUZR output can also be used as the P3-1 I/O port. To switch the P3-1 output to BUZR output, set "1" to BUZR ON bit.

It is necessary to set of the BUZR data before setting the BUZRON bit to "1".

Setting the data to BUZR data port ($\phi$L1C), the BUZR data is transferred to the BUZR data Latch, and then changed BUZR frequency.

The BUZR output has a frequency of 75 kHz divided by 2 × n (n = B0~B7). The B0~B7 setting range and frequency range is $2 \leqq n \leqq 255$. This can be expressed as a formula as follows.

$$\frac{75\ \text{kHz}}{2 \times 2} = 18.75\ \text{kHz} \leqq f_{BUZR} \leqq \frac{75\ \text{kHz}}{2 \times 255} = 147\ \text{Hz}$$

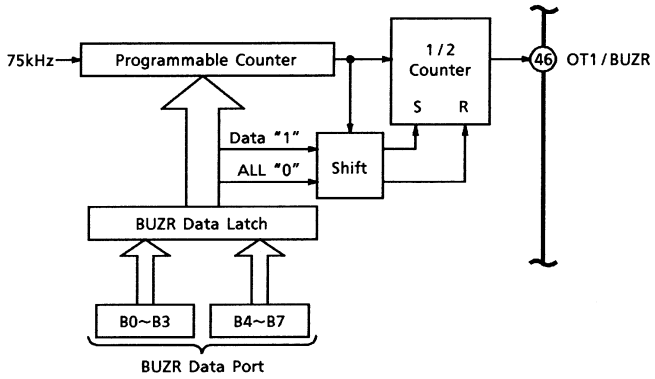
Set B0~B7 to 1 or 0 to use the pin for OT1 output. The output states are as follows.

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | OT1 Output |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Low level output |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | High level output |

To set the above data, use the OUT1 instruction with the operand [$C_N$ = BH~EH].

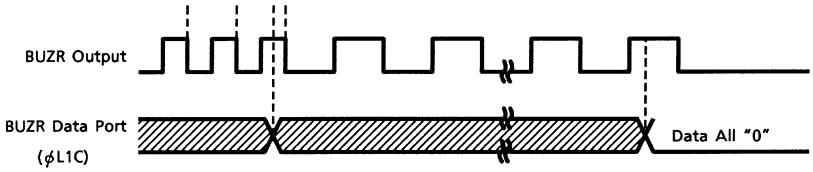
Note 37: After a system reset, the BUZR data port is reset to "0".

## 2. BUZR Circuit Structure




The buzzer circuit consists of an 8 bit programmable counter, a 1/2 counter, a buzzer latch, and a buzzer data port.

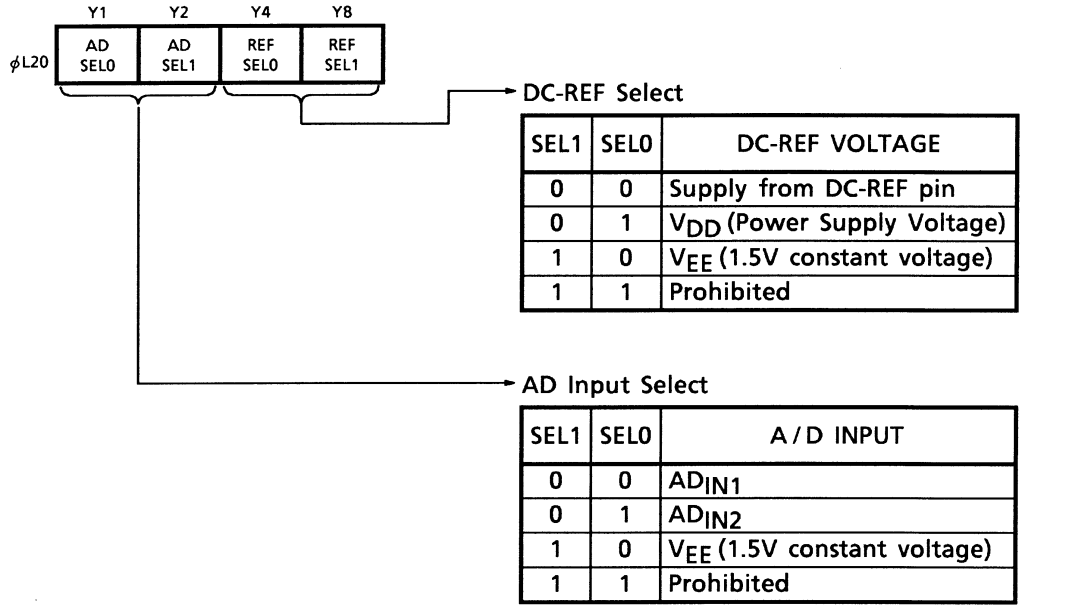
## 3. BUZR Output Timing (BUZR ON bit is "1")



## A/D Converter

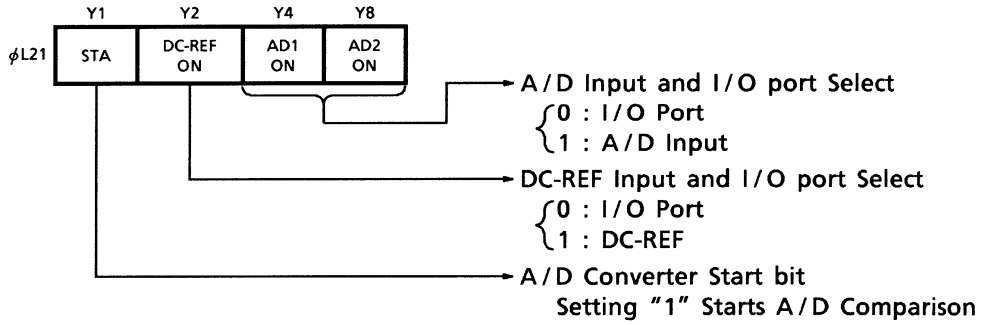
The 2 channel/6 bit resolution A/D converter is used for such purposes as measuring field intensity and battery voltage.

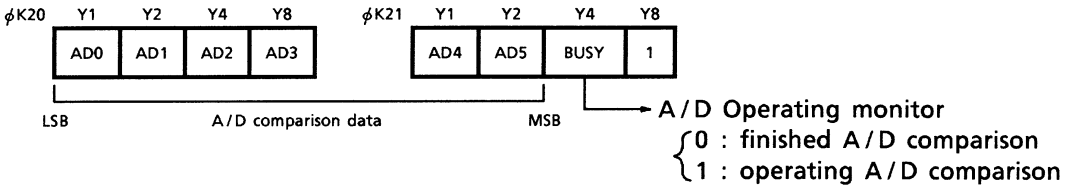
### 1. A/D Converter Control Port, Dare Port




| SEL1 | SEL0 | DC-REF VOLTAGE |
|---|---|---|
| 0 | 0 | Supply from DC-REF pin |
| 0 | 1 | $V_{DD}$ (Power Supply Voltage) |
| 1 | 0 | $V_{EE}$ (1.5V constant voltage) |
| 1 | 1 | Prohibited |

| SEL1 | SEL0 | A/D INPUT |
|---|---|---|
| 0 | 0 | $AD_{IN1}$ |
| 0 | 1 | $AD_{IN2}$ |
| 1 | 0 | $V_{EE}$ (1.5V constant voltage) |
| 1 | 1 | Prohibited |



The A/D converter is a 6 bit resolution. The reference voltage of A/D conversion can select the external voltage (DC-REF terminal), supply voltage and 1.5 V constant voltage ($V_{EE}$). The A/D conversion input is a multiplex method of 2-channel external input terminal ($AD_{IN1}$, $AD_{IN2}$ terminal) and also switchable to 1.5 V constant voltage ($V_{EE}$) as well.

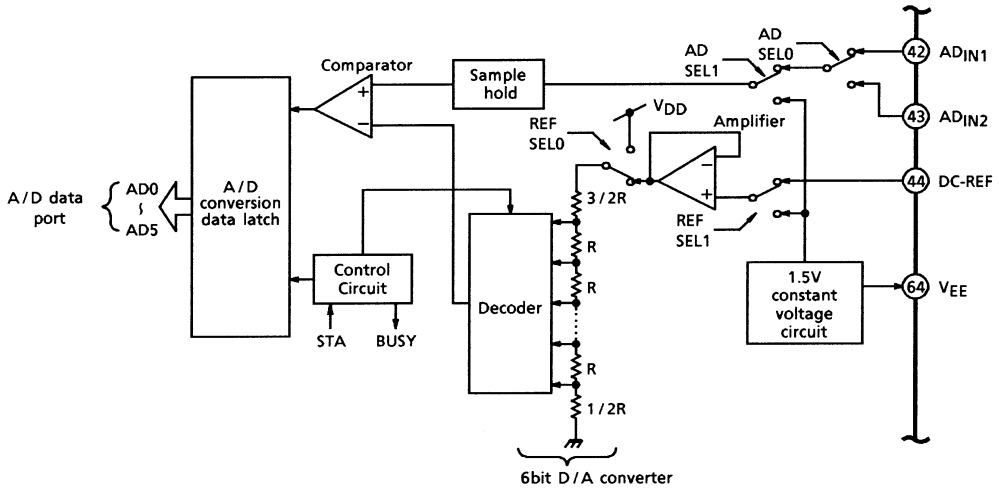
Normally field strength and volume level are measured by selecting external voltage or supply voltage as reference voltage and A/D converting the external input level.

The A/D converter can also measure battery and supply voltages. It outputs a battery singal or performes control for backup mode when battery voltage or supply voltage drop.

The A/D converter does A/D conversion whenever setting "1" to STA bit and the conversion will complete after 7 machine cycles (280 μs). Whether A/D conversion is completed can be judged by referring to BUSY bit. After A/D conversion is completed, the data will be loaded into data memory.

These controls are accessed when OUT2/IN2 instruction designated [$C_N$ = 0H, 1H] in the operand is executed.

## 2. A/D Converter Circuit Configuration




The A/D converter consists of: 6 bit D/A converter, comparator, A/D conversion latch, control circuit, A/D data port and 1.5 V constant voltage circuit (supply for LCD driver).

The A/D converter will latch the data to A/D conversion data latch sequentially by means of the 6 bit sequential comparison method.

Note 38: The DC-REF terminal is built-in an amplifier and is high impedance input.

Note 39: During A/D conversion, a proper data is not obtainable even if referring to the A/D conversion data. Therefore, make sure to confirm that the conversion has finished by referring to the A/D operation monitor.

## Input and Output Port

### 1. I/O Port P1-0~P1-3 (ϕKL22), P2-0~P2-3 (ϕKL23), P3-0~P3-1 (ϕKL24)

I/O port (P1-0~P1-3, P2-0~P2-3) are 4 bits and (P3-0~P3-1) are 2 bits CMOS type, and is capable of making input and output setting with each bit.

Input and output setting of I/O port is made by the content of I/O control internal port.

Setting to input port can be made by setting "0" to the bit of I/O control port corresponding to I/O port, while setting to output port can be made by setting "1" in the same.

In case of input port setting, the present data input I/O port is read into the data memory by the execution of IN2 instruction designated the operand part [$C_N$ = 2~4] (ϕK22, ϕK23, ϕK24).

In case of output port setting, output condition of I/O port is controlled execution of OUT2 instruction designated the operand part [$C_N$ = 2~4] (ϕL22, ϕL23, ϕL24).

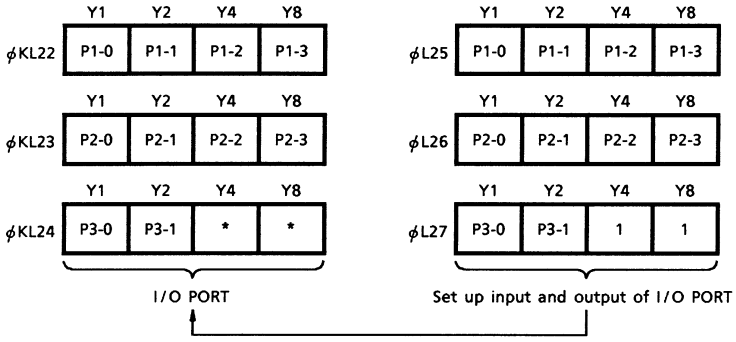
I/O port 2~3 are also used for A/D converter and BUZR output.

After system reset, these ports are set to I/O port.

Note 40: I/O control port is made access by OUT2 instruction designated the operand part [$C_N$ = 5~7].

Note 41: During the clock stop mode (executing CKSTP instruction), output condition of I/O port set at output mode is all fixed at "L" level automatically, but each output latch holds on the data just before the clock stop mode.

Note 42: At the time of changing input condition of P1-0~P1-3 port set at input mode, it cancels the execution of WAIT and CKSTP instructions and makes the operation restart. In case of setting "1" to I/O bit of MUTE control port, MUTE port is made to set to "1" compulsorily by the same condition.



## Register Port

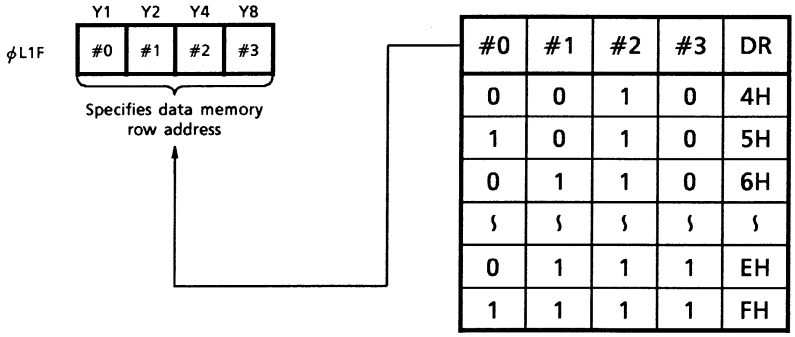
The G-register (mentioned in the CPU description) and the data register are treated as internal ports.

### 1. G-Register (ϕL1F)

This register sets the row address ($D_R$ = 4H~FH) in data memory for the MVGD and MVGS instructions. To access this register, execute the OUT1 instruction with the operand [$C_N$ = FH].

Note 43: The register value is only used when the MVGD or MVGS instructions are executed.

The register is ignored for other instructions.



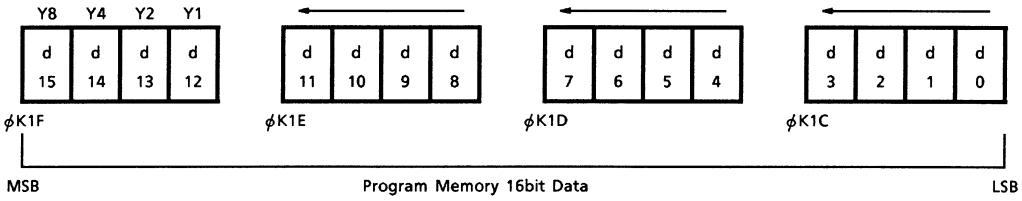

| #0 | #1 | #2 | #3 | DR |
|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 4H |
| 1 | 0 | 1 | 0 | 5H |
| 0 | 1 | 1 | 0 | 6H |
| ≀ | ≀ | ≀ | ≀ | ≀ |
| 0 | 1 | 1 | 1 | EH |
| 1 | 1 | 1 | 1 | FH |

Note 44: Setting data 0H~FH in the G register allows all the data memory row addresses to be specified indirectly. ($D_R$ = 0H~FH)

### 2. Data Register (ϕK1C~ϕK1F)

This is a 16 bit register to load the program memory data when the DAL instruction is executed. The contents of the register are read to data memory in units of 4 bits by the IN1 instruction with the operands [$C_N$ = CH~FH].

This register can be used for such purposes as LCD segment decoding, radio band edge data, or for coefficient data for binary-to-BCD conversion.

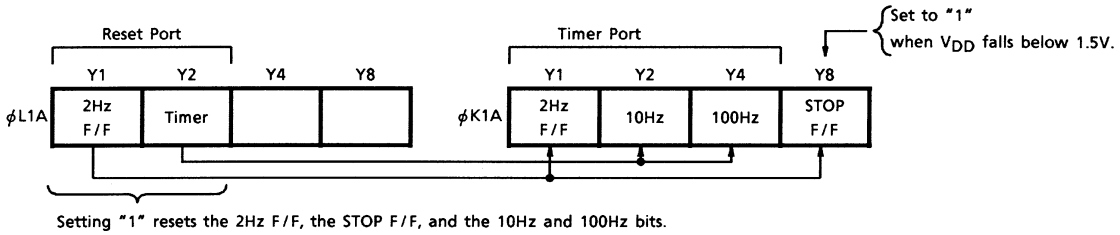


## Timer and CPU Stop Function

The timer has 100 Hz, 10 Hz, and 2 Hz flip-flop bits. These are used for counting operations, such as for a clock or tuning scan mode.

The CPU stop function uses a voltage detector circuit to shut down the CPU when the $V_{DD}$ voltage applied to the CPU falls below 1.5 V. This prevents CPU malfunction.

### 1. Timer Port, STOP Flip-Flop Bit

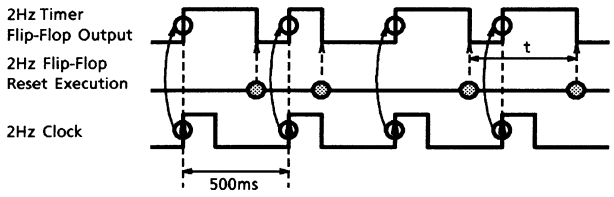



To access the timer port and the STOP flip-flop bit, execute the OUT1/IN1 instruction with the operand [$C_N$ = AH].

### 2. Timer Port Timing

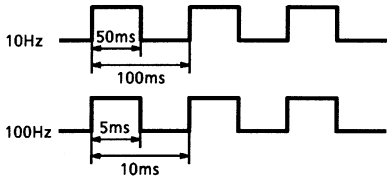
The 2 Hz timer flip-flop is set by the 2 Hz (500 ms) signal, and reset by setting the RESET port 2 Hz flip-flop to "1". This bit can normally be used for the clock count.

The 2 Hz timer flip-flop is only reset by the 2 Hz flip-flop in the RESET port. Therefore, if the flip-flop is not reset within 500 ms, the next count is missed and the correct time is not obtained.




t < 500 ms

The 10 Hz and 100 Hz timers are output to the 10 Hz and 100 Hz bits with a cycle of 100 ms and 10 ms, respectively, and a pulse duty of 50%. Whenever the RESET port timer bit is set to "1", counters below 1 kHz are reset.



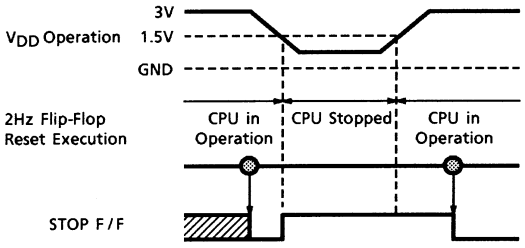
### 3. CPU Stop Function, STOP Flip-Flop Bit

The STOP flip-flop bit is set to "1" when the $V_{DD}$ voltage applied to the CPU falls below 1.5 V.

This prevents CPU malfunction by shutting down the CPU. When a voltage of 1.5 V or less is applied to the $V_{DD}$ pin, the program counter stops and instruction execution ceases in the CPU.

When a voltage higher than 1.5 V is again applied to the $V_{DD}$ pin, the CPU starts up again. As the CPU was shut down, the clock and other timings are no longer valid. Use the STOP flip-flop to test whether the CPU stop function operated. Perform initialization or clock correction if required.

The STOP flip-flop bit is reset to "0" whenever the RESET port 2 Hz flip-flop is set to "1".




Note 45: After a system reset or execution of the CKSTP instruction, the timer port and the STOP flip-flop are reset to "0".

Note 46: If the $V_{DD}$ voltage falls below 1.5 V when clock-stop mode is set, the CKSTP instruction cannot be executed. Be careful with the supply voltage timing, for example, when the radio is off.

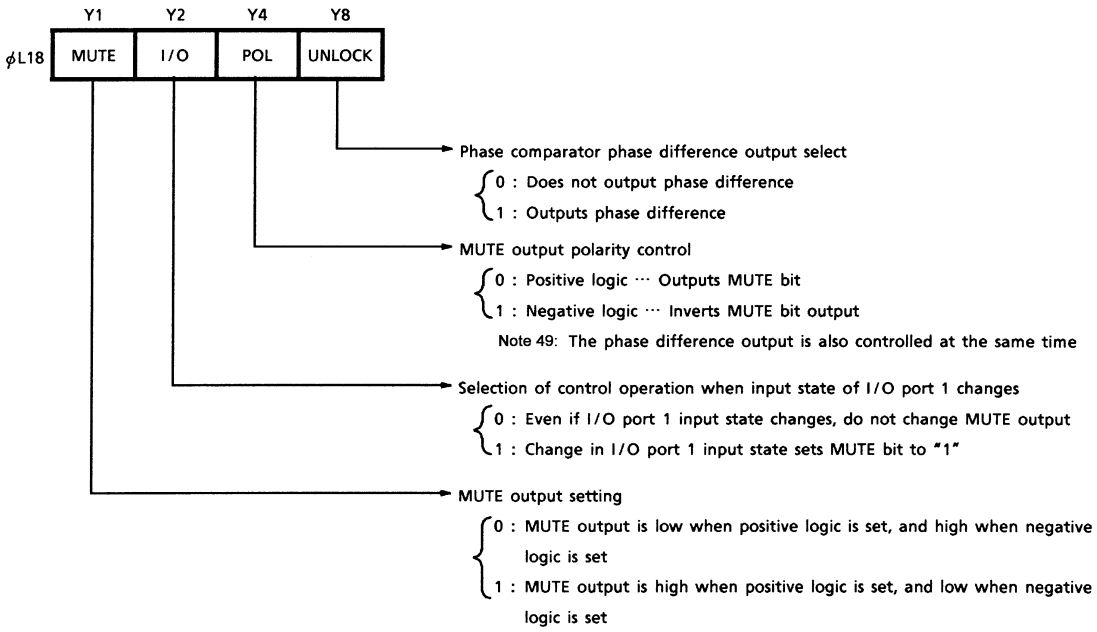
Note 47: The key scan input data immediately after restarting the CPU are undefined.

Note 48: If the interal Test port from #0 to #3 bit ($\phi$L1D) is set to "1", the CPU stop function is inhibited.

### MUTE Output

This is a 1 bit CMOS-format output-only port for muting control.

### 1. MUTE Port



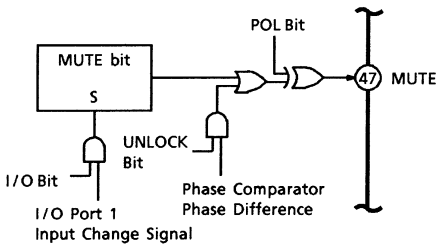

Access the MUTE port by executing the OUT1 instruction with the operand [$C_N$ = 8H]. The MUTE output is used for muting control. At such times as switching bands using the I/O port 1 input, the MUTE bit can be set to "1".

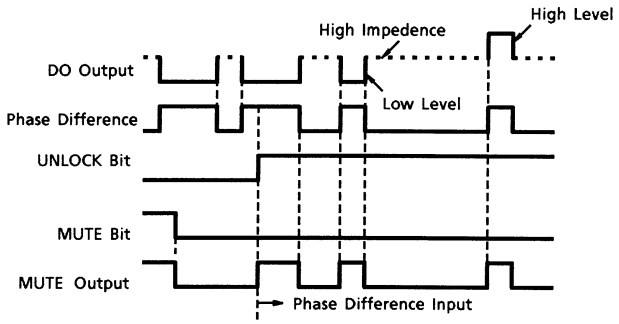
When using the I/O port 1 input to switch bands (using a slide switch, for example), this function prevents linear circuit switching noise. This control is based on I/O bit values.

The POL bit sets the MUTE output logic.

The mute output can also control muting using the phase difference output. A pulse is output to indicate when the PLL is not locked. By connecting an external low-pass filter to the MUTE output, the output can be used as a MUTE signal. Use the UNLOCK bit to perform selection.

## 2. MUTE Output Structure and Timing




Note 50: When POL bit = 0

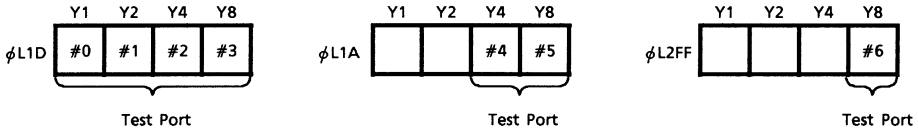
Note 51: When using the phase difference output by the phase comparator, externally connect a low-pass filter to the MUTE output.

### Test Ports

These are internal ports for testing the device's functions. Access the ports by executing the OUT1 instruction with the operand [$C_N$ = AH] or [$C_N$ = DH], or the OUT2 instruction with the operands [$C_N$ = FFH]. The ports are normally set to "0" by software.

If the data "1" is set to Test port bit from #0 to #3, the CPU stop function is inhibited and the data "0" is set, the CPU function is operating.

In case of using supply voltage detection externally, set CPU stop function as inhibition.




Note 52: The ports are reset to "0" after a system reset.

## Absolute Maximum Ratings (Ta = 25°C)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | $V_{DD}$ | −0.3~4.0 | V |
| Input voltage | $V_{IN}$ | −0.3~$V_{DD}$ + 0.3 | V |
| Power dissipation | $P_D$ | 100 | mW |
| Operating temperature | $T_{opr}$ | −10~60 | °C |
| Storage temperature | $T_{stg}$ | −55~125 | °C |

## Electrical Characteristics (unless otherwise noted, Ta = 25°C, $V_{DD}$ = 3.0 V)

| Characteristics | Symbol | Test Circuit | Test Condition | | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Range of operating supply voltage | $V_{DD}$ | — | * | | 1.8 | 3.0 | 3.6 | V |
| Range of memory retention voltage | $V_{HD}$ | — | Crystal ocillation stopped (CKSTP instruction executed) * | | 1.0 | ~ | 3.6 | V |
| Operating current | $I_{DD1}$ | — | Under ordinary operation and PLL on operation, no output load $FM_{IN}$ = 230 MHz input | $V_{DD}$ = 3.0 V | — | 7.0 | 12 | mA |
| | | | Under ordinary operation and PLL on operation, no output load $FM_{IN}$ = 130 MHz input | $V_{DD}$ = 3.0 V | — | 6.0 | 10 | |
| | $I_{DD2}$ | — | Under CPU operation only (PLL off, display turned on) | $V_{DD}$ = 3.0 V | — | 40 | 80 | μA |
| | $I_{DD3}$ | — | Soft Wait mode (crystal oscllator, display circuit operating, CPU stopped, PLL off) | | — | 25 | 50 | |
| | $I_{DD4}$ | — | Hard Wait mode (crystal oscillator operating only) | | — | 15 | 30 | |
| Memory retention current | $I_{HD}$ | — | Crystal oscillation stopped (CKSTP instruction executed) | | — | 0.1 | 10 | μA |
| Crystal oscillation frequency | $f_{XT}$ | — | * | | — | 75 | — | kHz |
| Crystal oscillation startup time | $t_{ST}$ | — | Crystal oscillation $f_{XT}$ = 75 kHz | | — | — | 1.0 | s |

Note 53: For conditions marked by an asterisk (*), guaranteed when $V_{DD}$ = 1.8~3.6 V, Ta = −10~60°C.

### Voltage Doubler Circuit

| Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Voltage doubler reference voltage | $V_{EE}$ | — | GND reference ($V_{EE}$) | 1.3 | 1.5 | 1.7 | V |
| Constant voltage temperature characteristics | $D_V$ | — | GND reference ($V_{EE}$) | — | −5 | — | mV/°C |
| Voltage doubler boosting voltage | $V_{LCD}$ | — | GND reference ($V_{LCD}$) | 2.6 | 3.0 | 3.4 | V |

### Operating Frequency Ranges for Programmable Counter and IF Counter

| Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| $FM_{IN}$ (VHF mode) | $f_{VHF}$ | — | Sine wave input when $V_{IN}$ = 0.2 $V_{p-p}$ * | 50 | ~ | 230 | MHz |
| $FM_{IN}$ (FM mode) | $f_{FM}$ | — | Sine wave input when $V_{IN}$ = 0.2 $V_{p-p}$ * | 40 | ~ | 130 | MHz |
| $AM_{IN}$ (HF mode) | $f_{HL}$ | — | Sine wave input when $V_{IN}$ = 0.2 $V_{p-p}$ * | 1 | ~ | 45 | MHz |
| $AM_{IN}$ (LF mode) | $f_{LF}$ | — | Sine wave input when $V_{IN}$ = 0.2 $V_{p-p}$ * | 0.5 | ~ | 12 | MHz |
| $IF_{IN}$ | $f_{IF}$ | — | Sine wave input when $V_{IN}$ = 0.2 $V_{p-p}$ * | 0.35 | ~ | 12 | MHz |
| Input amplitude | $V_{IN}$ | — | $FM_{IN}$, $AM_{IN}$, $IF_{IN}$ input * | 0.2 | ~ | $V_{DD}$ − 0.8 | $V_{p-p}$ |

Note 53: For conditions marked by an asterisk (*), guaranteed when $V_{DD}$ = 1.8~3.6 V, Ta = −10~60°C.

### LCD Common Output/Segment Output (COM1~COM3, $S_1$~$S_{23}$)

| Characteristics | | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Output current | "H" level | $I_{OH1}$ | — | $V_{LCD}$ = 3 V, $V_{OH}$ = 2.7 V | −0.5 | −1.0 | — | mA |
| | "L" level | $I_{OL1}$ | — | $V_{LCD}$ = 3 V, $V_{OL}$ = 0.3 V | 0.5 | 1.0 | — | |
| Output voltage 1/2 level | | $V_{BS}$ | — | No load | 1.3 | 1.5 | 1.7 | V |

### $\overline{HOLD}$ Input Port

| Characteristics | | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input leak current | | $I_{LI}$ | — | $V_{IH}$ = 3.0 V, $V_{IL}$ = 0 V | — | — | ±1.0 | μA |
| Input voltage | "H" level | $V_{IH1}$ | — | — | 2.4 | ~ | 3.0 | V |
| | "L" level | $V_{IL1}$ | — | — | 0 | ~ | 1.2 | |

### A/D Converter ($A/D_{IN1}$, $A/D_{IN2}$, DC-REF)

| Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Analog input voltage range | $V_{AD}$ | — | $AD_{IN1}$, $AD_{IN2}$ | 0 | ~ | $V_{DD}$ | V |
| Analog reference voltage range | $V_{REF}$ | — | DC-REF, $V_{DD}$ = 2.0~3.6 V | 1.0 | ~ | $V_{DD}$ × 0.9 | V |
| Resolution | $V_{RES}$ | — | — | — | 6.0 | — | bit |
| Conversion total error | — | — | $V_{DD}$ = 2.0~3.6 V | — | ±1.0 | ±4.0 | LSB |
| Analog input leak | $I_{LI}$ | — | $V_{IH}$ = 3.0 V, $V_{IL}$ = 0 V ($AD_{IN1}$, $AD_{IN2}$, DC-REF) | — | — | ±1.0 | μA |

### Key Input Port ($K_0$~$K_3$)

| Characteristics | | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| N-ch/P-ch input resistance | | $R_{IN1}$ | — | — | 75 | 150 | 300 | kΩ |
| Input voltage | "H" level | $V_{IH2}$ | — | When input with pull-down resistance | 1.8 | ~ | 3.0 | V |
| | "L" level | $V_{IL2}$ | — | When input with pull-down resistance | 0 | ~ | 0.3 | |
| Input voltage | "H" level | $V_{IH3}$ | — | When input with pull-up resistance | 2.7 | ~ | 3.0 | V |
| | "L" level | $V_{IL3}$ | — | When input with pull-up resistance | 0 | ~ | 1.2 | |
| Input leak current | | $I_{LI}$ | — | When input resistance off, $V_{IH}$ = 3.0 V, $V_{IL}$ = 0 V | — | — | ±1.0 | μA |

### Timing Output Port (T0~T5)

| Characteristics | | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Output current | "H" level | $I_{OH1}$ | — | $V_{OH}$ = 2.7 V | −0.5 | −1.0 | — | mA |
| | "L" level | $I_{OL1}$ | — | $V_{OL}$ = 0.3 V, Use LCD key-return mode | 0.5 | 1.0 | — | |
| N-ch load resistance | | $R_{ON}$ | — | No used LCD key-return mode | 75 | 150 | 300 | kΩ |

### DO1/OT, DO2 Output; MUTE Output

| Characteristics | | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Output current | "H" level | $I_{OH1}$ | — | $V_{OH}$ = 2.7 V | −0.5 | −1.0 | — | mA |
| | "L" level | $I_{OL1}$ | — | $V_{OL}$ = 0.3 V | 0.5 | 1.0 | — | |
| Output off leak current | | $I_{TL}$ | — | $V_{TLH}$ = 3.0 V, $V_{TLL}$ = 0 V (DO1, DO2) | — | — | ±100 | nA |

### General-Purpose I/O Ports (P1-0~P3-1)

| Characteristics | | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Output current | "H" level | $I_{OH1}$ | — | $V_{OH}$ = 2.7 V | −0.5 | −1.0 | — | mA |
| | "L" level | $I_{OL1}$ | — | $V_{OL}$ = 0.3 V | 0.5 | 1.0 | — | |
| Input leak current | | $I_{LI}$ | — | $V_{IH}$ = 3.0 V, $V_{IL}$ = 0 V | — | — | ±1.0 | μA |
| Input voltage | "H" level | $V_{IH4}$ | — | — | 2.4 | ~ | 3.0 | V |
| | "L" level | $V_{IL4}$ | — | — | 0 | ~ | 0.6 | |

### IN, $\overline{\text{RESET}}$ Input Port

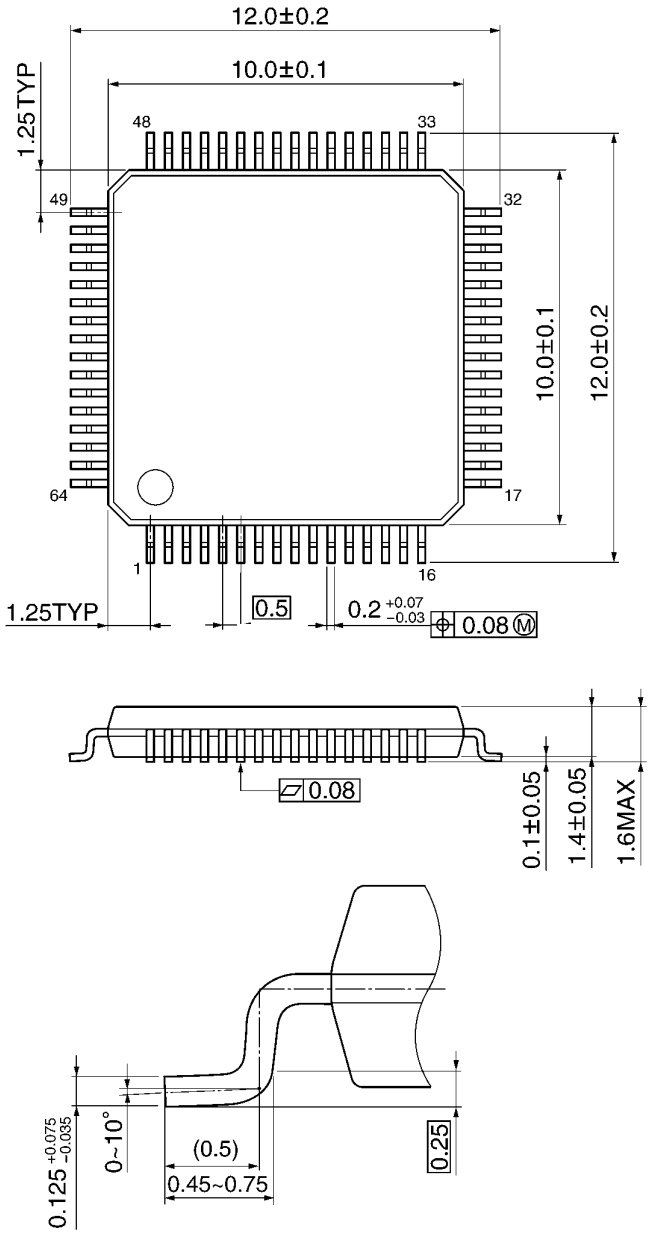
| Characteristics | | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input leak current | | $I_{LI}$ | — | $V_{IH}$ = 3.0 V, $V_{IL}$ = 0 V | — | — | ±1.0 | μA |
| Input voltage | "H" level | $V_{IH4}$ | — | — | 2.4 | ~ | 3.0 | V |
| | "L" level | $V_{IL4}$ | — | — | 0 | ~ | 0.6 | |

**Others**

| Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Input pull-down resistance | $R_{IN2}$ | — | (TEST) | 25 | 50 | 100 | kΩ |
| $X_{IN}$ amp feedback resistance | $R_{fXT}$ | — | ($X_{IN}$-$X_{OUT}$) | — | 20 | — | MΩ |
| $X_{OUT}$ output resistance | $R_{OUT}$ | — | ($X_{OUT}$) | — | 3 | — | kΩ |
| Input amp feedback resistance | $R_{fIN1}$ | — | ($FM_{IN}$, $AM_{IN}$) | 150 | 300 | 600 | kΩ |
| | $R_{fIN2}$ | — | ($IF_{IN}$) | 500 | 1000 | 2000 | |
| Voltage used to detect supply voltage drop | $V_{STP}$ | — | ($V_{DD}$) | 1.35 | 1.55 | 1.75 | V |
| Supply voltage drop detection temperature characteristics | $D_S$ | — | ($V_{DD}$) | — | −2 | — | mV/°C |

## Package Dimensions

P-LQFP64-1010-0.50E Unit: mm

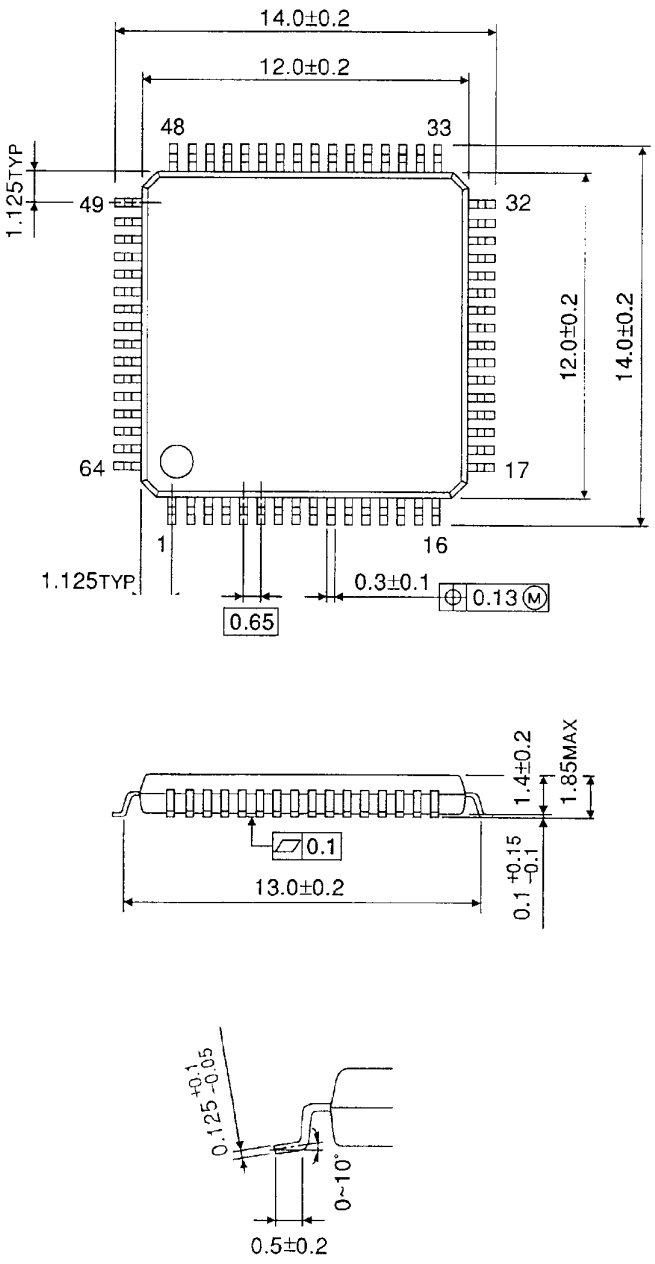



Note: Pd-plated leads.

Weight: 0.32 g (typ.)

## Package Dimensions

P-LQFP64-1212-0.65A Unit : mm




Note: Pd-plated leads.

Weight: 0.45 g (typ.)

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060116EBA

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About solderability, following conditions were confirmed

- Solderability

  (1) Use of Sn-37Pb solder Bath
  - solder bath temperature = 230°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

  (2) Use of Sn-3.0Ag-0.5Cu solder Bath
  - solder bath temperature = 245°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux