Features

- Incorporates the ARM926EJ-S™ ARM® Thumb® Processor
  - DSP instruction Extensions, ARM Jazelle® Technology for Java® Acceleration
  - 8 Kbyte Data Cache, 16 Kbyte Instruction Cache, Write Buffer
  - 200 MIPS at 180 MHz
  - Memory Management Unit
  - EmbeddedICE™, Debug Communication Channel Support
- Additional Embedded Memories
  - One 32 Kbyte Internal ROM, Single-cycle Access at Maximum Matrix Speed
  - One 32 Kbyte (for AT91SAM9XE256 and AT91SAM9XE512) or 16 Kbyte (for AT91SAM9XE128) Internal SRAM, Single-cycle Access at Maximum Matrix Speed
  - 128, 256 or 512 Kbytes of Internal High-speed Flash for AT91SAM9XE128, AT91SAM9XE256 or AT91SAM9XE512 Respectively. Organized in 256, 512 or 1024 Pages of 512 Bytes Respectively.
    - 128-bit Wide Access
    - Fast Read Time: 45 ns
    - Page Programming Time: 4 ms, Including Page Auto-erase, Full Erase Time: 10 ms
    - 10,000 Write Cycles, 10 Years Data Retention, Page Lock Capabilities, Flash Security Bit
- Enhanced Embedded Flash Controller (EEFC)
  - Interface of the Flash Block with the 32-bit Internal Bus
  - Increases Performance in ARM and Thumb Mode with 128-bit Wide Memory Interface
- External Bus Interface (EBI)
  - Supports SDRAM, Static Memory, ECC-enabled NAND Flash and CompactFlash™
- USB 2.0 Full Speed (12 Mbits per second) Device Port
  - On-chip Transceiver, 2,688-byte Configurable Integrated DPRAM
- USB 2.0 Full Speed (12 Mbits per second) Host Single Port in the 208-pin PQFP Device and Double Port in 217-ball LFBGA Device
  - Single or Dual On-chip Transceivers
  - Integrated FIFOs and Dedicated DMA Channels
- Ethernet MAC 10/100 Base-T
  - Media Independent Interface or Reduced Media Independent Interface
  - 128-byte FIFOs and Dedicated DMA Channels for Receive and Transmit
- Image Sensor Interface
  - ITU-R BT. 601/656 External Interface, Programmable Frame Capture Rate
  - 12-bit Data Interface for Support of High Sensibility Sensors
  - SAV and EAV Synchronization, Preview Path with Scaler, YCbCr Format
- Bus Matrix
  - Six 32-bit-layer Matrix
  - Remap Command
- Fully-featured System Controller, including
  - Reset Controller, Shutdown Controller
  - Four 32-bit Battery Backup Registers for a Total of 16 Bytes
  - Clock Generator and Power Management Controller
  - Advanced Interrupt Controller and Debug Unit
  - Periodic Interval Timer, Watchdog Timer and Real-time Timer

AT91 ARM Thumb Microcontrollers

AT91SAM9XE128
AT91SAM9XE256
AT91SAM9XE512
Preliminary

Summary

NOTE: This is a summary document. The complete document is available on the Atmel website at www.atmel.com.

6254BS–ATARM–29-Apr-09

- Reset Controller (RSTC)
  - Based on a Power-on Reset Cell, Reset Source Identification and Reset Output Control
- Clock Generator (CKGR)
  - Selectable 32,768 Hz Low-power Oscillator or Internal Low Power RC Oscillator on Battery Backup Power Supply, Providing a Permanent Slow Clock
  - 3 to 20 MHz On-chip Oscillator, One Up to 240 MHz PLL and One Up to 100 MHz PLL
- Power Management Controller (PMC)
  - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
  - Two Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Three External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - 2-wire UART and support for Debug Communication Channel, Programmable ICE Access Prevention
  - Mode for General Purpose Two-wire UART Serial Communication
- Periodic Interval Timer (PIT)
  - 20-bit Interval Timer Plus 12-bit Interval Counter
- Watchdog Timer (WDT)
  - Key-protected, Programmable Only Once, Windowed 16-bit Counter Running at Slow Clock
- Real-Time Timer (RTT)
  - 32-bit Free-running Backup Counter Running at Slow Clock with 16-bit Prescaler
- One 4-channel 10-bit Analog to Digital Converter
- Three 32-bit Parallel Input/Output Controllers (PIOA, PIOB, PIOC,)
  - 96 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
- Peripheral DMA Controller Channels (PDC)
- Two-slot Multimedia Card Interface (MCI)
  - SDCard/SDIO and MultiMediaCard™ Compliant
  - Automatic Protocol Control and Fast Automatic Data Transfers with PDC
- One Synchronous Serial Controllers (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I²S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Four Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation, Manchester Encoding/Decoding
  - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
  - Full Modem Signal Control on USART0
- One 2-wire UART
- Two Master/Slave Serial Peripheral Interface (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
  - Synchronous Communications
- Two Three-channel 16-bit Timer/Counters (TC)
  - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
  - High-Drive Capability on Outputs TIOA0, TIOA1, TIOA2
- Two Two-wire Interfaces (TWI)
  - Master, Multi-master and Slave Mode Operation
  - General Call Supported in Slave Mode
  - Connection to PDC Channel to Optimize Data Transfers in Master Mode Only

- **IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins**
- **Required Power Supplies:**
  - **1.65V to 1.95V for VDDBU, VDDCORE and VDDPLL**
  - **1.65V to 3.6V for VDDIOP1 (Peripheral I/Os)**
  - **3.0V to 3.6V for VDDIOP0 and VDDANA (Analog-to-digital Converter)**
  - **Programmable 1.65V to 1.95V or 3.0V to 3.6V for VDDIOM (Memory I/Os)**
- **Available in a 208-pin PQFP Green and a 217-ball LFBGA Green Package**

1. AT91SAM9XE128/256/512 Description

The AT91SAM9XE128/256/512 is based on the integration of an ARM926EJ-S processor with fast ROM and RAM, 128, 256 or 512 Kbytes of Flash and a wide range of peripherals.

The embedded Flash memory can be programmed in-system via the JTAG-ICE interface or via a parallel interface on a production programmer prior to mounting. Built-in lock bits a security bit and MMU protect the firmware from accidental overwrite and preserve its confidentiality.

The AT91SAM9XE128/256/512 embeds an Ethernet MAC, one USB Device Port, and a USB Host Controller. It also integrates several standard peripherals, like six UARTs, SPI, TWI, Timer Counters, Synchronous Serial Controller, ADC and a MultiMedia/SD Card Interface.

The AT91SAM9XE128/256/512 system controller includes a reset controller capable of managing the power-on sequence of the microcontroller and the complete system. Correct device operation can be monitored by a built-in brownout detector and a watchdog running off an integrated RC oscillator.

The AT91SAM9XE128/256/512 is architectured on a 6-layer matrix, allowing a maximum internal bandwidth of six 32-bit buses. It also features an External Bus Interface capable of interfacing with a wide range of memory devices.

The pinout and ball-out are fully compatible with the AT91SAM9260 with the exception that the pin BMS is replaced by the pin ERASE.

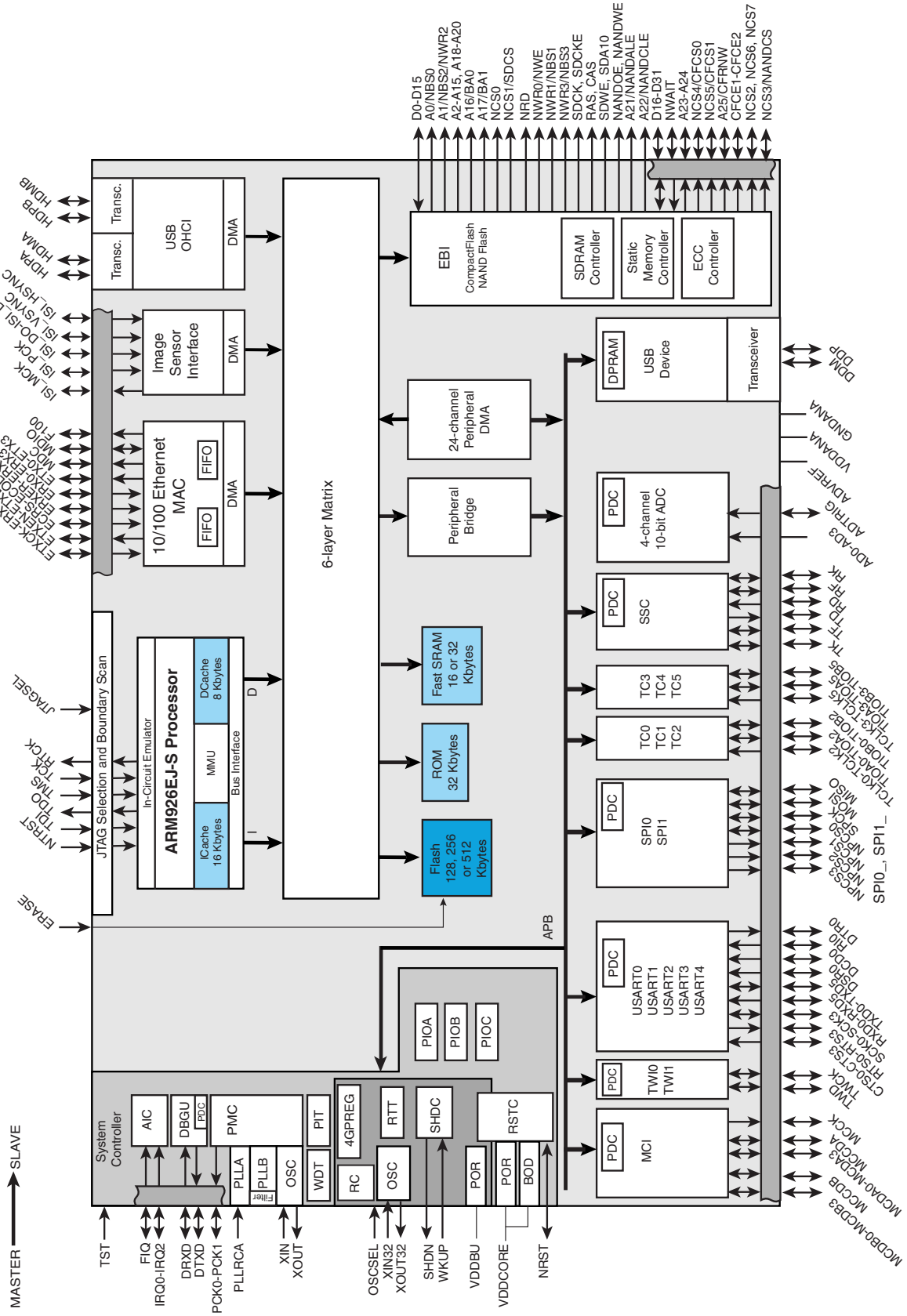
2. AT91SAM9XE128/256/512 Block Diagram

The block diagram shows all the features for the 217-LFBGA package. Some functions are not accessible in the 208-PQFP package and the unavailable pins are highlighted in “Multiplexing on PIO Controller A” on page 37, “Multiplexing on PIO Controller B” on page 38, “Multiplexing on PIO Controller C” on page 39. The USB Host Port B is also not available. Table 2-1 on page 4 defines all the multiplexed and not multiplexed pins not available in the 208-PQFP package.

Table 2-1. Unavailable Signals in 208-pin PQFP Device

PIO	Peripheral A	Peripheral B
-	HDPB	-
-	HDMB	-
PA30	SCK2	RXD4
PA31	SCK0	TXD4
PB12	TWD1	ISI_D10
PB13	TWCK1	ISI_D11
PC2	AD2	PCK1
PC3	AD3	SPI1_NPCS3
PC12	IRQ0	NCS7

Figure 2-1. AT91SAM9XE128/256/512 Block Diagram



3. Signal Description

Table 3-1 gives details on the signal name classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
Power Supplies					
VDDIOM	EBI I/O Lines Power Supply	Power			1.65V to 1.95V or 3.0V to 3.6V
VDDIOP0	Peripherals I/O Lines Power Supply	Power			3.0V to 3.6V
VDDIOP1	Peripherals I/O Lines Power Supply	Power			1.65V to 3.6V
VDDBU	Backup I/O Lines Power Supply	Power			1.65V to 1.95V
VDDANA	Analog Power Supply	Power			3.0V to 3.6V
VDDPLL	PLL Power Supply	Power			1.65V to 1.95V
VDDCORE	Core Chip and Embedded Memories Power Supply	Power			1.65V to 1.95V
GND	Ground	Ground			
GNDPLL	PLL Ground	Ground			
GNDANA	Analog Ground	Ground			
GNDBU	Backup Ground	Ground			
Clocks, Oscillators and PLLs					
XIN	Main Oscillator Input	Input			
XOUT	Main Oscillator Output	Output			
XIN32	Slow Clock Oscillator Input	Input			
XOUT32	Slow Clock Oscillator Output	Output			
OSCSEL	Slow Clock Oscillator Selection	Input		VDDBU	Accepts between 0V and VDDBU.
PLLRCA	PLL A Filter	Input			
PCK0 - PCK1	Programmable Clock Output	Output		VDDIOP0	
Shutdown, Wakeup Logic					
SHDN	Shutdown Control	Output	Low	VDDBU	Driven at 0V only.
WKUP	Wake-Up Input	Input		VDDBU	Accepts between 0V and VDDBU.
ICE and JTAG					
NTRST	Test Reset Signal	Input	Low	VDDIOP0	Pull-Up resistor (100 kΩ)
TCK	Test Clock	Input		VDDIOP0	No pull-up resistor, Schmitt trigger
TDI	Test Data In	Input		VDDIOP0	No pull-up resistor, Schmitt trigger
TDO	Test Data Out	Output		VDDIOP0	
TMS	Test Mode Select	Input		VDDIOP0	No pull-up resistor, Schmitt trigger
JTAGSEL	JTAG Selection	Input		VDDBU	Pull-down resistor (15 kΩ).

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
RTCK	Return Test Clock	Output		VDDIOP0	
Flash Memory					
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	VDDIOP0	Pull-down resistor (15 kΩ)
Reset/Test					
NRST	Microcontroller Reset	I/O	Low	VDDIOP0	Open-drain output, Pull-Up resistor (100 kΩ). Inserted in the Boundary Scan.
TST	Test Mode Select	Input		VDDBU	Pull-down resistor (15 kΩ)
Debug Unit - DBGU					
DRXD	Debug Receive Data	Input		VDDIOP0	
DTXD	Debug Transmit Data	Output		VDDIOP0	
Advanced Interrupt Controller - AIC					
IRQ0 - IRQ2	External Interrupt Inputs	Input		VDDIOP0	
FIQ	Fast Interrupt Input	Input		VDDIOP0	
PIO Controller - PIOA - PIOB - PIOC					
PA0 - PA31	Parallel IO Controller A	I/O		VDDIOP0	Pulled-up input at reset (100kΩ)[1]
PB0 - PB30	Parallel IO Controller B	I/O		VDDIOP0	Pulled-up input at reset (100kΩ)[1]
PC0 - PC31	Parallel IO Controller C	I/O		VDDIOP0	Pulled-up input at reset (100kΩ)[1]
External Bus Interface - EBI					
D0 - D31	Data Bus	I/O		VDDIOM	Pulled-up input at reset
A0 - A25	Address Bus	Output		VDDIOM	0 at reset
NWAIT	External Wait Signal	Input	Low	VDDIOM	
Static Memory Controller - SMC					
NCS0 - NCS7	Chip Select Lines	Output	Low	VDDIOM	
NWR0 - NWR3	Write Signal	Output	Low	VDDIOM	
NRD	Read Signal	Output	Low	VDDIOM	
NWE	Write Enable	Output	Low	VDDIOM	
NBS0 - NBS3	Byte Mask Signal	Output	Low	VDDIOM	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
CompactFlash Support					
CFCE1 - CFCE2	CompactFlash Chip Enable	Output	Low	VDDIOM	
CFOE	CompactFlash Output Enable	Output	Low	VDDIOM	
CFWE	CompactFlash Write Enable	Output	Low	VDDIOM	
CFIOR	CompactFlash IO Read	Output	Low	VDDIOM	
CFIOW	CompactFlash IO Write	Output	Low	VDDIOM	
CFRNW	CompactFlash Read Not Write	Output		VDDIOM	
CFCS0 - CFCS1	CompactFlash Chip Select Lines	Output	Low	VDDIOM	
NAND Flash Support					
NANDCS	NAND Flash Chip Select	Output	Low	VDDIOM	
NANDOE	NAND Flash Output Enable	Output	Low	VDDIOM	
NANDWE	NAND Flash Write Enable	Output	Low	VDDIOM	
SDRAM Controller					
SDCK	SDRAM Clock	Output		VDDIOM	
SDCKE	SDRAM Clock Enable	Output	High	VDDIOM	
SDCS	SDRAM Controller Chip Select	Output	Low	VDDIOM	
BA0 - BA1	Bank Select	Output		VDDIOM	
SDWE	SDRAM Write Enable	Output	Low	VDDIOM	
RAS - CAS	Row and Column Signal	Output	Low	VDDIOM	
SDA10	SDRAM Address 10 Line	Output		VDDIOM	
Multimedia Card Interface MCI					
MCCK	Multimedia Card Clock	Output		VDDIOP0	
MCCDA	Multimedia Card Slot A Command	I/O		VDDIOP0	
MCDA0 - MCDA3	Multimedia Card Slot A Data	I/O		VDDIOP0	
MCCDB	Multimedia Card Slot B Command	I/O		VDDIOP0	
MCDB0 - MCDB3	Multimedia Card Slot B Data	I/O		VDDIOP0	
Universal Synchronous Asynchronous Receiver Transmitter USARTx					
SCKx	USARTx Serial Clock	I/O		VDDIOP0	
TXDx	USARTx Transmit Data	I/O		VDDIOP0	
RXDx	USARTx Receive Data	Input		VDDIOP0	
RTSx	USARTx Request To Send	Output		VDDIOP0	
CTSx	USARTx Clear To Send	Input		VDDIOP0	
DTR0	USART0 Data Terminal Ready	Output		VDDIOP0	
DSR0	USART0 Data Set Ready	Input		VDDIOP0	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
DCD0	USART0 Data Carrier Detect	Input		VDDIOP0	
RI0	USART0 Ring Indicator	Input		VDDIOP0	
Synchronous Serial Controller - SSC					
TD	SSC Transmit Data	Output		VDDIOP0	
RD	SSC Receive Data	Input		VDDIOP0	
TK	SSC Transmit Clock	I/O		VDDIOP0	
RK	SSC Receive Clock	I/O		VDDIOP0	
TF	SSC Transmit Frame Sync	I/O		VDDIOP0	
RF	SSC Receive Frame Sync	I/O		VDDIOP0	
Timer/Counter - TCx					
TCLKx	TC Channel x External Clock Input	Input		VDDIOP0	
TIOAx	TC Channel x I/O Line A	I/O		VDDIOP0	
TIOBx	TC Channel x I/O Line B	I/O		VDDIOP0	
Serial Peripheral Interface - SPIx_					
SPIx_MISO	Master In Slave Out	I/O		VDDIOP0	
SPIx_MOSI	Master Out Slave In	I/O		VDDIOP0	
SPIx_SPCK	SPI Serial Clock	I/O		VDDIOP0	
SPIx_NPCS0	SPI Peripheral Chip Select 0	I/O	Low	VDDIOP0	
SPIx_NPCS1-SPIx_NPCS3	SPI Peripheral Chip Select	Output	Low	VDDIOP0	
Two-Wire Interface					
TWDx	Two-wire Serial Data	I/O		VDDIOP0	
TWCKx	Two-wire Serial Clock	I/O		VDDIOP0	
USB Host Port					
HDPA	USB Host Port A Data +	Analog		VDDIOP0	
HDMA	USB Host Port A Data -	Analog		VDDIOP0	
HDPB	USB Host Port B Data +	Analog		VDDIOP0	
HDMB	USB Host Port B Data +	Analog		VDDIOP0	
USB Device Port					
DDM	USB Device Port Data -	Analog		VDDIOP0	
DDP	USB Device Port Data +	Analog		VDDIOP0	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
Ethernet 10/100					
ETXCK	Transmit Clock or Reference Clock	Input		VDDIOP0	MII only, REFCK in RMII
ERXCK	Receive Clock	Input		VDDIOP0	MII only
ETXEN	Transmit Enable	Output		VDDIOP0	
ETX0-ETX3	Transmit Data	Output		VDDIOP0	ETX0-ETX1 only in RMII
ETXER	Transmit Coding Error	Output		VDDIOP0	MII only
ERXDV	Receive Data Valid	Input		VDDIOP0	RXDV in MII, CRSDV in RMII
ERX0-ERX3	Receive Data	Input		VDDIOP0	ERX0-ERX1 only in RMII
ERXER	Receive Error	Input		VDDIOP0	
ECRS	Carrier Sense and Data Valid	Input		VDDIOP0	MII only
ECOL	Collision Detect	Input		VDDIOP0	MII only
EMDC	Management Data Clock	Output		VDDIOP0	
EMDIO	Management Data Input/Output	I/O		VDDIOP0	
EF100	Force 100Mbit/sec.	Output	High	VDDIOP0	
Image Sensor Interface					
ISI_D0- ISI_D11	Image Sensor Data	Input		VDDIOP1	
ISI_MCK	Image sensor Reference clock	output		VDDIOP1	
ISI_HSYNC	Image Sensor Horizontal Synchro	input		VDDIOP1	
ISI_VSYNC	Image Sensor Vertical Synchro	input		VDDIOP1	
ISI_PCK	Image Sensor Data clock	input		VDDIOP1	
Analog to Digital Converter					
AD0-AD3	Analog Inputs	Analog		VDDANA	Digital pulled-up inputs at reset
ADVREF	Analog Positive Reference	Analog		VDDANA	
ADTRG	ADC Trigger	Input		VDDANA	
Fast Flash Programming Interface					
PGMEN[2:0]	Programming Enabling	Input		VDDIOP0	
PGMNCMD	Programming Command	Input	Low	VDDIOP0	
PGMRDY	Programming Ready	Output	High	VDDIOP0	
PGMNOE	Programming Read	Input	Low	VDDIOP0	
PGMNVALID	Data Direction	Output	Low	VDDIOP0	
PGMM[3:0]	Programming Mode	Input		VDDIOP0	
PGMD[15:0]	Programming Data	I/O		VDDIOP0	

Note: 1. Programming of this pull-up resistor is performed independently for each I/O line through the PIO Controllers. After reset, all the I/O lines default as inputs with pull-up resistors enabled, except those which are multiplexed with the External Bus Interface signals that require to be enabled as Peripheral at reset. This is explicitly indicated in the column “Reset State” of the peripheral multiplexing tables.

4. Package and Pinout

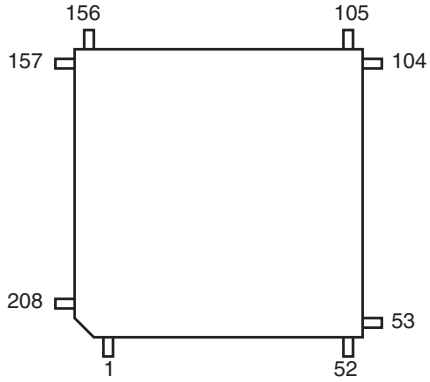
The AT91SAM9XE128/256/512 is available in a 208-pin PQFP Green package (0.5mm pitch) or in a 217-ball LFBGA Green package (0.8 mm ball pitch).

4.1 208-pin PQFP Package Outline

Figure 4-1 shows the orientation of the 208-pin PQFP package.

A detailed mechanical description is given in the section “AT91SAM9XE Mechanical Characteristics” of the product datasheet.

Figure 4-1. 208-pin PQFP Package Outline (Top View)



4.2 208-pin PQFP Package Pinout

Table 4-1. Pinout for 208-pin PQFP Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	PA24	53	GND	105	RAS	157	ADVREF
2	PA25	54	DDM	106	D0	158	PC0
3	PA26	55	DDP	107	D1	159	PC1
4	PA27	56	PC13	108	D2	160	VDDANA
5	VDDIOP0	57	PC11	109	D3	161	PB10
6	GND	58	PC10	110	D4	162	PB11
7	PA28	59	PC14	111	D5	163	PB20
8	PA29	60	PC9	112	D6	164	PB21
9	PB0	61	PC8	113	GND	165	PB22
10	PB1	62	PC4	114	VDDIOM	166	PB23
11	PB2	63	PC6	115	SDCK	167	PB24
12	PB3	64	PC7	116	SDWE	168	PB25
13	VDDIOP0	65	VDDIOM	117	SDCKE	169	VDDIOP1
14	GND	66	GND	118	D7	170	GND
15	PB4	67	PC5	119	D8	171	PB26
16	PB5	68	NCS0	120	D9	172	PB27
17	PB6	69	CFOE/NRD	121	D10	173	GND
18	PB7	70	CFWE/NWE/NWR0	122	D11	174	VDDCORE
19	PB8	71	NANDOE	123	D12	175	PB28
20	PB9	72	NANDWE	124	D13	176	PB29
21	PB14	73	A22	125	D14	177	PB30
22	PB15	74	A21	126	D15	178	PB31
23	PB16	75	A20	127	PC15	179	PA0
24	VDDIOP0	76	A19	128	PC16	180	PA1
25	GND	77	VDDCORE	129	PC17	181	PA2
26	PB17	78	GND	130	PC18	182	PA3
27	PB18	79	A18	131	PC19	183	PA4
28	PB19	80	BA1/A17	132	VDDIOM	184	PA5
29	TDO	81	BA0/A16	133	GND	185	PA6
30	TDI	82	A15	134	PC20	186	PA7
31	TMS	83	A14	135	PC21	187	VDDIOP0
32	VDDIOP0	84	A13	136	PC22	188	GND
33	GND	85	A12	137	PC23	189	PA8
34	TCK	86	A11	138	PC24	190	PA9
35	NTRST	87	A10	139	PC25	191	PA10
36	NRST	88	A9	140	PC26	192	PA11
37	RTCK	89	A8	141	PC27	193	PA12
38	VDDCORE	90	VDDIOM	142	PC28	194	PA13
39	GND	91	GND	143	PC29	195	PA14
40	ERASE	92	A7	144	PC30	196	PA15
41	OSCSEL	93	A6	145	PC31	197	PA16
42	TST	94	A5	146	GND	198	PA17
43	JTAGSEL	95	A4	147	VDDCORE	199	VDDIOP0
44	GNDBU	96	A3	148	VDDPLL	200	GND
45	XOUT32	97	A2	149	XIN	201	PA18
46	XIN32	98	NWR2/NBS2/A1	150	XOUT	202	PA19
47	VDDBU	99	NBS0/A0	151	GNDPLL	203	VDDCORE
48	WKUP	100	SDA10	152	NC	204	GND

Table 4-1. Pinout for 208-pin PQFP Package (Continued)

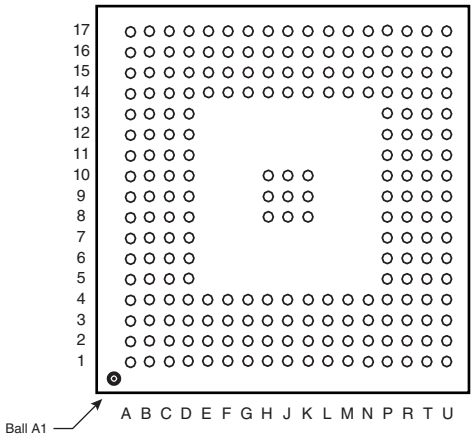
Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
49	SHDN	101	CFIOW/NBS3/NWR3	153	GNDPLL	205	PA20
50	HDMA	102	CFIOR/NBS1/NWR1	154	PLLRCA	206	PA21
51	HDPA	103	SDCS/NCS1	155	VDDPLL	207	PA22
52	VDDIOP0	104	CAS	156	GNDANA	208	PA23

4.3 217-ball LFBGA Package Outline

Figure 4-2 shows the orientation of the 217-ball LFBGA package.

A detailed mechanical description is given in the section “AT91SAM9XE Mechanical Characteristics” of the product datasheet.

Figure 4-2. 217-ball LFBGA Package Outline (Top View)



4.4 217-ball LFBGA Package Pinout

Table 4-2. Pinout for 217-ball LFBGA Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	CFIOW/NBS3/NWR3	D5	A5	J14	TDO	P17	PB5
A2	NBS0/A0	D6	GND	J15	PB19	R1	NC
A3	NWR2/NBS2/A1	D7	A10	J16	TDI	R2	GNDANA
A4	A6	D8	GND	J17	PB16	R3	PC29
A5	A8	D9	VDDCORE	K1	PC24	R4	VDDANA
A6	A11	D10	GND	K2	PC20	R5	PB12
A7	A13	D11	VDDIOM	K3	D15	R6	PB23
A8	BA0/A16	D12	GND	K4	PC21	R7	GND
A9	A18	D13	DDM	K8	GND	R8	PB26
A10	A21	D14	HDPB	K9	GND	R9	PB28
A11	A22	D15	NC	K10	GND	R10	PA0
A12	CFWE/NWE/NWR0	D16	VDDBU	K14	PB4	R11	PA4
A13	CFOE/NRD	D17	XIN32	K15	PB17	R12	PA5
A14	NCS0	E1	D10	K16	GND	R13	PA10
A15	PC5	E2	D5	K17	PB15	R14	PA21
A16	PC6	E3	D3	L1	GND	R15	PA23
A17	PC4	E4	D4	L2	PC26	R16	PA24
B1	SDCK	E14	HDPA	L3	PC25	R17	PA29
B2	CFIOR/NBS1/NWR1	E15	HDMA	L4	VDDIOP0	T1	PLLRCA
B3	SDCS/NCS1	E16	GNDBU	L14	PA28	T2	GNDPLL
B4	SDA10	E17	XOUT32	L15	PB9	T3	PC0
B5	A3	F1	D13	L16	PB8	T4	PC1
B6	A7	F2	SDWE	L17	PB14	T5	PB10
B7	A12	F3	D6	M1	VDDCORE	T6	PB22
B8	A15	F4	GND	M2	PC31	T7	GND
B9	A20	F14	OSCSEL	M3	GND	T8	PB29
B10	NANDWE	F15	ERASE	M4	PC22	T9	PA2
B11	PC7	F16	JTAGSEL	M14	PB1	T10	PA6
B12	PC10	F17	TST	M15	PB2	T11	PA8
B13	PC13	G1	PC15	M16	PB3	T12	PA11
B14	PC11	G2	D7	M17	PB7	T13	VDDCORE
B15	PC14	G3	SDCKE	N1	XIN	T14	PA20
B16	PC8	G4	VDDIOM	N2	VDDPLL	T15	GND
B17	WKUP	G14	GND	N3	PC23	T16	PA22
C1	D8	G15	NRST	N4	PC27	T17	PA27
C2	D1	G16	RTCK	N14	PA31	U1	GNDPLL
C3	CAS	G17	TMS	N15	PA30	U2	ADVREF
C4	A2	H1	PC18	N16	PB0	U3	PC2
C5	A4	H2	D14	N17	PB6	U4	PC3
C6	A9	H3	D12	P1	XOUT	U5	PB20
C7	A14	H4	D11	P2	VDDPLL	U6	PB21
C8	BA1/A17	H8	GND	P3	PC30	U7	PB25
C9	A19	H9	GND	P4	PC28	U8	PB27
C10	NANDOE	H10	GND	P5	PB11	U9	PA12
C11	PC9	H14	VDDCORE	P6	PB13	U10	PA13
C12	PC12	H15	TCK	P7	PB24	U11	PA14
C13	DDP	H16	NTRST	P8	VDDIOP1	U12	PA15
C14	HDMB	H17	PB18	P9	PB30	U13	PA19
C15	NC	J1	PC19	P10	PB31	U14	PA17
C16	VDDIOP0	J2	PC17	P11	PA1	U15	PA16
C17	SHDN	J3	VDDIOM	P12	PA3	U16	PA18

Table 4-2. Pinout for 217-ball LFBGA Package (Continued)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
D1	D9	J4	PC16	P13	PA7	U17	VDDIOP0
D2	D2	J8	GND	P14	PA9		
D3	RAS	J9	GND	P15	PA26		
D4	D0	J10	GND	P16	PA25		

5. Power Considerations

5.1 Power Supplies

The AT91SAM9XE128/256/512 has several types of power supply pins:

- VDDCORE pins: Power the core, including the processor, the embedded memories and the peripherals; voltage ranges from 1.65V and 1.95V, 1.8V nominal.
- VDDIOM pins: Power the External Bus Interface I/O lines; voltage ranges between 1.65V and 1.95V (1.8V typical) or between 3.0V and 3.6V (3.3V nominal). The expected voltage range is selectable by software.
- VDDIOP0 pins: Power the Peripheral I/O lines and the USB transceivers; voltage ranges from 3.0V and 3.6V, 3V or 3.3V nominal.
- VDDIOP1 pin: Powers the Peripherals I/O lines involving the Image Sensor Interface; voltage ranges from 1.65V and 3.6V, 1.8V, 2.5V, 3V or 3.3V nominal.
- VDDBU pin: Powers the Slow Clock oscillator and a part of the System Controller; voltage ranges from 1.65V to 1.95V, 1.8V nominal.
- VDDPLL pins: Power the PLL cells and the main oscillator; voltage ranges from 1.65V and 1.95V, 1.8V nominal.
- VDDANA pin: Powers the Analog to Digital Converter; voltage ranges from 3.0V and 3.6V, 3.3V nominal.

The power supplies VDDIOM, VDDIOP0 and VDDIOP1 are identified in the pinout table and their associated I/O lines in the multiplexing tables. These supplies enable the user to power the device differently for interfacing with memories and for interfacing with peripherals.

Ground pins GND are common to VDDCORE, VDDIOM, VDDIOP0 and VDDIOP1 pins power supplies. Separated ground pins are provided for VDDBU, VDDPLL and VDDANA. These ground pins are respectively GNDBU, GNDPLL and GNDANA.

6. I/O Line Considerations

6.1 ERASE Pin

The pin ERASE is used to re-initialize the Flash content and the NVM bits. It integrates a permanent pull-down resistor of about **15 kΩ**, so that it can be left unconnected for normal operations.

This pin is debounced on the RC oscillator or 32,768 Hz to improve the glitch tolerance. Minimum debouncing time is 200 ms.

6.2 I/O Line Drive Levels

The PIO lines PA0 to PA31 and PB0 to PB31 and PC0 to PC3 are high-drive current capable. Each of these I/O lines can drive up to 16 mA permanently with a total of 350 mA on all I/O lines.

Refer to the “DC Characteristics” section of the product datasheet.

6.3 Shutdown Logic Pins

The SHDN pin is a tri-state output only pin, which is driven by the Shutdown Controller. There is no internal pull-up. An external pull-up to VDDBU is needed and its value must be higher than 1 MΩ. The resisitor value is calculated according to the regulator enable implementation and the SHDN level.

The pin WKUP is an input-only. It can accept voltages only between 0V and VDDBU.

7. Processor and Architecture

7.1 ARM926EJ-S Processor

- RISC Processor Based on ARM v5TEJ Architecture with Jazelle technology for Java acceleration
- Two Instruction Sets
  - ARM High-performance 32-bit Instruction Set
  - Thumb High Code Density 16-bit Instruction Set
- DSP Instruction Extensions
- 5-Stage Pipeline Architecture:
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)
  - Data Memory (M)
  - Register Write (W)
- 8 KB Data Cache, 16 KB Instruction Cache
  - Virtually-addressed 4-way Associative Cache
  - Eight words per line
  - Write-through and Write-back Operation
  - Pseudo-random or Round-robin Replacement
- Write Buffer
  - Main Write Buffer with 16-word Data Buffer and 4-address Buffer

  - DCache Write-back Buffer with 8-word Entries and a Single Address Entry
  - Software Control Drain
- Standard ARM v4 and v5 Memory Management Unit (MMU)
  - Access Permission for Sections
  - Access Permission for large pages and small pages can be specified separately for each quarter of the page
  - 16 embedded domains
- Bus Interface Unit (BIU)
  - Arbitrates and Schedules AHB Requests
  - Separate Masters for both instruction and data access providing complete Matrix system flexibility
  - Separate Address and Data Buses for both the 32-bit instruction interface and the 32-bit data interface
  - On Address and Data Buses, data can be 8-bit (Bytes), 16-bit (Half-words) or 32-bit (Words)

7.2 Bus Matrix

- 6-layer Matrix, handling requests from 6 masters
- Programmable Arbitration strategy
  - Fixed-priority Arbitration
  - Round-Robin Arbitration, either with no default master, last accessed default master or fixed default master
- Burst Management
  - Breaking with Slot Cycle Limit Support
  - Undefined Burst Length Support
- One Address Decoder provided per Master
  - Three different slaves may be assigned to each decoded memory area: one for internal ROM boot, one for internal flash boot, one after remap
- Boot Mode Select
  - Non-volatile Boot Memory can be internal ROM or internal Flash
  - Selection is made by General purpose NVM bit sampled at reset
- Remap Command
  - Allows Remapping of an Internal SRAM in Place of the Boot Non-Volatile Memory (ROM or Flash)
  - Allows Handling of Dynamic Exception Vectors

7.2.1 Matrix Masters

The Bus Matrix of the AT91SAM9XE128/256/512 manages six Masters, thus each master can perform an access concurrently with others, depending on whether the slave it accesses is available.

Each Master has its own decoder, which can be defined specifically for each master. In order to simplify the addressing, all the masters have the same decodings.

Table 7-1. List of Bus Matrix Masters

Master 0	ARM926™ Instruction
Master 1	ARM926 Data
Master 2	Peripheral DMA Controller
Master 3	USB Host Controller
Master 4	Image Sensor Controller
Master 5	Ethernet MAC

7.2.2 Matrix Slaves

Each Slave has its own arbiter, thus allowing a different arbitration per Slave to be programmed.

Table 7-2. List of Bus Matrix Slaves

Slave 0	Internal Flash
Slave 1	Internal SRAM
Slave 2	Internal ROM
	USB Host User Interface
Slave 3	External Bus Interface
Slave 4	Reserved
Slave 5	Internal Peripherals

7.2.3 Masters to Slaves Access

All the Masters can normally access all the Slaves. However, some paths do not make sense, such as allowing access from the Ethernet MAC to the internal peripherals.

Thus, these paths are forbidden or simply not wired, and shown as "–" in the following table.

Table 7-3. AT91SAM9XE128/256/512 Masters to Slaves Access

Master / **Slave**		**0 and 1** ARM926 Instruction and Data	**2** Periphera DMA Controller	**3** ISI Controller	**4** Ethernet MAC	**5** USB Host Controller
0	Internal Flash	X	–	–	X	
1	Internal SRAM	X	X	X	X	X
2	Internal ROM	X	X	–	–	–
	UHP User Interface	X	–	–	–	–
3	External Bus Interface	X	X	X	X	X
4	Reserved	–	–	–	–	–
	Internal Peripherals	X	X	–	–	–

7.3 Peripheral DMA Controller

- Acting as one Matrix Master

- Allows data transfers from/to peripheral to/from any memory space without any intervention of the processor.
- Next Pointer Support, forbids strong real-time constraints on buffer management.
- Twenty-four channels
  - Two for each USART
  - Two for the Debug Unit
  - Two for each Serial Synchronous Controller
  - Two for each Serial Peripheral Interface
  - Two for the Two Wire Interface
  - One for Multimedia Card Interface
  - One for Analog To Digital Converter

The Peripheral DMA Controller handles transfer requests from the channel according to the following priorities (Low to High priorities):

- TWI0 Transmit Channel
- TWI1 Transmit Channel
- DBGU Transmit Channel
- USART4 Transmit Channel
- USART3 Transmit Channel
- USART2 Transmit Channel
- USART1 Transmit Channel
- USART0 Transmit Channel
- SPI1 Transmit Channel
- SPI0 Transmit Channel
- SSC Transmit Channel
- TWI0 Receive Channel
- TWI1 Receive Channel
- DBGU Receive Channel
- USART4 Receive Channel
- USART3 Receive Channel
- USART2 Receive Channel
- USART1 Receive Channel
- USART0 Receive Channel
- ADC Receive Channel
- SPI1 Receive Channel
- SPI0 Receive Channel
- SSC Receive Channel
- MCI Transmit/Receive Channel

7.4 Debug and Test Features

- ARM926 Real-time In-circuit Emulator
  - Two real-time Watchpoint Units

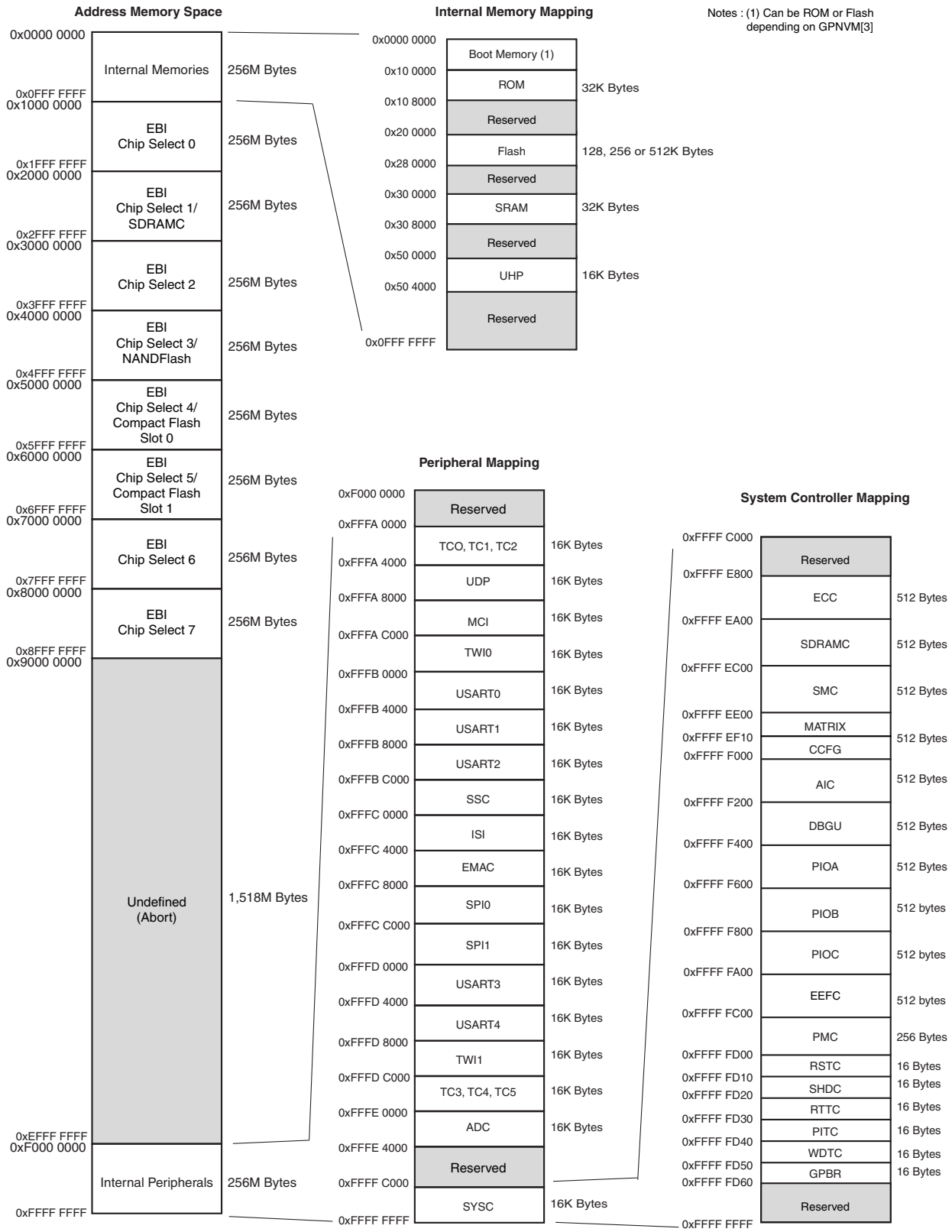
- Two Independent Registers: Debug Control Register and Debug Status Register
- Test Access Port Accessible through JTAG Protocol
- Debug Communications Channel

• Debug Unit
- Two-pin UART
- Debug Communication Channel Interrupt Handling
- Chip ID Register

• IEEE1149.1 JTAG Boundary-scan on All Digital Pins

8. Memories

Figure 8-1. AT91SAM9XE128/256/512 Memory Mapping



A first level of address decoding is performed by the Bus Matrix, i.e., the implementation of the Advanced High performance Bus (AHB) for its Master and Slave interfaces with additional features.

Decoding breaks up the 4 Gbytes of address space into 16 banks of 256 Mbytes. The banks 1 to 7 are directed to the EBI that associates these banks to the external chip selects EBI_NCS0 to EBI_NCS7. Bank 0 is reserved for the addressing of the internal memories, and a second level of decoding provides 1 Mbyte of internal memory area. The bank 15 is reserved for the peripherals and provides access to the Advanced Peripheral Bus (APB).

Other areas are unused and performing an access within them provides an abort to the master requesting such an access.

Each Master has its own bus and its own decoder, thus allowing a different memory mapping per Master. However, in order to simplify the mappings, all the masters have a similar address decoding.

Regarding Master 0 and Master 1 (ARM926 Instruction and Data), three different Slaves are assigned to the memory space decoded at address 0x0: one for internal boot, one for external boot, one after remap, refer to Table 8-3, “Internal Memory Mapping,” on page 26 for details.

A complete memory map is presented in Figure 8-1 on page 21.

8.1 Embedded Memories

8.1.1 AT91SAM9XE128

- 32 KB ROM
  - Single Cycle Access at full matrix speed
- 16 KB Fast SRAM
  - Single Cycle Access at full matrix speed
- 128 KB Embedded Flash

8.1.2 AT91SAM9XE256

- 32 KB ROM
  - Single Cycle Access at full matrix speed
- 32 KB Fast SRAM
  - Single Cycle Access at full matrix speed
- 256 KB Embedded Flash

8.1.3 AT91SAM9XE512

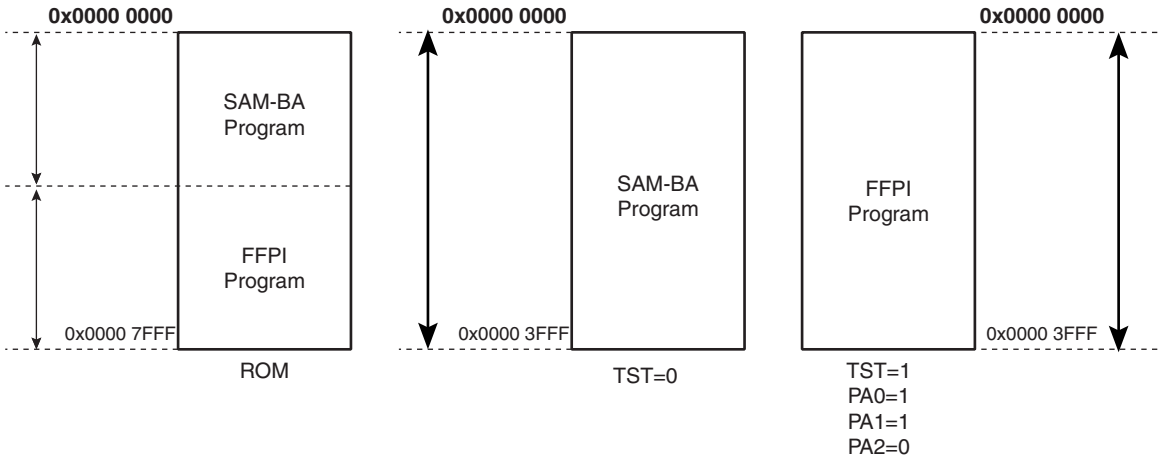
- 32 KB ROM
  - Single Cycle Access at full matrix speed
- 32 KB Fast SRAM
  - Single Cycle Access at full matrix speed
- 512 KB Embedded Flash

8.1.4 ROM Topology

The embedded ROM contains the Fast Flash Programming and the SAM-BA boot programs. Each of these two programs is stored at 16 KB Boundary and the program executed at address

zero depends on the combination of the TST pin and PA0 to PA2 pins. Figure 8-2 shows the contents of the ROM and the program available at address zero.

Figure 8-2. ROM Boot Memory Map



8.1.4.1 *Fast Flash Programming Interface*

The Fast Flash Programming Interface programs the device through a serial JTAG interface or a multiplexed fully-handshaked parallel port. It allows gang-programming with market-standard industrial programmers.

The FFPI supports read, page program, page erase, full erase, lock, unlock and protect commands.

The Fast Flash Programming Interface is enabled and the Fast Programming Mode is entered when the TST pin and the PA0 and PA1 pins are all tied high and PA2 is tied low.

Table 8-1. Signal Description

Signal Name	PIO	Type	Active Level	Comments
PGMEN0	PA0	Input	High	Must be connected to VDDIO
PGMEN1	PA1	Input	High	Must be connected to VDDIO
PGMEN2	PA2	Input	Low	Must be connected to GND
PGMNCMD	PA4	Input	Low	Pulled-up input at reset
PGMRDY	PA5	Output	High	Pulled-up input at reset
PGMNOE	PA6	Input	Low	Pulled-up input at reset
PGMNVALID	PA7	Output	Low	Pulled-up input at reset
PGMM[3:0]	PA8..PA10	Input		Pulled-up input at reset
PGMD[15:0]	PA12..PA27	Input/Output		Pulled-up input at reset

8.1.4.2 *SAM-BA® Boot Assistant*

The SAM-BA Boot Assistant is a default Boot Program that provides an easy way to program in situ the on-chip Flash memory.

The SAM-BA Boot Assistant supports serial communication through the DBGU or through the USB Device Port.

- Communication through the DBGU supports a wide range of crystals from 3 to 20 MHz via software auto-detection.
- Communication through the USB Device Port is depends on crystal selected:
  - limited to an 18,432 Hz crystal if the internal RC oscillator is selected
  - supports a wide range of crystals from 3 to 20 MHz if the 32,768 Hz crystal is selected

The SAM-BA Boot provides an interface with SAM-BA Graphic User Interface (GUI).

8.1.5 Embedded Flash

The Flash of the AT91SAM9XE128/256/512 is organized in 256/512/1024 pages of 512 bytes directly connected to the 32-bit internal bus. Each page contains 128 words.

The Flash contains a 512-byte write buffer allowing the programming of a page. This buffer is write-only as 128 32-bit words, and accessible all along the 1 MB address space, so that each word can be written at its final address.

The Flash benefits from the integration of a power reset cell and from a brownout detector to prevent code corruption during power supply changes, even in the worst conditions.

8.1.5.1 Enhanced Embedded Flash Controller

The Enhanced Embedded Flash Controller (EEFC) is continuously clocked.

The Enhanced Embedded Flash Controller (EEFC) is a slave for the bus matrix and is configurable through its User Interface on the APB bus. It ensures the interface of the Flash block with the 32-bit internal bus. Its 128-bit wide memory interface increases performance, four 32-bit data are read during each access, this multiply the throughput by 4 in case of consecutive data.

It also manages the programming, erasing, locking and unlocking sequences of the Flash using a full set of commands. One of the commands returns the embedded Flash descriptor definition that informs the system about the Flash organization, thus making the software generic programming of the access parameters of the Flash (number of wait states, timings, etc.)

8.1.5.2 Lock Regions

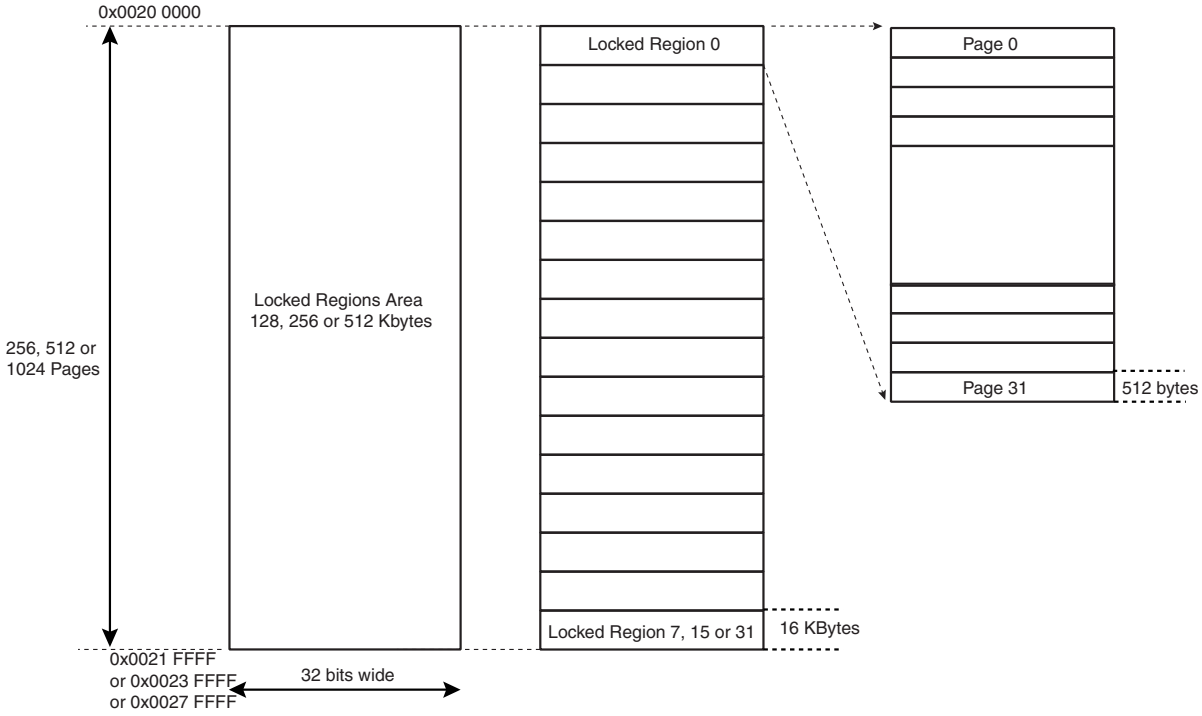
The memory plane of 128, 256 or 512 Kbytes is organized in 8, 16 or 32 locked regions of 32 pages each. Each lock region can be locked independently, so that the software protects the first memory plane against erroneous programming:

If a locked-regions erase or program command occurs, the command is aborted and the EEFC could trigger an interrupt.

The Lock bits are software programmable through the EEFC User Interface. The command “Set Lock Bit” enables the protection. The command “Clear Lock Bit” unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

Figure 8-3. Flash First Memory Plane Mapping



8.1.5.3 GPNVM Bits

The AT91SAM9XE128/256/512 features four GPNVM bits that can be cleared or set respectively through the commands “Clear GPNVM Bit” and “Set GPNVM Bit” of the EEFC User Interface.

Table 8-2. General-purpose Non volatile Memory Bits

GPNVMBit[#]	Function
0	Security Bit
1	Brownout Detector Enable
2	Brownout Detector Reset Enable
3	Boot Mode Select (BMS)

8.1.5.4 Security Bit

The AT91SAM9XE128/256/512 features a security bit, based on a specific GPNVM bit, GPNVMBit[0]. When the security is enabled, access to the Flash, either through the ICE interface or through the Fast Flash Programming Interface, is forbidden. This ensures the confidentiality of the code programmed in the Flash.

Disabling the security bit can only be achieved by asserting the ERASE pin at 1, and after a full Flash erase is performed. When the security bit is deactivated, all accesses to the Flash are permitted.

As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation.

8.1.5.5 *Non-volatile Brownout Detector Control*

Two GPNVM bits are used for controlling the brownout detector (BOD), so that even after a power loss, the brownout detector operations remain in their state.

- GPNVMBit[1] is used as a brownout detector enable bit. Setting GPNVMBit[1] enables the BOD, clearing it disables the BOD. Asserting ERASE clears GPNVMBit[1] and thus disables the brownout detector by default.
- GPNVMBit[2] is used as a brownout reset enable signal for the reset controller. Setting GPNVMBit[2] enables the brownout reset when a brownout is detected, clearing GPNVMBit[2] disables the brownout reset. Asserting ERASE disables the brownout reset by default.

8.1.6 Boot Strategies

Table 8-3 summarizes the Internal Memory Mapping for each Master, depending on the Remap status and the GPNVMBit[3] state at reset.

Table 8-3. Internal Memory Mapping

Address	REMAP = 0		REMAP = 1
	GPNVMBit[3] clear	GPNVMBit[3] set	
0x0000 0000	ROM	Flash	SRAM

The system always boots at address 0x0. To ensure a maximum number of possibilities for boot, the memory layout can be configured with two parameters.

REMAP allows the user to lay out the first internal SRAM bank to 0x0 to ease development. This is done by software once the system has booted. Refer to the section “AT91SAM9XE Bus Matrix” in the product datasheet for more details.

When REMAP = 0, a non volatile bit stored in Flash memory (GPNVMBit[3]) allows the user to lay out to 0x0, at his convenience, the ROM or the Flash. Refer to the section “Enhanced Embedded Flash Controller (EEFC)” in the product datasheet for more details.

Note: Memory blocks not affected by these parameters can always be seen at their specified base addresses. See the complete memory map presented in Figure 8-1 on page 21.

The AT91SAM9XE Matrix manages a boot memory that depends on the value of GPNVMBit[3] at reset. The internal memory area mapped between address 0x0 and 0x0FFF FFFF is reserved for this purpose.

If GPNVMBit[3] is set, the boot memory is the internal Flash memory

If GPNVMBit[3] is clear (Flash reset State), the boot memory is the embedded ROM. After a Flash erase, the boot memory is the internal ROM.

8.1.6.1 *GPNVMBit[3] = 0, Boot on Embedded ROM*

The system boots using the Boot Program.

- Boot on slow clock (On-chip RC or 32,768 Hz)
- Auto baudrate detection
- SAM-BA Boot in case no valid program is detected in external NVM, supporting
  - Serial communication on a DBGU
  - USB Device Port

8.1.6.2 *GPNVMBit[3] = 1, Boot on Internal Flash*

- Boot on slow clock (On-chip RC or 32,768 Hz)

The customer-programmed software must perform a complete configuration.

To speed up the boot sequence when booting at 32 kHz, the user must take the following steps:

1. Program the PMC (main oscillator enable or bypass mode)
2. Program and start the PLL
3. Switch the main clock to the new value.

8.2 External Memories

The external memories are accessed through the External Bus Interface. Each Chip Select line has a 256 MB memory area assigned.

Refer to the memory map in Figure 8-1 on page 21.

8.2.1 External Bus Interface

- Integrates three External Memory Controllers:
  - Static Memory Controller
  - SDRAM Controller
  - ECC Controller
- Additional logic for NANDFlash
- Full 32-bit External Data Bus
- Up to 26-bit Address Bus (up to 64 MB linear)
- Up to 8 chip selects, Configurable Assignment:
  - Static Memory Controller on NCS0
  - SDRAM Controller or Static Memory Controller on NCS1
  - Static Memory Controller on NCS2
  - Static Memory Controller on NCS3, Optional NAND Flash support
  - Static Memory Controller on NCS4 - NCS5, Optional CompactFlash support
  - Static Memory Controller on NCS6-NCS7

8.2.2 Static Memory Controller

- 8-, 16- or 32-bit Data Bus
- Multiple Access Modes supported
  - Byte Write or Byte Select Lines
  - Asynchronous read in Page Mode supported (4- up to 32-byte page size)
- Multiple device adaptability
  - Compliant with LCD Module
  - Control signals programmable setup, pulse and hold time for each Memory Bank
- Multiple Wait State Management
  - Programmable Wait State Generation
  - External Wait Request
  - Programmable Data Float Time
- Slow Clock mode supported

8.2.3 SDRAM Controller

- Supported devices:
  - Standard and Low Power SDRAM (Mobile SDRAM)
- Numerous configurations supported
  - 2K, 4K, 8K Row Address Memory Parts
  - SDRAM with two or four Internal Banks
  - SDRAM with 16- or 32-bit Data Path
- Programming facilities
  - Word, half-word, byte access
  - Automatic page break when Memory Boundary has been reached
  - Multibank Ping-pong Access
  - Timing parameters specified by software
  - Automatic refresh operation, refresh rate is programmable
- Energy-saving capabilities
  - Self-refresh, power down and deep power down modes supported
- Error detection
  - Refresh Error Interrupt
- SDRAM Power-up Initialization by software
- CAS Latency of 1, 2 and 3 supported
- Auto Precharge Command not used

8.2.4 Error Corrected Code Controller

- Hardware error corrected code generation
  - Detection and correction by software
- Supports NAND Flash and SmartMedia devices with 8- or 16-bit data path
- Supports NAND Flash and SmartMedia with page sizes of 528,1056, 2112 and 4224 bytes specified by software
- Supports 1 bit correction for a page of 512, 1024, 2112 and 4096 bytes with 8- or 16-bit data path
- Supports 1 bit correction per 512 bytes of data for a page size of 512, 2048 and 4096 bytes with 8-bit data path
- Supports 1 bit correction per 256 bytes of data for a page size of 512, 2048 and 4096 bytes with 8-bit data path

Ω

9. System Controller

The System Controller is a set of peripherals that allows handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc.

The System Controller User Interface also embeds the registers that configure the Matrix and a set of registers for the chip configuration. The chip configuration registers configure the EBI chip select assignment and voltage range for external memories.

The System Controller's peripherals are all mapped within the highest 16 KB of address space, between addresses 0xFFFF E800 and 0xFFFF FFFF.

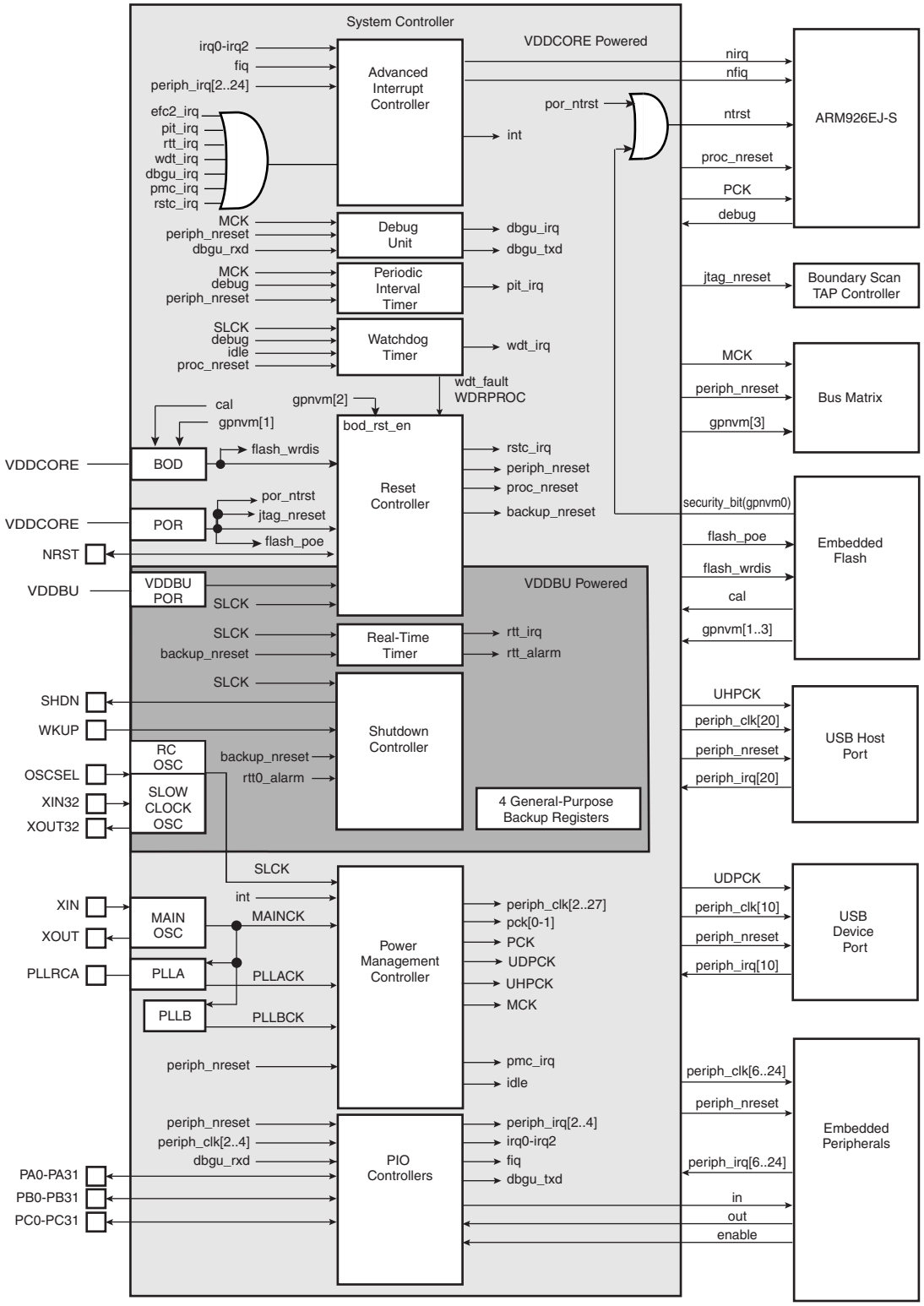
However, all the registers of System Controller are mapped on the top of the address space. All the registers of the System Controller can be addressed from a single pointer by using the standard ARM instruction set, as the Load/Store instruction have an indexing mode of ±4 KB.

Figure 9-1 on page 30 shows the System Controller block diagram.

Figure 8-1 on page 21 shows the mapping of the User Interfaces of the System Controller peripherals.

9.1 System Controller Block Diagram

Figure 9-1. AT91SAM9XE128/256/512 System Controller Block Diagram



9.2 Reset Controller

- Based on two Power-on reset cells
  - One on VDDBU and one on VDDCORE
- Status of the last reset
  - Either general reset (VDDBU rising), wake-up reset (VDDCORE rising), software reset, user reset or watchdog reset
- Controls the internal resets and the NRST pin output
  - Allows shaping a reset signal for the external devices

9.3 Brownout Detector and Power-on Reset

The AT91SAM9XE128/256/512 embeds one brownout detection circuit and power-on reset cells. The power-on reset are supplied with and monitor VDDCORE and VDDBU.

Signals (flash_poe and flash_wrdis) are provided to the Flash to prevent any code corruption during power-up or power-down sequences or if brownouts occur on the VDDCORE power supply.

The power-on reset cell has a limited-accuracy threshold at around 1.5V. Its output remains low during power-up until VDDCORE goes over this voltage level. This signal goes to the reset controller and allows a full re-initialization of the device.

The brownout detector monitors the VDDCORE level during operation by comparing it to a fixed trigger level. It secures system operations in the most difficult environments and prevents code corruption in case of brownout on the VDDCORE.

When the brownout detector is enabled and VDDCORE decreases to a value below the trigger level (Vbot-), the brownout output is immediately activated. For more details on Vbot, see the table “Brownout Detector Characteristics” in the section “AT91SAM9XE128/256/512 Electrical Characteristics” in the full datasheet.

When VDDCORE increases above the trigger level (Vbot+, defined as Vbot + Vhyst), the reset is released. The brownout detector only detects a drop if the voltage on VDDCORE stays below the threshold voltage for longer than about 1µs.

The VDDCORE threshold voltage has a hysteresis of about 50 mV typical, to ensure spike free brownout detection. The typical value of the brownout detector threshold is 1.55V with an accuracy of ± 2% and is factory calibrated.

The brownout detector is low-power, as it consumes less than 12 µA static current. However, it can be deactivated to save its static current. In this case, it consumes less than 1 µA. The deactivation is configured through the GPNVMBit[1] of the Flash.

Additional information can be found in the “Electrical Characteristics” section of the product datasheet.

9.4 Shutdown Controller

- Shutdown and Wake-Up logic
  - Software programmable assertion of the SHDN pin
  - Deassertion Programmable on a WKUP pin level change or on alarm

9.5 Clock Generator

- Embeds a low power 32,768 Hz slow clock oscillator and a low-power RC oscillator selectable with OSCSEL signal
  - Provides the permanent slow clock SLCK to the system
- Embeds the main oscillator
  - Oscillator bypass feature
  - Supports 3 to 20 MHz crystals
- Embeds 2 PLLs
  - PLL A outputs 80 to 240 MHz clock
  - PLL B outputs 70 MHz to 130 MHz clock
  - Both integrate an input divider to increase output accuracy
  - PLLB embeds its own filter

9.6 Power Management Controller

- Provides:
  - the Processor Clock PCK
  - the Master Clock MCK, in particular to the Matrix and the memory interfaces
  - the USB Device Clock UDPCK
  - independent peripheral clocks, typically at the frequency of MCK
  - 2 programmable clock outputs: PCK0, PCK1
- Five flexible operating modes:
  - Normal Mode, processor and peripherals running at a programmable frequency
  - Idle Mode, processor stopped waiting for an interrupt
  - Slow Clock Mode, processor and peripherals running at low frequency
  - Standby Mode, mix of Idle and Backup Mode, peripheral running at low frequency, processor stopped waiting for an interrupt
  - Backup Mode, Main Power Supplies off, VDDBU powered by a battery

9.7 Periodic Interval Timer

- Includes a 20-bit Periodic Counter, with less than 1 µs accuracy
- Includes a 12-bit Interval Overlay Counter
- Real Time OS or Linux®/WindowsCE® compliant tick generator

9.8 Watchdog Timer

- 16-bit key-protected only-once-Programmable Counter
- Windowed, prevents the processor to be in a dead-lock on the watchdog access

9.9 Real-time Timer

- Real-time Timer with 32-bit free-running back-up counter
- Integrates a 16-bit programmable prescaler running on slow clock
- Alarm Register capable to generate a wake-up of the system through the Shutdown Controller

9.10 General-purpose Back-up Registers

- Four 32-bit backup general-purpose registers

9.11 Advanced Interrupt Controller

- Controls the interrupt lines (nIRQ and nFIQ) of the ARM Processor
- Thirty-two individually maskable and vectored interrupt sources
  - Source 0 is reserved for the Fast Interrupt Input (FIQ)
  - Source 1 is reserved for system peripherals (PIT, RTT, PMC, DBGU, etc.)
  - Programmable Edge-triggered or Level-sensitive Internal Sources
  - Programmable Positive/Negative Edge-triggered or High/Low Level-sensitive
- Three External Sources plus the Fast Interrupt signal
- 8-level Priority Controller
  - Drives the Normal Interrupt of the processor
  - Handles priority of the interrupt sources 1 to 31
  - Higher priority interrupts can be served during service of lower priority interrupt
- Vectoring
  - Optimizes Interrupt Service Routine Branch and Execution
  - One 32-bit Vector Register per interrupt source
  - Interrupt Vector Register reads the corresponding current Interrupt Vector
- Protect Mode
  - Easy debugging by preventing automatic operations when protect models are enabled
- Fast Forcing
  - Permits redirecting any normal interrupt source on the Fast Interrupt of the processor

9.12 Debug Unit

- Composed of two functions
  - Two-pin UART
  - Debug Communication Channel (DCC) support
- Two-pin UART
  - Implemented features are 100% compatible with the standard Atmel USART
  - Independent receiver and transmitter with a common programmable Baud Rate Generator
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
  - Support for two PDC channels with connection to receiver and transmitter
- Debug Communication Channel Support
  - Offers visibility of and interrupt trigger from COMMRX and COMMTX signals from the ARM Processor's ICE Interface

9.13 Chip Identification

- Chip ID:
  - 0x329AA3A0 for the SAM9XE512
  - 0x329A93A0 for the SAM9XE256
  - 0x329973A0 for the SAM9XE128
- JTAG ID: 05B1_C03F
- ARM926 TAP ID: 0x0792603F

10. Peripherals

10.1 User Interface

The Peripherals are mapped in the upper 256 Mbytes of the address space between the addresses 0xFFFA 0000 and 0xFFFC FFFF. Each User Peripheral is allocated 16 Kbytes of address space. A complete memory map is presented in Figure 8-1 on page 21.

10.2 Peripheral Identifier

The AT91SAM9XE128/256/512 embeds a wide range of peripherals. Table 10-1 defines the Peripheral Identifiers of the AT91SAM9XE128/256/512. A peripheral identifier is required for the control of the peripheral interrupt with the Advanced Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 10-1. AT91SAM9XE128/256/512 Peripheral Identifiers

Peripheral ID	Peripheral Mnemonic	Peripheral Name	External Interrupt
0	AIC	Advanced Interrupt Controller	FIQ
1	SYSC	System Controller Interrupt	
2	PIOA	Parallel I/O Controller A	
3	PIOB	Parallel I/O Controller B	
4	PIOC	Parallel I/O Controller C	
5	ADC	Analog-to-digital Converter	
6	US0	USART 0	
7	US1	USART 1	
8	US2	USART 2	
9	MCI	Multimedia Card Interface	
10	UDP	USB Device Port	
11	TWI0	Two Wire Interface 0	
12	SPI0	Serial Peripheral Interface 0	
13	SPI1	Serial Peripheral Interface1	
14	SSC	Synchronous Serial Controller	
15	-	Reserved	
16	-	Reserved	
17	TC0	Timer/Counter 0	
18	TC1	Timer/Counter 1	
19	TC2	Timer/Counter 2	
20	UHP	USB Host Port	
21	EMAC	Ethernet MAC	
22	ISI	Image Sensor Interface	
23	US3	USART 3	
24	US4	USART 4	
25	TWI1	Two Wire Interface 1	
26	TC3	Timer/Counter 3	
27	TC4	Timer/Counter 4	
28	TC5	Timer/Counter 5	
29	AIC	Advanced Interrupt Controller	IRQ0
30	AIC	Advanced Interrupt Controller	IRQ1
31	AIC	Advanced Interrupt Controller	IRQ2

Note: Setting AIC, SYSC, UHP, ADC and IRQ0-2 bits in the clock set/clear registers of the PMC has no effect. The ADC clock is automatically started for the first conversion. In Sleep Mode the ADC clock is automatically stopped after each conversion.

10.2.1 Peripheral Interrupts and Clock Control

10.2.1.1 System Interrupt

The System Interrupt in Source 1 is the wired-OR of the interrupt signals coming from:

- the SDRAM Controller
- the Debug Unit
- the Periodic Interval Timer
- the Real-time Timer
- the Watchdog Timer
- the Reset Controller
- the Power Management Controller
- Enhanced Embedded Flash Controller

The clock of these peripherals cannot be deactivated and Peripheral ID 1 can only be used within the Advanced Interrupt Controller.

10.2.1.2 External Interrupts

All external interrupt signals, i.e., the Fast Interrupt signal FIQ or the Interrupt signals IRQ0 to IRQ2, use a dedicated Peripheral ID. However, there is no clock control associated with these peripheral IDs.

10.3 Peripheral Signals Multiplexing on I/O Lines

The AT91SAM9XE128/256/512 features 3 PIO controllers, PIOA, PIOB, PIOC, which multiplex the I/O lines of the peripheral set.

Each PIO Controller controls up to 32 lines. Each line can be assigned to one of two peripheral functions, A or B. The multiplexing tables in the following paragraphs define how the I/O lines of the peripherals A and B are multiplexed on the PIO Controllers. The two columns “Function” and “Comments” have been inserted in this table for the user’s own comments; they may be used to track how pins are defined in an application.

Note that some peripheral function which are output only, might be duplicated within the both tables.

The column “Reset State” indicates whether the PIO Line resets in I/O mode or in peripheral mode. If I/O is mentioned, the PIO Line resets in input with the pull-up enabled, so that the device is maintained in a static state as soon as the reset is released. As a result, the bit corresponding to the PIO Line in the register PIO_PSR (Peripheral Status Register) resets low.

If a signal name is mentioned in the “Reset State” column, the PIO Line is assigned to this function and the corresponding bit in PIO_PSR resets high. This is the case of pins controlling memories, in particular the address lines, which require the pin to be driven as soon as the reset is released. Note that the pull-up resistor is also enabled in this case.

10.3.1 PIO Controller A Multiplexing

Table 10-2. Multiplexing on PIO Controller A

PIO Controller A						Application Usage	
I/O Line	Peripheral A	Peripheral B	Comments	Reset State	Power Supply	Function	Comments
PA0	SPI0_MISO	MCDB0		I/O	VDDIOP0		
PA1	SPI0_MOSI	MCCDB		I/O	VDDIOP0		
PA2	SPI0_SPCK			I/O	VDDIOP0		
PA3	SPI0_NPCS0	MCDB3		I/O	VDDIOP0		
PA4	RTS2	MCDB2		I/O	VDDIOP0		
PA5	CTS2	MCDB1		I/O	VDDIOP0		
PA6	MCDA0			I/O	VDDIOP0		
PA7	MCCDA			I/O	VDDIOP0		
PA8	MCCK			I/O	VDDIOP0		
PA9	MCDA1			I/O	VDDIOP0		
PA10	MCDA2	ETX2		I/O	VDDIOP0		
PA11	MCDA3	ETX3		I/O	VDDIOP0		
PA12	ETX0			I/O	VDDIOP0		
PA13	ETX1			I/O	VDDIOP0		
PA14	ERX0			I/O	VDDIOP0		
PA15	ERX1			I/O	VDDIOP0		
PA16	ETXEN			I/O	VDDIOP0		
PA17	ERXDV			I/O	VDDIOP0		
PA18	ERXER			I/O	VDDIOP0		
PA19	ETXCK			I/O	VDDIOP0		
PA20	EMDC			I/O	VDDIOP0		
PA21	EMDIO			I/O	VDDIOP0		
PA22	ADTRG	ETXER		I/O	VDDIOP0		
PA23	TWD0	ETX2		I/O	VDDIOP0		
PA24	TWCK0	ETX3		I/O	VDDIOP0		
PA25	TCLK0	ERX2		I/O	VDDIOP0		
PA26	TIOA0	ERX3		I/O	VDDIOP0		
PA27	TIOA1	ERXCK		I/O	VDDIOP0		
PA28	TIOA2	ECRS		I/O	VDDIOP0		
PA29	SCK1	ECOL		I/O	VDDIOP0		
PA30[1]	SCK2	RXD4		I/O	VDDIOP0		
PA31[1]	SCK0	TXD4		I/O	VDDIOP0		

Note: 1. Not available in the 208-lead PQFP package.

10.3.2 PIO Controller B Multiplexing

Table 10-3. Multiplexing on PIO Controller B

PIO Controller B					Application Usage		
I/O Line	**Peripheral A**	**Peripheral B**	**Comments**	**Reset State**	**Power Supply**	**Function**	**Comments**
PB0	SPI1_MISO	TIOA3		I/O	VDDIOP0		
PB1	SPI1_MOSI	TIOB3		I/O	VDDIOP0		
PB2	SPI1_SPCK	TIOA4		I/O	VDDIOP0		
PB3	SPI1_NPCS0	TIOA5		I/O	VDDIOP0		
PB4	TXD0			I/O	VDDIOP0		
PB5	RXD0			I/O	VDDIOP0		
PB6	TXD1	TCLK1		I/O	VDDIOP0		
PB7	RXD1	TCLK2		I/O	VDDIOP0		
PB8	TXD2			I/O	VDDIOP0		
PB9	RXD2			I/O	VDDIOP0		
PB10	TXD3	ISI_D8		I/O	VDDIOP1		
PB11	RXD3	ISI_D9		I/O	VDDIOP1		
PB12[1]	TWD1	ISI_D10		I/O	VDDIOP1		
PB13[1]	TWCK1	ISI_D11		I/O	VDDIOP1		
PB14	DRXD			I/O	VDDIOP0		
PB15	DTXD			I/O	VDDIOP0		
PB16	TK0	TCLK3		I/O	VDDIOP0		
PB17	TF0	TCLK4		I/O	VDDIOP0		
PB18	TD0	TIOB4		I/O	VDDIOP0		
PB19	RD0	TIOB5		I/O	VDDIOP0		
PB20	RK0	ISI_D0		I/O	VDDIOP1		
PB21	RF0	ISI_D1		I/O	VDDIOP1		
PB22	DSR0	ISI_D2		I/O	VDDIOP1		
PB23	DCD0	ISI_D3		I/O	VDDIOP1		
PB24	DTR0	ISI_D4		I/O	VDDIOP1		
PB25	RI0	ISI_D5		I/O	VDDIOP1		
PB26	RTS0	ISI_D6		I/O	VDDIOP1		
PB27	CTS0	ISI_D7		I/O	VDDIOP1		
PB28	RTS1	ISI_PCK		I/O	VDDIOP1		
PB29	CTS1	ISI_VSYNC		I/O	VDDIOP1		
PB30	PCK0	ISI_HSYNC		I/O	VDDIOP1		
PB31	PCK1	ISI_MCK		I/O	VDDIOP1		

Note: 1. Not available in the 208-lead PQFP package.

10.3.3 PIO Controller C Multiplexing

Table 10-4. Multiplexing on PIO Controller C

PIO Controller C					Application Usage		
I/O Line	**Peripheral A**	**Peripheral B**	**Comments**	**Reset State**	**Power Supply**	**Function**	**Comments**
PC0		SCK3	AD0	I/O	VDDIOP0		
PC1		PCK0	AD1	I/O	VDDIOP0		
PC2[1]		PCK1	AD2	I/O	VDDIOP0		
PC3[1]		SPI1_NPCS3	AD3	I/O	VDDIOP0		
PC4	A23	SPI1_NPCS2		A23	VDDIOM		
PC5	A24	SPI1_NPCS1		A24	VDDIOM		
PC6	TIOB2	CFCE1		I/O	VDDIOM		
PC7	TIOB1	CFCE2		I/O	VDDIOM		
PC8	NCS4/CFCS0	RTS3		I/O	VDDIOM		
PC9	NCS5/CFCS1	TIOB0		I/O	VDDIOM		
PC10	A25/CFRNW	CTS3		A25	VDDIOM		
PC11	NCS2	SPI0_NPCS1		I/O	VDDIOM		
PC12[1]	IRQ0	NCS7		I/O	VDDIOM		
PC13	FIQ	NCS6		I/O	VDDIOM		
PC14	NCS3/NANDCS	IRQ2		I/O	VDDIOM		
PC15	NWAIT	IRQ1		I/O	VDDIOM		
PC16	D16	SPI0_NPCS2		I/O	VDDIOM		
PC17	D17	SPI0_NPCS3		I/O	VDDIOM		
PC18	D18	SPI1_NPCS1		I/O	VDDIOM		
PC19	D19	SPI1_NPCS2		I/O	VDDIOM		
PC20	D20	SPI1_NPCS3		I/O	VDDIOM		
PC21	D21	EF100		I/O	VDDIOM		
PC22	D22	TCLK5		I/O	VDDIOM		
PC23	D23			I/O	VDDIOM		
PC24	D24			I/O	VDDIOM		
PC25	D25			I/O	VDDIOM		
PC26	D26			I/O	VDDIOM		
PC27	D27			I/O	VDDIOM		
PC28	D28			I/O	VDDIOM		
PC29	D29			I/O	VDDIOM		
PC30	D30			I/O	VDDIOM		
PC31	D31			I/O	VDDIOM		

Note: 1. Not available in the 208-lead PQFP package.

10.4 Embedded Peripherals

10.4.1 Serial Peripheral Interface

- Supports communication with serial external devices
  - Four chip selects with external decoder support allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
- Very fast transfers supported
  - Transfers with baud rates up to MCK
  - The chip select line may be left active to speed up transfers on the same device

10.4.2 Two-wire Interface

- Master, Multi-master and Slave modes supported
- General call supported in Slave mode
- Connection to PDC Channel

10.4.3 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB- or LSB-first
  - Optional break generation and detection
  - By 8 or by 16 oversampling receiver frequency
  - Hardware handshaking RTS-CTS
  - Receiver time-out and transmitter timeguard
  - Optional Multi-drop Mode with address generation and detection
  - Optional Manchester Encoding
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit

- IrDA modulation and demodulation
  - Communication at up to 115.2 Kbps
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo

10.4.4 Serial Synchronous Controller

- Provides serial synchronous communication links used in audio and telecom applications (with CODECs in Master or Slave Modes, I^2S, TDM Buses, Magnetic Card Reader, etc.)
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

10.4.5 Timer Counter

- Six 16-bit Timer Counter Channels
- Wide range of functions including:
  - Frequency Measurement
  - Event Counting
  - Interval Measurement
  - Pulse Generation
  - Delay Timing
  - Pulse Width Modulation
  - Up/down Capabilities
- Each channel is user-configurable and contains:
  - Three external clock inputs
  - Five internal clock inputs
  - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels

10.4.6 Multimedia Card Interface

- One double-channel Multimedia Card Interface
- Compatibility with MultiMedia Card Specification Version 2.2
- Compatibility with SD Memory Card Specification Version 1.0
- Compatibility with SDIO Specification Version V1.0.
- Cards clock rate up to Master Clock divided by 2
- Embedded power management to slow down clock rate when not used
- MCI has two slot, each supporting
  - One slot for one MultiMediaCard bus (up to 30 cards) or
  - One SD Memory Card
- Support for stream, block and multi-block data read and write

10.4.7 USB Host Port

- Compliance with Open HCI Rev 1.0 Specification
- Compliance with USB V2.0 Full-speed and Low-speed Specification
- Supports both Low-Speed 1.5 Mbps and Full-speed 12 Mbps devices
- Root hub integrated with two downstream USB ports in the 217-LFBGA package
- Two embedded USB transceivers
- Supports power management
- Operates as a master on the Matrix

10.4.8 USB Device Port

- USB V2.0 full-speed compliant, 12 MBits per second
- Embedded USB V2.0 full-speed transceiver
- Embedded 2,688-byte dual-port RAM for endpoints
- Suspend/Resume logic
- Ping-pong mode (two memory banks) for isochronous and bulk endpoints
- Eight general-purpose endpoints
  - Endpoint 0 and 3: 64 bytes, no ping-pong mode
  - Endpoint 1, 2, 6, 7: 64 bytes, ping-pong mode
  - Endpoint 4 and 5: 512 bytes, ping-pong mode
- Embedded pad pull-up

10.4.9 Ethernet 10/100 MAC

- Compatibility with IEEE Standard 802.3
- 10 and 100 MBits per second data throughput capability
- Full- and half-duplex operations
- MII or RMII interface to the physical layer
- Register Interface to address, data, status and control registers
- DMA Interface, operating as a master on the Memory Controller
- Interrupt generation to signal receive and transmit completion
- 128-byte transmit and 128-byte receive FIFOs
- Automatic pad and CRC generation on transmitted frames
- Address checking logic to recognize four 48-bit addresses
- Support promiscuous mode where all valid frames are copied to memory
- Support physical layer management through MDIO interface control of alarm and update time/calendar data in

10.4.10 Image Sensor Interface

- ITU-R BT. 601/656 8-bit mode external interface support
- Support for ITU-R BT.656-4 SAV and EAV synchronization
- Vertical and horizontal resolutions up to 2048 x 2048
- Preview Path up to 640*480
- Support for packed data formatting for YCbCr 4:2:2 formats

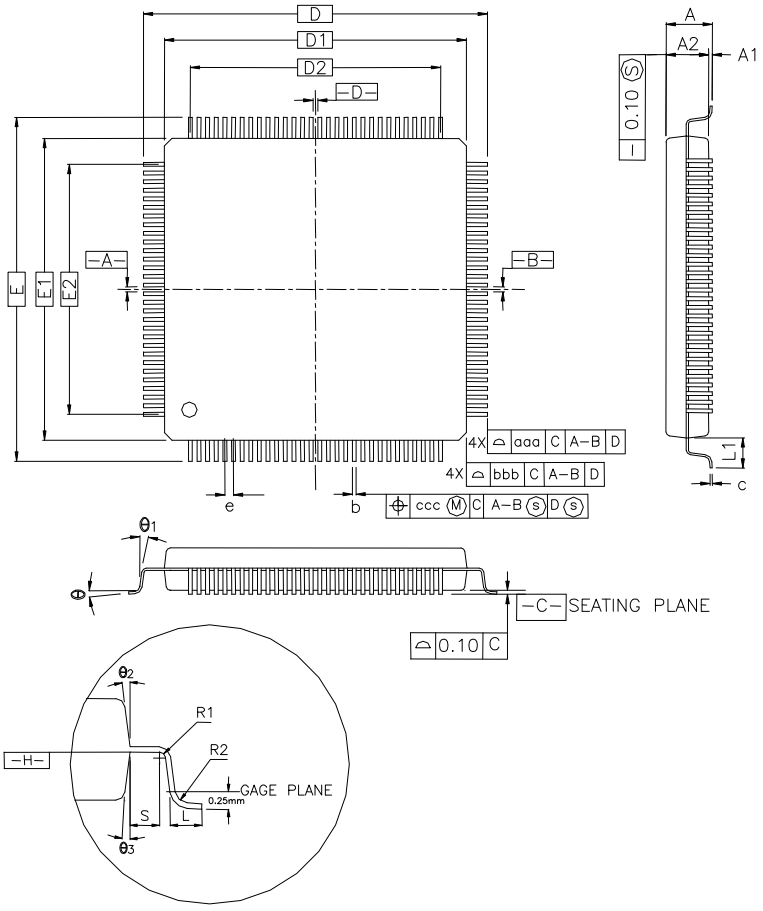
- Preview scaler to generate smaller size image

10.4.11 Analog-to-digital Converter

- 4-channel ADC
- 10-bit 312K samples/sec. Successive Approximation Register ADC
- -2/+2 LSB Integral Non Linearity, -1/+1 LSB Differential Non Linearity
- Individual enable and disable of each channel
- External voltage reference for better accuracy on low voltage inputs
- Multiple trigger source – Hardware or software trigger – External trigger pin – Timer Counter 0 to 2 outputs TIOA0 to TIOA2 trigger
- Sleep Mode and conversion sequencer – Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels
- Four analog inputs shared with digital signals

11. Package Drawings

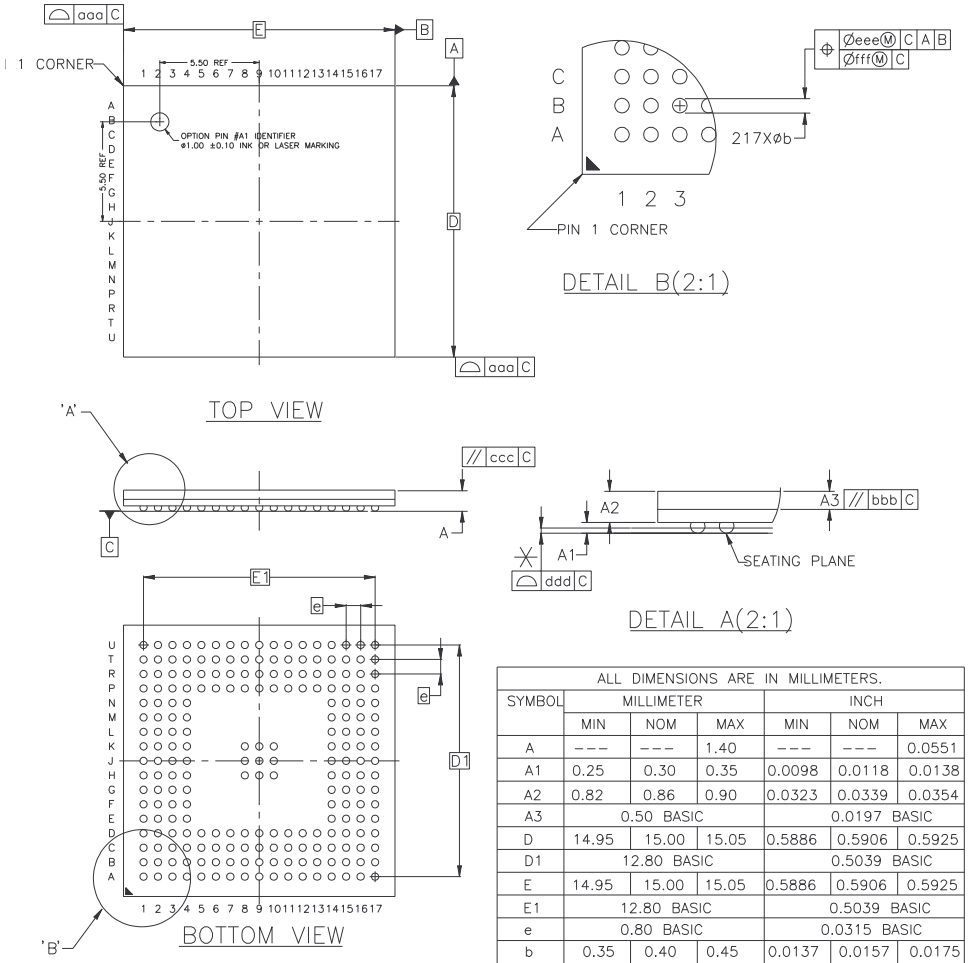
Figure 11-1. 208-pin PQFP Package Drawing



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	4.10	—	—	0.161
A_1	0.25	—	—	0.010	—	—
A_2	3.20	3.32	3.60	0.126	0.131	0.142
D	31.20 BASIC			1.228 BASIC		
D_1	28.00 BASIC			1.102 BASIC		
E	31.20 BASIC			1.228 BASIC		
E_1	28.00 BASIC			1.102 BASIC		
R_2	0.13	—	0.30	0.005	—	0.012
R_1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ_1	0°	—	—	0°	—	—
θ_2	8° REF			8° REF		
θ_3	8° REF			8° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L_1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	25.50			1.004		
E2	25.50			1.004		
TOLERANCES OF FORM AND POSITION						
aaa	0.25			0.010		
bbb	0.20			0.008		
ccc	0.08			0.003		

Figure 11-2. 217-ball LFBGA Package Drawing



ALL DIMENSIONS ARE IN MILLIMETERS.						
SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.0551
A1	0.25	0.30	0.35	0.0098	0.0118	0.0138
A2	0.82	0.86	0.90	0.0323	0.0339	0.0354
A3	0.50 BASIC			0.0197 BASIC		
D	14.95	15.00	15.05	0.5886	0.5906	0.5925
D1	12.80 BASIC			0.5039 BASIC		
E	14.95	15.00	15.05	0.5886	0.5906	0.5925
E1	12.80 BASIC			0.5039 BASIC		
e	0.80 BASIC			0.0315 BASIC		
b	0.35	0.40	0.45	0.0137	0.0157	0.0175
aaa	0.15			0.0059		
bbb	0.25			0.0098		
ccc	0.20			0.0079		
ddd	0.12			0.0047		
eee	0.15			0.0059		
fff	0.08			0.0031		

12. AT911SAM9XE128/256/512 Ordering Information

Table 12-1. AT91SAM9XE128/256/512 Ordering Information

Ordering Code	Package	Package Type	Temperature Operating Range
AT91SAM9XE128-QU	PQFP208	Green	Industrial -40°C to 85°C
AT91SAM9XE128-CU	BGA217	Green	
AT91SAM9XE256-QU	PQFP208	Green	Industrial -40°C to 85°C
AT91SAM9XE256-CU	BGA217	Green	
AT91SAM9XE512-QU	PQFP208	Green	Industrial -40°C to 85°C
AT91SAM9XE512-CU	BGA217	Green	

13. Revision History

Doc. Ref.	Comments	Change Request Ref.
6254BS	Removed 6.8, Slow CLock Selection (is shown in 27.5 of the full datasheet) Removed fomer Section 5.2 “Power Consumption”. Removed Clock Generator block diagram from Section 9.5 “Clock Generator” (is shown in Figure 27.1 of the full datasheet). Removed PMC block diagram from Section 9.6 “Power Management Controller” (is shown in Figure 28.1 of the full datasheet).	rfo
	“Features”, “Ethernet MAC 10/100 Base-T”, 128-byte FIFOs (typo corrected). Debug Unit (DBGU), added, Mode for general purpose6-2-wire UART serial communication Section 9.13 “Chip Identification”, SAM9XE512 chip ID is 0x329AA3A0. Table 3-1, “Signal Description List,””, comment column updated in certain instances and “PIO Controller - PIOA - PIOB - PIOC” , has a foot note added to its comments column. SHDWN is active Low. Section 5.1 “Power Supplies”, added “Caution: VDDCORE and VDDIO constraints..... Section 6. “I/O Line Considerations”, unneeded paragraphs removed. “Features”, “Additional Embedded Memories”Fast Read Time: 45 ns “Features”, “Four Universal Synchronous/Asynchronous Receiver Transmitters (USART)”, added Manchester Encoding/Decoding.	5800 5846 5800 rfo 5930
	Section 6.3 “Shutdown Logic Pins”, updated with external pull-up requirement.	rfo
6254AS	First issue.	

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