EPSON

# SRM2AW216LLBT1/7

## 2M-bit Static RAM

Super Low Voltage Operation Products

- Super Low Voltage Operation and Low Current Consumption
- Access Time 100ns (1.8V) / 70ns (2.2V)
- 131,072 Words x 16-bit Asynchronous
- Wide Temperature Range

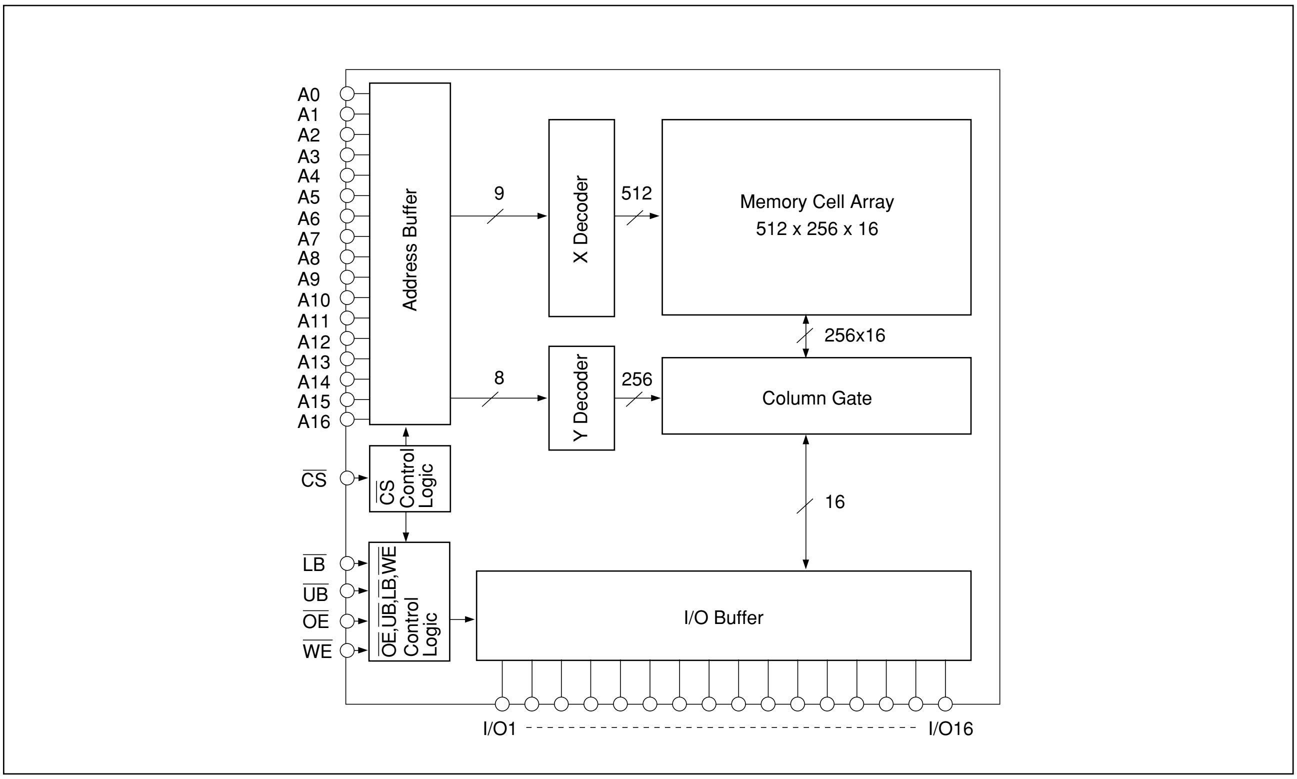
## ■ DESCRIPTION

The SRM2AW216LLBT1/7 is a 131,072 words x 16-bit asynchronous, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock and no refreshing circuit. It is possible to contorol the data width by the data byte control. 3-state output allows easy expansion of memory capacity. The temperature range of the SRM2AW216LLBT1/7 is from –40 to 85°C, and it is suitable for the industrial products.

## ■ FEATURES

- Fast Access time ........................ 100ns (at 1.8V) / 70ns (at 2.2V)
- Low supply current ..................... LL Version
- Completely static ........................ No clock required
- Supply voltage ............................ 1.8V to 3.0V
- 3-state output with wired-OR capability
- Non-volatile storage with back-up batteries
- Package ..................................... SRM2AW216LLBT TFBGA-48 pin (Tape CSP)

## ■ BLOCK DIAGRAM



## ■ PIN CONFIGURATION

TFBGA-48 pin

SRM2AW216LLBT

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| A | $\overline{LB}$ | $\overline{OE}$ | A0 | A1 | A2 | NC |
| B | I/O9 | $\overline{UB}$ | A3 | A4 | $\overline{CS}$ | I/O1 |
| C | I/O10 | I/O11 | A5 | A6 | I/O2 | I/O3 |
| D | $V_{SS}$ | I/O12 | NC | A7 | I/O4 | $V_{DD}$ |
| E | $V_{DD}$ | I/O13 | NC | A16 | I/O5 | $V_{SS}$ |
| F | I/O15 | I/O14 | A14 | A15 | I/O6 | I/O7 |
| G | I/O16 | NC | A12 | A13 | $\overline{WE}$ | I/O8 |
| H | NC | A8 | A9 | A10 | A11 | NC |

Top view (Looking through part)

## ■ PIN DESCRIPTION

| | |
|---|---|
| A0 to A16 | Address Input |
| $\overline{WE}$ | Write Enable |
| $\overline{OE}$ | Output Enable |
| $\overline{CS}$ | Chip Select |
| $\overline{LB}$ | LOWER Byte Enable |
| $\overline{UB}$ | UPPER Byte Enable |
| I/O1 to 16 | Data I/O |
| $V_{DD}$ | Power Supply (1.8V to 3.0V) |
| $V_{SS}$ | Power Supply (0V) |
| NC | No connection |

## ■ ABSOLUTE MAXIMUM RATINGS

($V_{SS}$=0V)

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | $V_{DD}$ | – 0.5 to 3.6 | V |
| Input voltage | $V_I$ | – 0.5 * to $V_{DD}$ + 0.3 | V |
| Input/Output voltage | $V_{I/O}$ | – 0.5 * to $V_{DD}$ + 0.3 | V |
| Power dissipation | $P_D$ | 0.5 | W |
| Operating temperature | $T_{opr}$ | – 40 to 85 | °C |
| Storage temperature | $T_{stg}$ | – 65 to 150 | °C |
| Soldering temperature and time | $T_{sol}$ | 260°C, 10s (at lead) | – |

* $V_I$,$V_{I/O}$ (Min.) = –2.0V (when pulse width is less than 50ns)

## ■ DC RECOMMENDED OPERATING CONDITIONS

(Ta = –40 to 85 °C)

| Parameter | Symbol | $V_{DD}$ = 1.8 to 2.2V | | | $V_{DD}$ = 2.2 to 3.0V | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Supply voltage | $V_{DD}$ | 1.8 | 2.0 | 2.2 | 2.2 | 2.5 | 3.0 | V |
| | $V_{SS}$ | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | V |
| Input voltege | $V_{IH}$ | 0.75$V_{DD}$ | – | $V_{DD}$+0.3 | 0.75$V_{DD}$ | – | $V_{DD}$+0.3 | V |
| | $V_{IL}$ | – 0.3* | – | 0.3 | – 0.3 * | – | 0.3 | V |

* if pulse width is less than 50ns it is – 2.0V

## ■ ELECTRICAL CHARACTERISTICS

### ● DC Electrical Characteristics

($V_{SS}$ =0V, Ta = –40 to 85 °C)

| Parameter | Symbol | Conditions | | $V_{DD}$ = 1.8 to 2.2V | | | $V_{DD}$ = 2.2 to 3.0V | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. *1 | Max. | Min. | Typ.*2 | Max. | |
| Input leakage current | $I_{LI}$ | $V_I$ = 0 to $V_{DD}$ | | –1.0 | – | 1.0 | –1.0 | – | 1.0 | µA |
| Output leakage current | $I_{LO}$ | $\overline{LB}$ and $\overline{UB}$ = $V_{IH}$ or $\overline{CS}$ = $V_{IH}$ or $\overline{WE}$ = $V_{IL}$ or $\overline{OE}$ = $V_{IH}$, $V_{I/O}$ = 0 to $V_{DD}$ | | –1.0 | – | 1.0 | –1.0 | – | 1.0 | µA |
| High level output voltage | $V_{OH}$ | VDD≥ 2.2V, $I_{OH}$ = -0.5mA | | – | – | – | 1.8 | – | – | V |
| | | $I_{OH}$ = –100µA | | $V_{DD}$–0.2 | – | – | $V_{DD}$–0.2 | – | – | |
| Low level output voltage | $V_{OL}$ | VDD≥ 2.2V, $I_{OL}$ = 0.5mA | | – | – | – | – | – | 0.4 | V |
| | | $I_{OL}$ = 100µA | | – | – | 0.2 | – | – | 0.2 | |
| Standby supply current | $I_{DDS}$ | $\overline{CS}$ = $V_{IH}$ | | – | – | 0.8 | – | – | 1.0 | mA |
| | $I_{DDS1}$ | $\overline{CS}$ ≥ $V_{DD}$ – 0.2V | LL –40 to 85 °C | – | – | 15 | – | – | 20 | µA |
| | | | LL –40 to 70 °C | – | – | 10 | – | – | 13.5 | |
| | | | LL –40 to 40 °C | – | – | 3.0 | – | – | 4.0 | |
| | | | LL 25 °C | – | 0.15 | 1.5 | – | 0.2 | 2.0 | |
| Average operating current | $I_{DDA}$ | $V_I$ = $V_{IL}$ or $V_{IH}$ $I_{I/O}$ = 0mA, tcyc = Min. | | – | 20 | 30 | – | 25 | 35 | mA |
| Operating Supply Current | $I_{DDA1}$ | $V_I$ = $V_{IL}$ or $V_{IH}$ $I_{I/O}$ = 0mA, tcyc = 1µs | | – | 2.5 | 4 | – | 3 | 5 | mA |
| | $I_{DDO}$ | $V_I$ = $V_{IL}$ or $V_{IH}$ $I_{I/O}$ = 0mA | | – | 2.5 | 4 | – | 3 | 5 | mA |

*1 : Typical values are measured at Ta = 25°C and VDD = 2.0V
*2 : Typical values are measured at Ta = 25°C and VDD = 2.5V

### ● Terminal Capacitance

(Ta = 25°C, f = 1MHz)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Address Capacitance | $C_{ADD}$ | $V_{ADD}$ = 0V | – | – | 8 | pF |
| Input Capacitance | $C_I$ | $V_I$ = 0V | – | – | 8 | pF |
| I/O Capacitance | $C_{I/O}$ | $V_{I/O}$ = 0V | – | – | 10 | pF |

Note : This parameter is made by the inspection data of sample, not of all products

## ● AC Electrical Characteristics

### ❍ Read Cycle

($V_{SS}$ = 0V, Ta = –40 to 85°C)

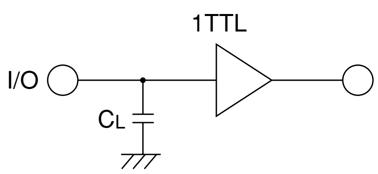
| Parameter | Symbol | Test Conditions | SRM2AW216LLBT1 | | SRM2AW216LLBT7 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | 1.8 to 2.2V | | 2.2 to 3.0V | | |
| | | | Min. | Max. | Min. | Max. | |
| Read cycle time | $t_{RC}$ | 1 | 100 | – | 70 | – | ns |
| Address access time | $t_{ACC}$ | 1 | – | 100 | – | 70 | ns |
| $\overline{CS}$ access time | $t_{ACS}$ | 1 | – | 100 | – | 70 | ns |
| $\overline{OE}$ access time | $t_{OE}$ | 1 | – | 60 | – | 40 | ns |
| $\overline{LB}$, $\overline{UB}$ access time | $t_{AB}$ | 1 | – | 60 | – | 40 | ns |
| $\overline{CS}$ output set time | $t_{CLZ}$ | 2 | 5 | – | 5 | – | ns |
| $\overline{CS}$ output floating | $t_{CHZ}$ | 2 | – | 40 | – | 30 | ns |
| $\overline{LB}$, $\overline{UB}$ output set time | $t_{BLZ}$ | 2 | 0 | – | 0 | – | ns |
| $\overline{LB}$, $\overline{UB}$ output floating | $t_{BHZ}$ | 2 | – | 40 | – | 30 | ns |
| $\overline{OE}$ output set time | $t_{OLZ}$ | 2 | 0 | – | 0 | – | ns |
| $\overline{OE}$ output floating | $t_{OHZ}$ | 2 | – | 40 | – | 30 | ns |
| Output hold time | $t_{OH}$ | 1 | 10 | – | 5 | – | ns |

### ❍ Write Cycle

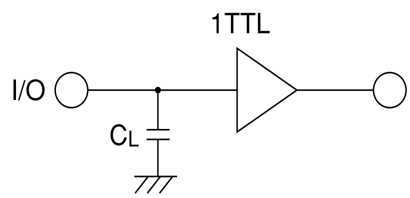
($V_{SS}$ = 0V, Ta = –40 to 85°C)

| Parameter | Symbol | Test Conditions | SRM2AW216LLBT1 | | SRM2AW216LLBT7 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | 1.8 to 2.2V | | 2.2 to 3.0V | | |
| | | | Min. | Max. | Min. | Max. | |
| Write cycle time | $t_{WC}$ | 1 | 100 | – | 70 | – | ns |
| Chip select time ($\overline{CS}$) | $t_{CW}$ | 1 | 85 | – | 60 | – | ns |
| Address enable time | $t_{AW}$ | 1 | 85 | – | 60 | – | ns |
| Address setup time | $t_{AS}$ | 1 | 0 | – | 0 | – | ns |
| Write pulse width | $t_{WP}$ | 1 | 80 | – | 55 | – | ns |
| $\overline{LB}$, $\overline{UB}$ select time | $t_{BW}$ | 1 | 85 | – | 60 | – | ns |
| Address hold time | $t_{WR}$ | 1 | 0 | – | 0 | – | ns |
| Data setup time | $t_{DW}$ | 1 | 50 | – | 35 | – | ns |
| Data hold time | $t_{DH}$ | 1 | 0 | – | 0 | – | ns |
| $\overline{WE}$ output floating | $t_{WHZ}$ | 2 | – | 40 | – | 30 | ns |
| $\overline{WE}$ output set time | $t_{OW}$ | 2 | 5 | – | 5 | – | ns |

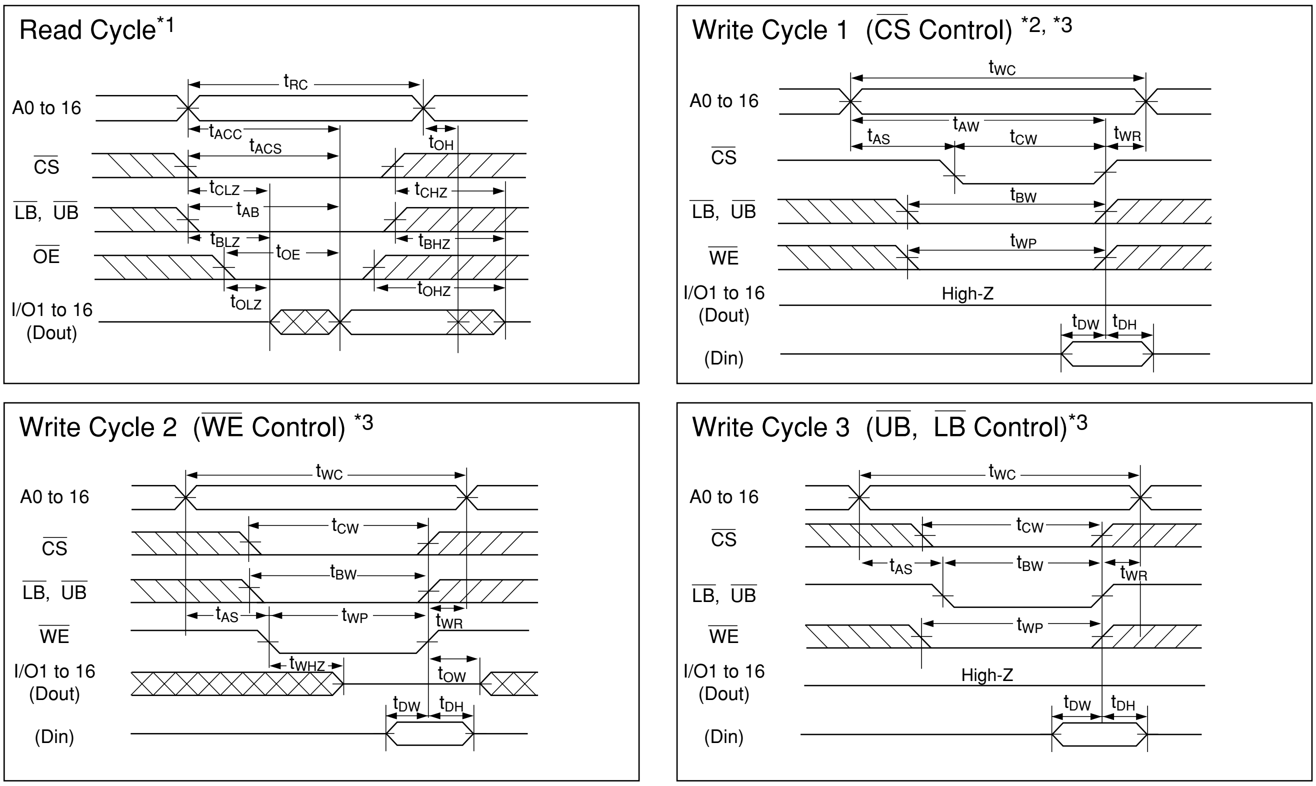
*1 Test Conditions
1. Input pulse level : 0.3V to 0.8$V_{DD}$(1.8V to 3.0V)
2. $t_r$ = $t_f$ = 5ns
3. Input and output timing reference levels :1/2$V_{DD}$(1.8V to 3.0V)
4. Output load : $C_L$ =50pF (Includes Jig Capacitance)




*2 Test Conditions
1. Input pulse level : 0.3V to 0.8$V_{DD}$(1.8V to 3.0V)
2. $t_r$ = $t_f$ = 5ns
3. Input timing reference levels :1/2$V_{DD}$(1.8V to 3.0V)
4. Output timing reference levels : ±200mV (The level changed from stable output voltage level)
5. Output load :$C_L$ = 5pF (Includes Jig Capacitance)



## ● Timing Chart




Note : *1 During read cycle time, $\overline{WE}$ is to be "High" level.
*2 In write cycle time that is controlled by $\overline{CS}$, output buffer is to be "Hi-Z" state even if $\overline{OE}$ is "Low" level.
*3 When output buffer is in output state, be careful that do not input the opposite signals to the output data.

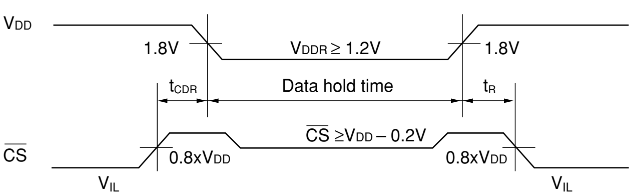
## ● DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

($V_{SS}$ = 0V, Ta = –40 to 85°C)

| Parameter | Symbol | Conditions | | | Min. | Typ.* | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDR}$ | | | | 1.2 | – | 3.0 | V |
| Data retention curren | $I_{DDR}$ | $V_{DDR}$ = 2.5V, $\overline{CS} \geq V_{DD} - 0.2V$ | LL | –40 to 85°C | – | – | 17 | µA |
| | | | | –40 to 70°C | – | – | 12 | |
| | | | | –40 to 40°C | – | – | 3.5 | |
| | | | | +25°C | – | 0.2 | 1.8 | |
| Data hold time | $t_{CDR}$ | | | | 0 | – | – | ns |
| Operation recovery time | $t_R$ | | | | 5 | – | – | ms |

* : Reference data at Ta = 25°C

### Data retention timing ($\overline{CS}$ Control)



## ■ FUNCTIONS

### ● Truth Table

| $\overline{CS}$ | $\overline{LB}$ | $\overline{UB}$ | $\overline{OE}$ | $\overline{WE}$ | I/O1 to 8 | I/O9 to 16 | MODE | $I_{DD}$ |
|---|---|---|---|---|---|---|---|---|
| H | X | X | X | X | High-Z | High-Z | Not Selected | $I_{DDS}$, $I_{DDS1}$ |
| L | H | H | X | X | High-Z | High-Z | Output disable | $I_{DDA}$, $I_{DDA1}$ |
| L | L | H | X | L | Data In | High-Z | Lower Byte Write | $I_{DDA}$, $I_{DDA1}$ |
| L | H | L | X | L | High-Z | Data In | Upper Byte Write | $I_{DDA}$, $I_{DDA1}$ |
| L | L | L | X | L | Data In | Data In | All Byte Write | $I_{DDA}$, $I_{DDA1}$ |
| L | L | H | L | H | DataOut | High-Z | Lower Byte Read | $I_{DDA}$, $I_{DDA1}$ |
| L | H | L | L | H | High-Z | DataOut | Upper Byte Read | $I_{DDA}$, $I_{DDA1}$ |
| L | L | L | L | H | Data Out | Data Out | All Byte Read | $I_{DDA}$, $I_{DDA1}$ |
| L | X | X | H | H | High-Z | High-Z | Output disable | $I_{DDA}$, $I_{DDA1}$ |

X : High or Low

### ● Reading data

It is possible to control the data width by $\overline{LB}$ and $\overline{UB}$ pins.

(1) Reading data from lower byte

Data is able to be read when the address is set while holding $\overline{CS}$ ="Low", $\overline{OE}$= "Low", $\overline{LB}$ ="Low" and $\overline{WE}$ = "High".

(2) Reading data from upper byte

Data is able to be read when the address is set while holding $\overline{CS}$ = "Low", $\overline{OE}$ = "Low", $\overline{UB}$ = "Low" and $\overline{WE}$ ="High".

(3) Reading data from both bytes

Data is able to be read when the address is set while holding $\overline{CS}$ = "Low", $\overline{OE}$ ="Low", $\overline{UB}$ ="Low", $\overline{LB}$ = "Low", and $\overline{WE}$ = "High"

Since I/O pins are in "Hi-Z" state when $\overline{OE}$ = "High", the data bus line can be used for any other objective, then access time is apparently able to be cut down.

### ● Writing data

(1) Writing data into lower byte

There are the following three ways of writing data into memory.

i) Hold $\overline{WE}$ = "Low", $\overline{UB}$ = "High" and $\overline{LB}$ = "Low", set address and give "Low" pulse to $\overline{CS}$.

ii) Hold $\overline{CS}$ = "Low", $\overline{UB}$ = "High" and $\overline{LB}$ = "Low", set address and give "Low" pulse to $\overline{WE}$.

iii) Hold $\overline{WE}$="Low", $\overline{CS}$ ="Low" and $\overline{UB}$ = "High", set address and give "Low" pulse to $\overline{LB}$.

Anyway, data on I/O pins are latched up into the memory cell during $\overline{CS}$ ="Low", $\overline{WE}$ ="Low", and $\overline{LB}$ = "Low".

(2) Writing data into upper byte

There are the following three ways of writing data into the memory.

i) Hold $\overline{WE}$ = "Low", $\overline{LB}$ = "High" and $\overline{UB}$ = "Low", set address and give "Low" pulse to $\overline{CS}$ .

ii) Hold $\overline{CS}$ = "Low", $\overline{LB}$ = "High" and $\overline{UB}$ = "Low", set address and give "Low" pulse to $\overline{WE}$.

iii) Hold $\overline{WE}$="Low", $\overline{CS}$="Low" and $\overline{LB}$ = "High", set address and give "Low" pulse to $\overline{UB}$.

Anyway, data on I/O pins are latched up into the memory cell during $\overline{CS}$ = "Low", $\overline{WE}$ = "Low", and $\overline{UB}$ = "Low".

(3)Writing data into both bytes

There are the following three ways of writing data into the memory.

i) Hold $\overline{WE}$ = "Low", $\overline{LB}$ and $\overline{UB}$ = "Low", set address and give "Low" pulse to $\overline{CS}$.

ii) Hold $\overline{CS}$ = "Low", $\overline{LB}$ and $\overline{UB}$ = "Low", set address and give "Low" pulse to $\overline{WE}$.

iii) Hold $\overline{WE}$="Low" and $\overline{CS}$ ="Low" , set address and give "Low" pulse to $\overline{LB}$ and $\overline{UB}$.

Anyway, data on I/O pins are latched up into the memory cell during $\overline{CS}$ = "Low" , $\overline{WE}$ = "Low", $\overline{UB}$ and $\overline{LB}$ = "Low".

As DATA I/O pins are in "Hi-Z" when $\overline{CS}$="High", $\overline{OE}$="High", or $\overline{LB}$ and $\overline{UB}$="High", the contention on the data bus can be avoided. But while I/O pins are in the output state, the data that is opposite to the output data should not be given

## ● Standby mode

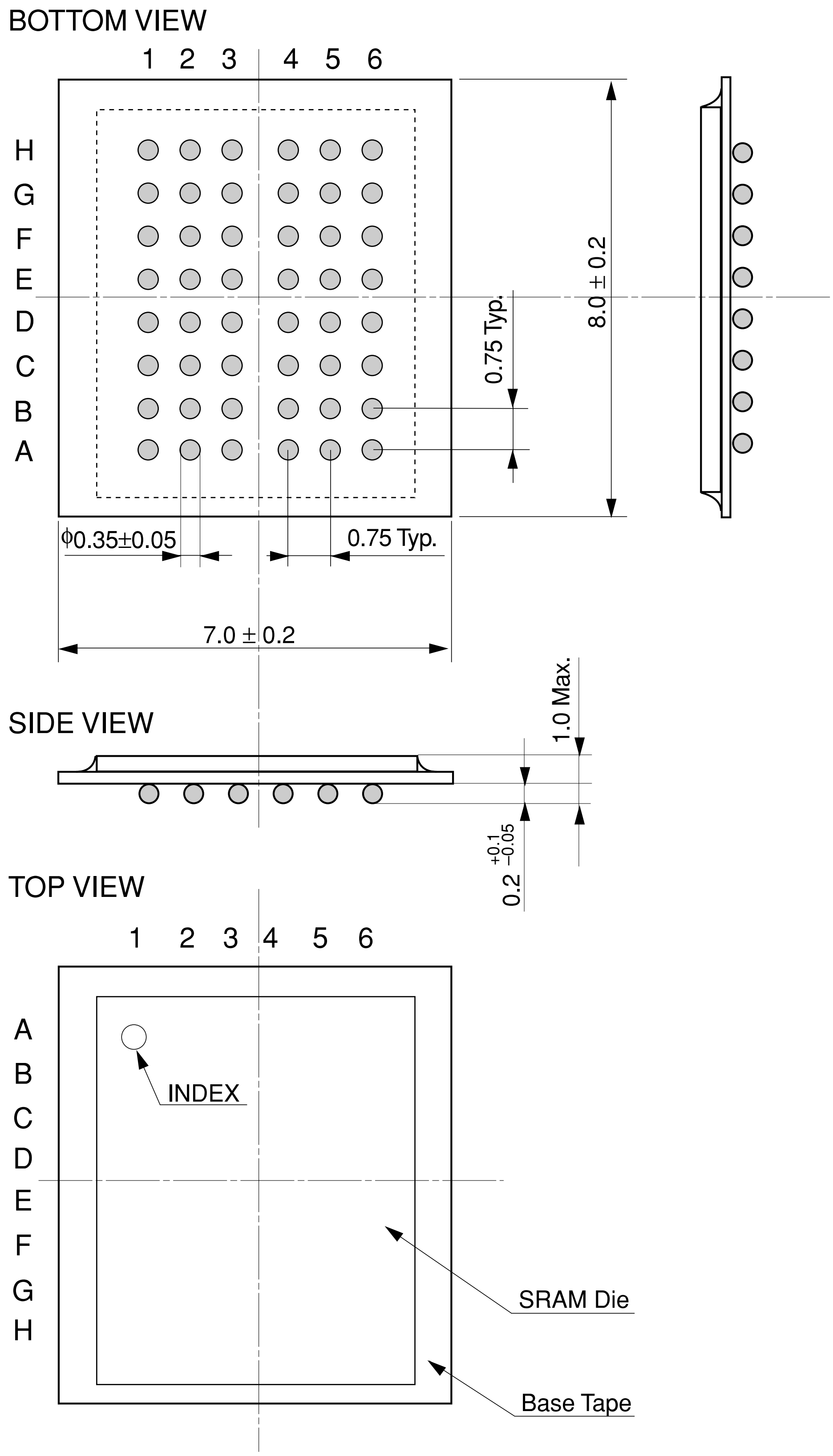
When $\overline{CS}$ is "High" , the chip is in the standby mode (only retaining data operation). In this case data I/O pins are Hi-Z, and all inputs of addresses, $\overline{WE}$, $\overline{OE}$, $\overline{UB}$, $\overline{LB}$, and data are inhibited. When $\overline{CS}$ is in the range over $V_{DD}$–0.2V, there is almost no current flow except through the high resistance parts of the memory.

## ● Data retention at low voltage

In case of the data retention in the stadby mode, the power supply can be gone down till the specified voltage. But it is impossible to write or read in this mode.

## ■ PACKAGE DIMENSIONS

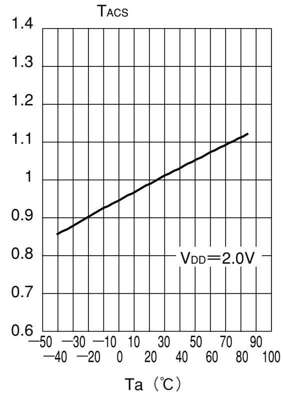
**TFBGA-48 pin**



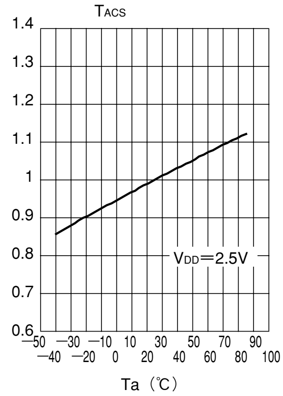

Unit : mm

## ■ CHARACTERICS CURVES

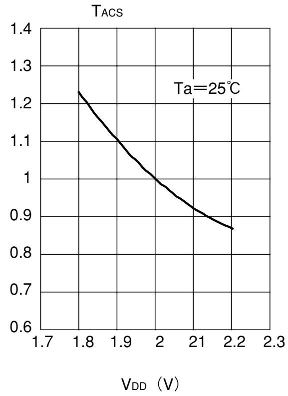
Normalized TACC–Ta (VDD=1.8～2.2V)



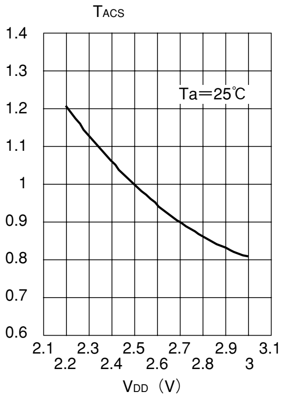

Normalized TACC–Ta (VDD=2.2～3.0V)



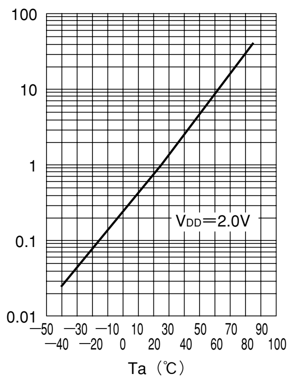

Normalized TACC–VDD (VDD=1.8～2.2V)



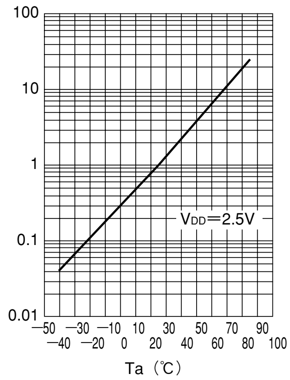

Normalized TACC–VDD (VDD=2.2～3.0V)



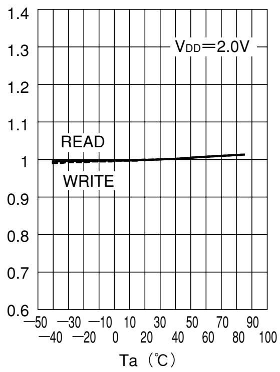

Normalize IDDS1–Ta (VDD=1.8～2.2V)



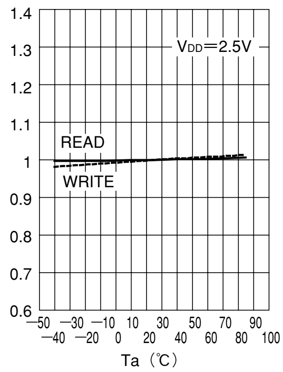

Normalize IDDS1–Ta (VDD=2.2～3.0V)



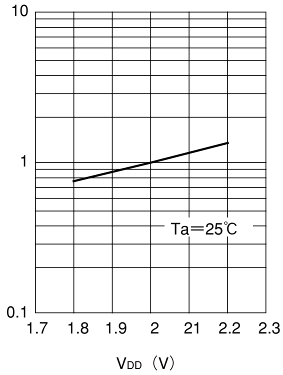

Normalized IDDA—Ta (VDD=1.8～2.2V)



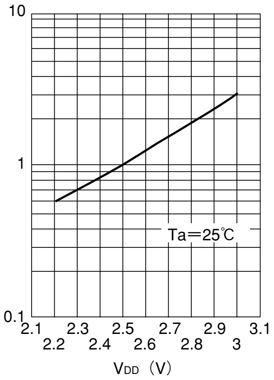

Normalized IDDA—Ta (2.2～3.0V)



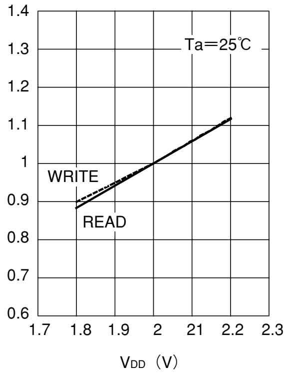

Normalized IDDS1—VDD (1.8～2.2V)



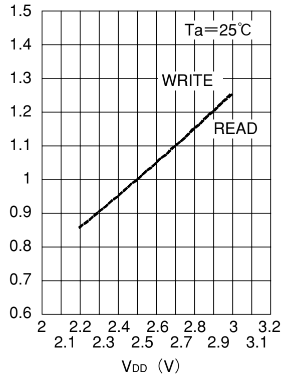

Normalized IDDS1—VDD (2.2～3.0V)



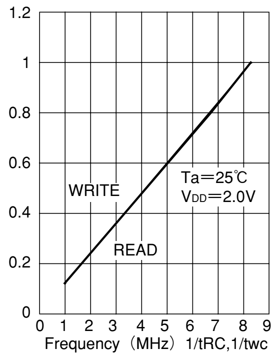

Normalized IDDA—VDD (VDD=1.8～2.2V)



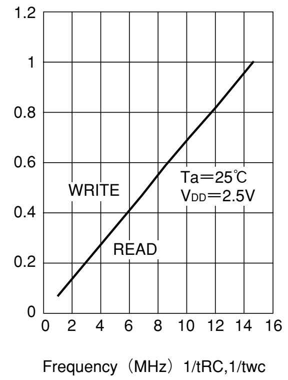

Normalized IDDA—VDD (VDD=2.2～3.0V)



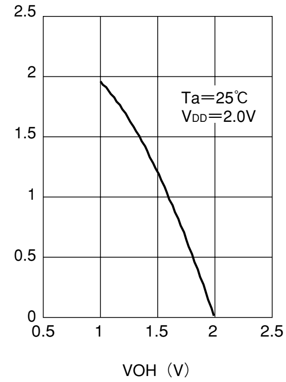
Normalized IDDA–Frequency（VDD=1.8～2.2V）



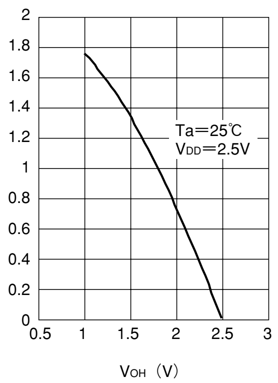

Normalized IDDA–Frequency（VDD=2.2～3.0V）



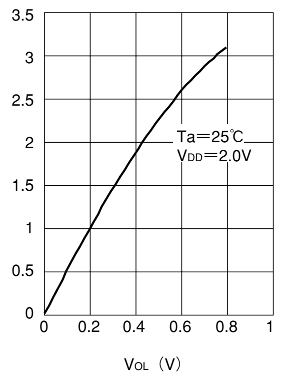

Normalized IOH–VOH（1.8～2.2V）



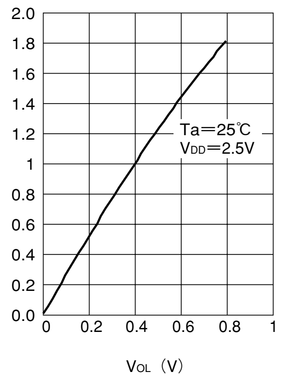

Normalized IOH–VOH（VDD=2.2～3.0V）



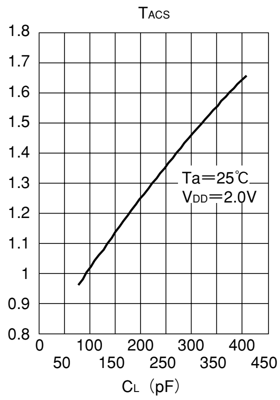

Normalized IOL–VOL（1.8～2.2V）



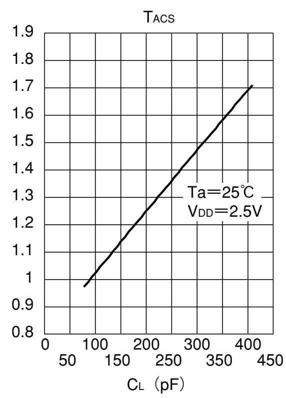

Normalized IOL–VOL（2.2～3.0V）




Normalized TACC–CL（1.8～2.2V）




Normalized TACC–CL（2.2～3.0V）



**SEIKO EPSON CORPORATION**
ELECTRONIC DEVICES MARKETING DIVISION
**IC Marketing & Engineering Group**

**ED International Marketing Department Europe & U.S.A.**
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone : 042-587-5812  FAX : 042-587-5564

**ED International Marketing Department Asia**
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone : 042-587-5814  FAX : 042-587-5110

■ EPSON Electronic Devices Website
**http://www.epson.co.jp/device/**

Revised JUNE, 2000 Printed in Japan Ⓣ
Rev.1.4