

**8 x 8-bit Parallel Multiplier****LMU557/558****FEATURES**

- ❑ 60 ns Worst-Case Multiply Time
- ❑ Low Power CMOS Technology
- ❑ Replaces Am25S557/558, 54S557/558
- ❑ Fully Combinatorial, No Clocks Required
- ❑ Two's Complement, Unsigned, or Mixed Operands
- ❑ Three-State Outputs
- ❑ Available Screened to MIL-STD-883, Class B
- ❑ Package Styles Available:
  - 40-pin Plastic DIP
  - 40-pin Sidebrazed, Hermetic DIP

**DESCRIPTION**

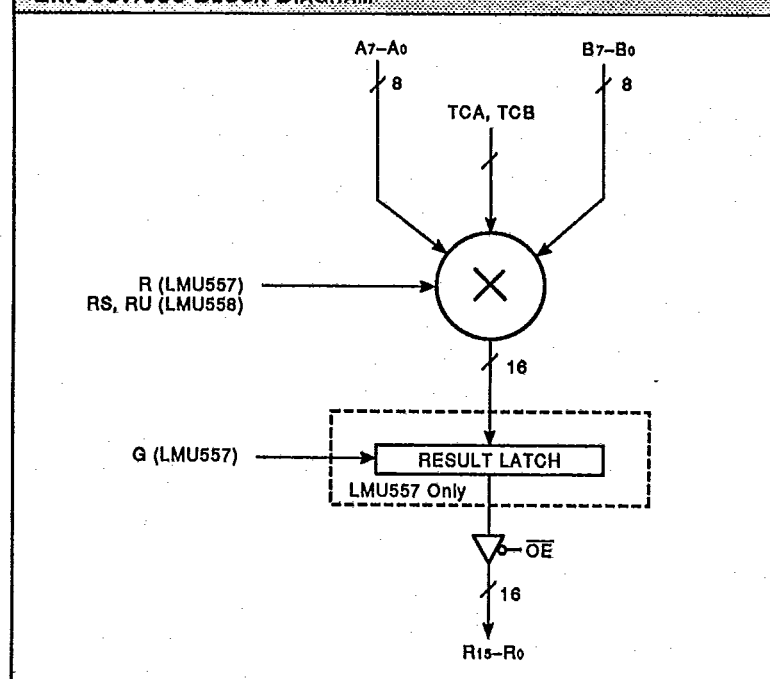
The LMU557 and LMU558 are 8-bit parallel multipliers with high speed and low power operation. They are pin for pin equivalents with 54S557 and 54S558 type multipliers. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

Both the LMU557 and LMU558 produce the 16-bit product of two 8-bit signed or unsigned numbers in a single unlocked operation. Assertion of control inputs TCA and TCB indicate that the corresponding input value is in two's complement notation.

Provision is made for proper rounding for any combination of signed or unsigned inputs. The RU input to the LMU557 causes the product to be rounded to 8 bits of precision for unsigned or mixed mode multiplication. For multiplication of two signed operands, the RS input is used for rounding, and the most significant bit of the product is discarded. [It will be identical to the sign bit for all except the  $(-2^8) \cdot (-2^8)$  case, which will cause overflow if the result MSB is not considered.]

The LMU558 internally produces the RU and RS controls from a single round input, denoted R. With R asserted, RS rounding occurs if either TCA or TCB is asserted, while RU rounding is implemented for TCA and TCB not asserted. This implementation frees a pin for control of the transparent output latch in the LMU557 via the G input.

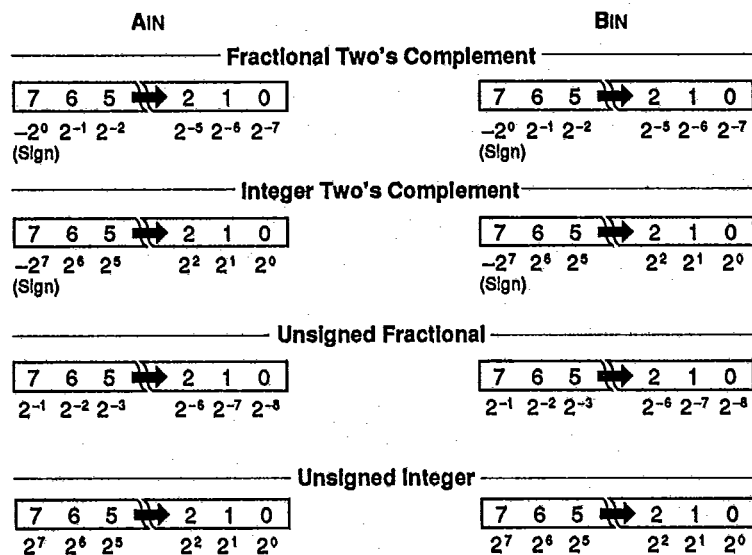
Both the LMU557 and LMU558 offer three-state output buffers controlled by the  $\overline{OE}$  input. The LMU557 has a 16-bit transparent latch between the multiplier array and the output drivers for flexibility in implementing pipelined systems. This latch is transparent when G is high, and holds its state when G is low. In addition, both polarities of the result MSB (R15) are available as separate output pins to allow simple expansion to longer word lengths in signed multiplication.

**LMU557/558 BLOCK DIAGRAM****LOGIC**

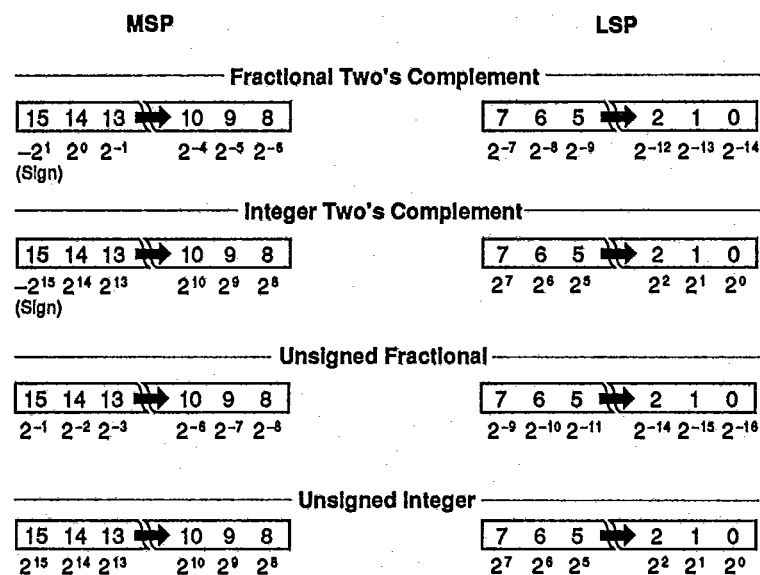
DEVICES INCORPORATED

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# INPUT FORMATS



# OUTPUT FORMATS



**MAXIMUM RATINGS** Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature .....	-65°C to +150°C
Operating ambient temperature .....	-55°C to +125°C
V <sub>CC</sub> supply voltage with respect to ground .....	-0.5 V to +7.0 V
Input signal with respect to ground .....	-3.0 V to +7.0 V
Signal applied to high impedance output .....	-3.0 V to +7.0 V
Output current into low outputs .....	25 mA
Latchup current .....	> 400 mA

**OPERATING CONDITIONS** To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V <sub>CC</sub> ≤ 5.25 V
Active Operation, Military	-55°C to +125°C	4.50 V ≤ V <sub>CC</sub> ≤ 5.50 V

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**ELECTRICAL CHARACTERISTICS** Over Operating Conditions

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -2.0 mA	3.5			V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8.0 mA			0.5	V
V <sub>IH</sub>	Input High Voltage		2.0		V <sub>CC</sub>	V
V <sub>IL</sub>	Input Low Voltage	(Note 3)	0.0		0.8	V
I <sub>IX</sub>	Input Current	Ground ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>			±20	μA
I <sub>OZ</sub>	Output Leakage Current	Ground ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub>			±20	μA
I <sub>OS</sub>	Output Short Current	V <sub>OUT</sub> = Ground, V <sub>CC</sub> = Max (Notes 4, 8)			-250	mA
I <sub>CC1</sub>	V <sub>CC</sub> Current, Dynamic	(Notes 5, 6)		17	35	mA
I <sub>CC2</sub>	V <sub>CC</sub> Current, Quiescent	(Note 7)			1.0	mA

## SWITCHING CHARACTERISTICS

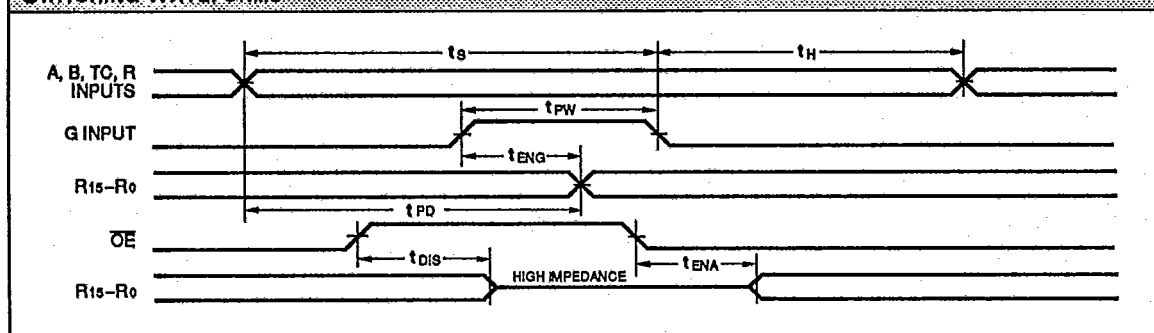
### COMMERCIAL OPERATING RANGE (0°C to +70°C) Notes 9, 10 (ns)

Symbol Parameter		LMU557/558-60	
		Min	Max
t <sub>PD</sub>	A, B, TC, R Inputs to R15-R8, R15		60
t <sub>PD</sub>	A, B, TC, R Inputs to R7-R0		55
t <sub>ENG</sub>	G Enable to Result		30
t <sub>ENA</sub>	Output Enable Time (Note 11)		25
t <sub>DIS</sub>	Output Disable Time (Note 11)		20
t <sub>PW</sub>	G Pulse Width	15	
t <sub>H</sub>	G to A, B, TC, R Hold Time	0	
t <sub>S</sub>	A, B, TC, R Inputs to G Setup Time	45	

### MILITARY OPERATING RANGE (-55°C to +125°C) Notes 9, 10 (ns)

Symbol Parameter		LMU557/558-70	
		Min	Max
t <sub>PD</sub>	A, B, TC, R Inputs to R15-R8, R15		70
t <sub>PD</sub>	A, B, TC, R Inputs to R7-R0		60
t <sub>ENG</sub>	G Enable to Result		35
t <sub>ENA</sub>	Output Enable Time (Note 11)		30
t <sub>DIS</sub>	Output Disable Time (Note 11)		25
t <sub>PW</sub>	G Pulse Width	20	
t <sub>H</sub>	G to A, B, TC, R Hold Time	0	
t <sub>S</sub>	A, B, TC, R Inputs to G Setup Time	55	

## SWITCHING WAVEFORMS



## NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above VCC will be clamped beginning at -0.6 V and VCC + 0.6 V. The device can withstand indefinite operation with inputs in the range of -3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs

C = capacitive load per output

V = supply voltage

F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of VCC or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except tEN/tDIS test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified IOL and IOH plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 μF ceramic capacitor should be installed between VCC and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device VCC and the tester common, and device ground and tester common.

b. Ground and VCC supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and VCC noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

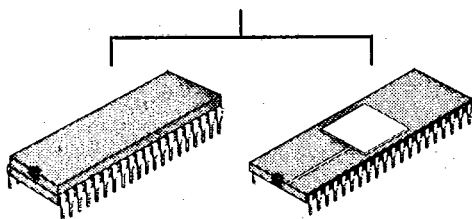
11. Transition is measured ±200 mV from steady-state voltage with specified loading.

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**ORDERING INFORMATION**

40-pin

A0	1	40	TCA
A1	2	39	R0
A2	3	38	R1
A3	4	37	R2
A4	5	36	R3
A5	6	35	R4
A6	7	34	R5
A7	8	33	R6
RS/R	9	32	R7
VCC	10	31	R8
RU/G	11	30	GND
B0	12	29	R9
B1	13	28	R10
B2	14	27	R11
B3	15	26	R12
B4	16	25	R13
B5	17	24	R14
B6	18	23	R15
B7	19	22	R15
TCB	20	21	OE



Speed	Plastic DIP (P3)	Sidebrazed Hermetic DIP (D3)
<b>0°C to +70°C — COMMERCIAL SCREENING</b>		
60 ns	LMU557PC60 or LMU558PC60	LMU557DC60 or LMU558DC60
<b>-55°C to +125°C — COMMERCIAL SCREENING</b>		
70 ns		LMU557DM70 or LMU558DM70
<b>-55°C to +125°C — EXTENDED SCREENING</b>		
70 ns		LMU557DME70 or LMU558DME70
<b>-55°C to +125°C — MIL-STD-883 COMPLIANT</b>		
70 ns		LMU557DMB70 or LMU558DMB70