REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
E	Convert to military drawing format. Add burn-in condition C. Add vendor CAGE 50088. Editorial changes throughout. Change code ident. no. to 67268.	88-08-25	Michael A. Frye
F	Add device type 03. Update boilerplate. Editorial changes throughout. – tvn	99-04-26	Monica L. Poelking

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED

REV																			
SHEET																			
REV	F	F																	
SHEET	15	16																	

REV STATUS OF SHEETS	REV	F	F	F	F	F	F	F	F	F	F	F	F	F
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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Michael A. Frye

DRAWING APPROVAL DATE
77-05-17

REVISION LEVEL
F

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, 4-BIT MICROPROCESSOR, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**77007**

SHEET 1 OF 16

DSCC FORM 2233
APR 97

5962-E160-99

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1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

77007	01	X	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	2901A	4-bit bipolar microprocessor
02	2901	4-bit bipolar microprocessor
03	2901	4-bit bipolar microprocessor

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line package
Z	See figure 1	42	Flat package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC}) ..... -0.5 V dc to +6.3 V dc
Input voltage range..... -0.5 V to 5.5 V
Input current ..... -30 mA to +5 mA
Output current (into outputs) ..... 30 mA
Maximum junction temperature (T_J) ..... +150°C
Storage temperature range ..... -65°C to +150°C
Lead temperature (soldering, 5 seconds) ..... +270°C
Maximum power dissipation (P_D) ..... 1.54 W
Thermal resistance, junction-to-case (Θ_{JC})
Case Q ..... See MIL-PRF-38535
Case Z ..... 0.04°C/mW

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1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc
Supply voltage (V_{SS})	0.0 V dc
Applied voltage to outputs for high state	-0.5 V to V_{CC} maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.7 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Minimum read-modify-write cycle	120 ns
Minimum clock low time (t_{PWL})	30 ns
Minimum clock high time (t_{PWH})	30 ns
Minimum clock period (t_{CP})	120 ns
Maximum clock frequency to shift Q register (f_C)	8.3 MHz

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
High level output voltage, Y_0, Y_1, Y_2, Y_3, $\overline{G}$	V_{OH1}	V_{CC} = 4.5 V V_{IH} = 2.0 V V_{IL} = 0.7 V	I_{OH} = -1.6 mA	All	1, 2, 3	2.4		V
High level output voltage, C_{n+4}	V_{OH2}		I_{OH} = -1.0 mA			2.4		
High level output voltage, OVR, $\overline{P}$	V_{OH3}		I_{OH} = -800 µA			2.4		
High level output voltage, F_3, RAM_0, RAM_3, Q_0, Q_3	V_{OH4}		I_{OH} = -600 µA			2.4		
Low level output voltage, Y_0, Y_1, Y_2, Y_3, $\overline{G}$	V_{OL1}	V_{CC} = 4.5 V V_{IH} = 2.0 V V_{IL} = 0.7 V	I_{OL} = 16 mA	All	1, 2, 3		0.5	V
Low level output voltage, C_{n+4}, F = 0	V_{OL2}		I_{OL} = 10 mA				0.5	
Low level output voltage, OVR, $\overline{P}$	V_{OL3}		I_{OL} = 8 mA				0.5	
Low level output voltage, F_3, RAM_0, RAM_3, Q_0, Q_3	V_{OL4}		I_{OL} = 6 mA				0.5	
Input clamp voltage	V_I	V_{CC} = 4.5 V, I_I = -18 mA		All	1		-1.5	V
Output leakage current for F = 0 output	I_{CEX}	V_{CC} = 4.5 V, V_{OH} = 5.5 V V_{IH} = 2.0 V, V_{IL} = 0.7 V		All	1, 2, 3		250	µA
Short circuit output current 1/	I_{OS}	V_{CC} = 5.5 V		All	1, 2, 3	-15	-85	mA
Low level input current, Clock, $\overline{OE}$	I_{IL1}	V_{CC} = 5.5 V, V_{IN} = 0.5 V		All	1, 2, 3		-0.36	mA
Low level input current, A_0, A_1, A_2, A_3	I_{IL2}						-0.36	
Low level input current, B_0, B_1, B_2, B_3	I_{IL3}						-0.36	
Low level input current, D_0, D_1, D_2, D_3	I_{IL4}						-0.72	
Low level input current, I_0, I_1, I_2, I_6, I_8	I_{IL5}						-0.36	
Low level input current, I_3, I_4, I_5, I_7	I_{IL6}						-0.72	
Low level input current, RAM_0, RAM_3, Q_0, Q_3 (At high Z state) 2/	I_{IL7}						-0.8	
Low level input current, C_n	I_{IL8}						-3.6	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
High level input current, Clock, $\overline{OE}$	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.7 V		All	1, 2, 3		20	µA
High level input current, A_0, A_1, A_2, A_3	I_{IH2}						20	
High level input current, B_0, B_1, B_2, B_3	I_{IH3}						20	
High level input current, D_0, D_1, D_2, D_3	I_{IH4}						40	
High level input current, I_0, I_1, I_2, I_6, I_8	I_{IH5}						20	
High level input current, I_3, I_4, I_5, I_7	I_{IH6}						40	
High level input current, RAM_0, RAM_3, Q_0, Q_3 (At high Z state) 2/	I_{IH7}						100	
High level input current, C_n	I_{IH8}						200	
Supply current	I_{CC}	V_{CC} = 5.5 V		All	1, 2, 3		280	mA
Input current at maximum input voltage	I_I	V_{CC} = 5.5 V, V_I = 5.5 V		All	1, 2, 3		1	mA
Off-state (high Z) output current, Y_0, Y_1, Y_2, Y_3	I_{OZH1}	V_{CC} = 5.5 V	V_{OUT} = 2.4 V	All	1, 2, 3		50	µA
	I_{OZL1}		V_{OUT} = 0.5 V				-50	
Off-state (high Z) output current, RAM_0, RAM_3, Q_0, Q_3 2/	I_{OZH2}		V_{OUT} = 2.4 V				100	
	I_{OZL2}		V_{OUT} = 0.5 V				-800	
Propagation delay time, clock to Y 3/	t_{CY}	V_{CC} = 4.5 V and 5.5 V C_L = 15 Pf R_L = 470Ω (at F = 0) R = 5 kΩ		01, 03	9, 10, 11		65	ns
				02			125	
Propagation delay time, clock to F_3	t_{CF3}			01, 03	9, 10, 11		65	ns
				02			95	
Propagation delay time, clock to C_{n+4}	t_{CC4}			01, 03	9, 10, 11		65	ns
				02			110	
Propagation delay time, clock to $\overline{G}$, $\overline{P}$	t_{CGP}			01, 03	9, 10, 11		55	ns
				02			110	
Propagation delay time, clock to F = 0	t_{CF0}			01, 03	9, 10, 11		85	ns
				02			120	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Propagation delay time, clock to OVR	t_{COV}	V_{CC} = 4.5 V and 5.5 V C_L = 15 pF R_L = 470Ω (at F = 0) R = 5 kΩ	01, 03	9, 10, 11		75	ns
			02			105	
Propagation delay time, clock to RAM	t_{CRM}		01, 03	9, 10, 11		85	ns
			02			115	
Propagation delay time, clock to Q	t_{CQ}		01, 03	9, 10, 11		35	ns
			02			65	
Propagation delay time, A, B to Y	t_{PA1}		01, 03	9, 10, 11		85	ns
			02			120	
Propagation delay time, A, B to F_3	t_{PA2}		01, 03	9, 10, 11		85	ns
			02			95	
Propagation delay time, A, B to C_{n+4}	t_{PA3}		01, 03	9, 10, 11		80	ns
			02			90	
Propagation delay time, A, B to $\overline{G}$, $\overline{P}$	t_{PA4}		01, 03	9, 10, 11		70	ns
			02			90	
Propagation delay time, A, B to F = 0	t_{PA5}		01, 03	9, 10, 11		100	ns
			02			120	
Propagation delay time, A, B to OVR	t_{PA6}		All	9, 10, 11		90	ns
Propagation delay time, A, B to RAM	t_{PA7}		01, 03	9, 10, 11		100	ns
			02			120	
Propagation delay time, D to Y	t_{PD1}		01, 03	9, 10, 11		50	ns
			02			110	
Propagation delay time, D to F_3	t_{PD2}		01, 03	9, 10, 11		50	ns
			02			80	
Propagation delay time, D to C_{n+4}	t_{PD3}		01, 03	9, 10, 11		50	ns
			02			75	
Propagation delay time, D to $\overline{G}$, $\overline{P}$	t_{PD4}		01, 03	9, 10, 11		40	ns
			02			75	
Propagation delay time, D to F = 0	t_{PD5}		01, 03	9, 10, 11		65	ns
			02			110	
Propagation delay time, D to OVR	t_{PD6}		01, 03	9, 10, 11		60	ns
			02			65	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Propagation delay time, D to RAM	t_{PD7}	V_{CC} = 4.5 V and 5.5 V C_L = 15 pF R_L = 470Ω (at F = 0) R = 5 kΩ	01, 03	9, 10, 11		70	ns
			02			105	
Propagation delay time, C_n to Y	t_{PC1}		01, 03	9, 10, 11		45	ns
			02			60	
Propagation delay time, C_n to F_3	t_{PC2}		01, 03	9, 10, 11		45	ns
			02			40	
Propagation delay time, C_n to C_{n+4}	t_{PC3}		All	9, 10, 11		30	ns
Propagation delay time, C_n to F = 0	t_{PC5}		01, 03	9, 10, 11		55	ns
			02			55	
Propagation delay time, C_n to OVR	t_{PC6}		01, 03	9, 10, 11		35	ns
			02			45	
Propagation delay time, C_n to RAM	t_{PC7}		01, 03	9, 10, 11		55	ns
			02			60	
Propagation delay time, I_0, I_1, I_2 to Y	t_{PI1}		01, 03	9, 10, 11		60	ns
			02			90	
Propagation delay time, I_0, I_1, I_2 to F_3	t_{PI2}		01, 03	9, 10, 11		60	ns
			02			70	
Propagation delay time, I_0, I_1, I_2 to C_{n+4}	t_{PI3}		01, 03	9, 10, 11		55	ns
			02			70	
Propagation delay time, I_0, I_1, I_2 to $\overline{G}$, $\overline{P}$	t_{PI4}		01, 03	9, 10, 11		50	ns
			02			70	
Propagation delay time, I_0, I_1, I_2 to F = 0	t_{PI5}		01, 03	9, 10, 11		75	ns
			02			85	
Propagation delay time, I_0, I_1, I_2 to OVR	t_{PI6}		01, 03	9, 10, 11		70	ns
			02			70	
Propagation delay time, I_0, I_1, I_2 to RAM	t_{PI7}		01, 03	9, 10, 11		80	ns
			02			85	
Propagation delay time, I_3, I_4, I_5 to Y	t_{PJ1}		01, 03	9, 10, 11		60	ns
			02			75	
Propagation delay time, I_3, I_4, I_5 to F_3	t_{PJ2}		01, 03	9, 10, 11		60	ns
			02			60	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Propagation delay time, I_3, I_4, I_5 to C_{n+4}	t_{PJ3}	V_{CC} = 4.5 V and 5.5 V C_L = 15 pF R_L = 470Ω (at F = 0) R = 5 kΩ	01, 03	9, 10, 11		60	ns
			02			65	
Propagation delay time, I_3, I_4, I_5 to $\overline{G}$, $\overline{P}$	t_{PJ4}		01, 03	9, 10, 11		55	ns
			02			65	
Propagation delay time, I_3, I_4, I_5 to F = 0	t_{PJ5}		01, 03	9, 10, 11		75	ns
			02			75	
Propagation delay time, I_3, I_4, I_5 to OVR	t_{PJ6}		01, 03	9, 10, 11		70	ns
			02			65	
Propagation delay time, I_3, I_4, I_5 to RAM	t_{PJ7}		All	9, 10, 11		80	ns
Propagation delay time, I_6, I_7, I_8 to Y	t_{PJ8}		01	9, 10, 11		35	ns
			02			60	
			03			50	
Propagation delay time, I_6, I_7, I_8 to RAM	t_{PJ9}		01	9, 10, 11		35	ns
			02			35	
			03			50	
Propagation delay time, I_6, I_7, I_8 to Q	t_{PJ0}		All	9, 10, 11		35	ns
Propagation delay time, $\overline{OE}$ enable to Y	t_{POY1}		All	9, 10, 11		40	ns
Propagation delay time, $\overline{OE}$ disable to Y	t_{POY2}		All	9, 10, 11		25	ns
Propagation delay time, A bypassing ALU (I = 2xx) to Y	t_{ABY}		01, 03	9, 10, 11		50	ns
			02			65	
Setup time, A, B source 4/	t_{SAB}	5/	All	9, 10, 11	6/		ns
Setup time, B dest. 4/	t_{SBD}	All setup and hold times are relative to the clock positive going edge. V_{CC} = 4.5 V and 5.5 V C_L = 15 pF R_L = 470Ω (at F = 0) R = 5 kΩ	01	9, 10, 11	7/		ns
			02		7/		
			03		7/		
Setup time, D	t_{SD}		01, 03	9, 10, 11	75		ns
			02		110		
Setup time, C_n	t_{SC}		01, 03	9, 10, 11	60		ns
			02		60		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Setup time, I_0, I_1, I_2	t_{SI0}	5/ All setup and hold times are relative to the clock positive going edge. V_{CC} = 4.5 V and 5.5 V C_L = 15 pF R_L = 470Ω (at F = 0) R = 5 kΩ	01, 03	9, 10, 11	85		ns
			02		90		
Setup time, I_3, I_4, I_5	t_{SI3}		01, 03	9, 10, 11	85		ns
			02		75		
Setup time, I_6, I_7, I_8	t_{SI6}		All	9, 10, 11	8/		ns
Setup time, RAM_0, RAM_3, Q_0,Q_3	t_{SRQ}		01, 03	9, 10, 11	25		ns
			02		30		

1/ Not more than one output should be shorted at a time, and duration should not exceed one second.

2/ RAM_0, RAM_3, Q_0, Q_3 are three-state outputs internally connected to TTL inputs. Input characteristics are measured with I_6, I_7, I_8 in a state such that the three-state output is off.

3/ Clock pulse must be trailing edge, positive going.

4/ If the B address is used as a source operand, allow for the "A, B source" setup time; if it is used only for the destination address, use the "B dest." setup time.

5/ All hold times are "0".

6/ t_{SAB} = 120 ns or (t_{PWL} + 30 ns), whichever is greater. t_{PWL} is the clock low time.

7/ For device types 01 and 02, $t_{SBD} = t_{PWL}$ + 15 ns.
For device type 03, $t_{SBD} = t_{PWL}$ + 35 ns.
Where t_{PWL} is the clock low time.

8/ $t_{SI6} = t_{PWL}$ + 30 ns; where t_{PWL} is the clock low time.

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Case Z

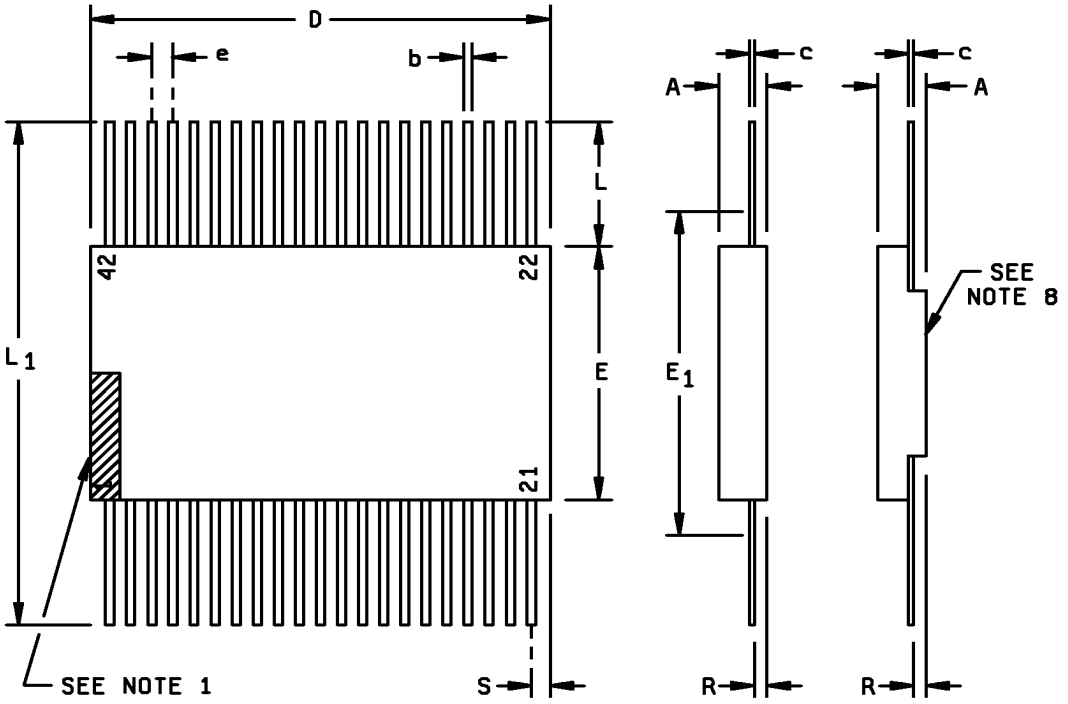

FIGURE 1. Case outline.

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Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.070	.115	1.78	2.92	
b	.017	.023	0.43	0.58	5
c	.006	.012	0.15	0.30	5
D	1.030	1.090	26.16	27.69	
E	.600	.660	15.24	16.76	
E_1	---	.690	---	17.53	3
e	.045	.055	1.14	1.40	4, 6
L	.250	.370	6.35	9.40	
L_1	1.300	1.370	33.02	34.80	
R	.020	.045	0.51	1.14	2
S	---	.040	---	1.02	7

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. Dimension R shall be measured at the point of exit of the lead from the body.
3. This dimension allows for off-center lid, meniscus and glass overrun.
4. The basic pin spacing is .050 (1.27 mm) between centerlines. Each pin centerline shall be located within ±.005 (0.13 mm) of its exact longitudinal position relative to pins 1 and 42.
5. All leads – increase maximum limit by .003 (0.08 mm) measured at the center of the flat, when lead finish A is applied.
6. Forty spaces.
7. Applies to all four corners (leads number 1, 21, 22, and 42).
8. Optional configuration. If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

FIGURE 1. Case outline – Continued.

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Device type	All		
Case outline	Q		
Terminal number	Terminal name	Terminal number	Terminal name
1	A_3	21	Q_0
2	A_2	22	D_3
3	A_1	23	D_2
4	A_0	24	D_1
5	I_6	25	D_0
6	I_8	26	I_3
7	I_7	27	I_5
8	RAM_3	28	I_4
9	RAM_0	29	C_n
10	V_{CC}	30	GND
11	F = 0	31	F_3
12	I_0	32	$\overline{G}$
13	I_1	33	C_{n+4}
14	I_2	34	OVR
15	CP	35	$\overline{P}$
16	Q_3	36	Y_0
17	B_0	37	Y_1
18	B_1	38	Y_2
19	B_2	39	Y_3
20	B_3	40	$\overline{OE}$

FIGURE 2. Terminal connections.

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Device type	All		
Case outline	Z		
Terminal number	Terminal name	Terminal number	Terminal name
1	I_8	22	D_0
2	I_7	23	I_3
3	RAM_3	24	I_5
4	NC	25	I_4
5	RAM_0	26	C_n
6	V_{CC}	27	GND
7	F = 0	28	F_3
8	I_0	29	$\overline{G}$
9	I_1	30	C_{n+4}
10	I_2	31	OVR
11	CP	32	$\overline{P}$
12	NC	33	Y_0
13	Q_3	34	Y_1
14	B_0	35	Y_2
15	B_1	36	Y_3
16	B_2	37	$\overline{OE}$
17	B_3	38	A_3
18	Q_0	39	A_2
19	D_3	40	A_1
20	D_2	41	A_0
21	D_1	42	I_6

FIGURE 2. Terminal connections - Continued.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 9
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3
Additional electrical subgroups for group C periodic inspections	10, 11

* PDA applies to subgroup 1.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C, D, or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125ºC, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

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4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C, D, or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125ºC, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 99-04-26

Approved sources of supply for SMD 77007 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
7700701QX	3/	
7700701ZX	3/	
7700702QX	3/	
7700703QA	0DKS7	GEM06803QQA
7700703QC	0DKS7	GEM06803QQC
7700703ZA	0DKS7	GEM06803QZA
7700703ZC	0DKS7	GEM06803QZC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ No longer available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0DKS7	Sarnoff, David Research Center 201 Washington Road Princeton, NJ 08540-5300

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

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