MOTOROLA

Product Preview

32K x 8 Bit BiCMOS Static Random Access Memory

6706A

Commercial Plus and Mil/Aero Applications

ELECTRICALLY TESTED PER:
MPG6706A

The 6706A is a 262,144 bit static random access memory organized as 32,768 words of 8 bits, fabricated using high performance silicon-gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

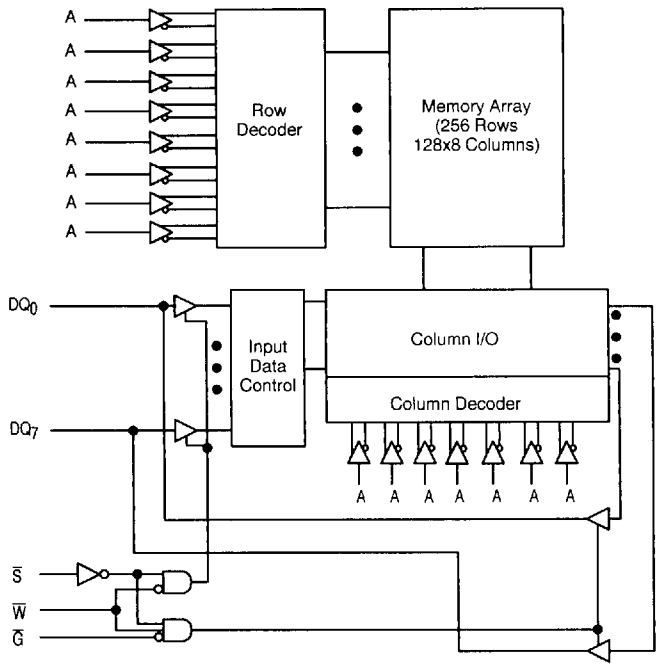
The 6706A is available in a 600 mil, 28 lead sidebraze package.

- Single 5.0 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Fast Access Times: 15/20 ns

AVAILABLE AS
1) JAN: N/A
2) SMD: N/A
3) 883: 6706A - XX/BXAJC
X = CASE OUTLINE AS FOLLOWS:
PACKAGE: DIL: X

XX = Speed in ns (15, 20)

BLOCK DIAGRAM



PIN NAMES	
A_0 - A_{14}	Address
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
$\overline{G}$	Output Enable
DQ_0 - DQ_7	Data Input/Output
V_{CC}	+5.0 V Power Supply
V_{SS}	Ground

Truth Table

$\overline{S}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle
H	X	X	Not Selected	High - Z	—
L	H	H	Read	High - Z	—
L	L	H	Read	D_{OUT}	Read Cycle
L	X	L	Write	D_{IN}	Write Cycle

X = Don't Care

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

Absolute Maximum Ratings: (See Note)			
Rating	**Symbol**	**Value**	**Unit**
Power Supply Voltage	V_{CC}	-0.5 to +7.0	V
Voltage Relative to V_{SS} for any Pin Except V_{CC}	V_{IN}, V_{OUT}	-0.5 to V_{CC} +0.5	V
Output Current	I_{OUT}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	-55 to +125	°C
Operating Temperature	T_A	-55 to +125	°C
Storage Temperature	T_{stg}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

PIN ASSIGNMENTS	
Function	**DIL Case 719-03**
A_{14}	1
A_{12}	2
A_7	3
A_6	4
A_5	5
A_4	6
A_3	7
A_2	8
A_1	9
A_0	10
DQ_2	11
DQ_1	12
DQ_0	13
V_{SS}	14

PIN ASSIGNMENTS	
Function	**DIL Case 719-03**
DQ_3	15
DQ_4	16
DQ_5	17
DQ_6	18
DQ_7	19
$\overline{S}$	20
A_{10}	21
$\overline{G}$	22
A_{11}	23
A_9	24
A_8	25
A_{13}	26
$\overline{W}$	27
V_{CC}	28

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = – 55°C to +125°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3 *	V
Input Low Voltage	V_{IL}	– 0.5 **	—	0.8	V

* V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = + 2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20 mA.
** V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20 mA.

DC CHARACTERISTICS				
Parameter	**Symbol**	**Min**	**Max**	**Unit**
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	±2.0	µA
Output Leakage Current ($\overline{S}$ = V_{IH}, V_{OUT} = 0 to V_{CC})	$I_{lkg(O)}$	—	±2.0	µA
AC Supply Current (I_{OUT} = 0 mA) 6706-15: t_{AVAV} = 15 ns	I_{CCA}	—	175	mA
AC Supply Current (I_{OUT} = 0 mA) 6706-20: t_{AVAV} = 20 ns	I_{CCA}	—	160	mA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)			
Characteristic	**Symbol**	**Max**	**Unit**
Address Input Capacitance	C_{in}	5	pF
Control Pin Input Capacitance ($\overline{S}$, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
I/O Capacitance	$C_{I/O}$	6	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = – 55°C to +125°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level	1.5 V
Input Pulse levels	0 to 3.0 V
Input Rise/Fall Times	≤ 3.0 ns
Output Timing Measurement Reference Level	1.5 V

AC TEST LOADS OR EQUIVALENT

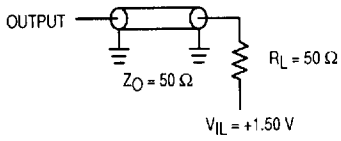


Figure 1A.

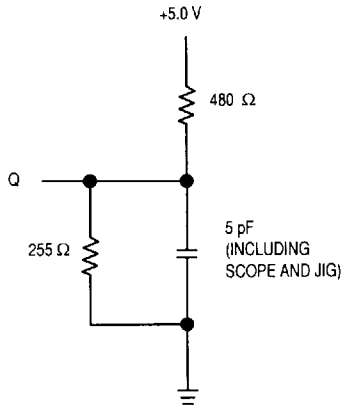
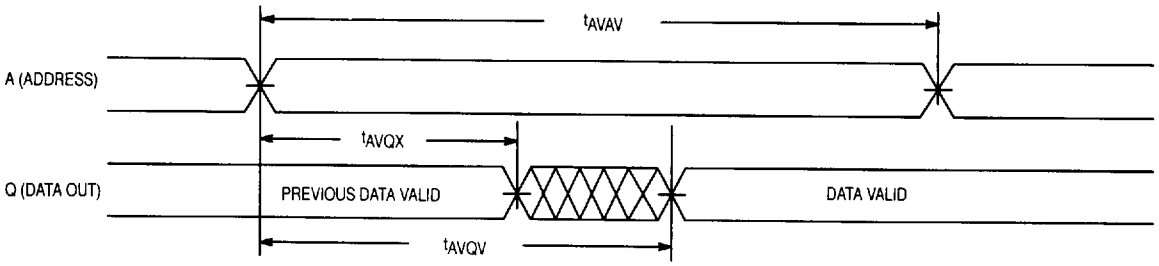
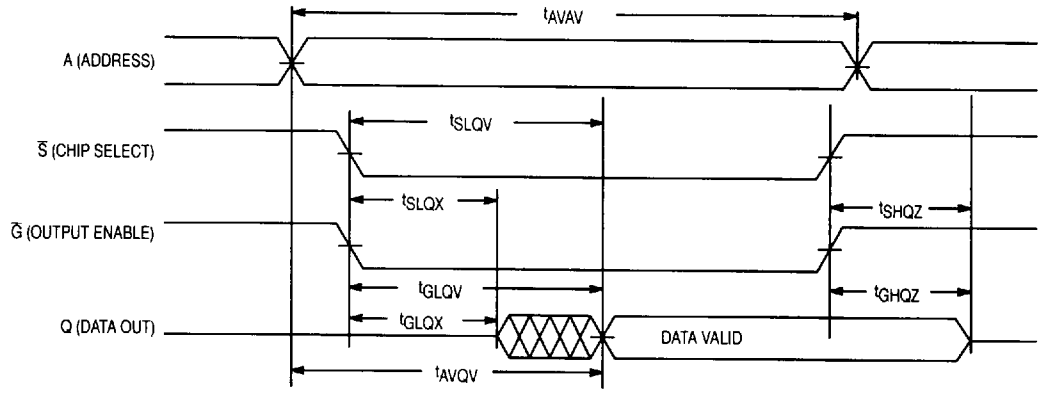


Figure 1B.

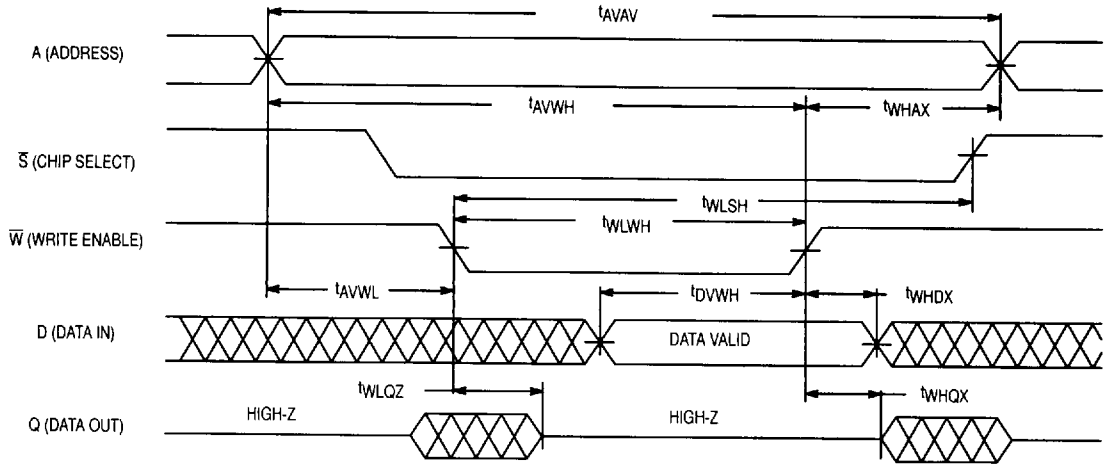
READ CYCLE 1 (See Note 7)



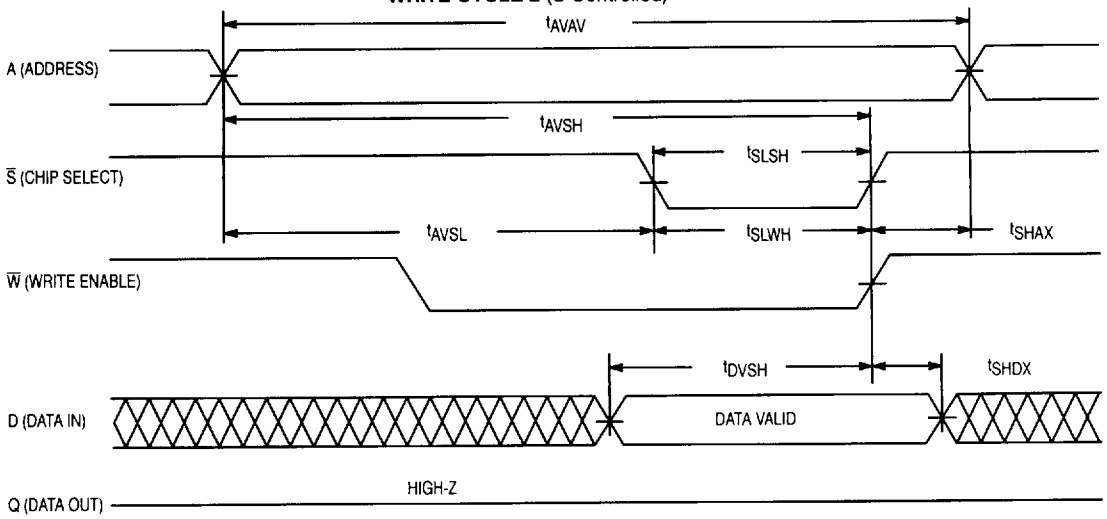
READ CYCLE 2 (See Note 8)



WRITE CYCLE 1 ($\overline{W}$ Controlled)



WRITE CYCLE 2 ($\overline{S}$ Controlled)



TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.