REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. Editorial changes throughout.	1990 APRIL 10	

REV																								
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REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A		A	A	A			A	A	A	A				
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19				

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Todd S. Cook

CHECKED BY: Ray Monnin

APPROVED BY:

DRAWING APPROVAL DATE: 15 JUNE 1988

REVISION LEVEL: A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, NMOS, NUMERIC DATA PROCESSOR, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-88547

SHEET 1 OF 1

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-88547	01	Q	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device types	Generic number	Circuit function	Clock speed
01	8087-2	Numeric data processor (NDP)	8 MHz
02	8087	Numeric data processor (NDP)	5 MHz

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 2.096" x .620" x .225"), dual-in-line package

1.3 Absolute maximum ratings.

Storage temperature range	-65°C to +150°C
Voltage on any pin with respect to ground	-1.0 V dc to +7 V dc
Power dissipation (P_D)	3.0 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J)	+200°C

1.4 Recommended operating conditions.

Case operating temperature range (T_C)	-55°C to +125°C
Supply voltage (V_{CC})	4.75 V dc $\leq V_{CC} \leq$ 5.25 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Functional block diagram. The functional block diagram shall be as specified on figure 2.

3.2.3 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.7 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.75\ V \le V_{CC} \le 5.25\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}		1,2,3	All	-0.5 1/	.8	V
Input high voltage	V_{IH}				2.0	V_{CC}+0.5 1/	
Output low voltage Status lines All others	V_{OL}	I_{OL} = 2.0 mA				.60	
Output high voltage	V_{OH}	I_{OH} = -400 µA			2.4		
Power supply current	I_{CC}	V_{CC} = 5.25 V	3			600	mA
Input leakage current	I_{LI}	V_{IN} = 0.0 V or 5.5 V	1,2,3			±10	µA
Output leakage current	I_{LO}	V_{OUT} = 0.45 V or 5.5 V				±10	
Clock input low voltage	V_{CL}				-.5 1/	.6	V
Clock input high voltage	V_{CH}				3.9	V_{CC}+1.0 1/	
Capacitance of inputs	C_{IN}	See 4.3.1c 2/	4			10	pF
Capacitance I/O buffer	$C_{I/O}$					15	
Capacitance of outputs	C_{OUT}					10	
Functional tests		See 4.3.1d	7,8				

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.75\ V \le V_{CC} \le 5.25\ V$, unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
CLK cycle period	t_{CLCL}	See figures 3 and 4	9,10,11	01	125	500	ns
				02	200	500	
CLK low time	t_{CLCH}			01	68 1/		
				02	2/3 (t_{CLCL}) -15		
CLK high time	t_{CHCL}			01	44		
				02	1/3 (t_{CLCL}) +2		
CLK rise time 1/	t_{CH1CH2}			All		10	
CLK fall time 1/	t_{CL2CL1}					10	
Data in setup time	t_{DVCL}			01	20		
				02	30		
Data in hold time	t_{CLDX}			All	10		
READY setup time	t_{RYHCH}			01	68		
				02	2/3 (t_{CLCL}) -15		
READY hold time	t_{CHRYX}			01	20		
				02	30		
READY inactive to CLK	t_{RYLCL}			All	-8		
$\overline{RQ}$/GT setup time	t_{GVCH}			01	15		
				02	30		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.75\ V \le V_{CC} \le 5.25\ V$, unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
$\overline{RQ/GT}$ hold time	t_{CHGX}	See figures 3 and 4	9,10,11	01	30		ns
				02	40		
QSO-1 setup time	t_{QVCL}			All	30		
QSO-1 hold time	t_{CLQX}				10		
Status active setup time	t_{SACH}				30		
Status inactive setup time 1/	t_{SNCL}				30		
Input rise time (except CLK) 1/	t_{ILIH}					20	
Input fall time (except CLK) 1/	t_{IHIL}					12	
Ready active to status passive	t_{RYHSH}			01		65	
				02		110	
Status active delay	t_{CHSV}			01	10 1/	60	
				02	10 1/	110	
Status inactive delay	t_{CLSH}			01	10 1/	70	
				02	10 1/	130	
Address valid delay	t_{CLAV}			01	10 1/	60	
				02	10 1/	114	
Address hold time	t_{CLAX}			All	10		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.75\ V \le V_{CC} \le 5.25\ V$, unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Address float delay 1/	t_{CLAZ}	See figures 3 and 4	9,10,11	01	t_{CLAX}	50	ns
				02	t_{CLAX}	80	
Data valid delay	t_{CLDV}			01	10 1/	60	
				02	10 1/	110	
Data hold time	t_{CHDX}			All	10		
BUSY and INT valid delay	t_{CHBV}			01	10 1/	85	
				02	10 1/	150	
$\overline{RQ}/\overline{GT}$ active delay	t_{CLGL}			01	0 1/	50	
				02	0 1/	85	
$\overline{RQ}/\overline{GT}$ inactive delay	t_{CLGH}			01	0 1/	50	
				02	0 1/	85	
Output rise time 1/	t_{OLOH}			All		20	
Output fall time 1/	t_{OHOL}			All		12	

1/ Guaranteed to the limits specified herein if not tested.

2/ The capacitance measurements shall be made between the indicated terminal and ground at a frequency of 1 MHz at T_C of +25°C. The dc bias of the measuring instrument shall be less than ±0.1 V. The ac signal amplitude shall be less than 50 mV rms.

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Device types 01 and 02

Case Q

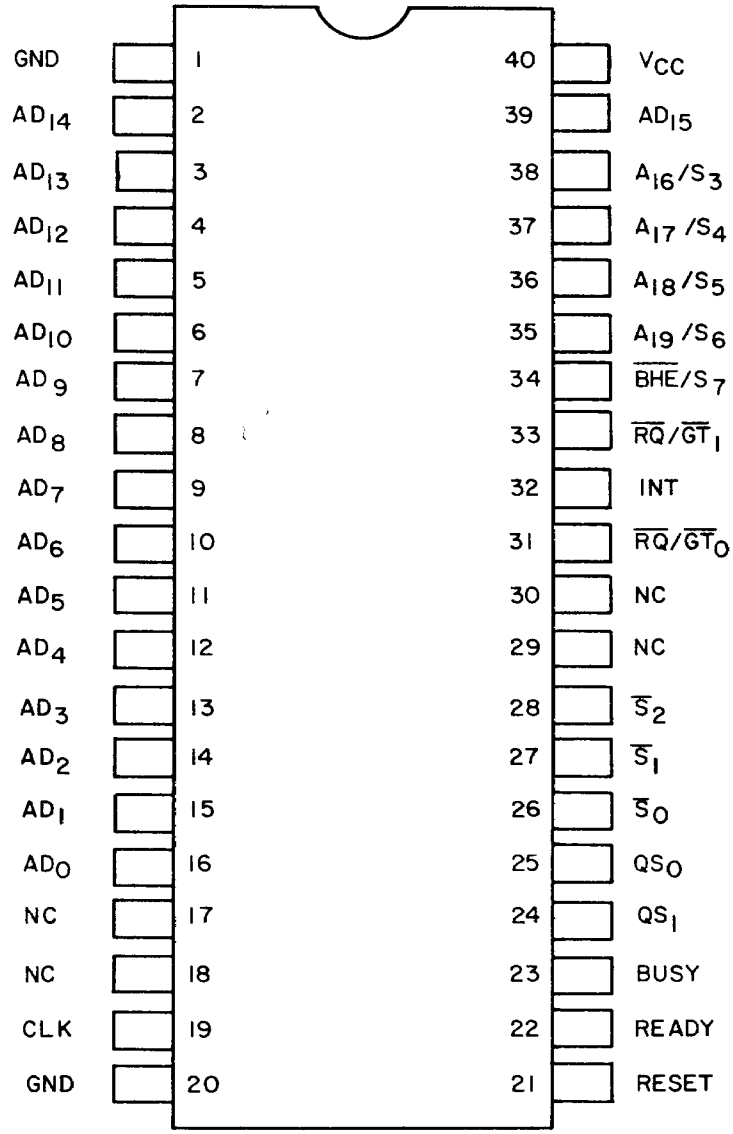

FIGURE 1. Terminal connections.

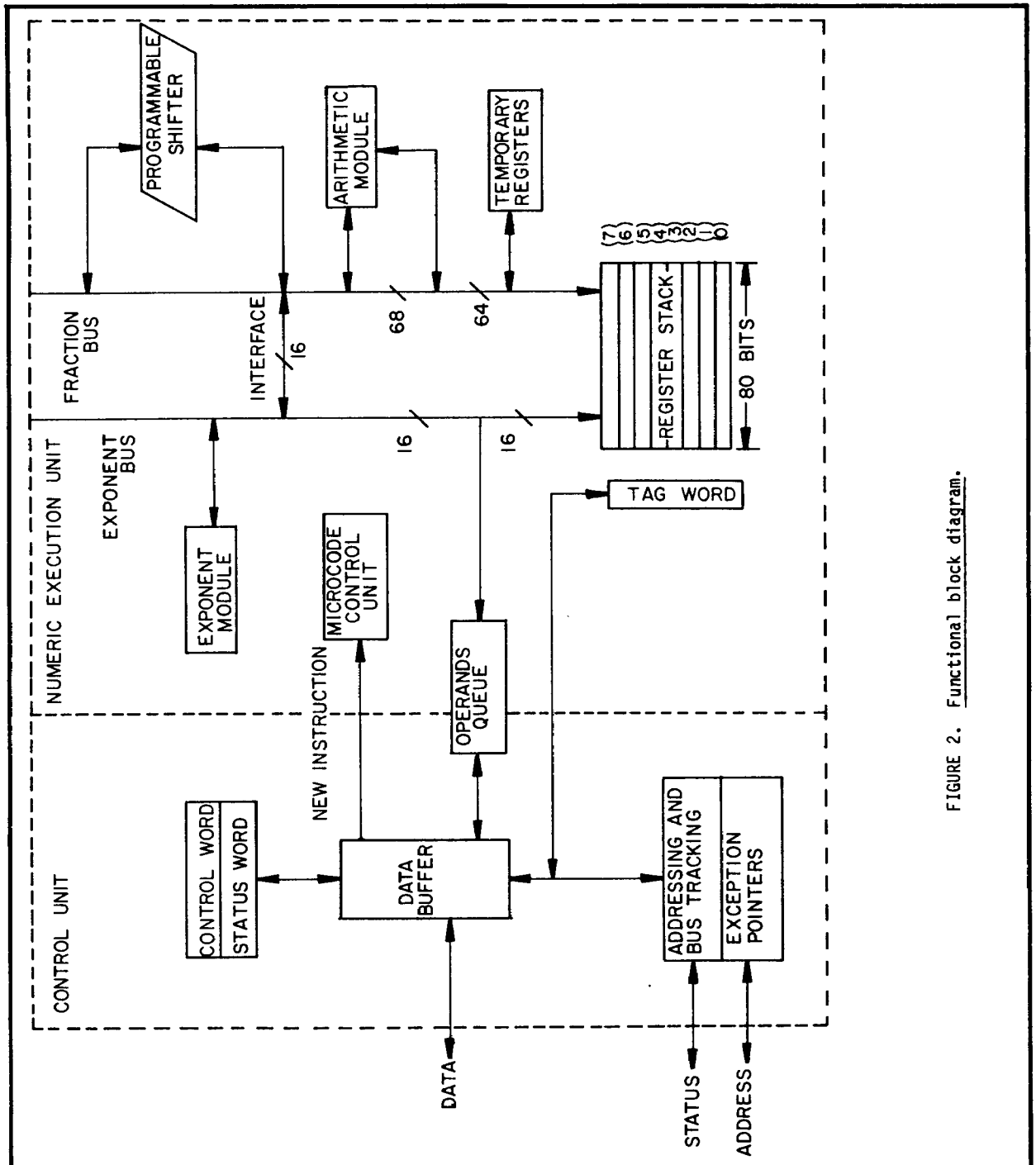

FIGURE 2. Functional block diagram.

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		REVISION LEVEL A	SHEET 9

DESC FORM 193A
SEP 87

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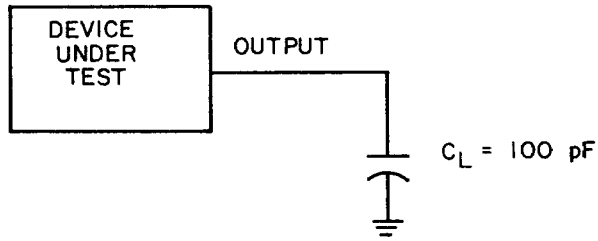
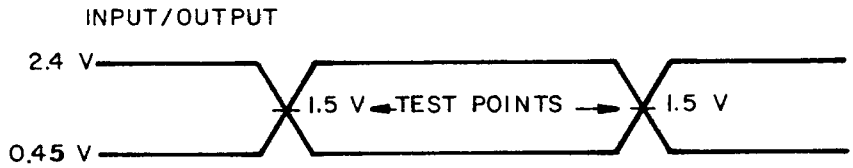


NOTE: C_L includes jig, probe, and stray capacitance.

FIGURE 3. Test load circuit.



NOTE: AC testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".

FIGURE 4. Switching waveforms.

MASTER MODE (WITH BUS CONTROLLER REFERENCES)

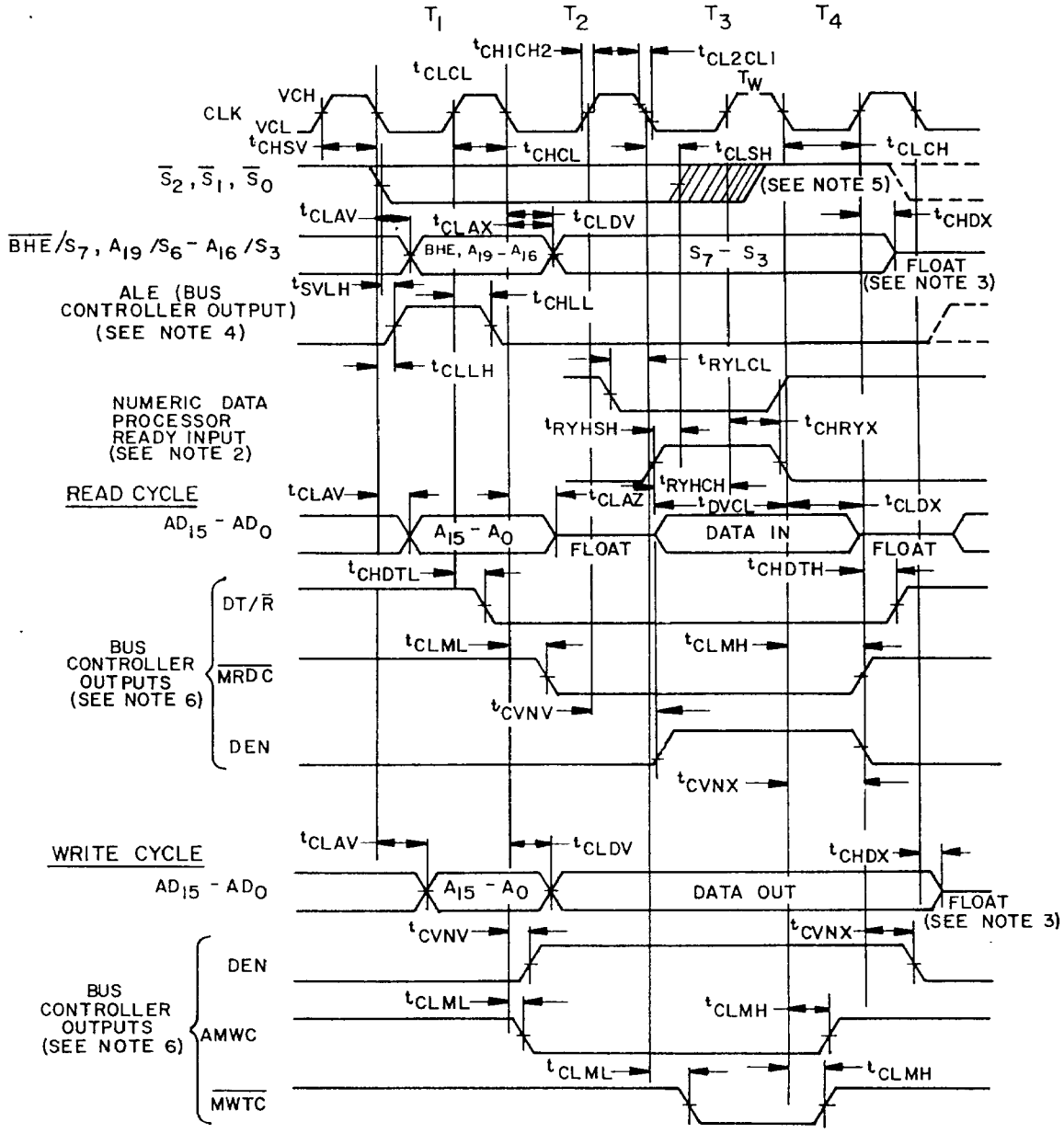


FIGURE 4. Switching waveforms - Continued.

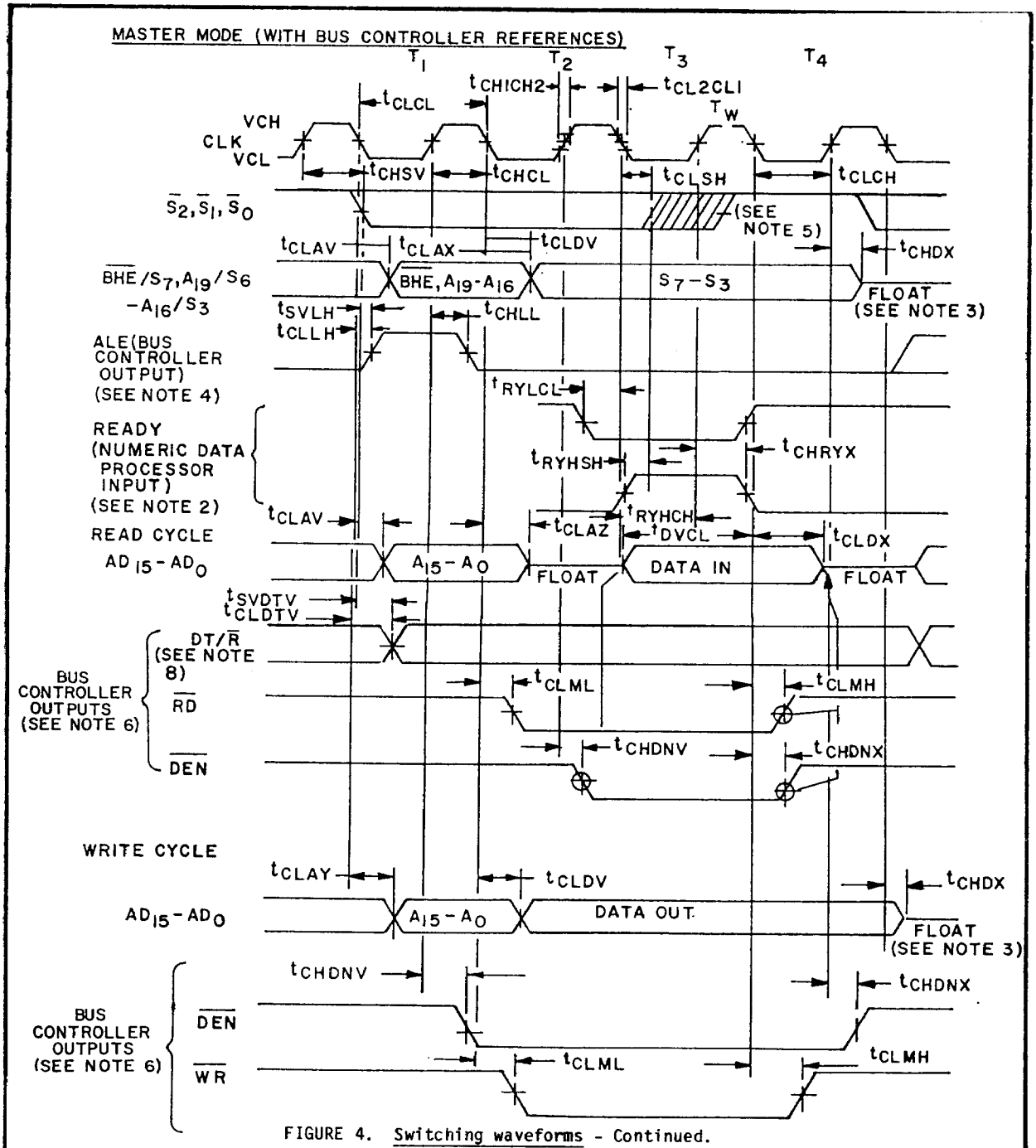
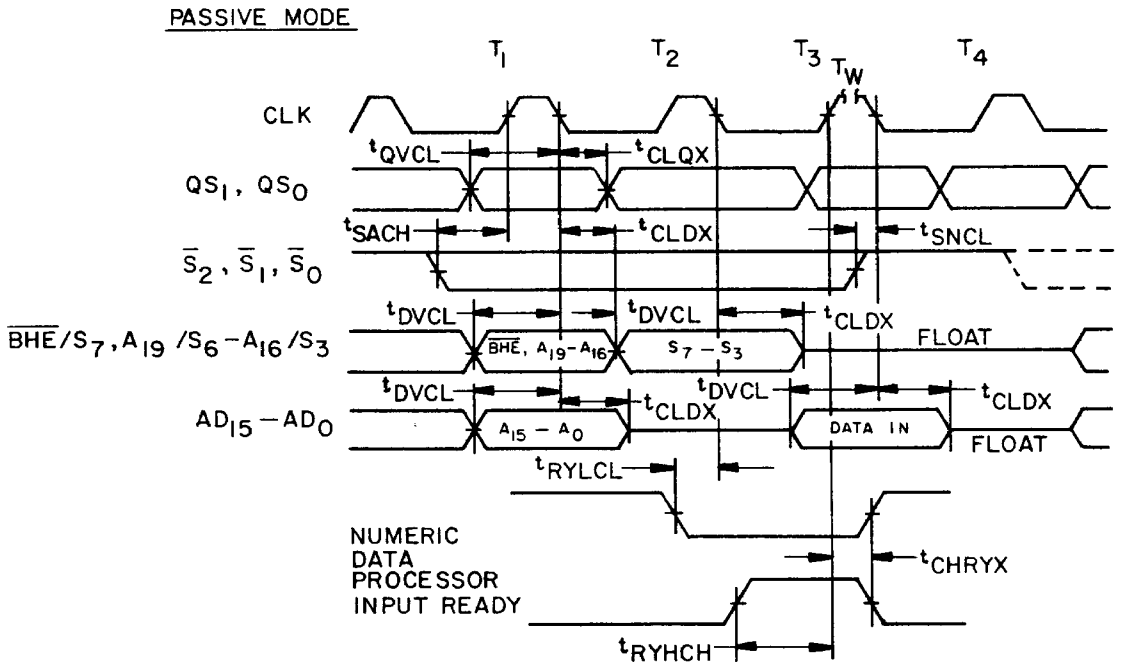


FIGURE 4. Switching waveforms - Continued.

NOTES:
1. All signals switch between V_{OL} and V_{OH} unless otherwise specified.
2. READY is sampled near the end of T_2, T_3, and T_W to determine if T_W machine states are to be inserted.
3. The local bus floats only if the numberic data processor is returning control to the CPU.
4. ALE rises at later of (t_{SVLH}, t_{CLLH}).
5. Status inactive in state just prior to T_4.
6. The issuance of bus controller command and control signals ($\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, and DEN) lags the active high bus controller CEN.
7. All timing measurements are made at 1.5 V unless otherwise specified.
8. DT/$\overline{R}$ becomes valid at the late of (t_{SVDTV}, t_{CLDTV}).
9. CLK rise and fall times are measured from 1.0 V to 3.5 V and from 3.5 V to 1.0 V respectively.

FIGURE 4. Switching waveforms - Continued.



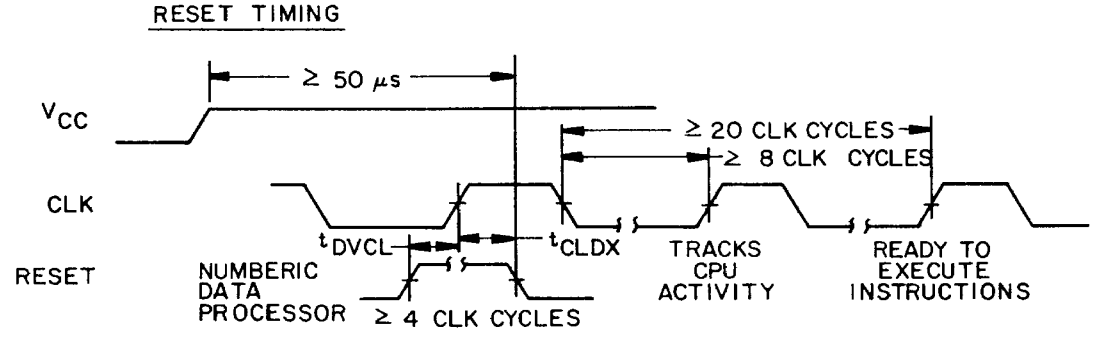
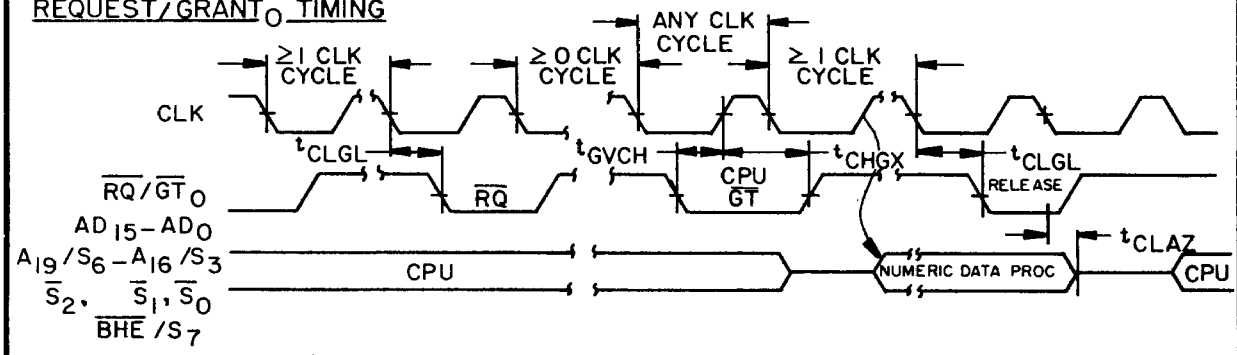
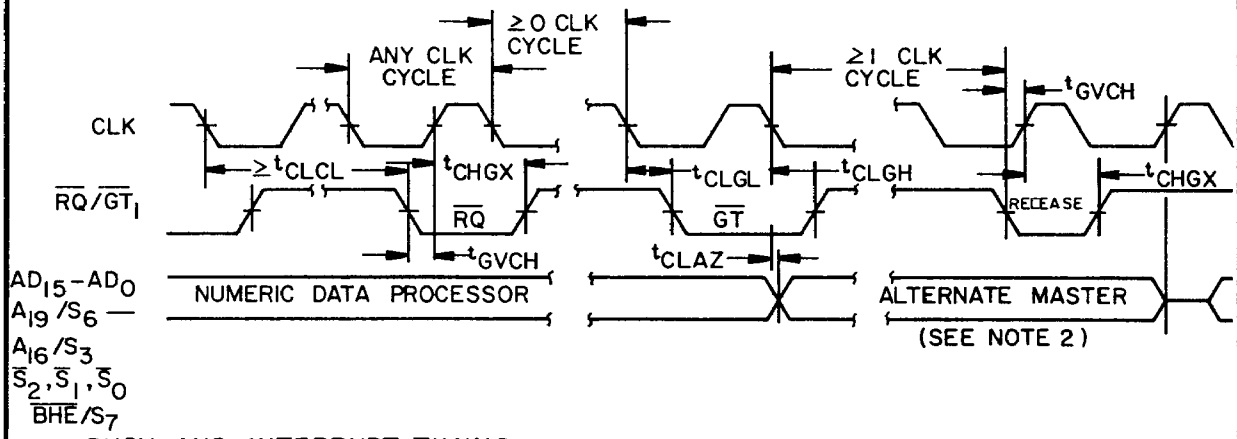


FIGURE 4. Switching waveforms - Continued.

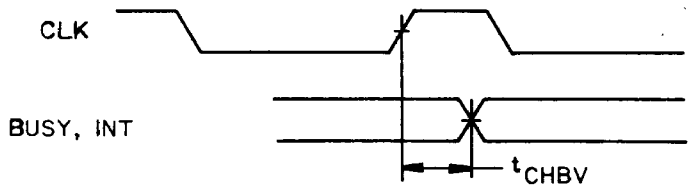
REQUEST/GRANT$_0$ TIMING



REQUEST GRANT$_1$ TIMING



BUSY AND INTERRUPT TIMING



NOTES:
1. The CPU provides active pullup of $\overline{RQ}/\overline{GT}_0$, see t_{CLGH}.
2. Alternate master may not drive the buses outside of the region shown without risking bus contention.
3. All timing measurements are made at 1.5 V unless otherwise specified.

FIGURE 4. Switching waveforms - Continued.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN}, C_{OUT}, and $C_{I/O}$ measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance.

d. Subgroups 7 and 8 shall be sufficient to verify the functional operation of the device. These tests form a part of the manufacturer's test tape and shall be maintained and available from the approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8A, 10

* PDA applies to subgroups 1 and 7.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-8525.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8525.

6.6 Pin description. Pin descriptions are as follows:

Mnemonic	Type	Description
AD15 - AD0	I/O	Address data. These are input/output lines for numeric data processor driven bus cycles and are inputs which the numeric data processor monitors when the CPU is in control of the bus.
A19/S6 A18/S5 A17/S4 A16/S3	I/O	Address memory. During T_1 these are the four most significant address lines for memory operations. During memory operations, status information is available during T_2, T_3, T_W, and T_4. During numeric data processor controlled bus cycles, S6, S4, and S3 are reserved and HIGH, while S5 is always LOW. These lines are inputs which the numeric data processor monitors when the CPU is in control of the bus.
$\overline{BHE}$/S7	I/O	Bus high enable. During T_1 the bus high enable signal should be used to enable data into the most significant half of the data bus. The S7 status information is available during T_2, T_3, T_W, and T_4.
$\overline{S2}$, $\overline{S1}$, $\overline{S0}$	I/O	Status. These lines are driven active during T_4, remain valid during T_1 and T_2, and are returned to the passive state during T_3 or during T_W when READY is HIGH. These signals are monitored by the numeric data processor when the CPU is in control of the bus.
$\overline{RQ}$/$\overline{GT0}$	I/O	Request/Grant$_0$. This line is used by the numeric data processor to gain control of the local bus from the CPU of operand transfers or on behalf of another bus master.
$\overline{RQ}$/$\overline{GT1}$	I/O	Request/Grant$_1$. This line is used by another local bus master to force the numeric data processor to request the the local bus.
QS1, QS0	I	QS1 and QS0 provide the numeric data processor with status to allow tracking of the CPU instruction queue.
INT	O	Interrupt. This line is used to indicate that an unmasked exception has occurred during a numeric instruction execution when the numeric data processor interrupts are enabled.

Mnemonic	Type	Description
BUSY	O	Busy. This is used to indicate that the numeric data processor is executing a numeric instruction.
READY	I	Ready. This is the acknowledgement from the addressed memory device that it will complete the data transfer.
RESET	I	Reset. This causes the numeric data processor to immediately terminate its present activity.
CLK	I	Clock. The clock provides the basic timing for the numeric data processor and the bus controller.
V_{CC}		Power. V_{CC} is the +5 V power supply pin.
GND		Ground. GND are the ground pins.

6.7 Approved source of supply. An approved source of supply is listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC. The approved source of supply listed below is for information purposes only and is current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8854701QX	34649	MD8087-2/B
5962-8854702QX	34649	MD8087/B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34649	Intel Corporation 3065 Bowers Avenue Santa Clara, CA 95051 Point of contact: 5000 W. Williams Field Road Chandler, AZ 85224

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