

VA2707

**DUAL HIGH-SPEED, FAST-SETTLING,
HIGH OUTPUT CURRENT
OPERATIONAL AMPLIFIER, $A_{CL} \geq 12$**

T-79-07-20

FEATURES

- Fast Settling Time: $\pm 0.1\%$ in 150ns
- High Slew Rate: 105 V/ μ s
- Large Gain-Bandwidth: 300 MHz
- Full Power Bandwidth: 5.6 MHz at 6V p-p
- Ease Of Use: Internally Compensated for $A_{CL} \geq 12$
- Minimal Crosstalk: >90dB Separation
- Large Output Current: $\pm 50mA$
- Wide Input Voltage Range: Within 1.5V of V_+ and 0.5V of V_-
- Short Circuit Protection
- Available In Commercial and Military Versions

DESCRIPTION

The VA2707 offers the high slew rate and high signal frequencies advantages as the VA707 in a dual package configuration. The high slew rate, output drive and open-loop voltage again makes the VA2707 ideal for analog amplification and processing of high-speed signals extending into the video range.

The VA2707 is offered in an 8-pin CERDIP, plastic or metal can, as well as a 20-pin LCC.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$\pm 6V$
Differential Input Voltages	$\pm 9V$
Common Mode Input Voltage	$ V_S - 0.5V$
Power Dissipation ($T_A = 70^\circ C$, Note 1)	450mW
Output Short Circuit Current Duration (Note 2)	Indefinite
Operating Temperature Range:		
Commercial (2707 J, K)	0° to $70^\circ C$
Military (2707 S)	-55° to +125° C
Storage Temperature Range	-65° to +150° C
Lead Temp. Range (Soldering to 60 Sec.)	300°C

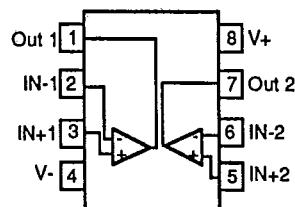
Note 1: Power derating above $T_A = 70^\circ C$ to be based on a maximum junction temperature of 150°C and the following thermal resistance factors:

PACKAGES	θ_{JC} (°C/W)	θ_{JA} (°C/W)
DIP	75	180
TO - 99	115	250

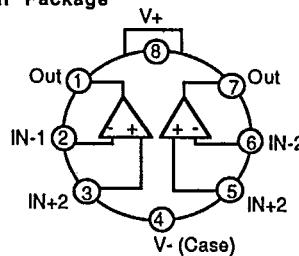
Note 2: Continuous short circuit protection is allowed on one amplifier per time up to the following case and ambient temperatures:

PACKAGES	T_C (°C)	T_A (°C)
DIP	100	30
TO - 99	75	(Note 3)

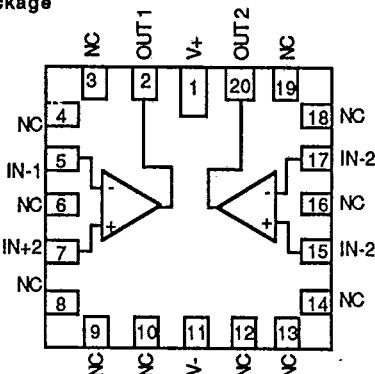
Note 3: Long duration shorts (>5 sec) will result in junction temperature exceeding 150°C which may result in part damage.

CONNECTION DIAGRAMS**Dual In-Line Package**

Top View

Metal Can Package

Top View

LCC Package

Top View

PACKAGE TYPES AVAILABLE

- 8-Pin Plastic DIP
- 8-Pin CERDIP
- 8-Pin Metal Can, TO-99
- 20-Pin LCC

T-79-07-20

ELECTRICAL CHARACTERISTICS ($V_S = \pm 5V$, $T_A = 25^\circ C$ unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	VA2707J			VA2707K			VA2707S			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage T_{Min} to T_{Max}	V_{OS}		5	12		3	6		3	6		mV
		$0^\circ \leq T_A \leq 70^\circ C$	8	16		5	10					
		$-55 \leq T_A \leq 125^\circ C$							6	12		
Average Offset Voltage Drift	$\frac{\Delta V_{OS}}{\Delta T}$	$0^\circ \leq T_A \leq 70^\circ C$		20		20						$\mu V^\circ C$
		$-55 \leq T_A \leq 125^\circ C$								15		
Input Bias Current T_{Min} to T_{Max}	I_B		650	1100		650	1100		650	1100		nA
		$0^\circ \leq T_A \leq 70^\circ C$		1700		1700						
		$-55 \leq T_A \leq 125^\circ C$								2200		
Input Offset Current	I_{OS}		35	120		35	120		35	120		nA
Input Common Mode Range	V_{CM}		+3 -4	+3.5 -4.5		+3 -4	+3.5 -4.5		+3 -4	+3.5 -4.5		V
Differential Input Resistance	R_{IND}	(Note 1)	3	10		3	10		3	10		MΩ
Common Mode Input Resistance	R_{INC}	(Note 1)	4	8		4	8		4	8		MΩ
Differential Input Capacitance	C_{IND}	(Note 1)		2			2			2		pF
Common Mode Input Capacitance	C_{INC}	(Note 1)		3			3			3		pF
Input Voltage Noise	θ_N	BW = 10Hz to 100KHz		12			12			12		µVRMS
Open Loop Voltage Gain	A_V	$V_{OUT} = \pm 3V$ $R_L = 2k\Omega$	2	5		5	10		5	10		V/mV
Output Voltage Swing	V_{OUT}	$R_L = 2k\Omega$	± 3.5			± 3.5			± 3.5			V
		$R_L = 51\Omega$	± 2.0	± 2.4		± 2.5	± 2.7		± 2.5	± 2.7		
Power Supply Current (Both Amplifiers)	I_S			15	20		15	20		15	20	mA
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 2V$	60	70		60	70		60	70		dB
Power Supply Rejection Ratio	PSRR	$\Delta V_{PS} = \pm 0.5V$	60	66		60	66		60	66		dB
Slew Rate	SR	10-90% of Leading Edge (Figure 1)	80	105		80	105		80	105		V/µs
Settling Time	t_S	To $\pm 0.1\%$ ($\pm 4mV$) of Final Value (Fig. 1, Note 1)		150	200		150	200		150	200	ns
Gain Bandwidth Product	GBW			300			300			300		MHz
Small Signal Rise/Fall Time	t_r / t_f	$\theta_O = \pm 200mV$ 10-90% (Figure 1)		9			9			9		ns
Full Power Bandwidth	BW_{FP}	$R_L = 2k\Omega$ $C_L = 50pF$ $V_{OUT} = 6V_{pp}$		5.6			5.6			5.6		MHz
Amplifier to Amplifier Crosstalk		Input Referenced $f = 10KHz$ (Figure 2)		-96			-96			-96		dB

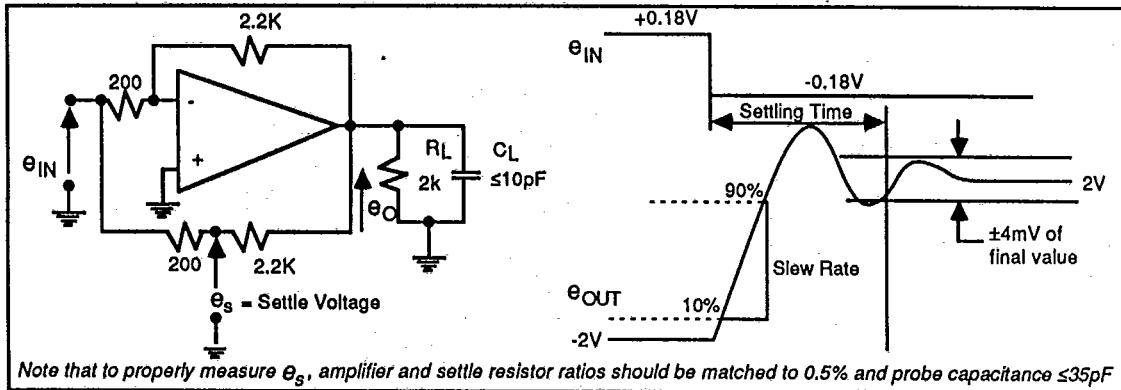
Notes: 1. Not tested, guaranteed by design.

LSP FAMILY DATA SHEETS

VA2707

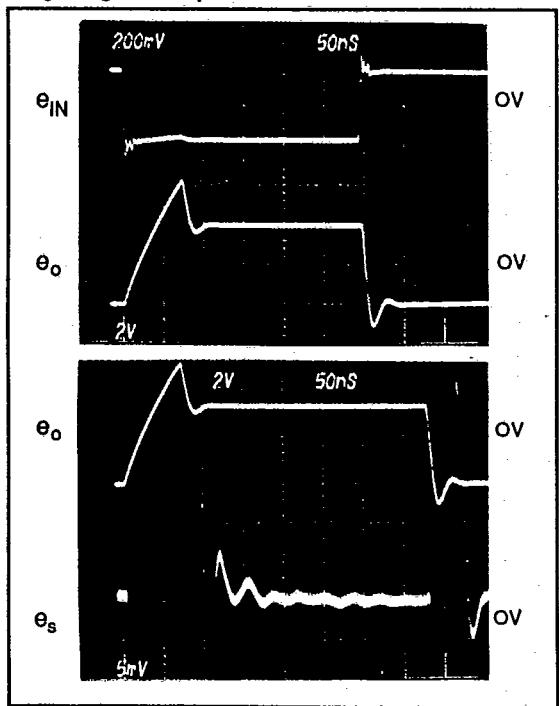
T-79-07-20

Figure 1: Settling Time and Slew Rate Test Circuit



Note that to properly measure θ_s , amplifier and settle resistor ratios should be matched to 0.5% and probe capacitance $\leq 35\text{pF}$

Large Signal Response



Small Signal Response

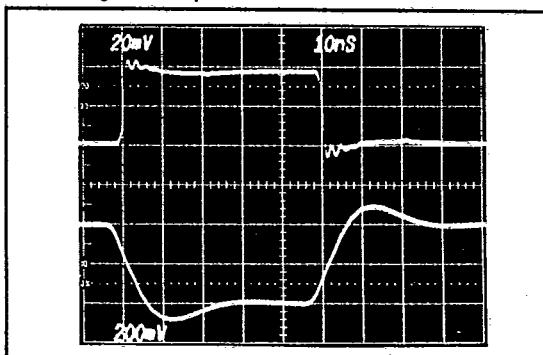
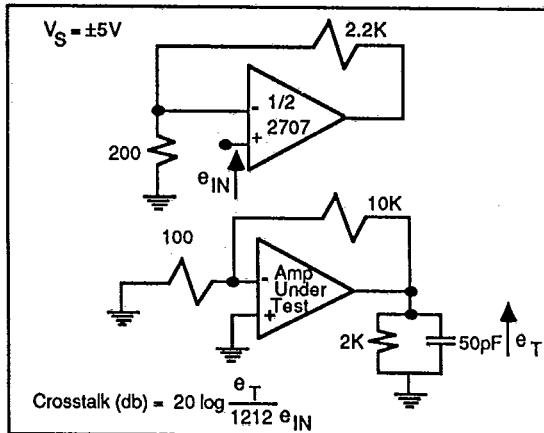


Figure 2: Crosstalk Test Circuit



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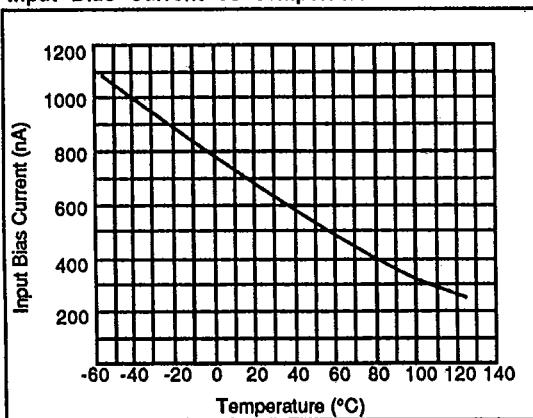
D

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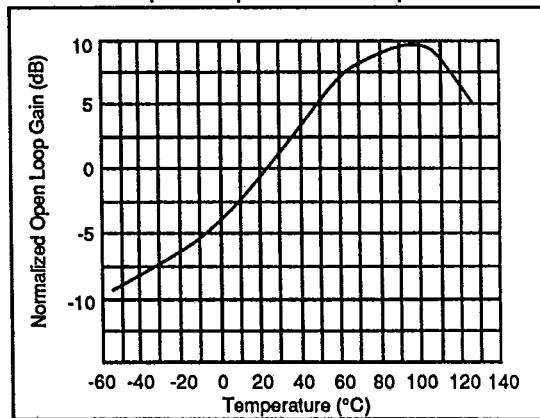
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TYPICAL PERFORMANCE CHARACTERISTICS ($V_S = \pm 5V$, $T_A = 25^\circ C$ unless otherwise stated)

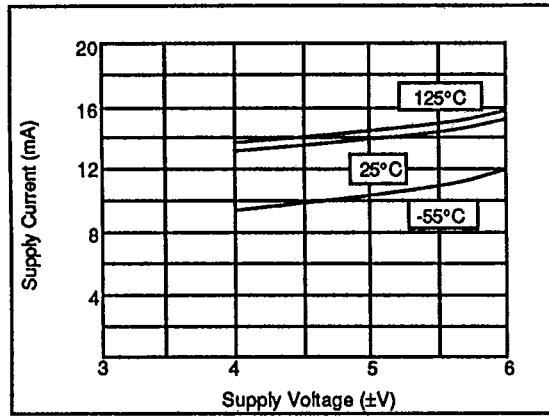
Input Bias Current vs Temperature



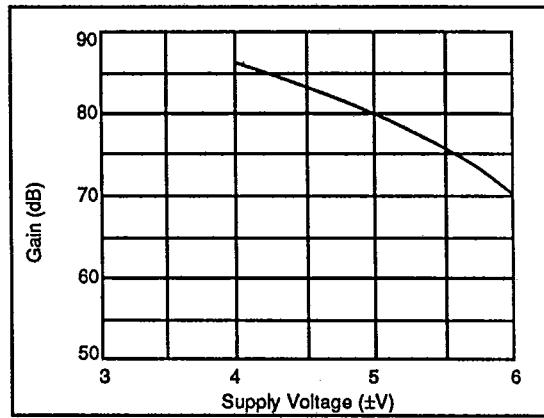
Normalized Open Loop Gain vs Temperature



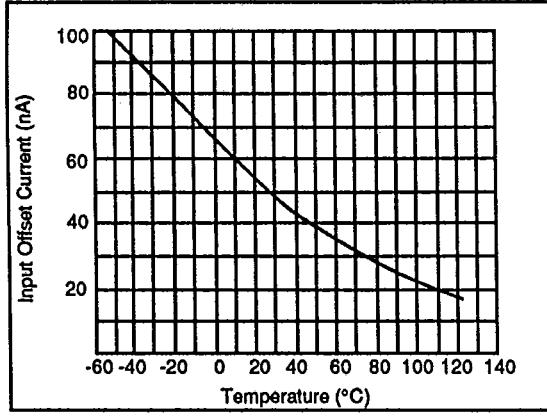
Supply Current vs Supply Voltage



Open Loop Gain vs Supply Voltage



Input Offset Current vs Temperature



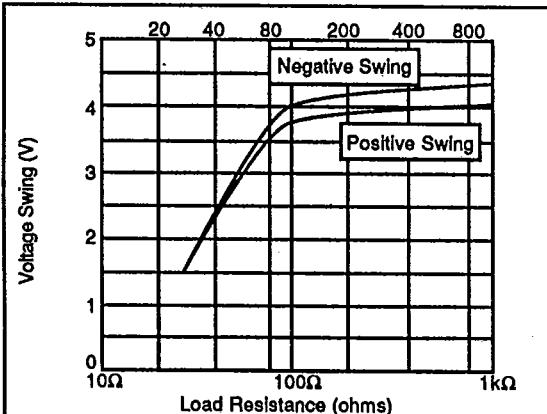
LSP FAMILY DATA SHEETS

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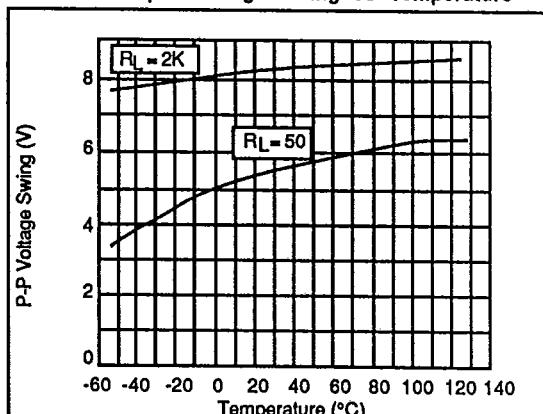
T-79-07-20

TYPICAL PERFORMANCE CHARACTERISTICS ($V_S = \pm 5V$, $T_A = 25^\circ C$ unless otherwise stated)

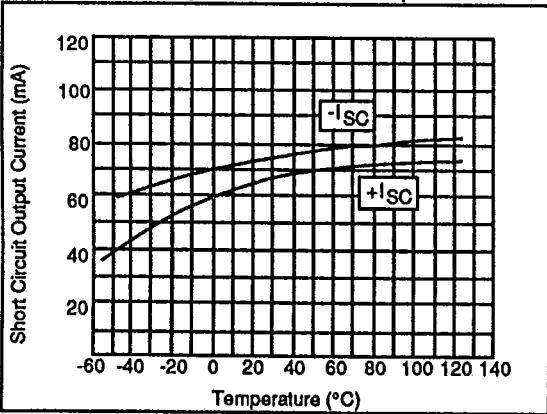
Maximum Output Voltage Swing vs Load Resistance



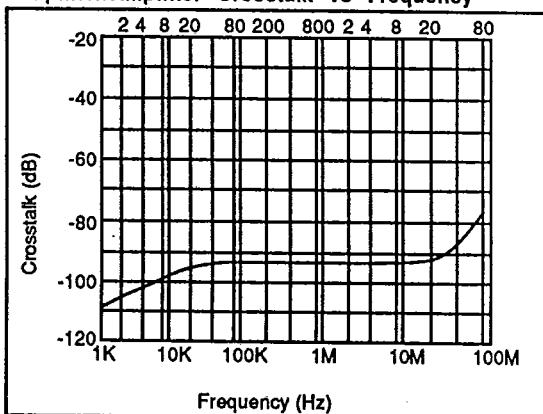
Maximum Output Voltage Swing vs Temperature



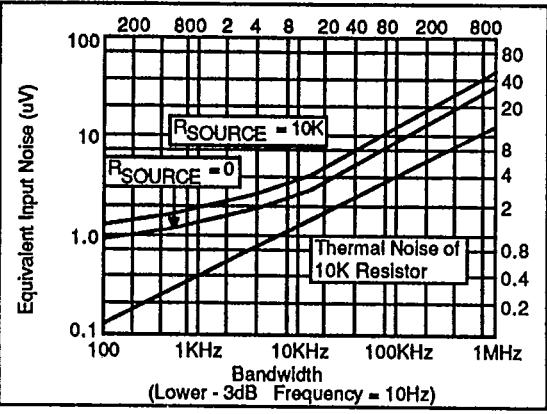
Short Circuit Output Current vs Temperature



Amplifier/Amplifier Crosstalk vs Frequency



Equivalent Input Noise vs Bandwidth

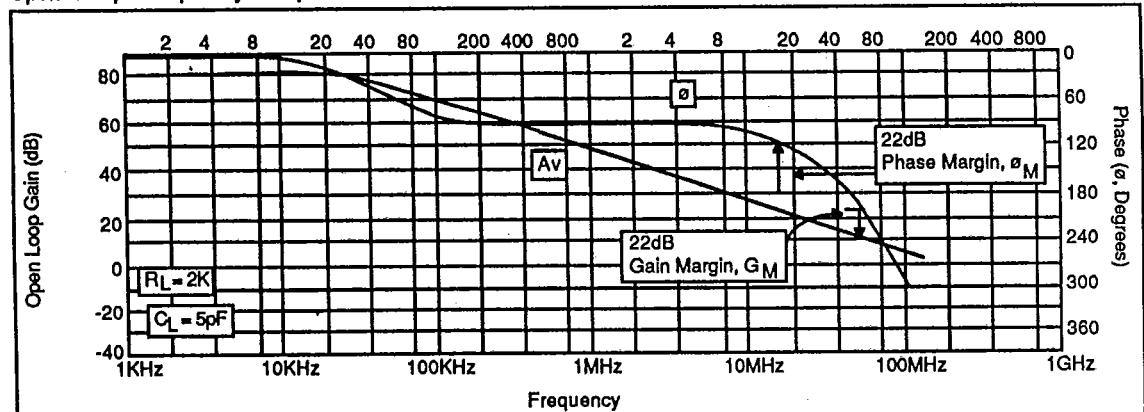


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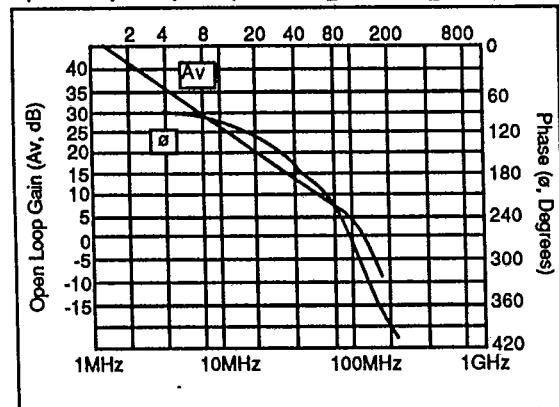
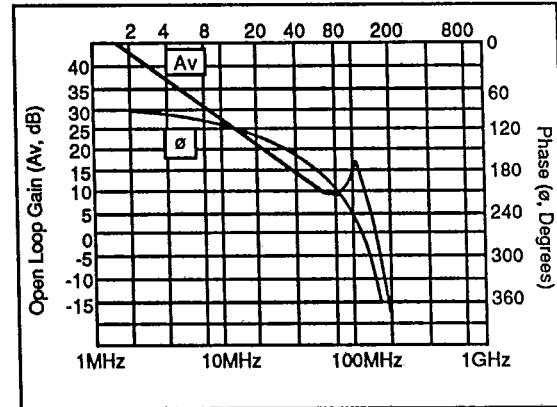
T-79-07-20

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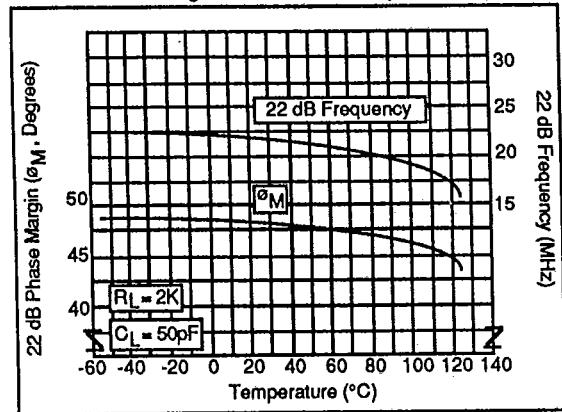
Open Loop Frequency Response



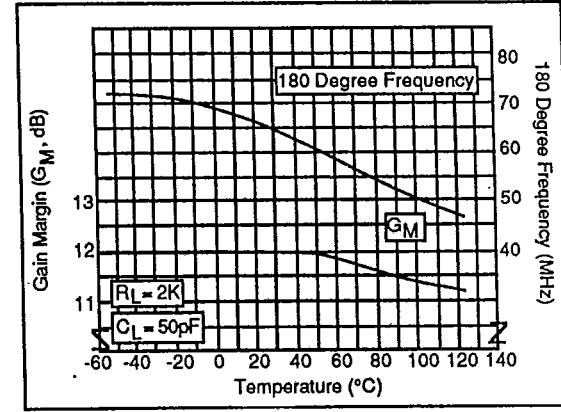
LSP FAMILY DATA SHEETS

Open Loop Freq. Response, $R_L = 50\Omega$, $C_L = 50pF$ Open Loop Freq. Response, $R_L = 2K\Omega$, $C_L = 50pF$ 

22 dB Phase Margin and 22 dB Freq. vs Temp.



Gain Margin and 180 Degree Freq. vs Temp.



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APPLICATION INFORMATION**AC Characteristics**

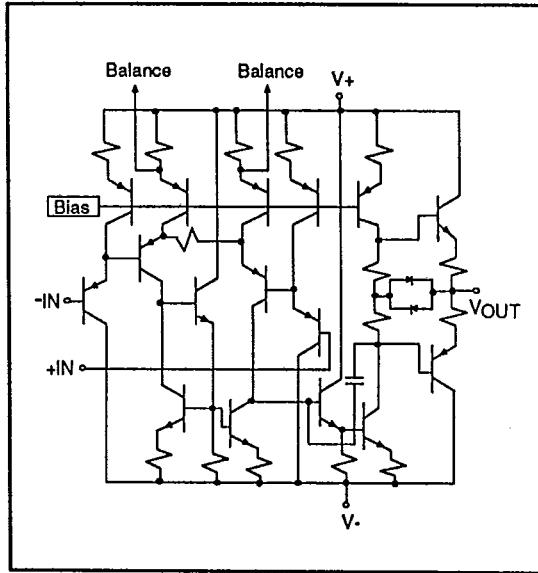
The 22dB (12.6 V/V) crossover frequency at 22MHz is achieved without feed forward compensation, a technique which can produce long tails in the recovery characteristics. The single pole rolloff follows the classic 20dB/decade slope to frequencies approaching 50MHz. The 22dB (12.6 V/V) phase margin of 48°, even with a capacitive load of 50pF, gives stable and predictable performance down to non-inverting gain configurations of approximately 12 V/V. At frequencies beyond 50MHz, the 20dB/decade slope is disturbed by additional poles as well as on output stage zero, the damping factor of which is dependent upon the R_L , C_L combination. For example, at $R_L = 2K$ and $C_L = 50pF$ an 8dB peak in the open loop characteristics results in a small amount of 100MHz ring for step response inputs.

Figure 3 shows a blow up of the open loop characteristics in the 10MHz to 200 MHz frequency range, as well as the corresponding closed loop characteristics for a gain of 12 V/V non-inverting amplifier under the same load conditions. Corresponding small signal step response characteristics show well behaved pulse waveforms with 16-33% overshoot. As expected a small amount of 100MHz ring is present at $R_L = 2K$, $C_L = 50pF$.

Layout Considerations

As with any high-speed wideband amplifier, certain layout considerations are necessary to ensure stable operation. All connections to the amplifier should be kept as short as possible, and the power supplies bypassed with $0.1\mu F$ capacitors to signal ground. It is suggested that a ground plane be considered as the best method for ensuring stability because it minimizes stray inductance and unwanted coupling in the ground signal paths.

To minimize capacitive effects, resistor values should be kept as small as possible, consistent with the application.

SIMPLIFIED SCHEMATIC

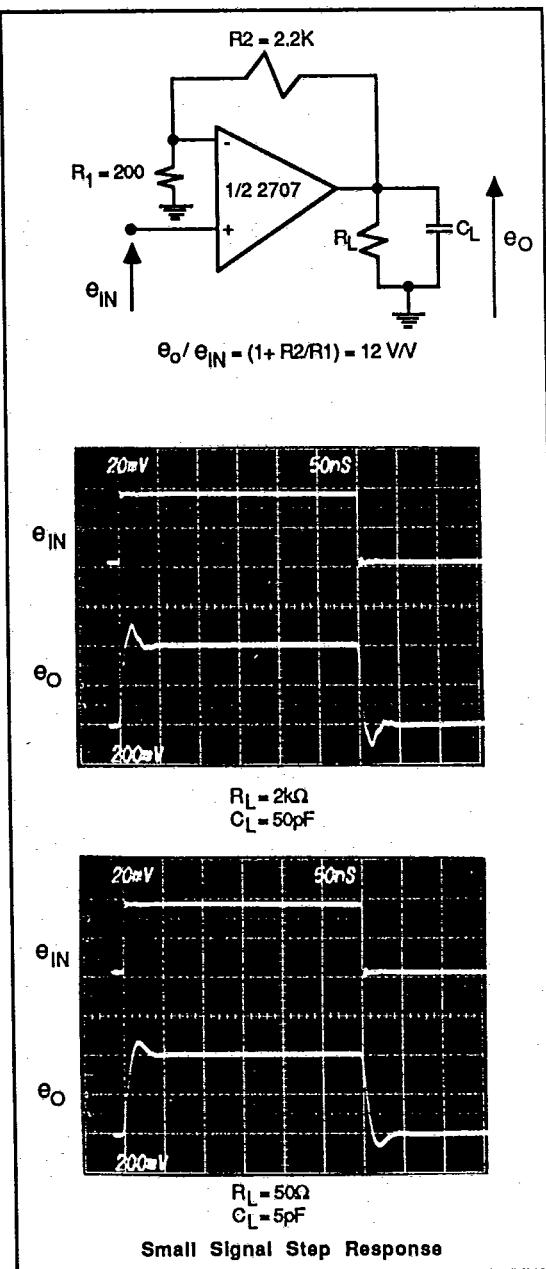
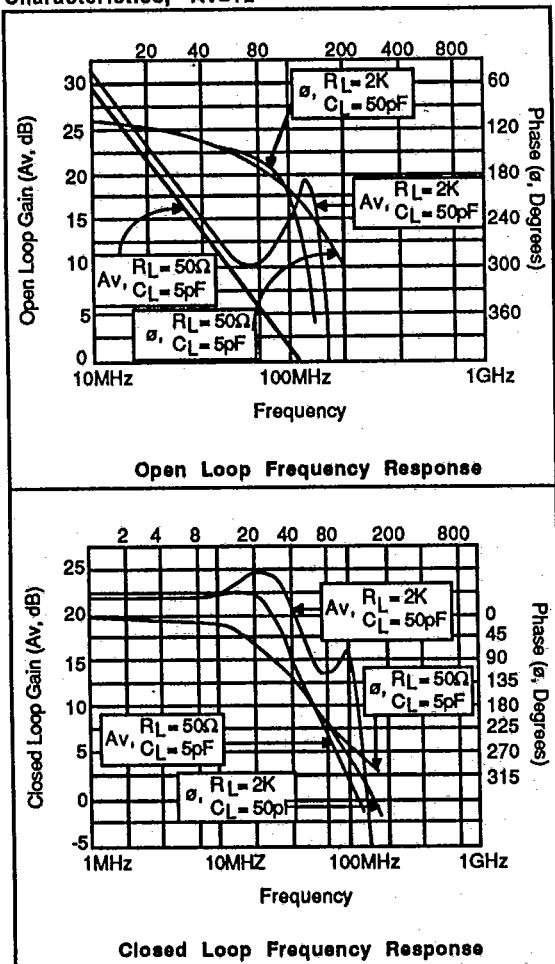
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Figure 3: Frequency and Time Domain Response Characteristics, Av=12

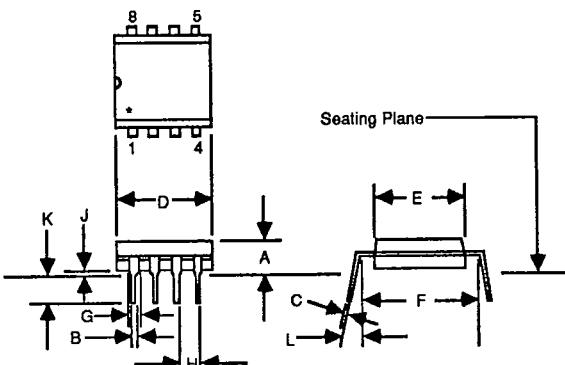


LSP FAMILY DATA
SHEETS

PACKAGE INFORMATION

8 PIN PLASTIC DIP

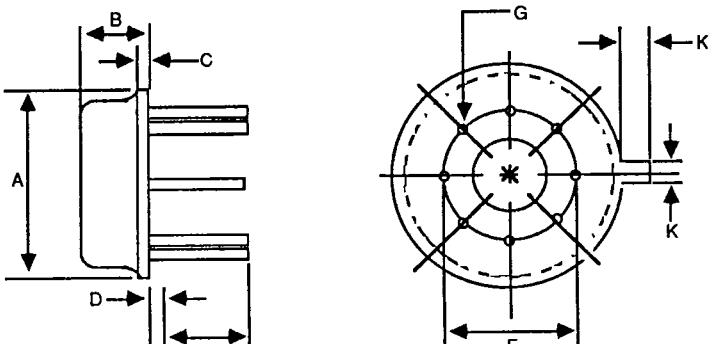
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.148	0.152	3.76	3.86
B	0.016	0.020	0.41	0.51
C	0.008	0.012	0.20	0.30
D	0.370	0.390	9.40	9.91
E	0.245	0.265	6.22	6.73
F	0.290	0.310	7.37	7.87
G	0.050	0.070	1.27	1.78
H	0.090	0.110	2.29	2.79
J	0.128	0.132	3.25	3.35
K	0.020	0.040	0.51	1.02
L	0.030	0.050	0.76	1.27
	0°	15°	0°	15°



*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

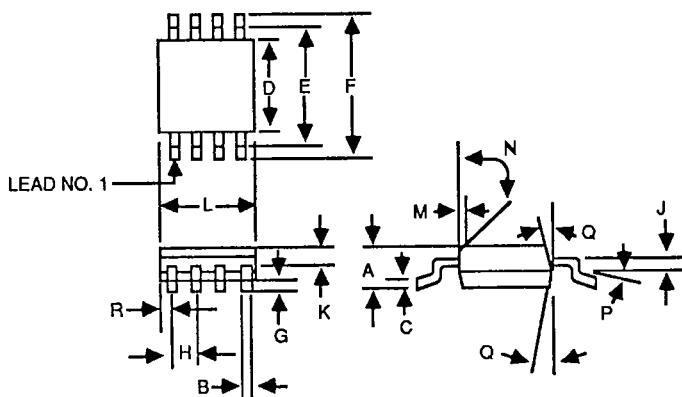
8 PIN METAL CAN

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	.345	.365	8.76	9.27
B	.165	.185	4.19	4.70
C	.020	.040	0.51	1.02
D	.010	.045	0.25	1.14
E	.500	.550	12.70	13.97
F	.200	BSC	5.08	BSC
G	.016	.021	0.41	0.53
J	.027	.045	0.69	1.14
K	.027	.034	0.69	0.86



8-PIN SOIC, PLASTIC

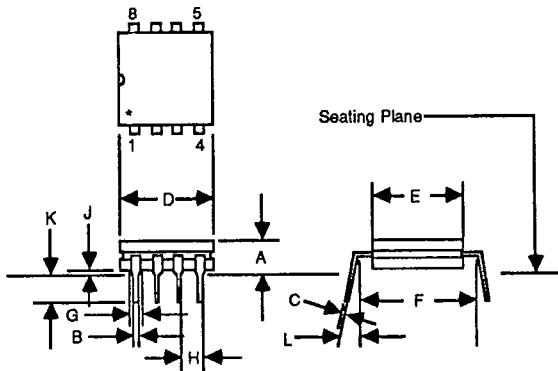
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	.053	.069	1.35	1.75
B	.014	.018	0.35	0.45
C	.007	.009	0.19	0.22
D	.150	.158	3.8	4.0
E	.181	.205	4.6	5.2
F	.228	.244	5.8	6.2
G	.004	.008	0.10	0.20
H	.50	BSC	1.27	BSC
J	.025	.030	0.64	0.77
K	.024	.031	0.61	0.78
L	.188	.197	4.8	5.0
M	.015	BSC	0.37	BSC
N	—	45°	—	45°
P	3°	6°	3°	6°
Q	—	7°	—	7°
R	.019	.022	0.49	0.56



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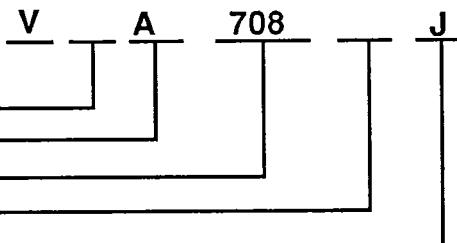
VA708

8 PIN CERAMIC DIP				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	—	0.200	—	5.08
B	0.014	0.023	0.36	0.58
C	0.008	0.015	0.20	0.38
D	—	1.060	—	26.92
E	0.220	0.310	5.59	7.87
F	0.290	0.320	7.37	8.13
G	0.030	0.070	0.76	1.78
H	0.090	0.110	2.29	2.79
J	0.015	0.060	0.38	1.52
K	0.125	0.200	3.18	5.08
L	0°	15°	0°	15°



*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

ORDERING INFORMATION:



Additional Processing _____

Family _____

Model _____

Package _____

Temperature _____

Range/Performance _____

ADDITIONAL PROCESSING

Blank = No Burn-In B = Burn-In (168 Hours, $T_j = 150^\circ\text{C}$ or equivalent)

PACKAGE TYPE

D = Cerdip P = Plastic Dip T = Metal Can X = Die PO = SOIC

TEMPERATURE RANGE/PERFORMANCE

J thru K = Commercial (0° to 70°C)

T = Military (-55°C to $+125^\circ\text{C}$)

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