

**8-BIT SINGLE-CHIP MICROCONTROLLER****DESCRIPTION**

The  $\mu$ PD78P064B is a product of  $\mu$ PD78064B subseries in 78K/0 series, in which the on-chip mask ROM of the  $\mu$ PD78064B is replaced by one-time PROM.

As program write by user is possible, the  $\mu$ PD78P064B is best suited for evaluation, short-run and multiple-device production, and early rise upon system development.

Functions are described in detail in the following User's Manuals, which should be read when carrying out design work.

$\mu$ PD78064B Subseries User's Manual: U10785E  
78K/0 Series User's Manual Instruction: U12326E

**FEATURES**

- Pin compatible with mask ROM products (except the  $V_{PP}$  pin)
- Internal PROM: 32K bytes  
One-time programming possible (most suitable for small-scale production)
- Internal high-speed RAM: 1024 bytes
- LCD display RAM:  $40 \times 4$  bits
- Operable in the same supply voltage as mask ROM products ( $V_{DD} = 2.0$  to  $6.0$  V)
- Corresponding to QTOP™ microcomputers

**Remarks 1.** For the differences between PROM products and mask ROM products, refer to **1. DIFFERENCES BETWEEN  $\mu$ PD78P064B AND MASK ROM PRODUCTS.**

- 2.** QTOP Microcomputer is the general name for a total support as far as writing service, marking, screening, and verification after programming one-time PROM internal signal-chip microcontroller offered by NEC.

**ORDERING INFORMATION**

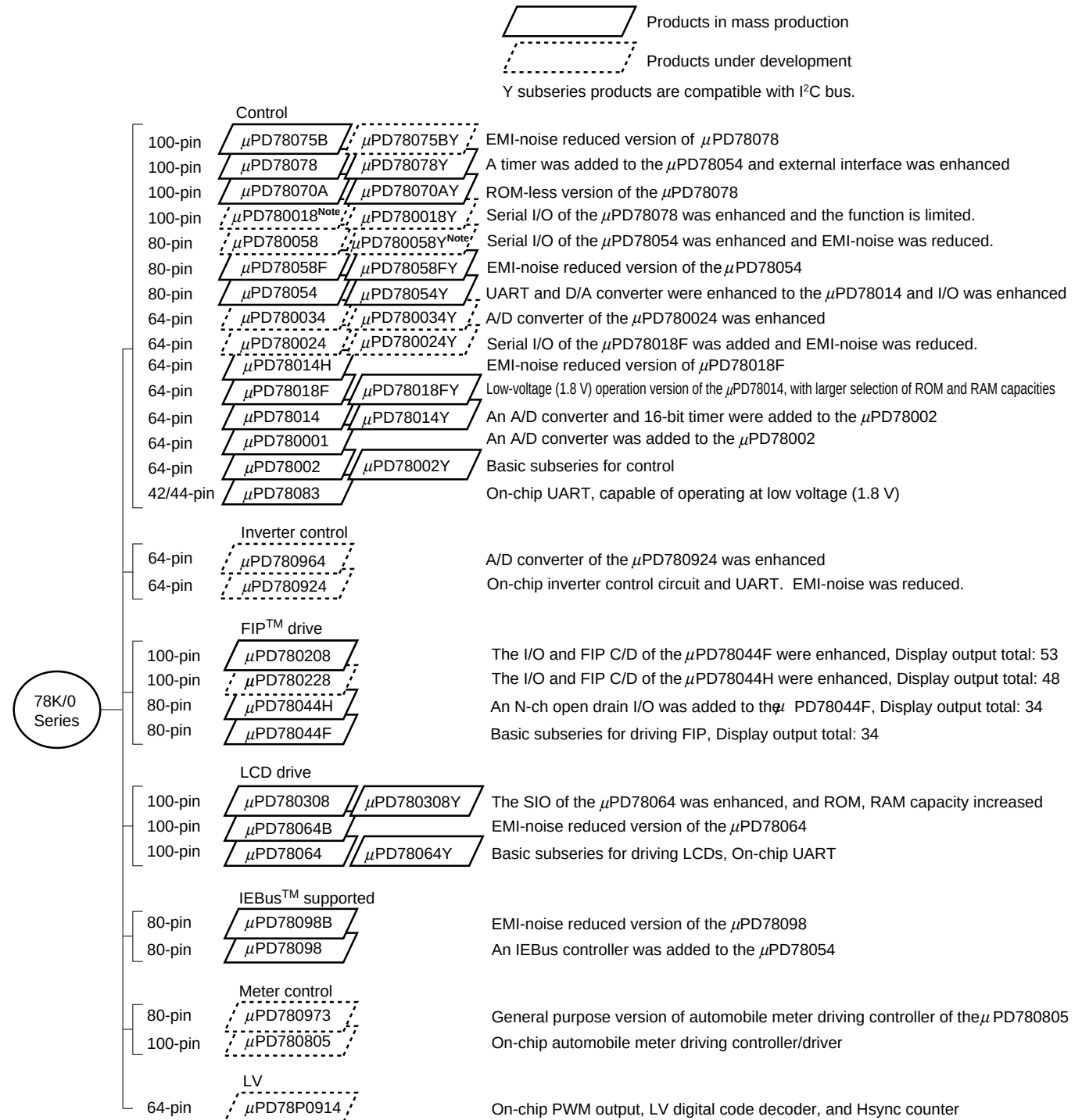
|   | Part Number           | Package                                                | On-Chip ROM   |
|---|-----------------------|--------------------------------------------------------|---------------|
|   | $\mu$ PD78P064BGC-7EA | 100-pin plastic QFP (fine pitch) ( $14 \times 14$ mm)  | One-time PROM |
| ★ | $\mu$ PD78P064BGC-8EU | 100-pin plastic LQFP (fine pitch) ( $14 \times 14$ mm) | One-time PROM |
|   | $\mu$ PD78P064BGF-3BA | 100-pin plastic QFP ( $14 \times 20$ mm)               | One-time PROM |

**Caution** The  $\mu$ PD78P064BGC has two types of package. (Refer to 7. PACKAGE DRAWINGS). For the package suppliable to your device, consult NEC sales personnels.

The information in this document is subject to change without notice.

# ★ 78K/0 SERIES DEVELOPMENT

The following shows the products organized according to usage. The names in the parallelograms are subseries names.



**Note** Under planning

The following lists the main functional differences between subseries products.

| Function<br>Subseries Name |            | ROM<br>Capacity | Timer |                 |       |                                 | 8-bit | 10-bit | 8-bit | Serial Interface              | I/O   | V <sub>DD</sub> MIN.<br>Value | External<br>Expansion |                                               |
|----------------------------|------------|-----------------|-------|-----------------|-------|---------------------------------|-------|--------|-------|-------------------------------|-------|-------------------------------|-----------------------|-----------------------------------------------|
|                            |            |                 | 8-bit | 16-bit          | Watch | WDT                             | A/D   | A/D    | D/A   |                               |       |                               |                       |                                               |
| Control                    | μPD78075B  | 32K-40K         | 4ch   | 1ch             | 1ch   | 1ch                             | 8ch   | –      | 2ch   | 3ch (UART: 1ch)               | 88    | 1.8 V                         | ○                     |                                               |
|                            | μPD78078   | 48K-60K         |       |                 |       |                                 |       |        |       |                               | 61    | 2.7 V                         |                       |                                               |
|                            | μPD78070A  | –               |       |                 |       |                                 |       |        |       |                               |       |                               |                       |                                               |
|                            | μPD780018  | 48K-60K         | 2ch   | –               | 2ch   | 3ch (time division 3-wire: 1ch) | 88    | 1.8 V  |       |                               |       |                               |                       |                                               |
|                            | μPD780058  | 24K-60K         |       |                 |       |                                 | 68    |        | 1.8 V |                               |       |                               |                       |                                               |
|                            | μPD78058F  | 48K-60K         |       |                 |       |                                 |       |        |       | 69                            | 2.7 V |                               |                       |                                               |
|                            | μPD78054   | 16K-60K         |       |                 |       |                                 | –     |        | 2.0 V |                               |       |                               |                       |                                               |
|                            | μPD780034  | 8K-32K          |       |                 |       |                                 |       |        |       | –                             | 8ch   | –                             |                       | 3ch (UART: 1ch,<br>time division 3-wire: 1ch) |
|                            | μPD780024  |                 |       |                 |       |                                 | 8ch   |        | –     |                               |       |                               |                       |                                               |
|                            | μPD78014H  |                 |       |                 |       |                                 |       |        |       |                               |       |                               |                       |                                               |
|                            | μPD78018F  | 8K-60K          | –     | 2.7 V           |       |                                 |       |        |       |                               |       |                               |                       |                                               |
|                            | μPD78014   | 8K-32K          |       |                 |       |                                 |       |        |       |                               |       |                               |                       |                                               |
|                            | μPD780001  | 8K              |       |                 | 39    | –                               |       |        |       |                               |       |                               |                       |                                               |
|                            | μPD78002   | 8K-16K          |       |                 |       |                                 | 53    | ○      |       |                               |       |                               |                       |                                               |
|                            | μPD78083   |                 | 8ch   | 1ch (UART: 1ch) | 33    | 1.8 V                           |       |        | –     |                               |       |                               |                       |                                               |
| Inverter<br>control        | μPD780964  | 8K-32K          | 3ch   | <b>Note</b>     | –     | 1ch                             | –     | 8ch    | –     | 2ch (UART: 2ch)               | 47    | 2.7 V                         | ○                     |                                               |
|                            | μPD780924  |                 |       |                 |       |                                 | 8ch   | –      |       |                               |       |                               |                       |                                               |
| FIP<br>drive               | μPD780208  | 32K-60K         | 2ch   | 1ch             | 1ch   | 1ch                             | 8ch   | –      | –     | 2ch                           | 74    | 2.7 V                         | –                     |                                               |
|                            | μPD780228  | 48K-60K         |       |                 |       |                                 |       |        |       | 3ch                           | –     | –                             |                       | 1ch                                           |
|                            | μPD78044H  | 32K-48K         | 2ch   | 1ch             | 1ch   | –                               | –     | 2ch    | 68    | 2.7 V                         |       |                               |                       |                                               |
|                            | μPD78044F  | 16K-40K         |       |                 |       |                                 |       |        |       |                               |       |                               |                       |                                               |
| LCD<br>drive               | μPD780308B | 48K-60K         | 2ch   | 1ch             | 1ch   | 1ch                             | 8ch   | –      | –     | 3ch (time division UART: 1ch) | 57    | 2.0 V                         | –                     |                                               |
|                            | μPD78064   | 32K             |       |                 |       |                                 |       |        |       | 2ch (UART: 1ch)               |       |                               |                       |                                               |
|                            | μPD78064   | 16K-32K         |       |                 |       |                                 |       |        |       |                               |       |                               |                       |                                               |
| IEBus<br>supported         | μPD78098B  | 40K-60K         | 2ch   | 1ch             | 1ch   | 1ch                             | 8ch   | –      | 2ch   | 3ch (UART: 1ch)               | 69    | 2.7 V                         | ○                     |                                               |
|                            | μPD78098   | 32K-60K         |       |                 |       |                                 |       |        |       |                               |       |                               |                       |                                               |
| Meter<br>control           | μPD780973  | 24K-32K         | 3ch   | 1ch             | 1ch   | 1ch                             | 5ch   | –      | –     | 2ch (UART: 1ch)               | 56    | 4.5 V                         | –                     |                                               |
|                            | μPD780805  | 40K-60K         |       |                 |       |                                 | 2ch   |        |       |                               | 8ch   | 39                            |                       | 2.7 V                                         |
| LV                         | μPD78P0914 | 32K             | 6ch   | –               | –     | 1ch                             | 8ch   | –      | –     | 2ch                           | 54    | 4.5 V                         | ○                     |                                               |

**Note** 10-bit timer: 1 channel

## FUNCTION DESCRIPTION

| Item                                                                |                                    | Function                                                                                                                                                                                                                              |
|---------------------------------------------------------------------|------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Internal memory                                                     |                                    | <ul style="list-style-type: none"> <li>PROM : 32 K bytes</li> <li>RAM</li> <li>High-speed RAM : 1024 bytes<sup>Note</sup></li> <li>LCD display RAM : 40 × 4 bits</li> </ul>                                                           |
| General-purpose register                                            |                                    | 8 bits × 32 registers (8 bits × 8 registers × 4 banks)                                                                                                                                                                                |
| Instruction cycles                                                  | When main system clock is selected | 0.4 $\mu$ s/0.8 $\mu$ s/1.6 $\mu$ s/3.2 $\mu$ s/6.4 $\mu$ s/12.8 $\mu$ s (when operating at 5.0 MHz)                                                                                                                                  |
|                                                                     | When subsystem clock is selected   | 122 $\mu$ s (when operating at 32.768 kHz)                                                                                                                                                                                            |
| Instruction set                                                     |                                    | <ul style="list-style-type: none"> <li>16-bit operation</li> <li>Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits)</li> <li>Bit manipulation (set, reset, test, boolean operation)</li> <li>BCD correction, etc.</li> </ul> |
| I/O ports<br>[ Include segment signal<br>output dual-function pin ] |                                    | <u>Total</u> : 57<br><ul style="list-style-type: none"> <li>CMOS input : 2</li> <li>CMOS input/output : 55</li> </ul>                                                                                                                 |
| A/D converter                                                       |                                    | <ul style="list-style-type: none"> <li>8-bit resolution × 8 ch</li> </ul>                                                                                                                                                             |
| LCD controller/driver                                               |                                    | <ul style="list-style-type: none"> <li>Segment signal output : 40 max.</li> <li>Common signal output : 4 max.</li> <li>Bias : 1/2, 1/3, Bias switchable</li> </ul>                                                                    |
| Serial interface                                                    |                                    | <ul style="list-style-type: none"> <li>3-wire serial I/O/SBI/2-wire serial I/O mode selectable : 1 ch</li> <li>3-wire serial I/O/UART mode selectable : 1 ch</li> </ul>                                                               |
| Timer                                                               |                                    | <ul style="list-style-type: none"> <li>16-bit timer/event counter : 1 ch</li> <li>8-bit timer/event counter : 2 ch</li> <li>Watch timer : 1 ch</li> <li>Watchdog timer : 1 ch</li> </ul>                                              |
| Timer output                                                        |                                    | 3 pins (14-bit PWM output enable 1 pin)                                                                                                                                                                                               |
| Clock output                                                        |                                    | 19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5.0 MHz (when operating at main system clock 5.0 MHz), 32.768 kHz (when operating at subsystem clock 32.768 kHz)                                          |
| Buzzer output                                                       |                                    | 1.2 kHz, 2.4 kHz, 4.9 kHz, 9.8 kHz (when operating at main system clock 5.0 MHz)                                                                                                                                                      |
| Vectored interrupt sources                                          | Maskable                           | Internal : 12, External : 6                                                                                                                                                                                                           |
|                                                                     | Non-maskable                       | Internal : 1                                                                                                                                                                                                                          |
|                                                                     | Software                           | 1                                                                                                                                                                                                                                     |
| Test input                                                          |                                    | Internal : 1, External : 1                                                                                                                                                                                                            |
| Supply voltage                                                      |                                    | V <sub>DD</sub> = 2.0 to 6.0 V                                                                                                                                                                                                        |
| Package                                                             |                                    | <ul style="list-style-type: none"> <li>100-pin plastic (fine pitch) QFP (14 × 14 mm)</li> <li>100-pin plastic LQFP (fine pitch) (14 × 14 mm)</li> <li>100-pin plastic QFP (14 × 20 mm)</li> </ul>                                     |

★

## PIN CONFIGURATION (Top View)

## (1) Normal operating mode

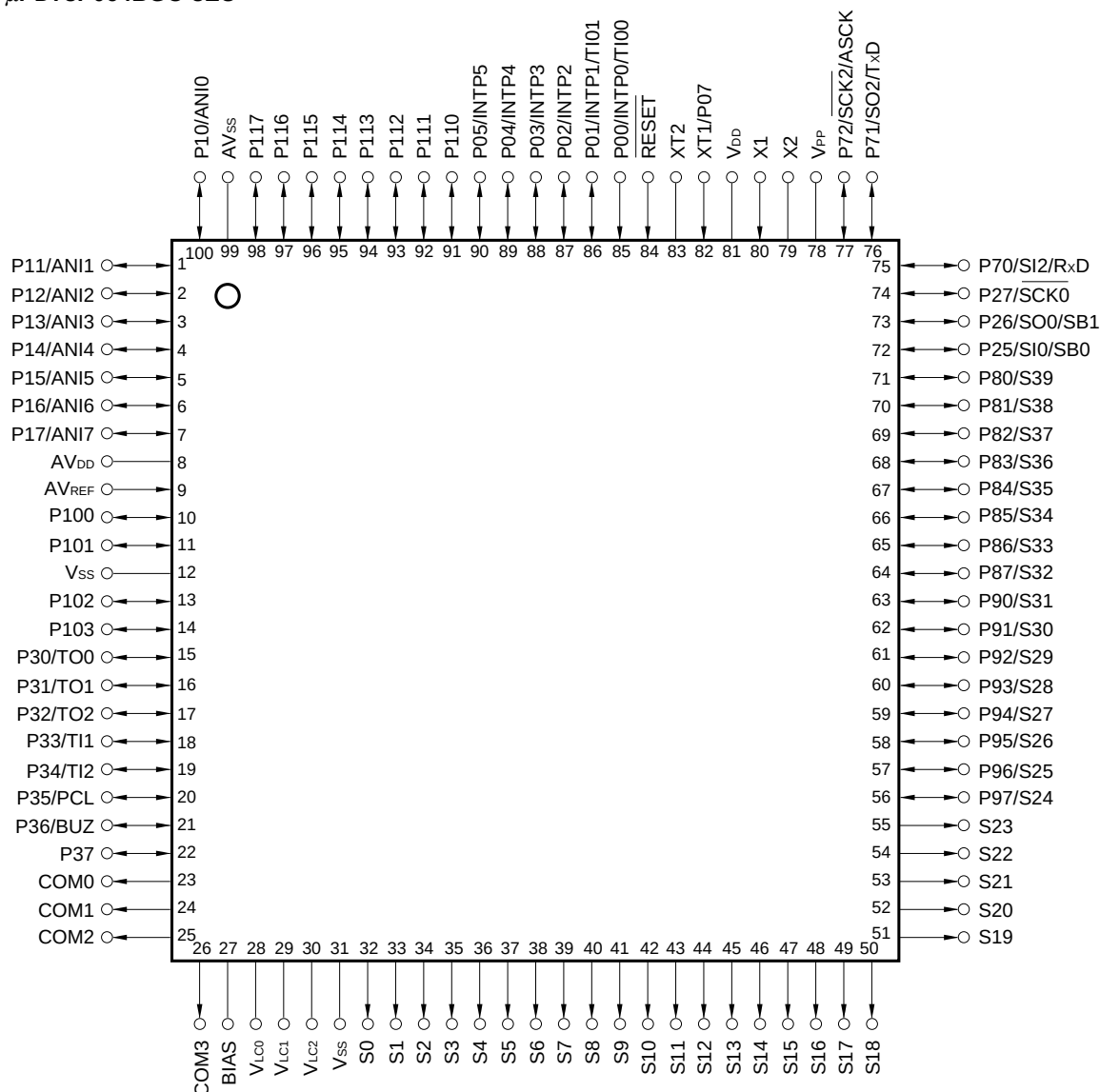
- 100-pin plastic QFP (fine pitch) (14 × 14 mm)

μPD78P064BGC-7EA

★

- 100-pin plastic LQFP (fine pitch) (14 × 14 mm)

μPD78P064BGC-8EU



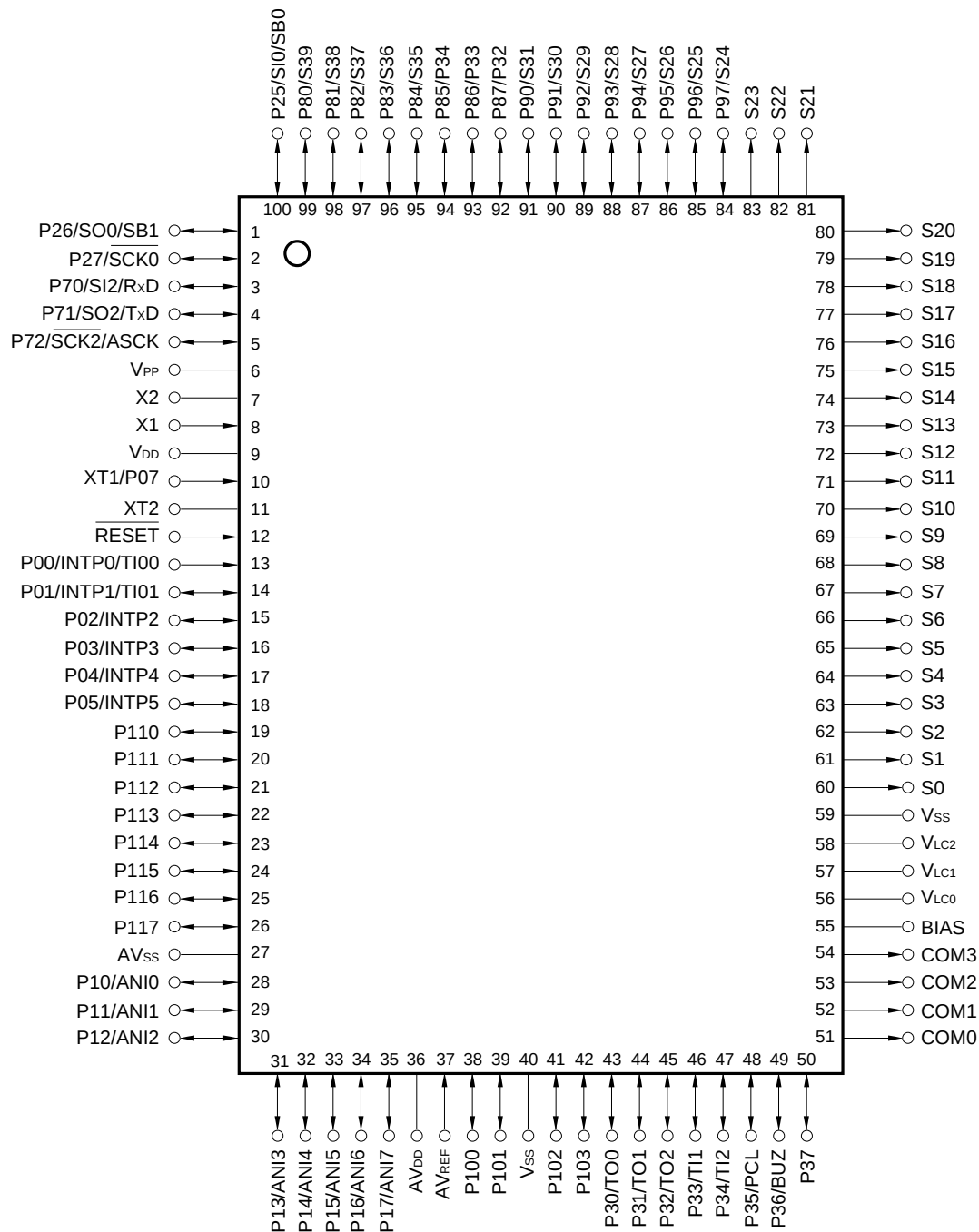
**Cautions** 1. Connect V<sub>PP</sub> pin directly to V<sub>SS</sub>.

2. AV<sub>DD</sub> pin shares the port power supply with that of the A/D converter. When using in applications where noise from inside the microcomputer has to be reduced, connect the AV<sub>DD</sub> pin to a separate power supply, whose electrical potential is the same as that of V<sub>DD</sub>.

3. AV<sub>SS</sub> pin shares the port GND with that of the A/D converter. When using in applications where noise from inside the microcomputer has to be reduced, connect the AV<sub>SS</sub> pin to a separate ground line.

- 100-pin plastic QFP (14 × 20 mm)

$\mu$ PD78P068BGF-3BA

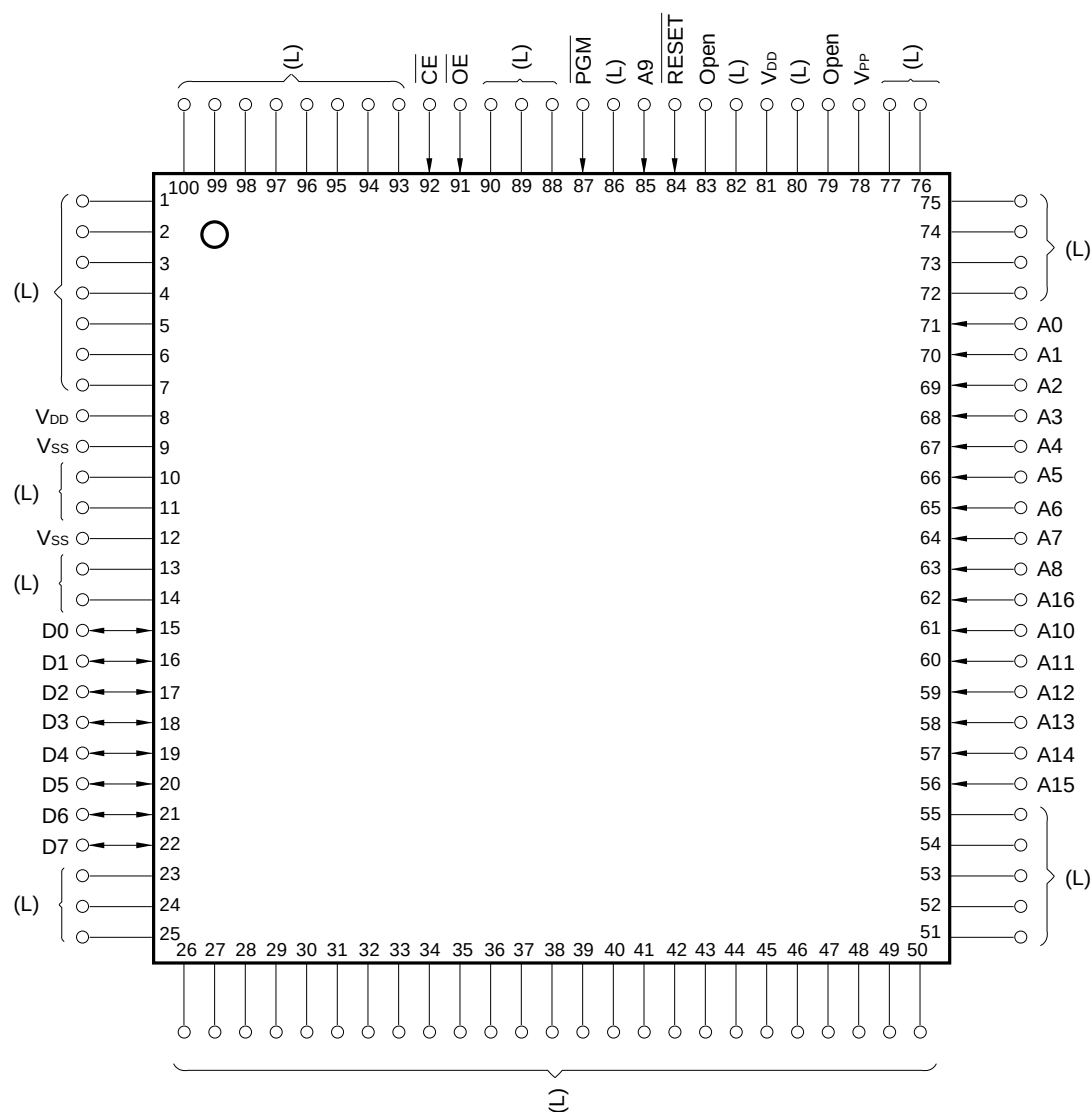


- Cautions**
1. Connect  $V_{PP}$  pin directly to  $V_{SS}$ .
  2.  $AV_{DD}$  pin shares the port power supply with that of the A/D converter. When using in applications where noise from inside the microcomputer has to be reduced, connect the  $AV_{DD}$  pin to a separate power supply, whose electrical potential is the same as that of  $V_{DD}$ .
  3.  $AV_{SS}$  pin shares the port GND with that of the A/D converter. When using in applications where noise from inside the microcomputer has to be reduced, connect the  $AV_{SS}$  pin to a separate ground line.

|                   |                                 |                                                  |                               |
|-------------------|---------------------------------|--------------------------------------------------|-------------------------------|
| ANIO-ANI7         | : Analog Input                  | PCL                                              | : Programmable Clock          |
| ASCK              | : Asynchronous Serial Clock     | $\overline{\text{RESET}}$                        | : Reset                       |
| AV <sub>DD</sub>  | : Analog Power Supply           | RxD                                              | : Receive Data                |
| AV <sub>REF</sub> | : Analog Reference Voltage      | S0-S39                                           | : Segment Output              |
| AV <sub>SS</sub>  | : Analog Ground                 | SB0, SB1                                         | : Serial Bus                  |
| BIAS              | : LCD Power Supply Bias Control | SI0, SI2                                         | : Serial Input                |
| BUZ               | : Buzzer Clock                  | SO0, SO2                                         | : Serial Output               |
| COM0-COM3         | : Common Output                 | $\overline{\text{SCK0}}, \overline{\text{SCK2}}$ | : Serial Clock                |
| INTP0-INTP5       | : Interrupt from Peripherals    | TI00, TI01                                       | : Timer Input                 |
| P00-P05, P07      | : Port 0                        | TI1, TI2                                         | : Timer Input                 |
| P10-P17           | : Port 1                        | TO0-TO2                                          | : Timer Output                |
| P25-P27           | : Port 2                        | TxD                                              | : Transmit Data               |
| P30-P37           | : Port 3                        | V <sub>DD</sub>                                  | : Power Supply                |
| P70-P72           | : Port 7                        | V <sub>LC0</sub> -V <sub>LC2</sub>               | : LCD Power Supply            |
| P80-P87           | : Port 8                        | V <sub>SS</sub>                                  | : Ground                      |
| P90-P97           | : Port 9                        | V <sub>PP</sub>                                  | : Programming Power Supply    |
| P100-P103         | : Port 10                       | X1, X2                                           | : Crystal (Main System Clock) |
| P110-P117         | : Port 11                       | XT1, XT2                                         | : Crystal (Subsystem Clock)   |

## (2) PROM programming mode

- 100-pin plastic QFP (fine pitch) (14 × 14 mm)  
μPD78P064BGC-7EA
- 100-pin plastic LQFP (fine pitch) (14 × 14 mm)  
★ μPD78P064BGC-8EU

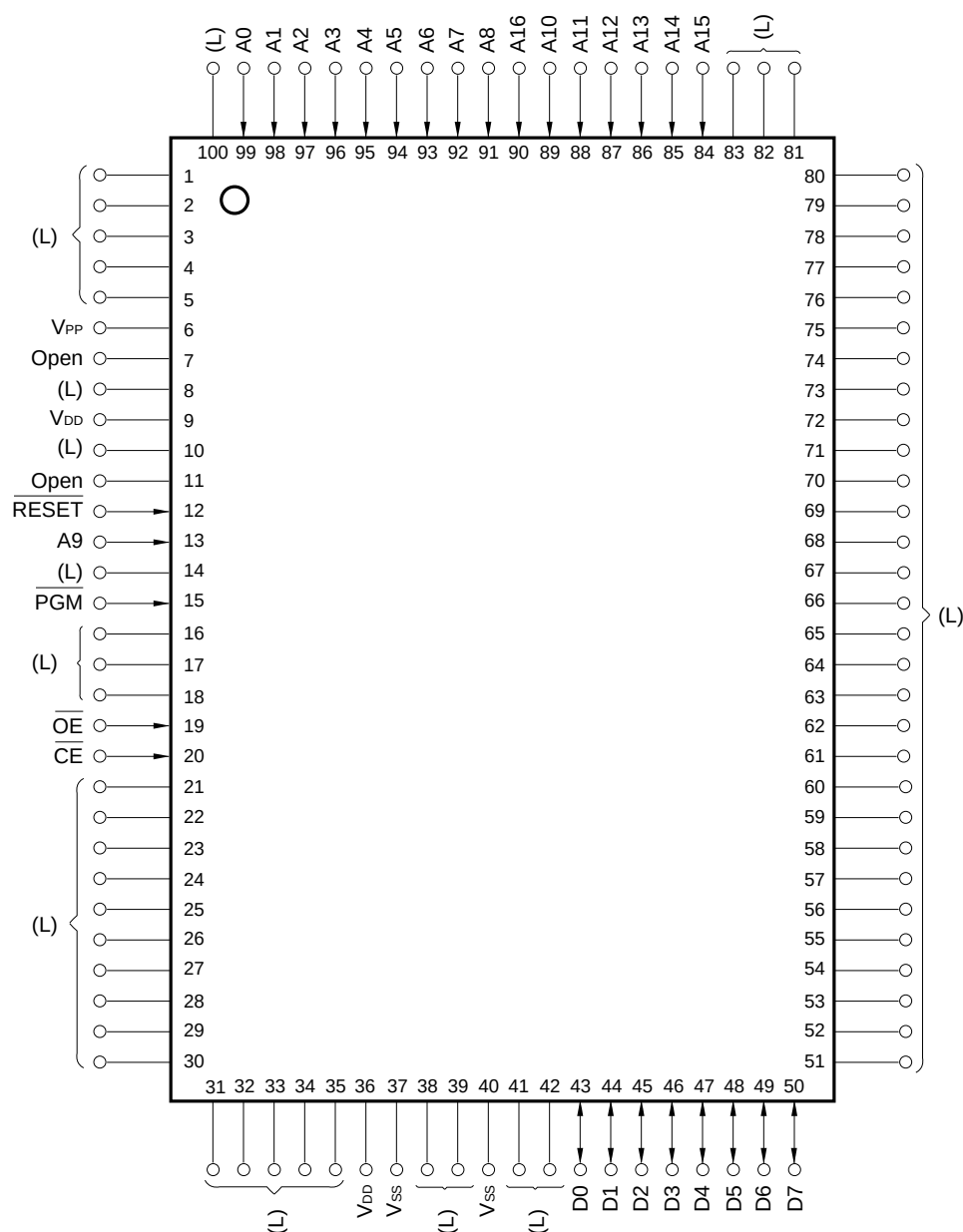


- Cautions**
1. (L) : Individually connect to Vss via a pull-down resistor.
  2. Vss : Connect to GND.
  3. RESET : Set to low level.
  4. Open : No connection



- 100-pin plastic QFP (14 × 20 mm)

μPD78P064BGF-3BA

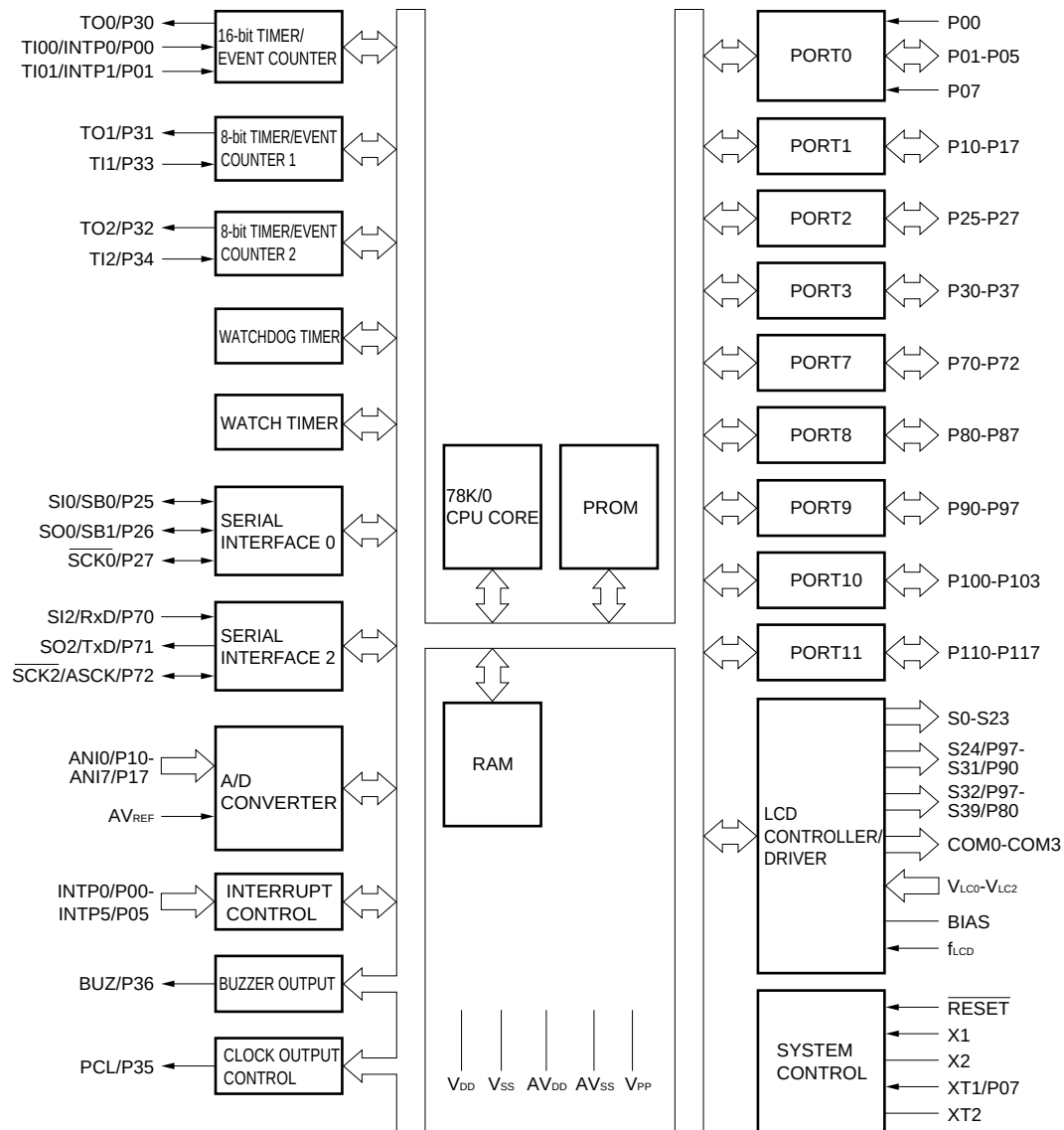


- Cautions**
1. (L) : Individually connect to V<sub>SS</sub> via a pull-down resistor.
  2. V<sub>SS</sub> : Connect to GND.
  3.  $\overline{\text{RESET}}$  : Set to low level.
  4. Open : No connection

A0 to A16 : Address Bus  
 $\overline{\text{CE}}$  : Chip Enable  
 D0 to D7 : Data Bus  
 $\overline{\text{OE}}$  : Output Enable  
 PGM : Program

$\overline{\text{RESET}}$  : Reset  
 V<sub>DD</sub> : Power Supply  
 V<sub>PP</sub> : Programming Power Supply  
 V<sub>SS</sub> : Ground

# BLOCK DIAGRAM



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## 1. DIFFERENCES BETWEEN $\mu$ PD78P064B AND MASK ROM PRODUCTS

The  $\mu$ PD78P064B is a single-chip microcontroller with an on-chip one-time writable PROM.

It is possible to make all the functions exception PROM specification, and mask option of LCD drive power supply dividing resistor, to the same as those of mask ROM products by setting the memory size switching register (IMS).

Difference between the PROM product ( $\mu$ PD78P064B) and mask ROM product ( $\mu$ PD78064B) are shown in Table 1-1.

**Table 1-1. Differences between  $\mu$ PD78P064B and Mask ROM Products**

| Item                                                    | $\mu$ PD78P064B                      | Mask ROM Products |
|---------------------------------------------------------|--------------------------------------|-------------------|
| Internal ROM structure                                  | One-time PROM                        | Mask ROM          |
| IC pin                                                  | No                                   | Yes               |
| V <sub>PP</sub> pin                                     | Yes                                  | No                |
| Mask option of LCD drive power supply dividing resistor | No                                   | Yes               |
| Electrical characteristics                              | Refer to Data Sheet for each product |                   |

★ **Caution** Noise resistance and noise radiation are different in PROM version and mask ROM versions. If using a mask ROM version instead of the PROM version for processes between prototype development and full production, be sure to fully evaluate the CS of the mask ROM version (not ES).

**Remark** The internal PROM becomes to 32K bytes and the internal high-speed RAM becomes 1024 bytes by the  $\overline{\text{RESET}}$  input.

## 2. PIN FUNCTION TABLE

### 2.1 PINS IN NORMAL OPERATING MODE

#### (1) PORT PINS (1/2)

| Pin Name              | Input/Output | Function                                                                                                                                                                          |                                                                                                                            | After Reset | Dual-Function Pin              |
|-----------------------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------|-------------|--------------------------------|
| P00                   | Input        | Port 0<br>7-bit input/output port                                                                                                                                                 | Input only                                                                                                                 | Input       | INTP0/TI00                     |
| P01                   | Input/output |                                                                                                                                                                                   | Input/output is specifiable bit-wise.<br>When used as the input port, an on-chip pull-up resistor can be used by software. | Input       | INTP1/TI01                     |
| P02                   |              |                                                                                                                                                                                   |                                                                                                                            |             | INTP2                          |
| P03                   |              |                                                                                                                                                                                   |                                                                                                                            |             | INTP3                          |
| P04                   |              |                                                                                                                                                                                   |                                                                                                                            |             | INTP4                          |
| P05                   |              |                                                                                                                                                                                   |                                                                                                                            |             | INTP5                          |
| P07 <sup>Note 1</sup> | Input        |                                                                                                                                                                                   | Input only                                                                                                                 | Input       | XT1                            |
| P10 to P17            | Input/output | Port 1<br>8-bit input/output port<br>Input/output is specifiable bit-wise.<br>When used as the input port, an on-chip pull-up resistor can be used by software. <sup>Note 2</sup> |                                                                                                                            | Input       | ANI0 to ANI7                   |
| P25                   | Input/output | Port 2<br>3-bit input/output port<br>Input/output is specifiable bit-wise.<br>When used as the input port, an on-chip pull-up resistor can be used by software.                   |                                                                                                                            | Input       | SI0/SB0                        |
| P26                   |              |                                                                                                                                                                                   |                                                                                                                            |             | SO0/SB1                        |
| P27                   |              |                                                                                                                                                                                   |                                                                                                                            |             | $\overline{\text{SCK0}}$       |
| P30                   | Input/output | Port 3<br>8-bit input/output port<br>Input/output is specifiable bit-wise.<br>When used as the input port, an on-chip pull-up resistor can be used by software.                   |                                                                                                                            | Input       | TO0                            |
| P31                   |              |                                                                                                                                                                                   |                                                                                                                            |             | TO1                            |
| P32                   |              |                                                                                                                                                                                   |                                                                                                                            |             | TO2                            |
| P33                   |              |                                                                                                                                                                                   |                                                                                                                            |             | TI1                            |
| P34                   |              |                                                                                                                                                                                   |                                                                                                                            |             | TI2                            |
| P35                   |              |                                                                                                                                                                                   |                                                                                                                            |             | PCL                            |
| P36                   |              |                                                                                                                                                                                   |                                                                                                                            |             | BUZ                            |
| P37                   |              |                                                                                                                                                                                   |                                                                                                                            |             | —                              |
| P70                   | Input/output | Port 7<br>3-bit input/output port<br>Input/output is specifiable bit-wise.<br>When used as the input port, an on-chip pull-up resistor can be used by software.                   |                                                                                                                            | Input       | SI2/RxD                        |
| P71                   |              |                                                                                                                                                                                   |                                                                                                                            |             | SO2/TxD                        |
| P72                   |              |                                                                                                                                                                                   |                                                                                                                            |             | $\overline{\text{SCK2}}$ /ASCK |

- Notes**
1. When P07/XT1 pins are used as the input ports, set processor clock control register (PCC) bit 6 (FRC) to 1. (Do not use the on-chip feedback resistor of the subsystem clock oscillation circuit.)
  2. When P10/ANI0 to P17/ANI7 pins are used as the analog inputs for A/D converter, set port 1 to input mode. The on-chip pull-up resistor is automatically disabled.

## (1) PORT PINS (2/2)

| Pin Name     | Input/Output | Function                                                                                                                                                                                                                                                                                 | After Reset | Dual-Function Pin |
|--------------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|-------------------|
| P80 to P87   | Input/output | Port 8<br>8-bit input/output port<br>Input/output is specifiable bit-wise.<br>When used as the input port, an on-chip pull-up resistor can be used by software.<br>Input/output port/segment signal output function specifiable in 2-bit units by LCD display control register (LDCD).   | Input       | S39 to S32        |
| P90 to P97   | Input/output | Port 9<br>8-bit input/output port.<br>Input/output is specifiable bit-wise.<br>When used as the input port, an on-chip pull-up resistor can be used by software.<br>Input/output port/segment signal output function specifiable in 2-bit units by LCD display control register. (LDCD). | Input       | S31 to S24        |
| P100 to P103 | Input/output | Port 10<br>4-bit input/output port<br>Input/output is specifiable in bit-wise.<br>When used as the input port, an on-chip pull-up resistor can be used by software.<br>It is possible to directly drive LED.                                                                             | Input       | —                 |
| P110 to P117 | Input/output | Port 11<br>8-bit input/output port<br>Input/output is specifiable in bit-wise.<br>When used as the input port, an on-chip pull-up resistor can be used by software.<br>Falling edge detection possible.                                                                                  | Input       | —                 |

**Caution** Do not perform the following operation on the pins shared with port pins during A/D conversion operation; otherwise, the specifications of the total error during A/D conversion cannot be satisfied (except the pins shared with LCD segment output pins).

- (1) Rewriting the output latch of an output pin used as a port pin
- (2) Changing the output level of an output pin even when it is not used as a port pin

## (2) PINS OTHER THAN PORT PINS (1/2)

| Pin Name                             | Input/Output | Function                                                                                                                      | After Reset | Dual-Function Pin             |
|--------------------------------------|--------------|-------------------------------------------------------------------------------------------------------------------------------|-------------|-------------------------------|
| INTP0                                | Input        | External interrupt request input with specifiable Valid edges (rising edge, falling edge, and both rising and falling edges). | Input       | P00/TI00                      |
| INTP1                                |              |                                                                                                                               |             | P01/TI01                      |
| INTP2                                |              |                                                                                                                               |             | P02                           |
| INTP3                                |              |                                                                                                                               |             | P03                           |
| INTP4                                |              |                                                                                                                               |             | P04                           |
| INTP5                                |              |                                                                                                                               |             | P05                           |
| SI0                                  | Input        | Serial data input of the serial interface                                                                                     | Input       | P25/SB0                       |
| SI2                                  |              |                                                                                                                               |             | P70/RxD                       |
| SO0                                  | Output       | Serial data output of the serial interface                                                                                    | Input       | P26/SB1                       |
| SO2                                  |              |                                                                                                                               |             | P71/TxD                       |
| SB0                                  | Input/output | Serial data input/output of the serial interface                                                                              | Input       | P25/SI0                       |
| SB1                                  |              |                                                                                                                               |             | P26/SO0                       |
| $\overline{\text{SCK0}}$             | Input/output | Serial clock input/output of the serial interface                                                                             | Input       | P27                           |
| $\overline{\text{SCK2}}$             |              |                                                                                                                               |             | P72/ASCK                      |
| RxD                                  | Input        | Serial data input for asynchronouse serial interface                                                                          | Input       | P70/SI2                       |
| TxD                                  | Output       | Serial data output for asynchronous serial interface                                                                          | Input       | P71/SO2                       |
| ASCK                                 | Input        | Serial clock input for asynchronous serial interface                                                                          | Input       | P72/ $\overline{\text{SCK2}}$ |
| TI00                                 | Input        | External count clock input to the 16-bit timer (TM0).                                                                         | Input       | P00/INTP0                     |
| TI01                                 |              | Capture trigger signal input to the capture register (CR00).                                                                  |             | P01/INTP1                     |
| TI1                                  |              | External count clock input to the 8-bit timer (TM1).                                                                          |             | P33                           |
| TI2                                  |              | External count clock input to the 8-bit timer (TM2).                                                                          |             | P34                           |
| TO0                                  | Output       | 16-bit timer (TM0) output (dual-function as 14-bit PWM output)                                                                | Input       | P30                           |
| TO1                                  |              | 8-bit timer (TM1) output                                                                                                      |             | P31                           |
| TO2                                  |              | 8-bit timer (TM2) output                                                                                                      |             | P32                           |
| PCL                                  | Output       | Clock output (for trimming main system clock and subsystem clock)                                                             | Input       | P35                           |
| BUZ                                  | Output       | Buzzer output                                                                                                                 | Input       | P36                           |
| S0 to S23                            | Output       | LCD controller/driver segment signal output                                                                                   | Output      | —                             |
| S24 to S31                           |              |                                                                                                                               | Input       | P97-P90                       |
| S32 to S39                           |              |                                                                                                                               |             | P87-P80                       |
| COM0 to COM3                         | Output       | LCD controller/driver common signal output                                                                                    | Output      | —                             |
| V <sub>LC0</sub> to V <sub>LC2</sub> | —            | LCD drive voltage                                                                                                             | —           | —                             |
| BIAS                                 | —            | LCD drive power supply                                                                                                        | —           | —                             |

## (2) PINS OTHER THAN PORT PINS (2/2)

| Pin Name                  | Input/Output | Function                                                                                                                 | After Reset | Dual-Function Pin |
|---------------------------|--------------|--------------------------------------------------------------------------------------------------------------------------|-------------|-------------------|
| ANI0 to ANI7              | Input        | Analog input of A/D converter                                                                                            | Input       | P10 to P17        |
| AV <sub>REF</sub>         | Input        | Reference voltage input of A/D converter                                                                                 | —           | —                 |
| AV <sub>DD</sub>          | —            | Analog power supply of A/D converter<br>(shared by power supply of port)                                                 | —           | —                 |
| AV <sub>SS</sub>          | —            | Ground potential of A/D converter<br>(shared by ground potential of port)                                                | —           | —                 |
| $\overline{\text{RESET}}$ | Input        | System reset input                                                                                                       | —           | —                 |
| X1                        | Input        | Main system clock oscillation crystal connection                                                                         | —           | —                 |
| X2                        | —            |                                                                                                                          | —           | —                 |
| XT1                       | Input        | Subsystem clock oscillation crystal connection                                                                           | Input       | P07               |
| XT2                       | —            |                                                                                                                          | —           | —                 |
| V <sub>DD</sub>           | —            | Positive power supply (except port)                                                                                      | —           | —                 |
| V <sub>PP</sub>           | —            | High-voltage applied during program write/verification<br>Connected directly to V <sub>SS</sub> in normal operating mode | —           | —                 |
| V <sub>SS</sub>           | —            | Ground potential (except port)                                                                                           | —           | —                 |

- Cautions**
1. AV<sub>DD</sub> pin shares the port power supply with that of the A/D converter. When using in applications where noise from inside the microcomputer has to be reduced, connect the AV<sub>DD</sub> pin to a separate power supply, whose electrical potential is the same as that of V<sub>DD</sub>.
  2. AV<sub>SS</sub> pin shares the port GND with that of the A/D converter. When using in applications where noise from inside the microcomputer has to be reduced, connect the AV<sub>SS</sub> pin to a separate ground line.

## 2.2 PINS IN PROM PROGRAMMING MODE

| Pin Name                  | Input/Output | Function                                                                                                                                                                                                           |
|---------------------------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $\overline{\text{RESET}}$ | Input        | PROM programming mode setting<br>When +5 V or +12.5 V is applied to the V <sub>PP</sub> pin and a low level signal is applied to the $\overline{\text{RESET}}$ pin, this chip is set in the PROM programming mode. |
| V <sub>PP</sub>           | Input        | PROM programming mode setting and high-voltage applied during program write/verification                                                                                                                           |
| A0 to A16                 | Input        | Address bus                                                                                                                                                                                                        |
| D0 to D7                  | Input/output | Data bus                                                                                                                                                                                                           |
| $\overline{\text{CE}}$    | Input        | PROM enable input/program pulse input                                                                                                                                                                              |
| $\overline{\text{OE}}$    | Input        | Read strobe input to PROM                                                                                                                                                                                          |
| $\overline{\text{PGM}}$   | Input        | Program/program inhibit input in PROM programing mode.                                                                                                                                                             |
| V <sub>DD</sub>           | —            | Positive power supply                                                                                                                                                                                              |
| V <sub>SS</sub>           | —            | Ground potential                                                                                                                                                                                                   |



## 2.3 PIN INPUT/OUTPUT CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

Types of input/output circuits of the pins and recommended connection of unused pins are shown in Table 2-1.  
For the configuration of each type of input/output circuit, refer to Figure 2-1.

**Table 2-1. Type of Input/Output Circuit of Each Pin**

| Pin Name                             | Input/Output<br>Circuit Type | I/O    | Recommended Connection<br>When not Used                                                              |
|--------------------------------------|------------------------------|--------|------------------------------------------------------------------------------------------------------|
| P00/INTP0/TI00                       | 2                            | Input  | Connect to V <sub>SS</sub> .                                                                         |
| P01/INTP1/TI01                       | 8-D                          | I/O    | Individually connect to V <sub>SS</sub> via a resistor                                               |
| P02/INTP2                            |                              |        |                                                                                                      |
| P03/INTP3                            |                              |        |                                                                                                      |
| P04/INTP4                            |                              |        |                                                                                                      |
| P05/INTP5                            |                              |        |                                                                                                      |
| P07/XT1                              | 16                           | Input  | Connect to V <sub>DD</sub> .                                                                         |
| P10/ANI0 to P17/ANI7                 | 11-C                         | I/O    | Individually connect to V <sub>DD</sub> or V <sub>SS</sub> via a resistor                            |
| P25/SI0/SB0                          | 10-C                         |        |                                                                                                      |
| P26/SO0/SB1                          |                              |        |                                                                                                      |
| P27/SCK0                             |                              |        |                                                                                                      |
| P30/TO0                              | 5-J                          |        |                                                                                                      |
| P31/TO1                              |                              |        |                                                                                                      |
| P32/TO2                              |                              |        |                                                                                                      |
| P33/TI1                              | 8-D                          |        |                                                                                                      |
| P34/TI2                              |                              |        |                                                                                                      |
| P35/PCL                              | 5-J                          |        |                                                                                                      |
| P36/BUZ                              |                              |        |                                                                                                      |
| P37                                  |                              |        |                                                                                                      |
| P70/SI2/RxD                          | 8-D                          |        |                                                                                                      |
| P71/SO2/TxD                          | 5-J                          |        |                                                                                                      |
| P72/SCK2/ASCK                        | 8-D                          |        |                                                                                                      |
| P80/S39 to P87/S32                   | 17-E                         |        |                                                                                                      |
| P90/S31 to P97/S24                   |                              |        |                                                                                                      |
| P100 to P103                         | 5-J                          |        |                                                                                                      |
| P110 to P117                         | 8-D                          |        | Individually connect to V <sub>DD</sub> via resistor                                                 |
| S0 to S23                            | 17-D                         | Output | Leave open                                                                                           |
| COM0 to COM3                         | 18-B                         |        |                                                                                                      |
| V <sub>LC0</sub> to V <sub>LC2</sub> | —                            | —      | —                                                                                                    |
| BIAS                                 |                              |        |                                                                                                      |
| RESET                                | 2                            | Input  | —                                                                                                    |
| XT2                                  | 16                           | —      | Leave open                                                                                           |
| AV <sub>REF</sub>                    | —                            |        | Connect to V <sub>SS</sub>                                                                           |
| AV <sub>DD</sub>                     |                              |        | Connect to separate power supply whose electrical potential is the same as that of V <sub>DD</sub> . |
| AV <sub>SS</sub>                     |                              |        | Connect to separate ground line whose electrical potential is the same as that of V <sub>SS</sub> .  |
| V <sub>PP</sub>                      |                              |        | Connect directly to V <sub>SS</sub>                                                                  |

Figure 2-1. List of Pin Input/Output Circuits (1/2)

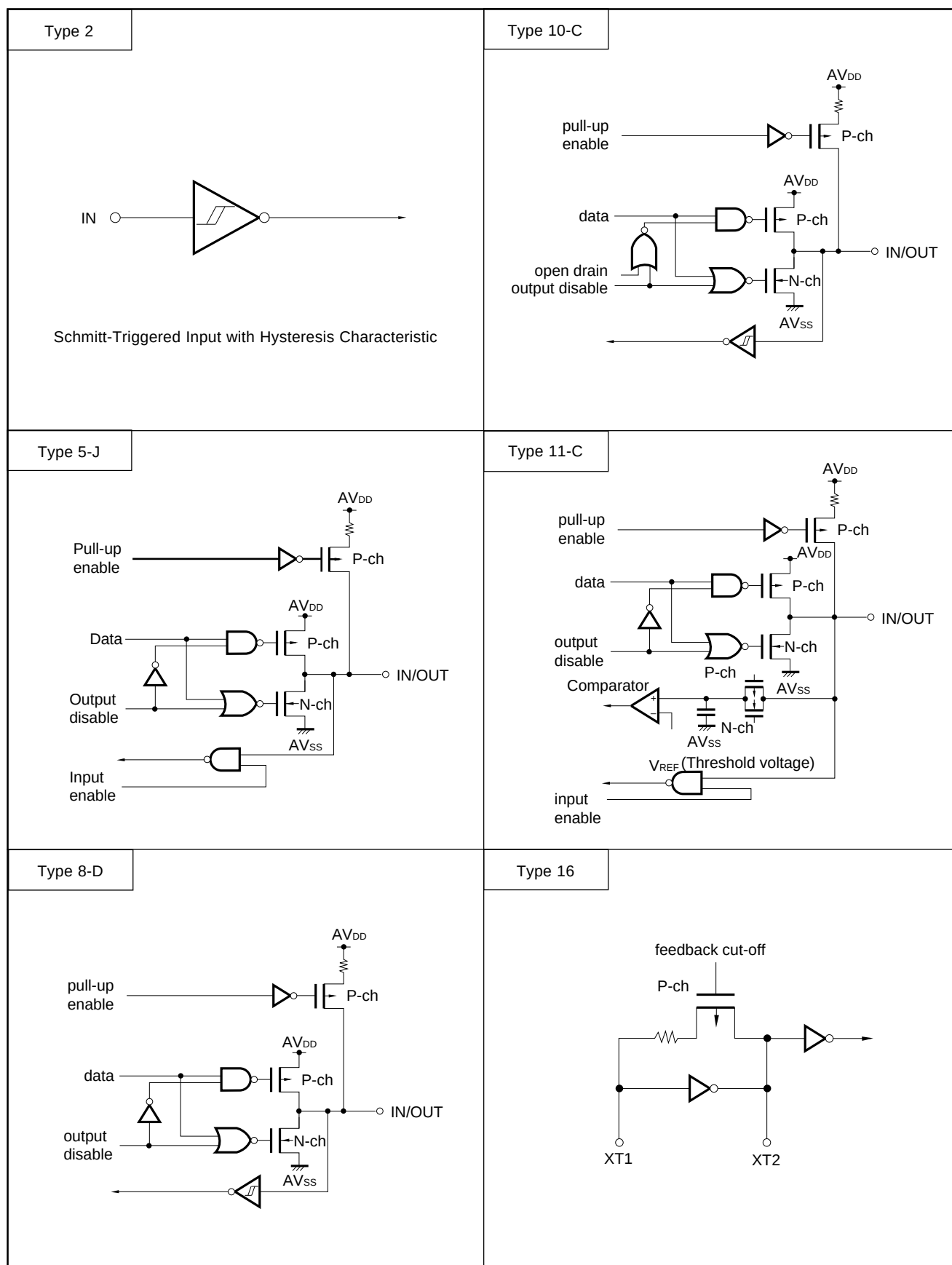
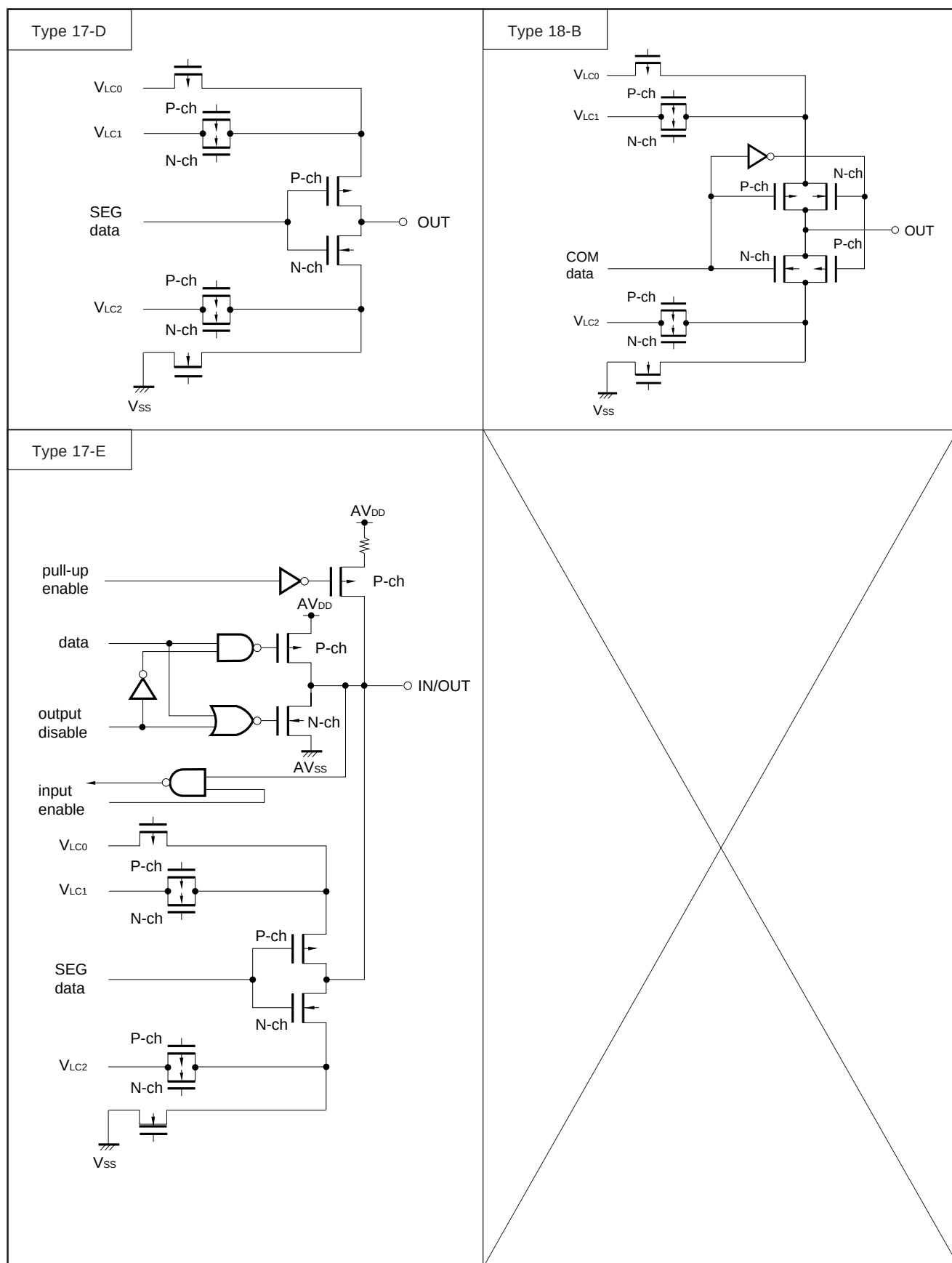


Figure 2-1. List of Pin Input/Output Circuits (2/2)



### 3. MEMORY SIZE SWITCHING REGISTER (IMS)

This is a register to disable use of part of internal memories by software. By setting this memory size switching register (IMS), it is possible to get the same memory mapping as that of mask ROM product having different internal memories (ROM, RAM).

The IMS is set up by the 8-bit memory manipulating instruction.

C8H will result by the RESET input.

**Figure 3-1. Memory Size Switching Register Format**

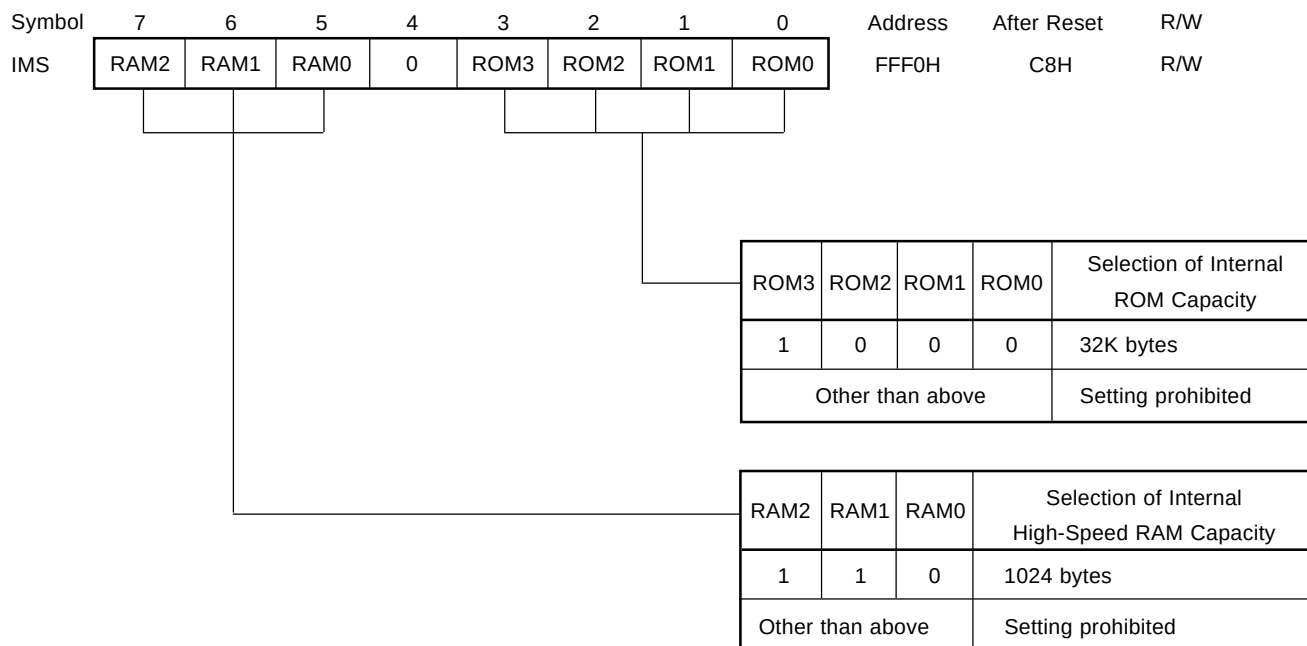


Table 3-1 shows the set values of IMS which makes the memory map the same as that of the various mask ROM products.

**Table 3-1. Memory Size Switching Register Setting Values**

| Target Mask ROM Product | IMS Setting Value |
|-------------------------|-------------------|
| μPD78064B               | C8H               |

## 4. PROM PROGRAMMING

The μPD78P064B has an on-chip 32K-byte PROM as a program memory. For programming, set the PROM programming mode by the  $V_{PP}$  and  $\overline{RESET}$  pins. For processing unused pins, refer to **Pin Configuration (2) PROM programming mode**.

**Caution** When writing in a program, use locations 0000H-7FFFH. (Specify the last address as 7FFFH). You cannot write in using a PROM programmer that cannot specify the addresses to write.

### 4.1 OPERATING MODES

When +5 V or +12.5 V is applied to the  $V_{PP}$  pin and a low level signal is applied to the  $\overline{RESET}$  pin, the PROM programming mode is set. This mode will become the operating mode as shown in Table 4-1 when the  $\overline{CE}$ ,  $\overline{OE}$  and  $\overline{PGM}$  pins are set as shown.

Further, when the read mode is set, it is possible to read the contents of the PROM.

**Table 4-1. Operating Modes of PROM Programming**

| <div>Pin</div> <div>Operating Mode</div> | $\overline{\text{RESET}}$ | V <sub>PP</sub> | V <sub>DD</sub> | $\overline{\text{CE}}$ | $\overline{\text{OE}}$ | $\overline{\text{PGM}}$ | D0 to D7       |
|------------------------------------------|---------------------------|-----------------|-----------------|------------------------|------------------------|-------------------------|----------------|
| Page data latch                          | L                         | +12.5 V         | +6.5 V          | H                      | L                      | H                       | Data input     |
| Page write                               |                           |                 |                 | H                      | H                      | L                       | High-impedance |
| Byte write                               |                           |                 |                 | L                      | H                      | L                       | Data input     |
| Program verify                           |                           |                 |                 | L                      | L                      | H                       | Data output    |
| Program inhibit                          |                           |                 |                 | ×                      | H                      | H                       | High-impedance |
|                                          |                           |                 |                 | ×                      | L                      | L                       |                |
| Read                                     | L                         | +5 V            | +5 V            | L                      | L                      | H                       | Data output    |
| Output disable                           |                           |                 |                 | L                      | H                      | ×                       | High-impedance |
| Standby                                  |                           |                 |                 | H                      | ×                      | ×                       | High-impedance |

× : L or H

**(1) Read mode**

Read mode is set if  $\overline{CE} = L$ ,  $\overline{OE} = L$  is set.

**(2) Output disable mode**

Data output becomes high-impedance, and is in the output disable mode, of  $\overline{OE} = H$  is set.

Therefore, it allows data to be read from any device by controlling the  $\overline{OE}$  pin, if multiple  $\mu$ PD78P064Bs are connected to the data bus.

**(3) Standby mode**

Standby mode is set if  $\overline{CE} = H$  is set.

In this mode, data outputs become high-impedance irrespective of the  $\overline{OE}$  status.

**(4) Page data latch mode**

Page data latch mode is set if  $\overline{CE} = H$ ,  $\overline{PGM} = H$ ,  $\overline{OE} = L$  are set at the beginning of page write mode.

In this mode, 1 page 4-byte data is latched in an internal address/data latch circuit.

**(5) Page write mode**

After 1 page 4 bytes of addresses and data are latched in the page data latch mode, a page write is executed by applying a 0.1 ms program pulse (active low) to the  $\overline{PGM}$  pin with  $\overline{CE} = H$ ,  $\overline{OE} = H$ . Then, program verification can be performed, if  $\overline{CE} = L$ ,  $\overline{OE} = L$  are set.

If programming is not performed by a one-time program pulse, X ( $X \leq 10$ ) write and verification operations should be executed repeatedly.

**(6) Byte write mode**

Byte write is executed when a 0.1 ms program pulse (active low) is applied to the  $\overline{PGM}$  pin with  $\overline{CE} = L$ ,  $\overline{OE} = H$ . Then, program verification can be performed if  $\overline{OE} = L$  is set.

If programming is not performed by a one-time program pulse, X ( $X \leq 10$ ) write and verification operations should be executed repeatedly.

**(7) Program verify mode**

Program verify mode is set if  $\overline{CE} = L$ ,  $\overline{PGM} = H$ ,  $\overline{OE} = L$  are set. In this mode, check if a write operation is performed correctly, after the write.

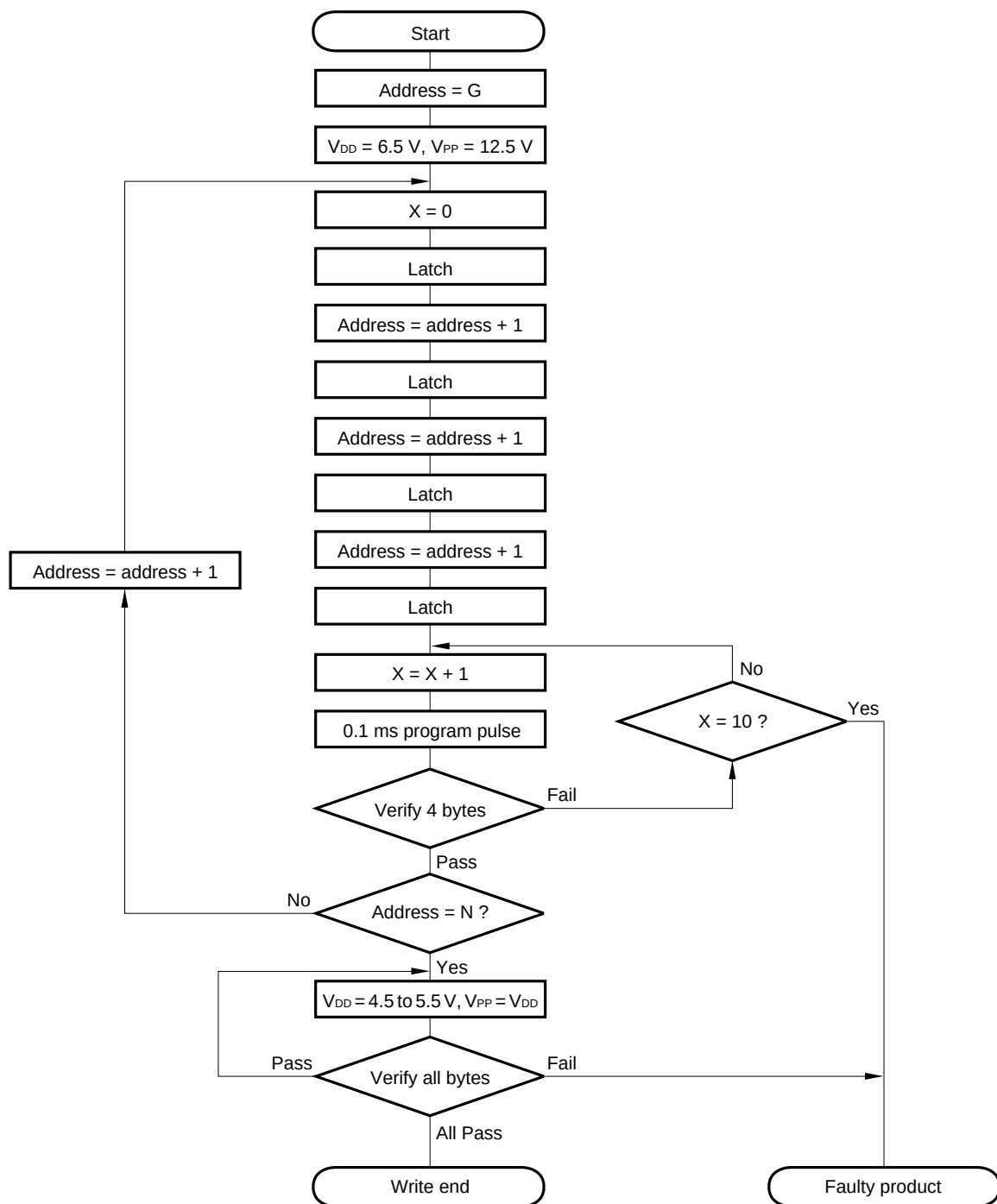
**(8) Program inhibit mode**

Program inhibit mode is used when the  $\overline{OE}$  pin,  $V_{PP}$  pin and D0 to D7 pins of multiple  $\mu$ PD78P064Bs are connected in parallel and a write is performed to one of those devices.

When a write operation is performed, the page write mode or byte write mode described above is used. At this time, a write is not performed to a device which has the  $\overline{PGM}$  pin driven high.

## 4.2 PROM WRITE PROCEDURE

Figure 4-1. Page Program Mode Flow Chart



G = Start address

N = Program last address

Figure 4-2. Page Program Mode Timing

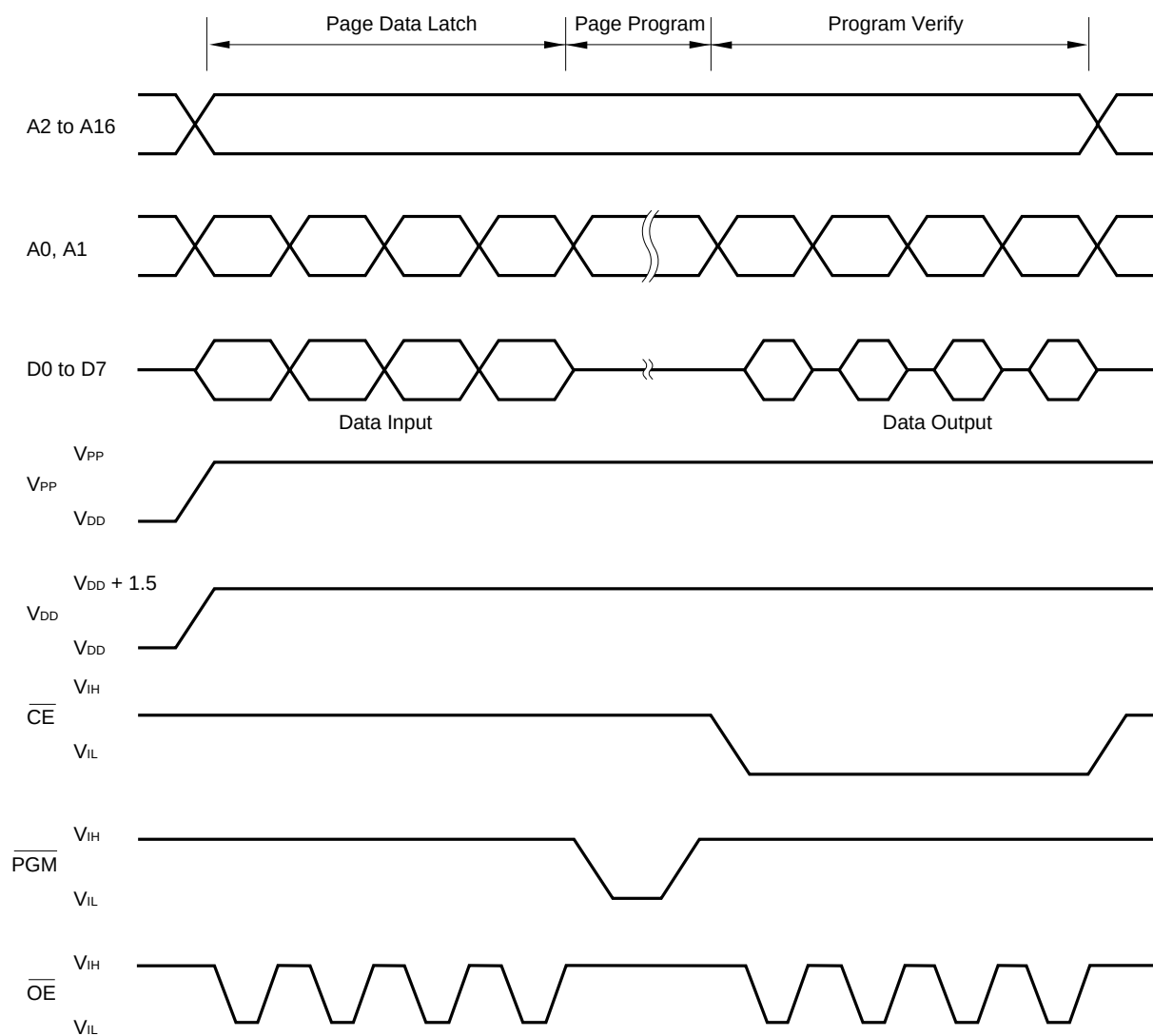
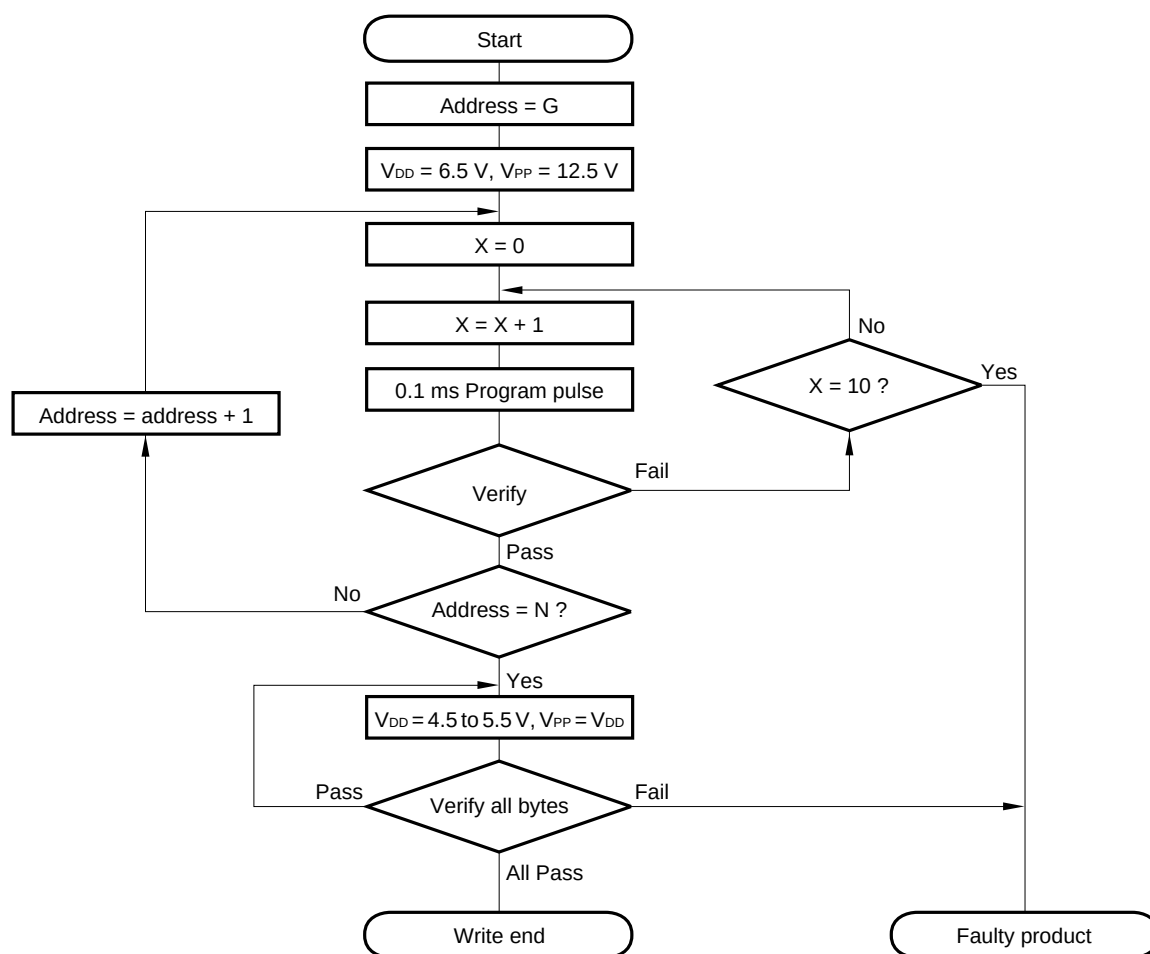




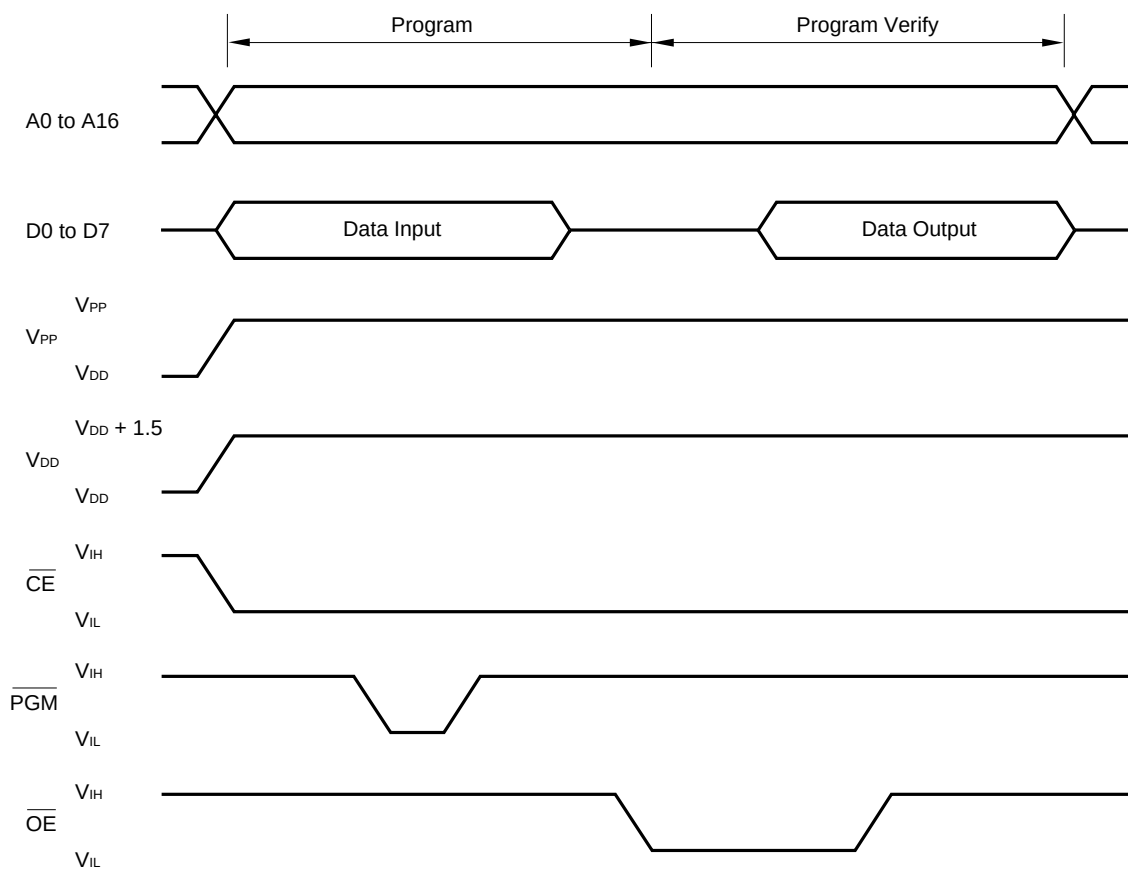
Figure 4-3. Byte Program Mode Flow Chart



G = Start address

N = Program last address

Figure 4-4. Byte Program Mode Timing



- Cautions**
1. V<sub>DD</sub> should be applied before V<sub>PP</sub> and cut after V<sub>PP</sub>.
  2. V<sub>PP</sub> must not exceed +13.5 V including overshoot.
  3. Reliability may be adversely affected of removal/reinsertion is performed while +12.5 V is being applied to V<sub>PP</sub>.

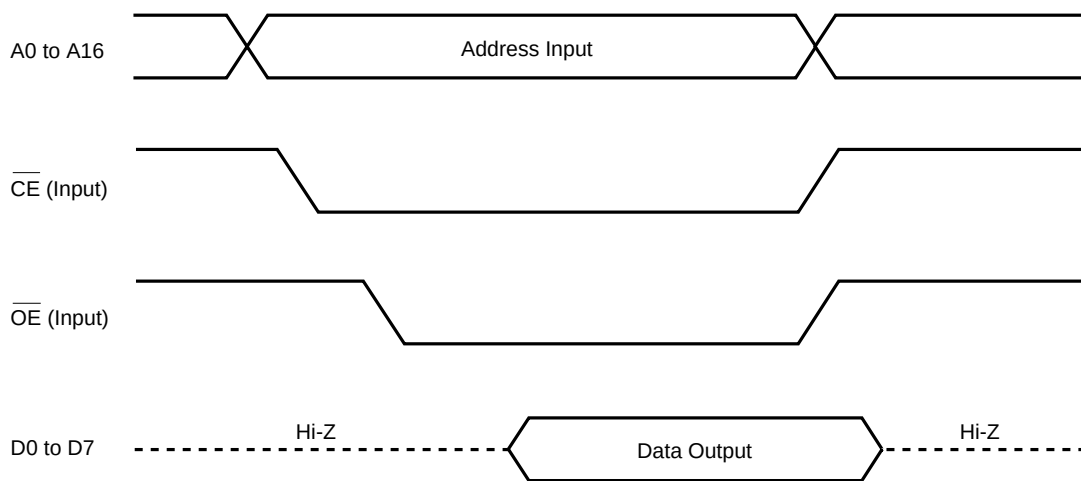
### 4.3 PROM READ PROCEDURE

The contents of PROM are readable to the external data bus (D0 to D7) according to the read procedure shown below.

- (1) Fix the  $\overline{\text{RESET}}$  pin at low level, supply +5 V to the  $V_{PP}$  pin, and process all other unused pins as shown in **Pin Configuration (2) PROM programming mode**.
- (2) Supply +5 V to the  $V_{DD}$  and  $V_{PP}$  pins.
- (3) Input address of read data into the A0 to A16 pins.
- (4) Read mode
- (5) Output data to D0 to D7 pins.

The timings of the above steps (2) to (5) are shown in Figure 4-5.

Figure 4-5. PROM Read Timings



## 5. ONE-TIME PROM PRODUCTS SCREENING

The one-time PROM product ( $\mu$ PD78P064BGC-7EA,  $\mu$ PD78P064BGC-8EU,  $\mu$ PD78P064BGF-3BA) can not be tested completely by NEC before it is shipped, because of its structure. It is recommended to perform screening to verify PROM after writing necessary data and performing high-temperature storage under the condition below.

| Storage Temperature | Storage Time |
|---------------------|--------------|
| 125 °C              | 24 hours     |

At present, a fee is charged by NEC for one-time PROM after-programming writing, marking, screening, and verify service for the QTOP Microcomputer. For details, contact your sales representative.

## 6. ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C)

| Parameter                     | Symbol               | Test Conditions                                                                                        |                  | Rating                                          | Unit |
|-------------------------------|----------------------|--------------------------------------------------------------------------------------------------------|------------------|-------------------------------------------------|------|
| Supply voltage                | V <sub>DD</sub>      |                                                                                                        |                  | −0.3 to +7.0                                    | V    |
|                               | V <sub>PP</sub>      |                                                                                                        |                  | −0.3 to +13.5                                   | V    |
|                               | AV <sub>DD</sub>     |                                                                                                        |                  | −0.3 to V <sub>DD</sub> +0.3                    | V    |
|                               | AV <sub>REF</sub>    |                                                                                                        |                  | −0.3 to V <sub>DD</sub> +0.3                    | V    |
|                               | AV <sub>SS</sub>     |                                                                                                        |                  | −0.3 to +0.3                                    | V    |
| Input voltage                 | V <sub>I</sub>       | P00-P05, P07, P10-P17, P25-P27,<br>P30-P37, P70-P72, P80-P87, P90-P97,<br>P100-P103, P110-P117         |                  | −0.3 to V <sub>DD</sub> +0.3                    | V    |
|                               | V <sub>I2</sub>      | A9 (PROM programming mode)                                                                             |                  | −0.3 to +13.5                                   | V    |
| Output voltage                | V <sub>O</sub>       |                                                                                                        |                  | −0.3 to V <sub>DD</sub> +0.3                    | V    |
| Analog input voltage          | V <sub>AN</sub>      | P10-P17                                                                                                | Analog input pin | AV <sub>SS</sub> −0.3 to AV <sub>REF</sub> +0.3 | V    |
| Output current, high          | I <sub>OH</sub>      | 1 pin                                                                                                  |                  | −10                                             | mA   |
|                               |                      | Total for P01-P05, P10-P17, P25-P27, P30-P37,<br>P70-P72, P80-P87, P90-P97, P100-P103,<br>P110-P117    |                  | −15                                             | mA   |
| Output current, low           | I <sub>OL</sub> Note | 1 pin                                                                                                  | Peak value       | 30                                              | mA   |
|                               |                      |                                                                                                        | R.m.s. value     | 15                                              | mA   |
|                               |                      | Total for P01-P05, P10-P17,<br>P25-P27, P30-P37, P70-P72,<br>P80-P87, P90-P97, P100-P103,<br>P110-P117 | Peak value       | 100                                             | mA   |
|                               |                      |                                                                                                        | R.m.s. value     | 70                                              | mA   |
| Operating ambient temperature | T <sub>A</sub>       |                                                                                                        |                  | −40 to +85                                      | °C   |
| Storage temperature           | T <sub>stg</sub>     |                                                                                                        |                  | −65 to +150                                     | °C   |

**Note** The r.m.s. value should be calculated as follows: [R.m.s. value] = [Peak value] ×  $\sqrt{\text{Duty}}$

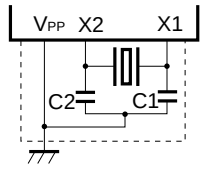
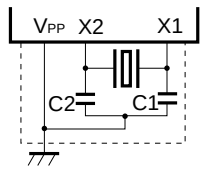
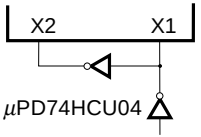
**Caution** The product quality may be damaged even if a value of only one of the above parameters exceeds the absolute maximum rating or any value exceeds the absolute maximum rating for an instant. That is, the absolute maximum rating is a rating value which may cause a product to be damaged physically. The absolute maximum rating values must therefore be observed in using the product.

**Remark** Unless specified otherwise, the characteristics of dual-function pins are the same as the those of port pins.

### CAPACITANCE (T<sub>A</sub> = 25 °C, V<sub>DD</sub> = V<sub>SS</sub> = 0 V)

| Parameter          | Symbol           | Test Conditions                               | MIN. | TYP. | MAX. | Unit |
|--------------------|------------------|-----------------------------------------------|------|------|------|------|
| Input capacitance  | C <sub>IN</sub>  | f = 1 MHz unmeasured<br>pins returned to 0 V. |      |      | 15   | pF   |
| Output capacitance | C <sub>OUT</sub> |                                               |      |      | 15   | pF   |
| I/O capacitance    | C <sub>IO</sub>  |                                               |      |      | 15   | pF   |

MAIN SYSTEM CLOCK OSCILLATION CIRCUIT CHARACTERISTICS (T<sub>A</sub> = -40 to +85 °C, V<sub>DD</sub> = 2.0 to 6.0 V)

| Resonator         | Recommended circuit                                                               | Parameter                                                          | Test conditions                                             | MIN. | TYP. | MAX.     | Unit |
|-------------------|-----------------------------------------------------------------------------------|--------------------------------------------------------------------|-------------------------------------------------------------|------|------|----------|------|
| Ceramic resonator |  | Oscillator frequency (f <sub>x</sub> ) <sup>Note 1</sup>           | V <sub>DD</sub> = Oscillator voltage range                  | 1    |      | 5        | MHz  |
|                   |                                                                                   | Oscillation stabilization time <sup>Note 2</sup>                   | After V <sub>DD</sub> reaches oscillator voltage range MIN. |      |      | 4        | ms   |
| Crystal resonator |  | Oscillator frequency (f <sub>x</sub> ) <sup>Note 1</sup>           |                                                             | 1    |      | 5        | MHz  |
|                   |                                                                                   | Oscillation stabilization time <sup>Note 2</sup>                   | V <sub>DD</sub> = 4.5 to 6.0 V                              |      |      | 10<br>30 | ms   |
| External clock    |  | X1 input frequency (f <sub>x</sub> ) <sup>Note 1</sup>             |                                                             | 1.0  |      | 5.0      | MHz  |
|                   |                                                                                   | X1 input high/low level width (t <sub>xH</sub> , t <sub>xL</sub> ) |                                                             | 85   |      | 500      | ns   |

- Notes**
1. Indicates only oscillation circuit characteristics. Refer to “AC Characteristics” for instruction execution time.
  2. Time required to stabilize oscillation after reset or STOP mode release.

- Cautions**
1. When using the main system clock oscillator, wiring in the area enclosed with the broken line should be carried out as follows to avoid an adverse effect from wiring capacitance.
    - Wiring should be as short as possible.
    - Wiring should not cross other signal lines.
    - Wiring should not be placed close to a varying high current.
    - The potential of the oscillator capacitor ground should be the same as V<sub>SS</sub>.
    - Do not ground it to the ground pattern in which a high current flows.
    - Do not fetch a signal from the oscillator.
  2. If the main system clock oscillation circuit is operated by the subsystem clock when the main system clock is stopped, reswitching to the main system clock should be performed after the stable oscillation time has been obtained by the program.

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 2.0$  to  $6.0$  V)

| Resonator         | Recommended Circuit | Parameter                                               | Test Conditions           | MIN. | TYP.   | MAX. | Unit          |
|-------------------|---------------------|---------------------------------------------------------|---------------------------|------|--------|------|---------------|
| Crystal resonator |                     | Oscillator frequency ( $f_{XT}$ ) <sup>Note 1</sup>     |                           | 32   | 32.768 | 35   | kHz           |
|                   |                     | Oscillation stabilization time <sup>Note 2</sup>        | $V_{DD} = 4.5$ to $6.0$ V |      | 1.2    | 2    | s             |
|                   |                     |                                                         |                           |      |        | 10   |               |
| External clock    |                     | XT1 input frequency ( $f_{XT}$ ) <sup>Note 1</sup>      |                           | 32   |        | 100  | kHz           |
|                   |                     | XT1 input high-/low-level width ( $t_{bXTH}/t_{bXTL}$ ) |                           | 5    |        | 15   | $\mu\text{s}$ |

- Notes**
1. Indicates only oscillation circuit characteristics. Refer to “AC Characteristics” for instruction execution time.
  2. Time required to stabilize oscillation after  $V_{DD}$  has reached the minimum oscillation voltage range.

- Cautions**
1. When using the subsystem clock oscillator, wiring in the area enclosed with the broken line should be carried out as follows to avoid an adverse effect from wiring capacitance.
    - Wiring should be as short as possible.
    - Wiring should not cross other signal lines.
    - Wiring should not be placed close to a varying high current.
    - The potential of the oscillator capacitor ground should be the same as  $V_{SS}$ .
    - Do not ground it to the ground pattern in which a high current flows.
    - Do not fetch a signal from the oscillator.
  2. The subsystem clock oscillation circuit is designed as a low amplification circuit to provide low consumption current, causing misoperation to noise more frequently than the main system clock oscillation circuit. Special care should therefore be taken to wiring method when the subsystem clock is used.

## RECOMMENDED OSCILLATION CIRCUIT CONSTANT

MAIN SYSTEM CLOCK: CERAMIC RESONATOR ( $T_A = -40$  to  $+85$  °C)

| Manufacturer                                | Product Name | Frequency (MHZ) | Recommended Circuit Constant |          | Oscillator Voltage Range |          | Remarks         |
|---------------------------------------------|--------------|-----------------|------------------------------|----------|--------------------------|----------|-----------------|
|                                             |              |                 | C1 (pF)                      | C2 (pF)  | MIN. (V)                 | MAX. (V) |                 |
| Murata Mfg. Co., Ltd.                       | CSA5.00MG    | 5.00            | 30                           | 30       | 2.7                      | 6.0      |                 |
|                                             | CST5.00MGW   | 5.00            | Built-in                     | Built-in | 2.7                      | 6.0      |                 |
| Matsushita Electronics Components Co., Ltd. | EF0GC5004A4  | 5.00            | Built-in                     | Built-in | 2.7                      | 6.0      | Lead type       |
|                                             | EF0EC5004A4  | 5.00            | Built-in                     | Built-in | 2.7                      | 6.0      | Round lead type |
|                                             | EF0EN5004A4  | 5.00            | 33                           | 33       | 2.7                      | 6.0      | Lead type       |
|                                             | EF0S5004B4   | 5.00            | Built-in                     | Built-in | 2.7                      | 6.0      | Chip type       |
| Kyocera Corporation                         | KBR-5.0MSA   | 5.00            | 33                           | 33       | 2.7                      | 6.0      | Lead type       |
|                                             | PBRC5.00A    | 5.00            | 33                           | 33       | 2.7                      | 6.0      | Chip type       |
|                                             | KBR-5.0MKS   | 5.00            | Built-in                     | Built-in | 2.7                      | 6.0      | Lead type       |
|                                             | KBR-5.0MWS   | 5.00            | Built-in                     | Built-in | 2.7                      | 6.0      | Chip type       |

**Caution** The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation but do not guarantee accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency in the application circuit. For this, it is necessary to directly contact the manufacturer of the resonator being used.



**DC CHARACTERISTICS ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 2.0$  to  $6.0$  V)**

| Parameter            | Symbol    | Test Conditions                                                           |                                                                         | MIN.          | TYP. | MAX.          | Unit |
|----------------------|-----------|---------------------------------------------------------------------------|-------------------------------------------------------------------------|---------------|------|---------------|------|
| Input voltage, high  | $V_{IH1}$ | P10-P17, P30-P32, P35-P37, P80-P87, P90-P97, P100-P103                    | $V_{DD} = 2.7$ to $6.0$ V                                               | $0.7 V_{DD}$  |      | $V_{DD}$      | V    |
|                      |           |                                                                           |                                                                         | $0.8 V_{DD}$  |      | $V_{DD}$      | V    |
|                      | $V_{IH2}$ | P00-P05, P25-P27, P33, P34, P70-P72, P110-P117, $\overline{\text{RESET}}$ | $V_{DD} = 2.7$ to $6.0$ V                                               | $0.8 V_{DD}$  |      | $V_{DD}$      | V    |
|                      |           |                                                                           |                                                                         | $0.85 V_{DD}$ |      | $V_{DD}$      | V    |
|                      | $V_{IH3}$ | X1, X2                                                                    | $V_{DD} = 2.7$ to $6.0$ V                                               | $V_{DD}-0.5$  |      | $V_{DD}$      | V    |
|                      |           |                                                                           |                                                                         | $V_{DD}-0.2$  |      | $V_{DD}$      | V    |
|                      | $V_{IH4}$ | XT1/P07, XT2                                                              | $4.5 \leq V_{DD} \leq 6.0$ V                                            | $0.8 V_{DD}$  |      | $V_{DD}$      | V    |
|                      |           |                                                                           | $2.7 \leq V_{DD} < 4.5$ V                                               | $0.9 V_{DD}$  |      | $V_{DD}$      | V    |
|                      |           |                                                                           | $2.0 \leq V_{DD} < 2.7$ V <sup>Note</sup>                               | $0.9 V_{DD}$  |      | $V_{DD}$      | V    |
| Input voltage, low   | $V_{IL1}$ | P10-P17, P30-P32, P35-P37, P80-P87, P90-P97, P100-P103                    | $V_{DD} = 2.7$ to $6.0$ V                                               | 0             |      | $0.3 V_{DD}$  | V    |
|                      |           |                                                                           |                                                                         | 0             |      | $0.2 V_{DD}$  | V    |
|                      | $V_{IL2}$ | P00-P05, P25-P27, P33, P34, P70-P72, P110-P117, $\overline{\text{RESET}}$ | $V_{DD} = 2.7$ to $6.0$ V                                               | 0             |      | $0.2 V_{DD}$  | V    |
|                      |           |                                                                           |                                                                         | 0             |      | $0.15 V_{DD}$ | V    |
|                      | $V_{IL3}$ | X1, X2                                                                    | $V_{DD} = 2.7$ to $6.0$ V                                               | 0             |      | 0.4           | V    |
|                      |           |                                                                           |                                                                         | 0             |      | 0.2           | V    |
|                      | $V_{IL4}$ | XT1/P07, XT2                                                              | $4.5 \leq V_{DD} \leq 6.0$ V                                            | 0             |      | $0.2 V_{DD}$  | V    |
|                      |           |                                                                           | $2.7 \leq V_{DD} < 4.5$ V                                               | 0             |      | $0.1 V_{DD}$  | V    |
|                      |           |                                                                           | $2.0 \leq V_{DD} < 2.7$ V <sup>Note</sup>                               | 0             |      | $0.1 V_{DD}$  | V    |
| Output voltage, high | $V_{OH}$  | $V_{DD} = 4.5$ to $6.0$ V $I_{OH} = -1$ mA                                |                                                                         | $V_{DD}-1.0$  |      | $V_{DD}$      | V    |
|                      |           | $I_{OH} = -100$ $\mu$ A                                                   |                                                                         | $V_{DD}-0.5$  |      | $V_{DD}$      | V    |
| Output voltage, low  | $V_{OL1}$ | P100-P103                                                                 | $V_{DD} = 4.5$ to $6.0$ V, $I_{OL} = 15$ mA                             |               | 0.4  | 2.0           | V    |
|                      |           | P01-P05, P10-P17, P25-P27, P30-P37, P70-P72, P80-P87, P90-P97, P110-P117  | $V_{DD} = 4.5$ to $6.0$ V, $I_{OL} = 1.6$ mA                            |               |      | 0.4           | V    |
|                      | $V_{OL2}$ | SB0, SB1, $\overline{\text{SCK0}}$                                        | $V_{DD} = 4.5$ to $6.0$ V, open-drain, pulled up ( $R = 1$ k $\Omega$ ) |               |      | $0.2 V_{DD}$  | V    |
|                      | $V_{OL3}$ | $I_{OL} = 400$ $\mu$ A                                                    |                                                                         |               |      | 0.5           | V    |

**Note** When used as P07, the inverse phase of P07 should be input to XT2 using an inverter.

**Remark** Unless specified otherwise, the characteristics of dual-function pins are the same as the those of port pins.

DC CHARACTERISTICS ( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 2.0$  to  $6.0$  V)

| Parameter                        | Symbol     | Test Conditions                                                                                     |                                                                                     | MIN. | TYP. | MAX. | Unit       |
|----------------------------------|------------|-----------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|------|------|------|------------|
| Input leakage current, high      | $I_{LIH1}$ | $V_{IN} = V_{DD}$                                                                                   | P00-P05, P10-P17, P25-P27, P30-P37, P70-P72, P80-P87, P90-P97, P100-P103, P110-P117 |      |      | 3    | $\mu$ A    |
|                                  | $I_{LIH2}$ |                                                                                                     | X1, X2, XT1/P07, XT2                                                                |      |      | 20   | $\mu$ A    |
| Input leakage current, low       | $I_{LIL1}$ | $V_{IN} = 0$ V                                                                                      | P00-P05, P10-P17, P25-P27, P30-P37, P70-P72, P80-P87, P90-P97, P100-P103, P110-P117 |      |      | -3   | $\mu$ A    |
|                                  | $I_{LIL2}$ |                                                                                                     | X1, X2, XT1/P07, XT2                                                                |      |      | -20  | $\mu$ A    |
| Output leakage current, high     | $I_{LOH}$  | $V_{OUT} = V_{DD}$                                                                                  |                                                                                     |      |      | 3    | $\mu$ A    |
| Output leakage current, low      | $I_{LOL}$  | $V_{OUT} = 0$ V                                                                                     |                                                                                     |      |      | -3   | $\mu$ A    |
| Software pull-up resistor        | R          | $V_{IN} = 0$ V, P01-P05, P10-P17, P25-P27, P30-P37, P70-P72, P80-P87, P90-P97, P100-P103, P110-P117 | $4.5$ V $\leq V_{DD} \leq 6.0$ V                                                    | 15   | 40   | 90   | k $\Omega$ |
|                                  |            |                                                                                                     | $2.7$ V $\leq V_{DD} < 4.5$ V                                                       | 20   |      | 500  | k $\Omega$ |
| Supply current <sup>Note 1</sup> | $I_{DD1}$  | 5.00 MHz, Crystal oscillation ( $f_{XX} = 2.5$ MHz) <sup>Note 2</sup> operating mode                | $V_{DD} = 5.0$ V $\pm 10$ % <sup>Note 5</sup>                                       |      | 5.0  | 15.0 | mA         |
|                                  |            |                                                                                                     | $V_{DD} = 3.0$ V $\pm 10$ % <sup>Note 6</sup>                                       |      | 0.7  | 2.1  | mA         |
|                                  |            |                                                                                                     | $V_{DD} = 2.2$ V $\pm 10$ % <sup>Note 6</sup>                                       |      | 0.4  | 1.2  | mA         |
|                                  |            | 5.00 MHz, Crystal oscillation ( $f_{XX} = 5.0$ MHz) <sup>Note 3</sup> operating mode                | $V_{DD} = 5.0$ V $\pm 10$ % <sup>Note 5</sup>                                       |      | 9.0  | 27.0 | mA         |
|                                  |            |                                                                                                     | $V_{DD} = 3.0$ V $\pm 10$ % <sup>Note 6</sup>                                       |      | 1.0  | 3.0  | mA         |
|                                  |            |                                                                                                     |                                                                                     |      |      |      |            |
|                                  | $I_{DD2}$  | 5.00 MHz, Crystal oscillation ( $f_{XX} = 2.5$ MHz) <sup>Note 2</sup> HALT mode                     | $V_{DD} = 5.0$ V $\pm 10$ %                                                         |      | 1.4  | 4.2  | mA         |
|                                  |            |                                                                                                     | $V_{DD} = 3.0$ V $\pm 10$ %                                                         |      | 500  | 1500 | $\mu$ A    |
|                                  |            |                                                                                                     | $V_{DD} = 2.2$ V $\pm 10$ %                                                         |      | 280  | 840  | $\mu$ A    |
|                                  |            | 5.00 MHz, Crystal oscillation ( $f_{XX} = 5.0$ MHz) <sup>Note 3</sup> HALT mode                     | $V_{DD} = 5.0$ V $\pm 10$ %                                                         |      | 1.6  | 4.8  | mA         |
|                                  |            |                                                                                                     | $V_{DD} = 3.0$ V $\pm 10$ %                                                         |      | 650  | 1950 | $\mu$ A    |
|                                  |            |                                                                                                     |                                                                                     |      |      |      |            |
|                                  | $I_{DD3}$  | 32.768 kHz, Crystal oscillation operating mode <sup>Note 4</sup>                                    | $V_{DD} = 5.0$ V $\pm 10$ %                                                         |      | 135  | 270  | $\mu$ A    |
|                                  |            |                                                                                                     | $V_{DD} = 3.0$ V $\pm 10$ %                                                         |      | 95   | 190  | $\mu$ A    |
|                                  |            |                                                                                                     | $V_{DD} = 2.2$ V $\pm 10$ %                                                         |      | 70   | 140  | $\mu$ A    |
|                                  | $I_{DD4}$  | 32.768 kHz, Crystal oscillation HALT mode <sup>Note 4</sup>                                         | $V_{DD} = 5.0$ V $\pm 10$ %                                                         |      | 25   | 55   | $\mu$ A    |
|                                  |            |                                                                                                     | $V_{DD} = 3.0$ V $\pm 10$ %                                                         |      | 5    | 15   | $\mu$ A    |
|                                  |            |                                                                                                     | $V_{DD} = 2.2$ V $\pm 10$ %                                                         |      | 2.5  | 12.5 | $\mu$ A    |
|                                  | $I_{DD5}$  | XT1 = $V_{DD}$<br>STOP mode<br>When feedback resistor is connected                                  | $V_{DD} = 5.0$ V $\pm 10$ %                                                         |      | 1    | 30   | $\mu$ A    |
|                                  |            |                                                                                                     | $V_{DD} = 3.0$ V $\pm 10$ %                                                         |      | 0.5  | 10   | $\mu$ A    |
|                                  |            |                                                                                                     | $V_{DD} = 2.2$ V $\pm 10$ %                                                         |      | 0.3  | 10   | $\mu$ A    |
|                                  | $I_{DD6}$  | XT1 = $V_{DD}$<br>STOP mode<br>When feedback resistor is disconnected                               | $V_{DD} = 5.0$ V $\pm 10$ %                                                         |      | 0.1  | 30   | $\mu$ A    |
|                                  |            |                                                                                                     | $V_{DD} = 3.0$ V $\pm 10$ %                                                         |      | 0.05 | 10   | $\mu$ A    |
|                                  |            |                                                                                                     | $V_{DD} = 2.2$ V $\pm 10$ %                                                         |      | 0.05 | 10   | $\mu$ A    |

**Notes** 1. Current flowing  $V_{DD}$  and  $AV_{DD}$  pin. Not including A/D converter, on-chip pull-up resistors or LCD dividing resistors.

2. Main system clock  $f_{XX} = f_X/2$  operation (when oscillation mode selection register (OSMS) is set to 00H)

3. Main system clock  $f_{XX} = f_X$  operation (when OSMS is set to 01H)

4. When the main system clock is stopped.

5. High-speed mode operation (when processor clock control register (PCC) is set to 00H)

6. Low-speed mode operation (when PCC is set to 04H)

**Remark** Unless specified otherwise, the characteristics of dual-function pins are the same as the those of port pins.

**DC CHARACTERISTICS (T<sub>A</sub> = -10 to +85 °C)**

**(1) Static Display Mode (V<sub>DD</sub> = 2.0 to 6.0 V)**

| Parameter                                              | Symbol           | Test Conditions        |                                                                                    | MIN. | TYP. | MAX.            | Unit |
|--------------------------------------------------------|------------------|------------------------|------------------------------------------------------------------------------------|------|------|-----------------|------|
| LCD drive voltage                                      | V <sub>LCD</sub> |                        |                                                                                    | 2.0  |      | V <sub>DD</sub> | V    |
| LCD dividing resistor                                  | R <sub>LCD</sub> |                        |                                                                                    | 60   | 100  | 150             | kΩ   |
| LCD output voltage deviation <sup>Note</sup> (common)  | V <sub>ODC</sub> | I <sub>O</sub> = ±5 μA | 2.0 V ≤ V <sub>LCD</sub> ≤ V <sub>DD</sub><br>V <sub>LCD0</sub> = V <sub>LCD</sub> | 0    |      | ±0.2            | V    |
| LCD output voltage deviation <sup>Note</sup> (segment) | V <sub>ODS</sub> | I <sub>O</sub> = ±1 μA |                                                                                    | 0    |      | ±0.2            | V    |

**Note** The voltage deviation is the difference from the out voltage corresponding to the ideal value of the segment and common outputs (V<sub>LCDn</sub>; n = 0, 1, 2).

**(2) 1/3 Bias Method (V<sub>DD</sub> = 2.5 to 6.0 V)**

| Parameter                                              | Symbol           | Test Conditions        |                                                                                                                                                                                                    | MIN. | TYP. | MAX.            | Unit |
|--------------------------------------------------------|------------------|------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|-----------------|------|
| LCD drive voltage                                      | V <sub>LCD</sub> |                        |                                                                                                                                                                                                    | 2.5  |      | V <sub>DD</sub> | V    |
| LCD dividing resistor                                  | R <sub>LCD</sub> |                        |                                                                                                                                                                                                    | 60   | 100  | 150             | kΩ   |
| LCD output voltage deviation <sup>Note</sup> (common)  | V <sub>ODC</sub> | I <sub>O</sub> = ±5 μA | 2.5 V ≤ V <sub>LCD</sub> ≤ V <sub>DD</sub><br>V <sub>LCD0</sub> = V <sub>LCD</sub><br>V <sub>LCD1</sub> = V <sub>LCD</sub> × $\frac{2}{3}$<br>V <sub>LCD2</sub> = V <sub>LCD</sub> × $\frac{1}{3}$ | 0    |      | ±0.2            | V    |
| LCD output voltage deviation <sup>Note</sup> (segment) | V <sub>ODS</sub> | I <sub>O</sub> = ±1 μA |                                                                                                                                                                                                    | 0    |      | ±0.2            | V    |

**Note** The voltage deviation is the difference from the out voltage corresponding to the ideal value of the segment and common outputs (V<sub>LCDn</sub>; n = 0, 1, 2).

**(3) 1/2 Bias Method (V<sub>DD</sub> = 2.7 to 6.0 V)**

| Parameter                                              | Symbol           | Test Conditions        |                                                                                                                                                                                     | MIN. | TYP. | MAX.            | Unit |
|--------------------------------------------------------|------------------|------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|-----------------|------|
| LCD drive voltage                                      | V <sub>LCD</sub> |                        |                                                                                                                                                                                     | 2.7  |      | V <sub>DD</sub> | V    |
| LCD dividing resistor                                  | R <sub>LCD</sub> |                        |                                                                                                                                                                                     | 60   | 100  | 150             | kΩ   |
| LCD output voltage deviation <sup>Note</sup> (common)  | V <sub>ODC</sub> | I <sub>O</sub> = ±5 μA | 2.7 V ≤ V <sub>LCD</sub> ≤ V <sub>DD</sub><br>V <sub>LCD0</sub> = V <sub>LCD</sub><br>V <sub>LCD1</sub> = V <sub>LCD</sub> × $\frac{1}{2}$<br>V <sub>LCD2</sub> = V <sub>LCD1</sub> | 0    |      | ±0.2            | V    |
| LCD output voltage deviation <sup>Note</sup> (segment) | V <sub>ODS</sub> | I <sub>O</sub> = ±1 μA |                                                                                                                                                                                     | 0    |      | ±0.2            | V    |

**Note** The voltage deviation is the difference from the out voltage corresponding to the ideal value of the segment and common outputs (V<sub>LCDn</sub>; n = 0, 1, 2).

## AC CHARACTERISTICS

(1) Basic Operation ( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 2.0$  to  $6.0$  V)

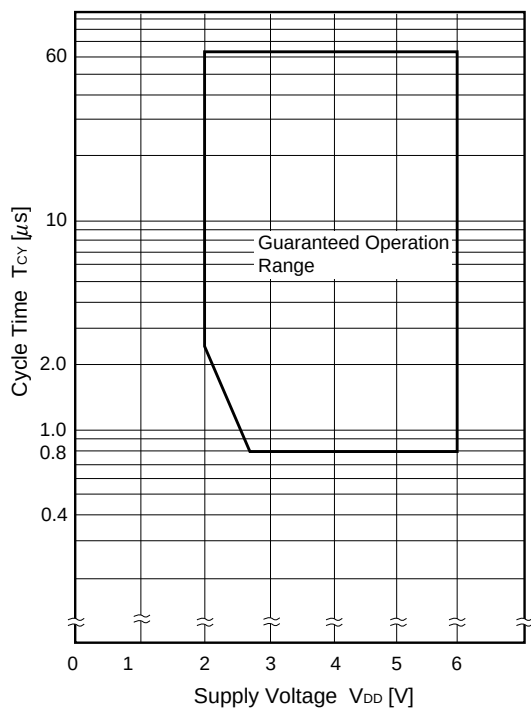
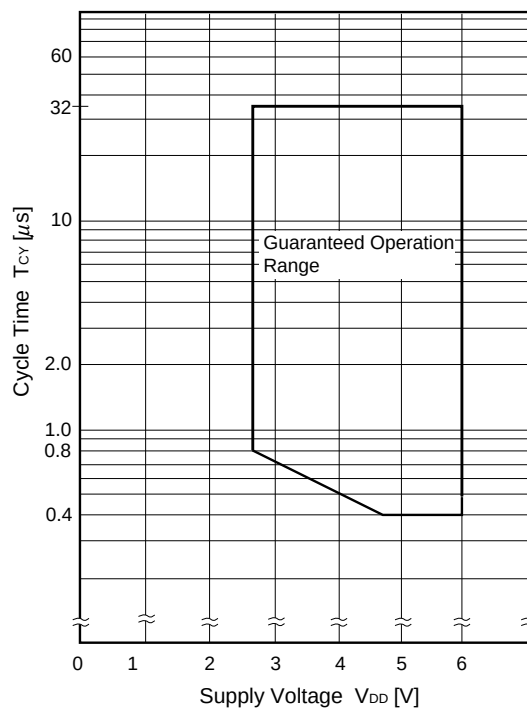
| Parameter                                          | Symbol                      | Test Conditions                                                           |                              | MIN.                                | TYP. | MAX. | Unit |
|----------------------------------------------------|-----------------------------|---------------------------------------------------------------------------|------------------------------|-------------------------------------|------|------|------|
| Cycle time<br>(Min. instruction<br>execution time) | $T_{CY}$                    | Operating on main system clock<br>( $f_{XX} = 2.5$ MHz) <sup>Note 1</sup> | $V_{DD} = 2.7$ to $6.0$ V    | 0.8                                 |      | 64   | μs   |
|                                                    |                             |                                                                           |                              | 2.2                                 |      | 64   | μs   |
|                                                    |                             | Operating on main system clock<br>( $f_{XX} = 5.0$ MHz) <sup>Note 2</sup> | $4.5 \leq V_{DD} \leq 6.0$ V | 0.4                                 |      | 32   | μs   |
|                                                    |                             |                                                                           | $2.7 \leq V_{DD} < 4.5$ V    | 0.8                                 |      | 32   | μs   |
| ★ TI00 input high/<br>low-level width              | $t_{TIH00},$<br>$t_{TIL00}$ | Operating on subsystem clock                                              |                              | 40 <sup>Note 3</sup>                | 122  | 125  | μs   |
|                                                    |                             | $4.5$ V $\leq V_{DD} \leq 6.0$ V                                          |                              | $2/f_{sam} + 0.1$ <sup>Note 4</sup> |      |      | μs   |
|                                                    |                             | $2.7$ V $\leq V_{DD} < 4.5$ V                                             |                              | $2/f_{sam} + 0.2$ <sup>Note 4</sup> |      |      | μs   |
|                                                    |                             | $2.0$ V $\leq V_{DD} < 2.7$ V                                             |                              | $2/f_{sam} + 0.5$ <sup>Note 4</sup> |      |      | μs   |
| ★ TI01 input high/<br>low-level width              | $t_{TIH01},$<br>$t_{TIL01}$ | $V_{DD} = 2.7$ to $6.0$ V                                                 |                              | 10                                  |      |      | μs   |
|                                                    |                             |                                                                           |                              | 20                                  |      |      | μs   |
|                                                    |                             |                                                                           |                              |                                     |      |      | μs   |
| TI input<br>frequency                              | $f_{TI}$                    | $V_{DD} = 4.5$ to $6.0$ V                                                 |                              | 0                                   |      | 4    | MHz  |
|                                                    |                             |                                                                           |                              | 0                                   |      | 275  | kHz  |
| TI1, TI2 input<br>high/low-level width             | $t_{TIH},$<br>$t_{TIL}$     | $V_{DD} = 4.5$ to $6.0$ V                                                 |                              | 100                                 |      |      | ns   |
|                                                    |                             |                                                                           |                              | 1.8                                 |      |      | μs   |
| Interrupt input<br>high/low-level<br>width         | $t_{INTH},$<br>$t_{INTL}$   | INTP0                                                                     |                              | $8/f_{sam}$ <sup>Note 4</sup>       |      |      | μs   |
|                                                    |                             | INTP1-INTP5, P110-P117                                                    | $V_{DD} = 2.7$ to $6.0$ V    | 10                                  |      |      | μs   |
|                                                    |                             |                                                                           |                              | 20                                  |      |      | μs   |
| $\overline{\text{RESET}}$ low level<br>width       | $t_{RST}$                   | $V_{DD} = 2.7$ to $6.0$ V                                                 |                              |                                     | 10   |      | μs   |
|                                                    |                             |                                                                           |                              | 20                                  |      |      | μs   |

**Notes** 1. Main system clock  $f_{XX} = f_X/2$  operation (when oscillation mode selection register (OSMS) is set to 00H)

2. Main system clock  $f_{XX} = f_X$  operation (when OSMS is set to 01H)

3. This is the value when the external clock is used. The value is 114 μs (min.) when the crystal resonator is used.

4. In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register (SCS), selection of  $f_{sam}$  is possible between  $f_{XX}/2^{N+1}$ ,  $f_{XX}/32$ ,  $f_{XX}/64$  and  $f_{XX}/128$  (when  $N = 0$  to 4).

$T_{CY}$  vs  $V_{DD}$  (At main system clock  $f_{xx} = f_x/2$  operation) $T_{CY}$  vs  $V_{DD}$  (At main system clock  $f_{xx} = f_x$  operation)**(2) Serial Interface ( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 2.0$  to  $6.0$  V)****(a) Serial interface channel 0****(i) 3-wire serial I/O mode ( $\overline{SCK0}$ ... Internal clock output)**

| Parameter                                              | Symbol     | Test Conditions                              | MIN.             | TYP. | MAX. | Unit |
|--------------------------------------------------------|------------|----------------------------------------------|------------------|------|------|------|
| $\overline{SCK0}$ cycle time                           | $t_{KCY1}$ | $4.5\text{ V} \leq V_{DD} \leq 6.0\text{ V}$ | 800              |      |      | ns   |
|                                                        |            | $2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$    | 1600             |      |      | ns   |
|                                                        |            |                                              | 3200             |      |      | ns   |
| $\overline{SCK0}$ high/low-level width                 | $t_{KH1},$ | $V_{DD} = 4.5\text{ to }6.0\text{ V}$        | $t_{KCY1}/2-50$  |      |      | ns   |
|                                                        | $t_{KL1}$  |                                              | $t_{KCY1}/2-100$ |      |      | ns   |
| SI0 setup time (to $\overline{SCK0}\uparrow$ )         | $t_{SIK1}$ | $4.5\text{ V} \leq V_{DD} \leq 6.0\text{ V}$ | 100              |      |      | ns   |
|                                                        |            | $2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$    | 150              |      |      | ns   |
|                                                        |            |                                              | 300              |      |      | ns   |
| SI0 hold time (from $\overline{SCK0}\uparrow$ )        | $t_{KSI1}$ |                                              | 400              |      |      | ns   |
| SO0 output delay time from $\overline{SCK0}\downarrow$ | $t_{KSO1}$ | $C = 100\text{ pF}^{\text{Note}}$            |                  |      | 300  | ns   |

**Note** C is the load capacitance of  $\overline{SCK0}$ , SO0 output line.

(ii) 3-wire serial I/O mode ( $\overline{\text{SCK0}}$ ...External clock input)

| Parameter                                                     | Symbol                                | Test Conditions                                       | MIN. | TYP. | MAX. | Unit |
|---------------------------------------------------------------|---------------------------------------|-------------------------------------------------------|------|------|------|------|
| $\overline{\text{SCK0}}$ cycle time                           | $t_{\text{KCY2}}$                     | $4.5 \text{ V} \leq V_{\text{DD}} \leq 6.0 \text{ V}$ | 800  |      |      | ns   |
|                                                               |                                       | $2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$    | 1600 |      |      | ns   |
|                                                               |                                       |                                                       | 3200 |      |      | ns   |
| $\overline{\text{SCK0}}$ high/low-level width                 | $t_{\text{KH2}},$<br>$t_{\text{KL2}}$ | $4.5 \text{ V} \leq V_{\text{DD}} \leq 6.0 \text{ V}$ | 400  |      |      | ns   |
|                                                               |                                       | $2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$    | 800  |      |      | ns   |
|                                                               |                                       |                                                       | 1600 |      |      | ns   |
| SI0 setup time (to $\overline{\text{SCK0}}\uparrow$ )         | $t_{\text{SIK2}}$                     |                                                       | 100  |      |      | ns   |
| SI0 hold time (from $\overline{\text{SCK0}}\uparrow$ )        | $t_{\text{KSI2}}$                     |                                                       | 400  |      |      | ns   |
| SO0 output delay time from $\overline{\text{SCK0}}\downarrow$ | $t_{\text{KSO2}}$                     | $C = 100 \text{ pF}$ <sup>Note</sup>                  |      |      | 300  | ns   |
| $\overline{\text{SCK0}}$ rise, fall time                      | $t_{\text{R2}},$<br>$t_{\text{F2}}$   |                                                       |      |      | 1000 | ns   |

**Note** C is the load capacitance of SO0 output line.

(iii) SBI mode ( $\overline{\text{SCK0}}$ ...Internal clock output)

| Parameter                                                          | Symbol                                | Test Conditions                                                  |                                                 | MIN.                    | TYP. | MAX. | Unit |
|--------------------------------------------------------------------|---------------------------------------|------------------------------------------------------------------|-------------------------------------------------|-------------------------|------|------|------|
| $\overline{\text{SCK0}}$ cycle time                                | $t_{\text{KCY3}}$                     | $V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$                  |                                                 | 800                     |      |      | ns   |
|                                                                    |                                       |                                                                  |                                                 | 3200                    |      |      | ns   |
| $\overline{\text{SCK0}}$ high/low-level width                      | $t_{\text{KH3}},$<br>$t_{\text{KL3}}$ | $V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$                  |                                                 | $t_{\text{KCY3}}/2-50$  |      |      | ns   |
|                                                                    |                                       |                                                                  |                                                 | $t_{\text{KCY3}}/2-150$ |      |      | ns   |
| SB0, SB1 setup time (to $\overline{\text{SCK0}}\uparrow$ )         | $t_{\text{SIK3}}$                     | $V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$                  |                                                 | 100                     |      |      | ns   |
|                                                                    |                                       |                                                                  |                                                 | 300                     |      |      | ns   |
| SB0, SB1 hold time (from $\overline{\text{SCK0}}\uparrow$ )        | $t_{\text{KSI3}}$                     |                                                                  |                                                 | $t_{\text{KCY3}}/2$     |      |      | ns   |
| SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$ | $t_{\text{KSO3}}$                     | $R = 1 \text{ k}\Omega,$<br>$C = 100 \text{ pF}$ <sup>Note</sup> | $V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$ | 0                       |      | 250  | ns   |
|                                                                    |                                       |                                                                  |                                                 | 0                       |      | 1000 | ns   |
| SB0, SB1 $\downarrow$ from $\overline{\text{SCK0}}\uparrow$        | $t_{\text{KSB}}$                      |                                                                  |                                                 | $t_{\text{KCY3}}$       |      |      | ns   |
| $\overline{\text{SCK0}}\downarrow$ from SB0, SB1 $\downarrow$      | $t_{\text{SBK}}$                      |                                                                  |                                                 | $t_{\text{KCY3}}$       |      |      | ns   |
| SB0, SB1 high-level width                                          | $t_{\text{SBH}}$                      |                                                                  |                                                 | $t_{\text{KCY3}}$       |      |      | ns   |
| SB0, SB1 low-level width                                           | $t_{\text{SBL}}$                      |                                                                  |                                                 | $t_{\text{KCY3}}$       |      |      | ns   |

**Note** R and C are the load resistance and load capacitance of the  $\overline{\text{SCK0}}$ , SB0 and SB1 output line.

(iv) SBI mode (SCK0...External clock input)

| Parameter                             | Symbol                                 | Test Conditions                          |                                | MIN.                 | TYP. | MAX. | Unit |
|---------------------------------------|----------------------------------------|------------------------------------------|--------------------------------|----------------------|------|------|------|
| SCK0 cycle time                       | t <sub>KCY4</sub>                      | V <sub>DD</sub> = 4.5 to 6.0 V           |                                | 800                  |      |      | ns   |
|                                       |                                        |                                          |                                | 3200                 |      |      | ns   |
| SCK0 high/low-level width             | t <sub>KH4</sub> ,<br>t <sub>KL4</sub> | V <sub>DD</sub> = 4.5 to 6.0 V           |                                | 400                  |      |      | ns   |
|                                       |                                        |                                          |                                | 1600                 |      |      | ns   |
| SB0, SB1 setup time (to SCK0↑)        | t <sub>SIK4</sub>                      | V <sub>DD</sub> = 4.5 to 6.0 V           |                                | 100                  |      |      | ns   |
|                                       |                                        |                                          |                                | 300                  |      |      | ns   |
| SB0, SB1 hold time (from SCK0↑)       | t <sub>KSI4</sub>                      |                                          |                                | t <sub>KCY4</sub> /2 |      |      | ns   |
| SB0, SB1 output delay time from SCK0↓ | t <sub>KSO4</sub>                      | R = 1 kΩ ,<br>C = 100 pF <sup>Note</sup> | V <sub>DD</sub> = 4.5 to 6.0 V | 0                    |      | 300  | ns   |
|                                       |                                        |                                          |                                | 0                    |      | 1000 | ns   |
| SB0, SB1↓ from SCK0↑                  | t <sub>KSB</sub>                       |                                          |                                | t <sub>KCY4</sub>    |      |      | ns   |
| SCK0↓ from SB0, SB1↓                  | t <sub>SBK</sub>                       |                                          |                                | t <sub>KCY4</sub>    |      |      | ns   |
| SB0, SB1 high-level width             | t <sub>SBH</sub>                       |                                          |                                | t <sub>KCY4</sub>    |      |      | ns   |
| SB0, SB1 low-level width              | t <sub>SBL</sub>                       |                                          |                                | t <sub>KCY4</sub>    |      |      | ns   |
| SCK0 rise, fall time                  | t <sub>R4</sub> ,<br>t <sub>F4</sub>   |                                          |                                |                      |      | 1000 | ns   |

**Note** R and C are the load resistance and load capacitance of the SB0 and SB1 output line.

(v) 2-wire serial I/O mode (SCK0... Internal clock output)

| Parameter                                                                                 | Symbol            | Test Conditions                         |                                                     | MIN.                    | TYP. | MAX. | Unit |
|-------------------------------------------------------------------------------------------|-------------------|-----------------------------------------|-----------------------------------------------------|-------------------------|------|------|------|
| $\overline{\text{SCK0}}$ cycle time                                                       | $t_{\text{KCY5}}$ | R = 1 kΩ,<br>C = 100 pF <sup>Note</sup> | V <sub>DD</sub> = 2.7 to 6.0 V                      | 1600                    |      |      | ns   |
|                                                                                           |                   |                                         |                                                     | 3200                    |      |      | ns   |
| $\overline{\text{SCK0}}$ high-level width                                                 | $t_{\text{KH5}}$  |                                         | V <sub>DD</sub> = 2.7 to 6.0 V                      | $t_{\text{KCY5}}/2-160$ |      |      | ns   |
|                                                                                           |                   |                                         |                                                     | $t_{\text{KCY5}}/2-190$ |      |      | ns   |
| $\overline{\text{SCK0}}$ low-level width                                                  | $t_{\text{KL5}}$  |                                         | V <sub>DD</sub> = 4.5 to 6.0 V                      | $t_{\text{KCY5}}/2-50$  |      |      | ns   |
|                                                                                           |                   |                                         |                                                     | $t_{\text{KCY5}}/2-100$ |      |      | ns   |
| SB0, $\overline{\text{SB1}}$ setup time<br>(to $\overline{\text{SCK0}}\uparrow$ )         | $t_{\text{SIK5}}$ |                                         | $4.5\text{ V} \leq V_{\text{DD}} \leq 6.0\text{ V}$ | 300                     |      |      | ns   |
|                                                                                           |                   |                                         | $2.7\text{ V} \leq V_{\text{DD}} < 4.5\text{ V}$    | 350                     |      |      | ns   |
|                                                                                           |                   |                                         |                                                     | 400                     |      |      | ns   |
| SB0, $\overline{\text{SB1}}$ hold time<br>(from $\overline{\text{SCK0}}\uparrow$ )        | $t_{\text{KSI5}}$ |                                         |                                                     | 600                     |      |      | ns   |
| SB0, $\overline{\text{SB1}}$ output delay<br>time from $\overline{\text{SCK0}}\downarrow$ | $t_{\text{KSO5}}$ |                                         |                                                     |                         |      | 300  | ns   |

**Note** R and C are the load resistance and load capacitance of the SCK0, SB0 and SB1 output line.

**(vi) 2-wire serial I/O mode ( $\overline{\text{SCK0}}$ ... External clock input)**

| Parameter                                                                              | Symbol                               | Test Conditions                                                   | MIN.                                            | TYP. | MAX. | Unit |
|----------------------------------------------------------------------------------------|--------------------------------------|-------------------------------------------------------------------|-------------------------------------------------|------|------|------|
| $\overline{\text{SCK0}}$ cycle time                                                    | $t_{\text{KCY6}}$                    | $V_{\text{DD}} = 2.7 \text{ to } 6.0 \text{ V}$                   | 1600                                            |      |      | ns   |
|                                                                                        |                                      |                                                                   | 3200                                            |      |      | ns   |
| $\overline{\text{SCK0}}$ high-level width                                              | $t_{\text{KH6}}$                     | $V_{\text{DD}} = 2.7 \text{ to } 6.0 \text{ V}$                   | 650                                             |      |      | ns   |
|                                                                                        |                                      |                                                                   | 1300                                            |      |      | ns   |
| $\overline{\text{SCK0}}$ low-level width                                               | $t_{\text{KL6}}$                     | $V_{\text{DD}} = 2.7 \text{ to } 6.0 \text{ V}$                   | 800                                             |      |      | ns   |
|                                                                                        |                                      |                                                                   | 1600                                            |      |      | ns   |
| SB0, $\overline{\text{SB1}}$ setup time (to $\overline{\text{SCK0}}\uparrow$ )         | $t_{\text{SIK6}}$                    |                                                                   | 100                                             |      |      | ns   |
| SB0, $\overline{\text{SB1}}$ hold time (from $\overline{\text{SCK0}}\uparrow$ )        | $t_{\text{KSI6}}$                    |                                                                   | $t_{\text{KCY6}}/2$                             |      |      | ns   |
| SB0, $\overline{\text{SB1}}$ output delay time from $\overline{\text{SCK0}}\downarrow$ | $t_{\text{KSO6}}$                    | $R = 1 \text{ k}\Omega$ ,<br>$C = 100 \text{ pF}$ <sup>Note</sup> | $V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$ | 0    | 300  | ns   |
|                                                                                        |                                      |                                                                   |                                                 | 0    | 500  | ns   |
| $\overline{\text{SCK0}}$ rise, fall time                                               | $t_{\text{R6}}$ ,<br>$t_{\text{F6}}$ |                                                                   |                                                 |      | 1000 | ns   |

**Note** R and C are the load resistance and load capacitance of the SB0 and SB1 output line.

**(b) Serial interface channel 2****(i) 3-wire serial I/O mode ( $\overline{\text{SCK2}}$ ... Internal clock output)**

| Parameter                                                     | Symbol                                 | Test Conditions                                       | MIN.                    | TYP. | MAX. | Unit |
|---------------------------------------------------------------|----------------------------------------|-------------------------------------------------------|-------------------------|------|------|------|
| $\overline{\text{SCK2}}$ cycle time                           | $t_{\text{KCY7}}$                      | $4.5 \text{ V} \leq V_{\text{DD}} \leq 6.0 \text{ V}$ | 800                     |      |      | ns   |
|                                                               |                                        | $2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$    | 1600                    |      |      | ns   |
|                                                               |                                        |                                                       | 3200                    |      |      | ns   |
| $\overline{\text{SCK2}}$ high/low-level width                 | $t_{\text{KH7}}$ ,<br>$t_{\text{KL7}}$ | $V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$       | $t_{\text{KCY7}}/2-50$  |      |      | ns   |
|                                                               |                                        |                                                       | $t_{\text{KCY7}}/2-100$ |      |      | ns   |
| SI2 setup time (to $\overline{\text{SCK2}}\uparrow$ )         | $t_{\text{SIK7}}$                      | $4.5 \text{ V} \leq V_{\text{DD}} \leq 6.0 \text{ V}$ | 100                     |      |      | ns   |
|                                                               |                                        | $2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$    | 150                     |      |      | ns   |
|                                                               |                                        |                                                       | 300                     |      |      | ns   |
| SI2 hold time (from $\overline{\text{SCK2}}\uparrow$ )        | $t_{\text{KSI7}}$                      |                                                       | 400                     |      |      | ns   |
| SO2 output delay time from $\overline{\text{SCK2}}\downarrow$ | $t_{\text{KSO1}}$                      | $C = 100 \text{ pF}$ <sup>Note</sup>                  |                         |      | 300  | ns   |

**Note** C is the load capacitance of  $\overline{\text{SCK2}}$ , SO2 output line.



**(ii) 3-wire serial I/O mode (SCK2...External clock input)**

| Parameter                                    | Symbol                  | Test Conditions                              | MIN. | TYP. | MAX. | Unit |
|----------------------------------------------|-------------------------|----------------------------------------------|------|------|------|------|
| SCK2 cycle time                              | $t_{KCY8}$              | $4.5\text{ V} \leq V_{DD} \leq 6.0\text{ V}$ | 800  |      |      | ns   |
|                                              |                         | $2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$    | 1600 |      |      | ns   |
|                                              |                         |                                              | 3200 |      |      | ns   |
| SCK2 high/low-level width                    | $t_{KH8},$<br>$t_{KL8}$ | $4.5\text{ V} \leq V_{DD} \leq 6.0\text{ V}$ | 400  |      |      | ns   |
|                                              |                         | $2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$    | 800  |      |      | ns   |
|                                              |                         |                                              | 1600 |      |      | ns   |
| SI2 setup time (to SCK2 $\uparrow$ )         | $t_{SIK8}$              |                                              | 100  |      |      | ns   |
| SI2 hold time (from SCK2 $\uparrow$ )        | $t_{KSI8}$              |                                              | 400  |      |      | ns   |
| SO2 output delay time from SCK2 $\downarrow$ | $t_{KSO8}$              | $C = 100\text{ pF}$ <sup>Note</sup>          |      |      | 300  | ns   |
| SCK2 rise, fall time                         | $t_{R8},$<br>$t_{F8}$   |                                              |      |      | 1000 | ns   |

**Note** C is the load capacitance of SO2 output line.

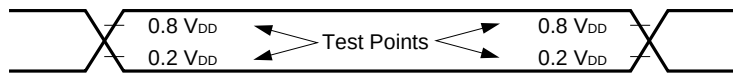
**(iii) UART mode (Dedicated baud rate generator output)**

| Parameter     | Symbol | Test Conditions                              | MIN. | TYP. | MAX.  | Unit |
|---------------|--------|----------------------------------------------|------|------|-------|------|
| Transfer rate |        | $4.5\text{ V} \leq V_{DD} \leq 6.0\text{ V}$ |      |      | 78125 | bps  |
|               |        | $2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$    |      |      | 39063 | bps  |
|               |        |                                              |      |      | 19531 | bps  |

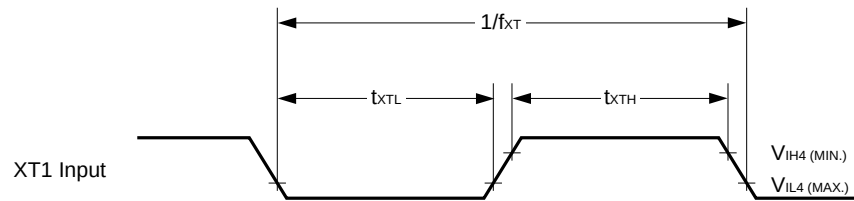
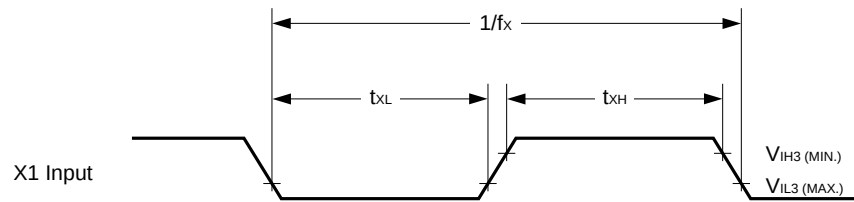
**(iv) UART mode (External clock input)**

| Parameter                 | Symbol                  | Test Conditions                              | MIN. | TYP. | MAX.  | Unit |
|---------------------------|-------------------------|----------------------------------------------|------|------|-------|------|
| ASCK cycle time           | $t_{KCY9}$              | $4.5\text{ V} \leq V_{DD} \leq 6.0\text{ V}$ | 800  |      |       | ns   |
|                           |                         | $2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$    | 1600 |      |       | ns   |
|                           |                         |                                              | 3200 |      |       | ns   |
| ASCK high/low-level width | $t_{KH9},$<br>$t_{KL9}$ | $4.5\text{ V} \leq V_{DD} \leq 6.0\text{ V}$ | 400  |      |       | ns   |
|                           |                         | $2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$    | 800  |      |       | ns   |
|                           |                         |                                              | 1600 |      |       | ns   |
| Transfer rate             |                         | $4.5\text{ V} \leq V_{DD} \leq 6.0\text{ V}$ |      |      | 39063 | bps  |
|                           |                         | $2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$    |      |      | 19531 | bps  |
|                           |                         |                                              |      |      | 9766  | bps  |
| ASCK rise, fall time      | $t_{R9},$<br>$t_{F9}$   |                                              |      |      | 1000  | ns   |

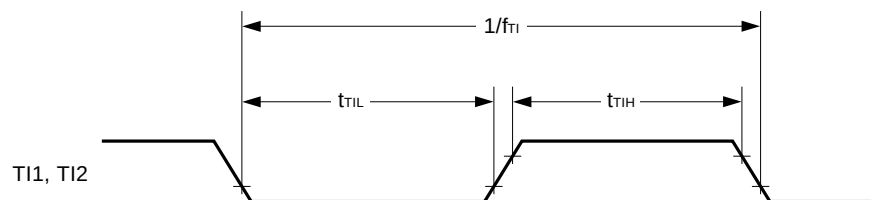
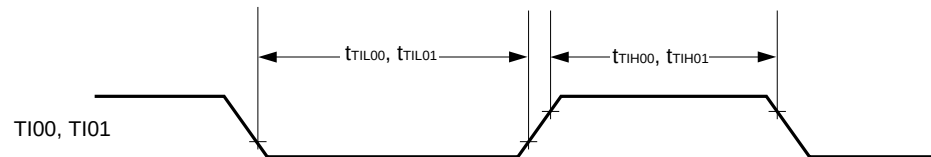
# AC Timing Test Point (Excluding X1, XT1 Input)



## Clock Timing

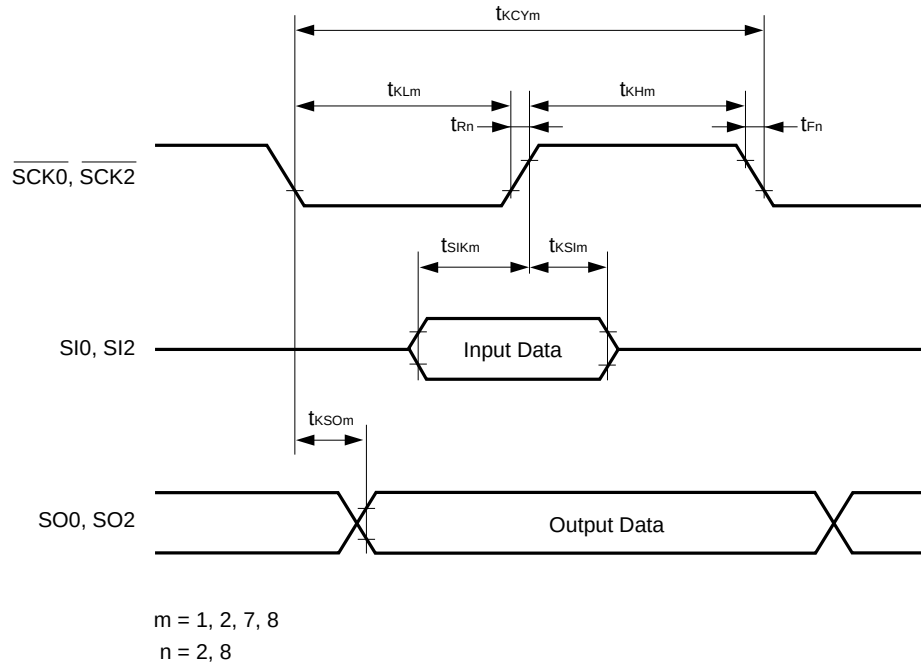


## T1 Timing

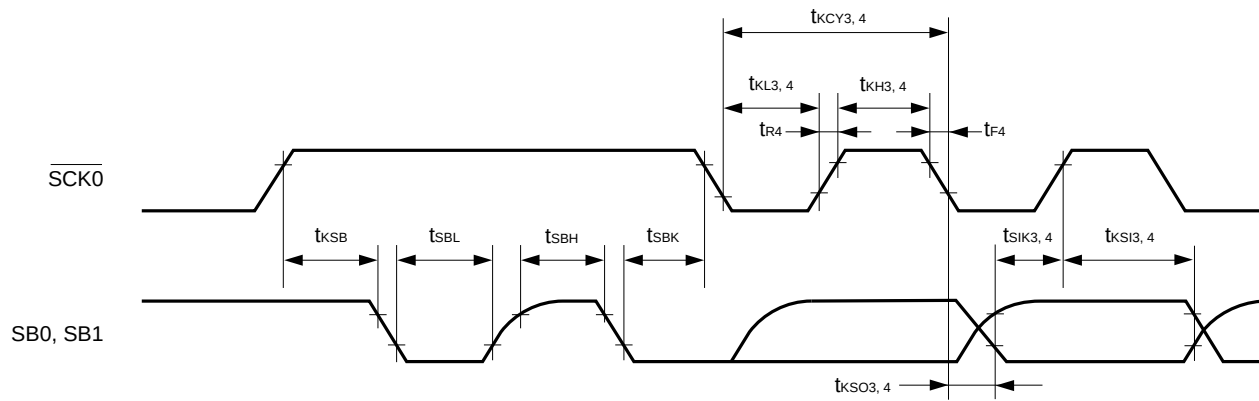


## Serial Transfer Timing

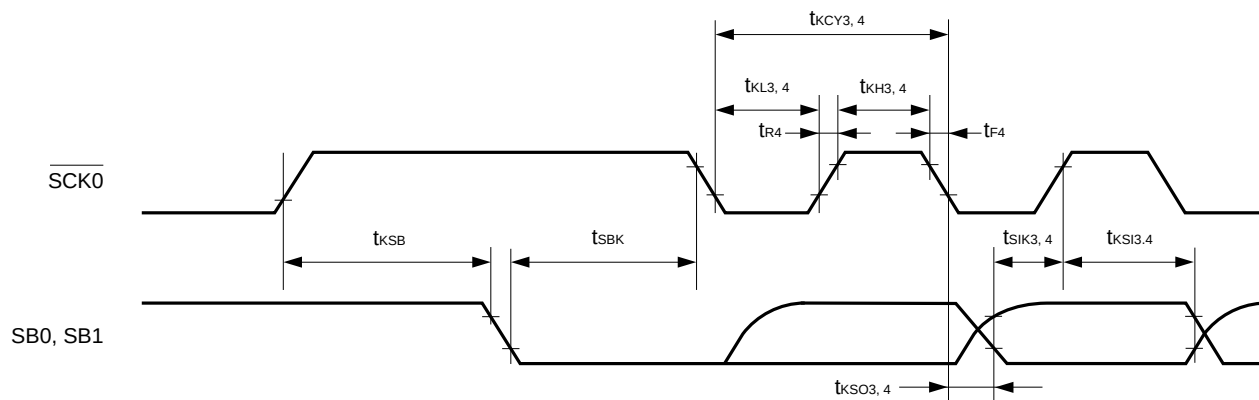
### 3-wire serial I/O mode:

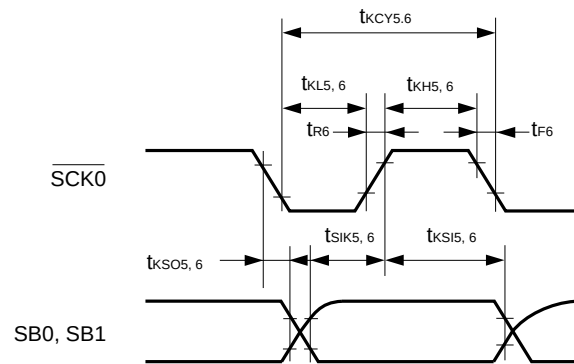
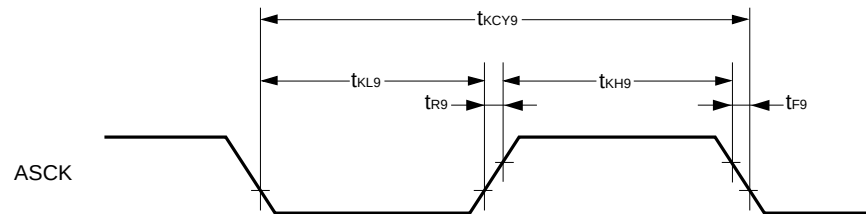


### SBI mode (bus release signal transfer):



### SBI mode (command signal transfer):



**2-wire serial I/O mode:****UART mode:****A/D Converter ( $T_A = -40$  to  $+85$  °C,  $\text{AV}_{\text{DD}} = \text{V}_{\text{DD}} = 4.5$  to  $6.0$  V,  $\text{AV}_{\text{SS}} = \text{V}_{\text{SS}} = 0$  V)**

| Parameter                                                 | Symbol                    | Test Conditions                                                        | MIN.                    | TYP. | MAX.                     | Unit             |
|-----------------------------------------------------------|---------------------------|------------------------------------------------------------------------|-------------------------|------|--------------------------|------------------|
| Resolution                                                |                           |                                                                        | 8                       | 8    | 8                        | bit              |
| Overall error <sup>Note</sup>                             |                           | $4.5 \text{ V} \leq \text{AV}_{\text{REF}} \leq \text{AV}_{\text{DD}}$ |                         |      | 2.0                      | %                |
| Conversion time                                           | $t_{\text{CONV}}$         |                                                                        | 19.1                    |      | 200                      | $\mu\text{s}$    |
| Sampling time                                             | $t_{\text{SAMP}}$         |                                                                        | $12/f_{\text{xx}}$      |      |                          | $\mu\text{s}$    |
| Analog input voltage                                      | $\text{V}_{\text{IAN}}$   |                                                                        | $\text{AV}_{\text{SS}}$ |      | $\text{AV}_{\text{REF}}$ | V                |
| Reference voltage                                         | $\text{AV}_{\text{REF}}$  |                                                                        | 2.0                     |      | $\text{AV}_{\text{DD}}$  | V                |
| $\text{AV}_{\text{REF}}\text{-AV}_{\text{SS}}$ resistance | $\text{RA}_{\text{IREF}}$ |                                                                        | 4                       | 14   |                          | $\text{k}\Omega$ |

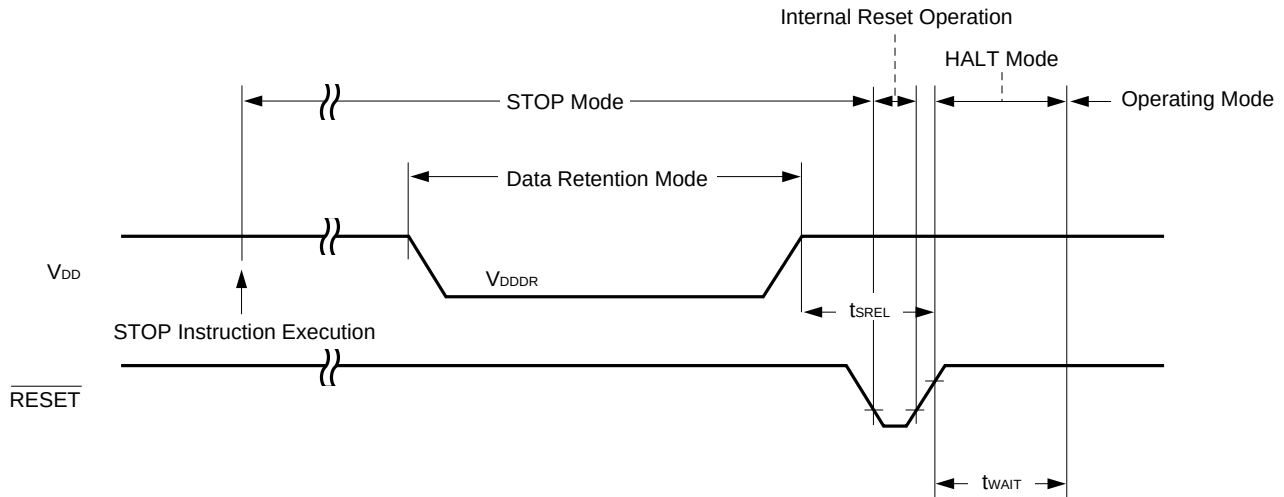
**Note** Quantization error ( $\pm 1/2$  LSB) is not included. This is expressed in proportion to the full-scale value.

**DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS ( $T_A = -40$  to  $+85$  °C)**

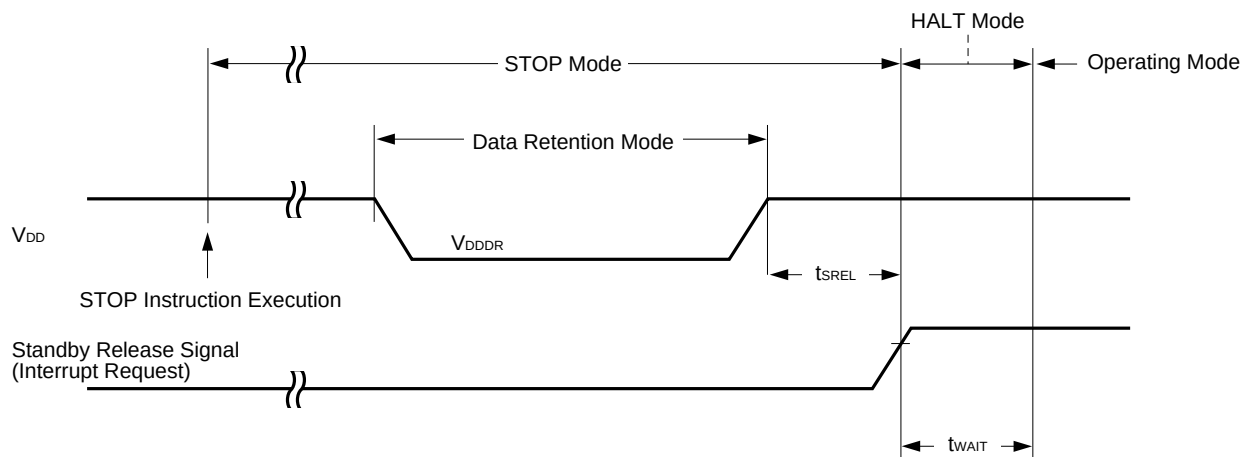
| Parameter                           | Symbol     | Test Conditions                                                                   | MIN. | TYP.         | MAX. | Unit |
|-------------------------------------|------------|-----------------------------------------------------------------------------------|------|--------------|------|------|
| Data retention supply voltage       | $V_{DDDR}$ |                                                                                   | 1.8  |              | 6.0  | V    |
| Data retention power supply current | $I_{DDDR}$ | $V_{DDDR} = 1.8$ V<br>Subsystem clock stop and<br>feed-back resistor disconnected |      | 0.1          | 10   | μA   |
| Release signal set time             | $t_{SREL}$ |                                                                                   | 0    |              |      | μs   |
| Oscillation stabilization wait time | $t_{WAIT}$ | Release by $\overline{RESET}$                                                     |      | $2^{17}/f_x$ |      | ms   |
|                                     |            | Release by interrupt                                                              |      | <b>Note</b>  |      | ms   |

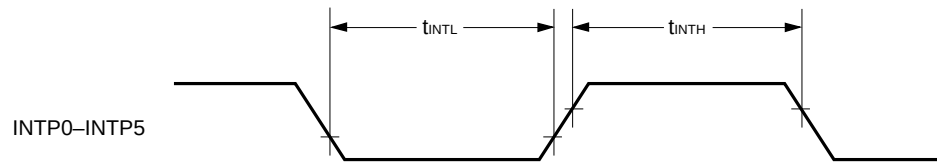
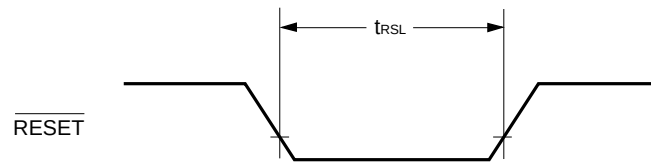
**Note** In combination with bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time select register (OSTS), selection of  $2^{12}/f_{xx}$  and  $2^{14}/f_{xx}$  to  $2^{17}/f_{xx}$  is possible.

**Data Retention Timing (STOP Mode Release by  $\overline{RESET}$ )**



**Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)**



**Interrupt Input Timing** **$\overline{\text{RESET}}$  Input Timing**

## PROM PROGRAMMING CHARACTERISTICS

## DC Characteristics

(1) PROM Write Mode ( $T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{DD} = 6.5 \pm 0.25\text{ V}$ ,  $V_{PP} = 12.5 \pm 0.3\text{ V}$ )

| Parameter               | Symbol   | Symbol <sup>Note</sup> | Test Conditions                  | MIN.           | TYP. | MAX.         | Unit          |
|-------------------------|----------|------------------------|----------------------------------|----------------|------|--------------|---------------|
| Input voltage, high     | $V_{IH}$ | $V_{IH}$               |                                  | $0.7 V_{DD}$   |      | $V_{DD}$     | V             |
| Input voltage, low      | $V_{IL}$ | $V_{IL}$               |                                  | 0              |      | $0.3 V_{DD}$ | V             |
| Output voltage, high    | $V_{OH}$ | $V_{OH}$               | $I_{OH} = -1\text{ mA}$          | $V_{DD} - 1.0$ |      |              | V             |
| Output voltage, low     | $V_{OL}$ | $V_{OL}$               | $I_{OL} = 1.6\text{ mA}$         |                |      | 0.4          | V             |
| Input leakage current   | $I_{LI}$ | $I_{LI}$               | $0 \leq V_{IN} \leq V_{DD}$      | -10            |      | +10          | $\mu\text{A}$ |
| $V_{PP}$ supply voltage | $V_{PP}$ | $V_{PP}$               |                                  | 12.2           | 12.5 | 12.8         | V             |
| $V_{DD}$ supply voltage | $V_{DD}$ | $V_{CC}$               |                                  | 6.25           | 6.5  | 6.75         | V             |
| $V_{PP}$ supply current | $I_{PP}$ | $I_{PP}$               | $\overline{\text{PGM}} = V_{IL}$ |                |      | 50           | mA            |
| $V_{DD}$ supply current | $I_{DD}$ | $I_{CC}$               |                                  |                |      | 50           | mA            |

**Note** Symbol corresponding to the  $\mu$ PD27C1001A.

(2) PROM Read Mode ( $T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{DD} = 5.0 \pm 0.5\text{ V}$ ,  $V_{PP} = V_{DD} \pm 0.6\text{ V}$ )

| Parameter               | Symbol    | Symbol <sup>Note</sup> | Test Conditions                                                | MIN.           | TYP.     | MAX.           | Unit          |
|-------------------------|-----------|------------------------|----------------------------------------------------------------|----------------|----------|----------------|---------------|
| Input voltage, high     | $V_{IH}$  | $V_{IH}$               |                                                                | $0.7 V_{DD}$   |          | $V_{DD}$       | V             |
| Input voltage, low      | $V_{IL}$  | $V_{IL}$               |                                                                | 0              |          | $0.3 V_{DD}$   | V             |
| Output voltage, high    | $V_{OH1}$ | $V_{OH1}$              | $I_{OH} = -1\text{ mA}$                                        | $V_{DD} - 1.0$ |          |                | V             |
|                         | $V_{OH2}$ | $V_{OH2}$              | $I_{OH} = -100\text{ }\mu\text{A}$                             | $V_{DD} - 0.5$ |          |                | V             |
| Output voltage, low     | $V_{OL}$  | $V_{OL}$               | $I_{OL} = 1.6\text{ mA}$                                       |                |          | 0.4            | V             |
| Input leakage current   | $I_{LI}$  | $I_{LI}$               | $0 \leq V_{IN} \leq V_{DD}$                                    | -10            |          | +10            | $\mu\text{A}$ |
| Output leakage current  | $I_{LO}$  | $I_{LO}$               | $0 \leq V_{OUT} \leq V_{DD}$ , $\overline{\text{OE}} = V_{IH}$ | -10            |          | +10            | $\mu\text{A}$ |
| $V_{PP}$ supply voltage | $V_{PP}$  | $V_{PP}$               |                                                                | $V_{DD} - 0.6$ | $V_{DD}$ | $V_{DD} + 0.6$ | V             |
| $V_{DD}$ supply voltage | $V_{DD}$  | $V_{CC}$               |                                                                | 4.5            | 5.0      | 5.5            | V             |
| $V_{PP}$ supply current | $I_{PP}$  | $I_{PP}$               | $V_{PP} = V_{DD}$                                              |                |          | 100            | $\mu\text{A}$ |
| $V_{DD}$ supply current | $I_{DD}$  | $I_{CCA1}$             | $\overline{\text{CE}} = V_{IL}$ , $V_{IN} = V_{IH}$            |                |          | 50             | mA            |

**Note** Symbol corresponding to the  $\mu$ PD27C1001A.

## AC Characteristics

## (1) PROM Write Mode

(a) Page program mode ( $T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{DD} = 6.5 \pm 0.25\text{ V}$ ,  $V_{PP} = 12.5 \pm 0.3\text{ V}$ )

| Parameter                                                                | Symbol     | Symbol <sup>Note</sup> | Test Conditions | MIN.  | TYP. | MAX.  | Unit          |
|--------------------------------------------------------------------------|------------|------------------------|-----------------|-------|------|-------|---------------|
| Address setup time (to $\overline{\text{OE}}\downarrow$ )                | $t_{AS}$   | $t_{AS}$               |                 | 2     |      |       | $\mu\text{s}$ |
| $\overline{\text{OE}}$ setup time                                        | $t_{OES}$  | $t_{OES}$              |                 | 2     |      |       | $\mu\text{s}$ |
| $\overline{\text{CE}}$ setup time (to $\overline{\text{OE}}\downarrow$ ) | $t_{CES}$  | $t_{CES}$              |                 | 2     |      |       | $\mu\text{s}$ |
| Input data setup time (to $\overline{\text{OE}}\downarrow$ )             | $t_{DS}$   | $t_{DS}$               |                 | 2     |      |       | $\mu\text{s}$ |
| Address hold time (from $\overline{\text{OE}}\uparrow$ )                 | $t_{AH}$   | $t_{AH}$               |                 | 2     |      |       | $\mu\text{s}$ |
|                                                                          | $t_{AHL}$  | $t_{AHL}$              |                 | 2     |      |       | $\mu\text{s}$ |
|                                                                          | $t_{AHV}$  | $t_{AHV}$              |                 | 0     |      |       | $\mu\text{s}$ |
| Input data hold time (from $\overline{\text{OE}}\uparrow$ )              | $t_{DH}$   | $t_{DH}$               |                 | 2     |      |       | $\mu\text{s}$ |
| Data output float delay time from $\overline{\text{OE}}\uparrow$         | $t_{DF}$   | $t_{DF}$               |                 | 0     |      | 250   | ns            |
| $V_{PP}$ setup time (to $\overline{\text{OE}}\downarrow$ )               | $t_{VPS}$  | $t_{VPS}$              |                 | 1.0   |      |       | ms            |
| $V_{DD}$ setup time (to $\overline{\text{OE}}\downarrow$ )               | $t_{VDS}$  | $t_{VCS}$              |                 | 1.0   |      |       | ms            |
| Program pulse width                                                      | $t_{PW}$   | $t_{PW}$               |                 | 0.095 | 0.1  | 0.105 | ms            |
| Valid data delay time from $\overline{\text{OE}}\downarrow$              | $t_{OE}$   | $t_{OE}$               |                 |       |      | 1     | $\mu\text{s}$ |
| $\overline{\text{OE}}$ pulse width during data latching                  | $t_{LW}$   | $t_{LW}$               |                 | 1     |      |       | $\mu\text{s}$ |
| $\overline{\text{PGM}}$ setup time                                       | $t_{PGMS}$ | $t_{PGMS}$             |                 | 2     |      |       | $\mu\text{s}$ |
| $\overline{\text{CE}}$ hold time                                         | $t_{CEH}$  | $t_{CEH}$              |                 | 2     |      |       | $\mu\text{s}$ |
| $\overline{\text{OE}}$ hold time                                         | $t_{OEH}$  | $t_{OEH}$              |                 | 2     |      |       | $\mu\text{s}$ |

**Note** Corresponding  $\mu$ PD27C1001A symbol

(b) Byte program mode ( $T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{DD} = 6.5 \pm 0.25\text{ V}$ ,  $V_{PP} = 12.5 \pm 0.3\text{ V}$ )

| Parameter                                                                 | Symbol    | Symbol <sup>Note</sup> | Test Conditions | MIN.  | TYP. | MAX.  | Unit          |
|---------------------------------------------------------------------------|-----------|------------------------|-----------------|-------|------|-------|---------------|
| Address setup time (to $\overline{\text{PGM}}\downarrow$ )                | $t_{AS}$  | $t_{AS}$               |                 | 2     |      |       | $\mu\text{s}$ |
| $\overline{\text{OE}}$ setup time                                         | $t_{OES}$ | $t_{OES}$              |                 | 2     |      |       | $\mu\text{s}$ |
| $\overline{\text{CE}}$ setup time (to $\overline{\text{PGM}}\downarrow$ ) | $t_{CES}$ | $t_{CES}$              |                 | 2     |      |       | $\mu\text{s}$ |
| Input data setup time (to $\overline{\text{PGM}}\downarrow$ )             | $t_{DS}$  | $t_{DS}$               |                 | 2     |      |       | $\mu\text{s}$ |
| Address hold time (from $\overline{\text{OE}}\uparrow$ )                  | $t_{AH}$  | $t_{AH}$               |                 | 2     |      |       | $\mu\text{s}$ |
| Input data hold time (from $\overline{\text{PGM}}\uparrow$ )              | $t_{DH}$  | $t_{DH}$               |                 | 2     |      |       | $\mu\text{s}$ |
| Data output float delay time from $\overline{\text{OE}}\uparrow$          | $t_{DF}$  | $t_{DF}$               |                 | 0     |      | 250   | ns            |
| $V_{PP}$ setup time (to $\overline{\text{PGM}}\downarrow$ )               | $t_{VPS}$ | $t_{VPS}$              |                 | 1.0   |      |       | ms            |
| $V_{DD}$ setup time (to $\overline{\text{PGM}}\downarrow$ )               | $t_{VDS}$ | $t_{VCS}$              |                 | 1.0   |      |       | ms            |
| Program pulse width                                                       | $t_{PW}$  | $t_{PW}$               |                 | 0.095 | 0.1  | 0.105 | ms            |
| Valid data delay time from $\overline{\text{OE}}\downarrow$               | $t_{OE}$  | $t_{OE}$               |                 |       |      | 1     | $\mu\text{s}$ |
| $\overline{\text{OE}}$ hold time                                          | $t_{OEH}$ | —                      |                 | 2     |      |       | $\mu\text{s}$ |

**Note** Corresponding  $\mu$ PD27C1001A symbol



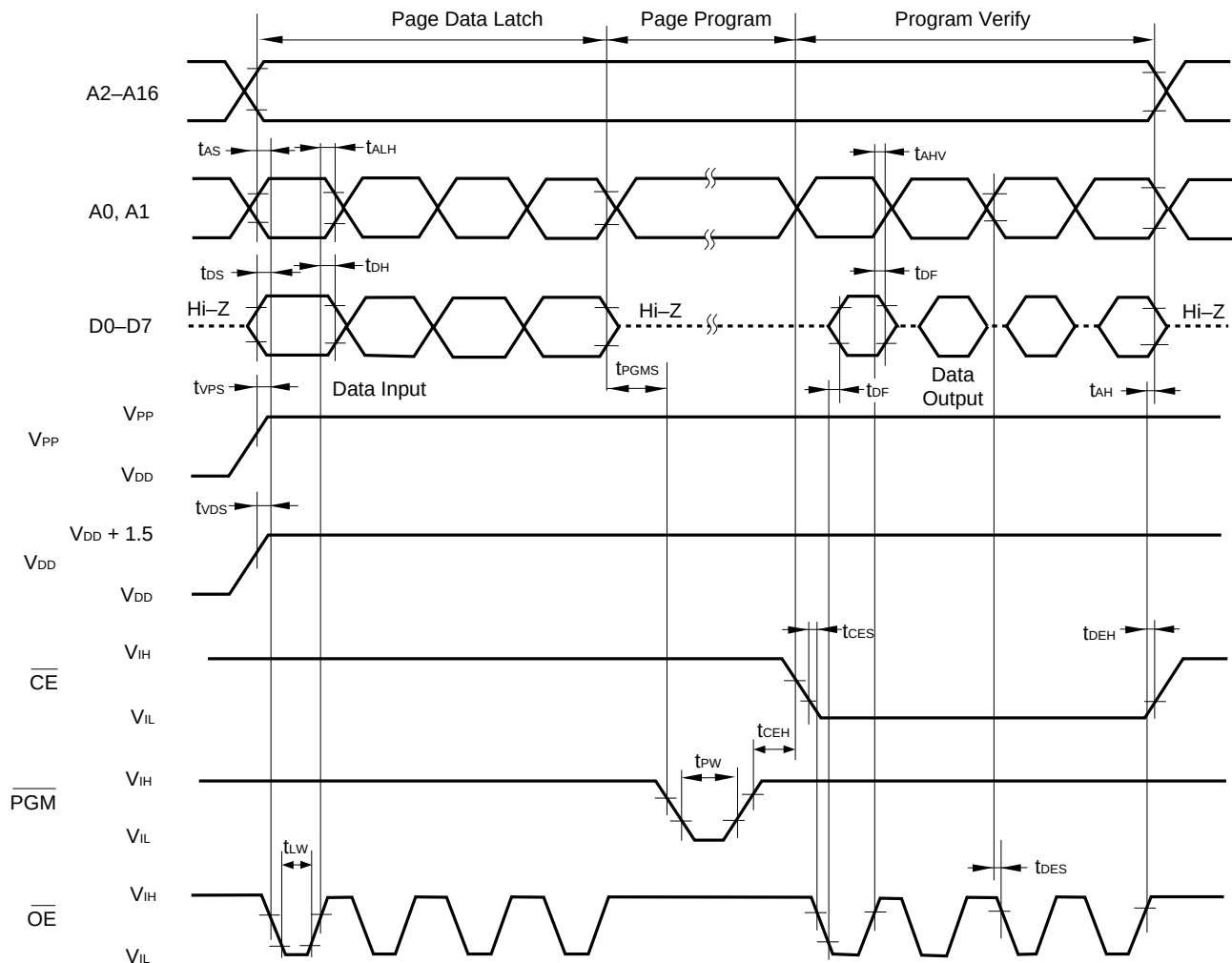
**(2) PROM Read Mode ( $T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{DD} = 5.0 \pm 0.5\text{ V}$ ,  $V_{PP} = V_{DD} \pm 0.6\text{ V}$ )**

| Parameter                                                 | Symbol    | Symbol <sup>Note</sup> | Test Conditions                          | MIN. | TYP. | MAX. | Unit |
|-----------------------------------------------------------|-----------|------------------------|------------------------------------------|------|------|------|------|
| Data output time from address                             | $t_{ACC}$ | $t_{ACC}$              | $\overline{CE} = \overline{OE} = V_{IL}$ |      |      | 800  | ns   |
| Data output delay time from $\overline{CE}\downarrow$     | $t_{CE}$  | $t_{CE}$               | $\overline{OE} = V_{IL}$                 |      |      | 800  | ns   |
| Data output delay time from $\overline{OE}\downarrow$     | $t_{OE}$  | $t_{OE}$               | $\overline{CE} = V_{IL}$                 |      |      | 200  | ns   |
| Data output float delay time from $\overline{OE}\uparrow$ | $t_{DF}$  | $t_{DF}$               | $\overline{CE} = V_{IL}$                 | 0    |      | 60   | ns   |
| Data hold time from address                               | $t_{DH}$  | $t_{DH}$               | $\overline{CE} = \overline{OE} = V_{IL}$ | 0    |      |      | ns   |

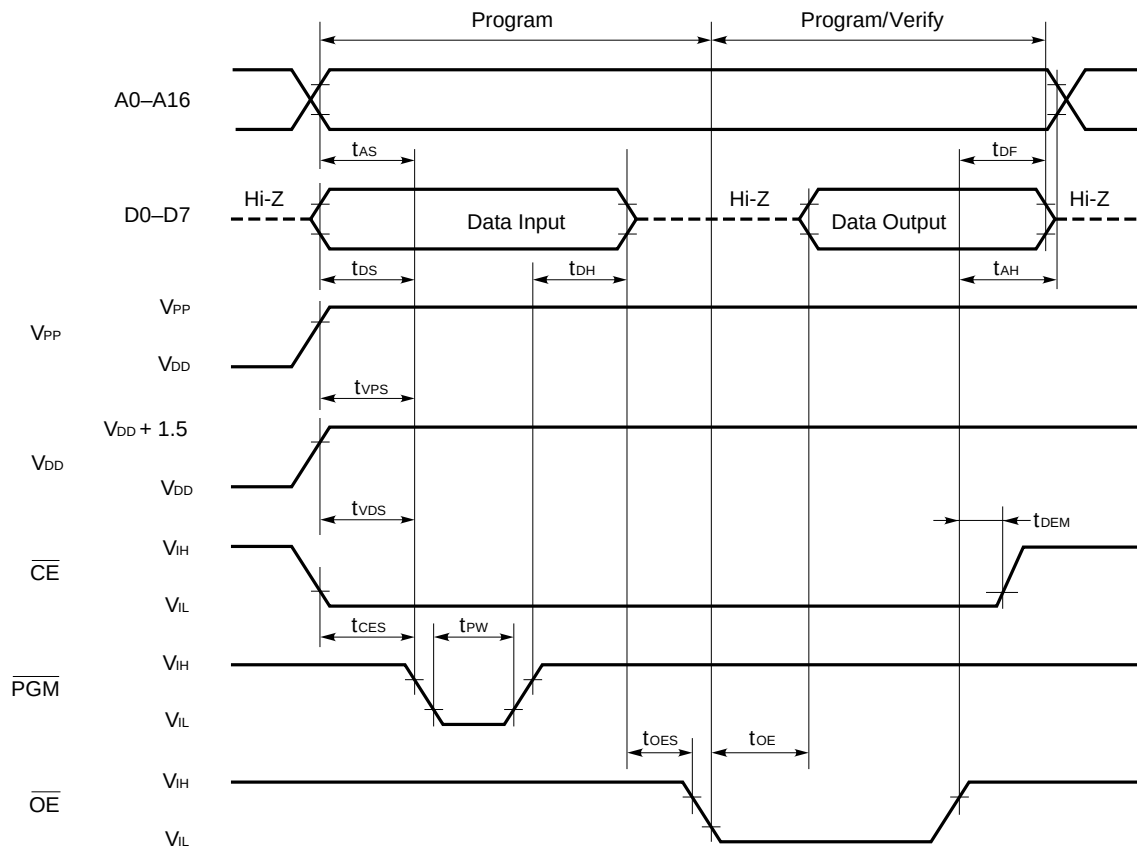
**Note** Corresponding  $\mu$ PD27C1001A symbol

**(3) PROM Programming Mode Setting ( $T_A = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$ )**

| Parameter                        | Symbol    | Test Conditions | MIN. | TYP. | MAX. | Unit          |
|----------------------------------|-----------|-----------------|------|------|------|---------------|
| PROM programming mode setup time | $t_{SMA}$ |                 | 10   |      |      | $\mu\text{s}$ |

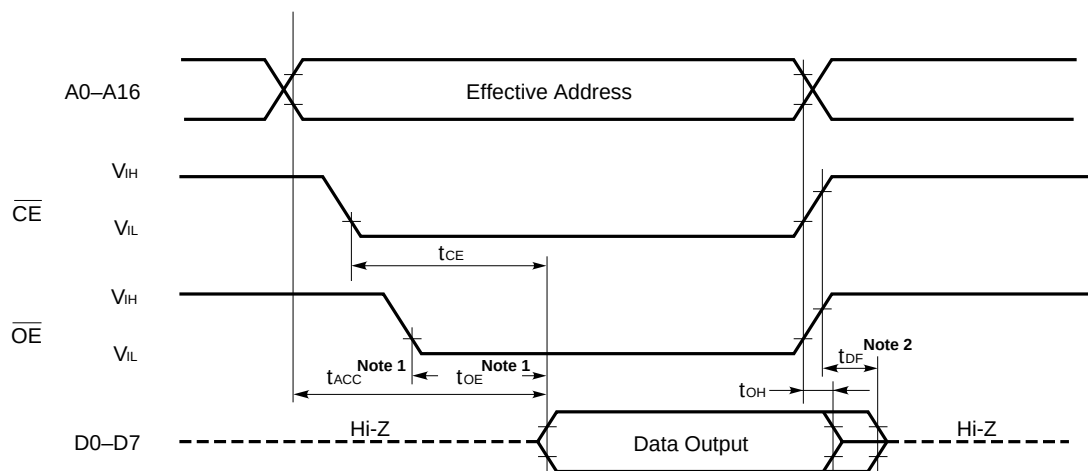
**PROM Write Mode Timing (Page program mode)**

## PROM Write Mode Timing (Byte program mode)



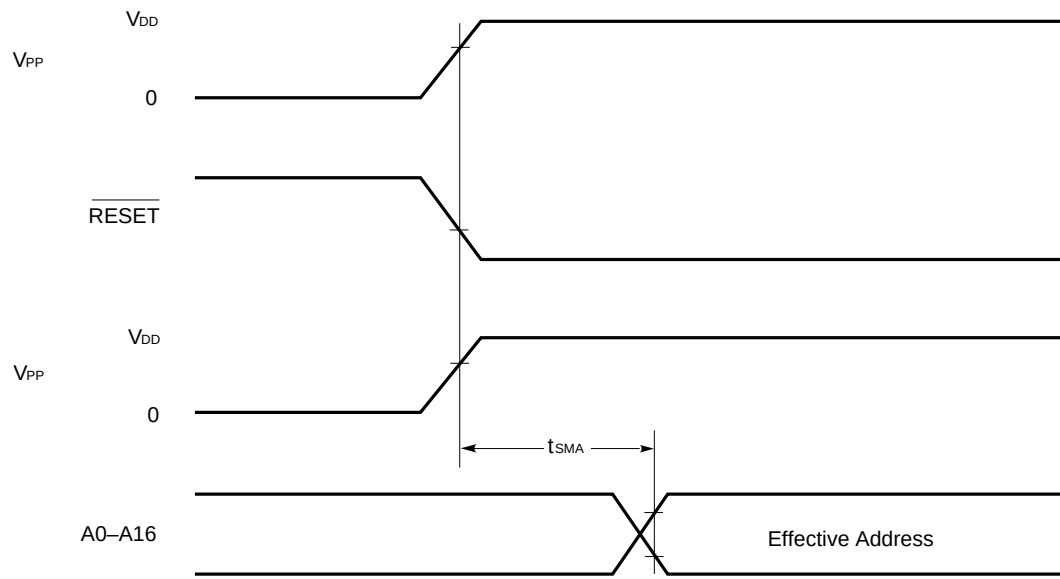
- Cautions**
1.  $V_{DD}$  must be applied before  $V_{PP}$  and cut off after  $V_{PP}$ .
  2.  $V_{PP}$  must not exceed +13.5 V including overshoot.
  3. Removing and reinserting may adversely affect in reliability while +12.5 V is applied to  $V_{PP}$ .

## PROM Read Mode Timing



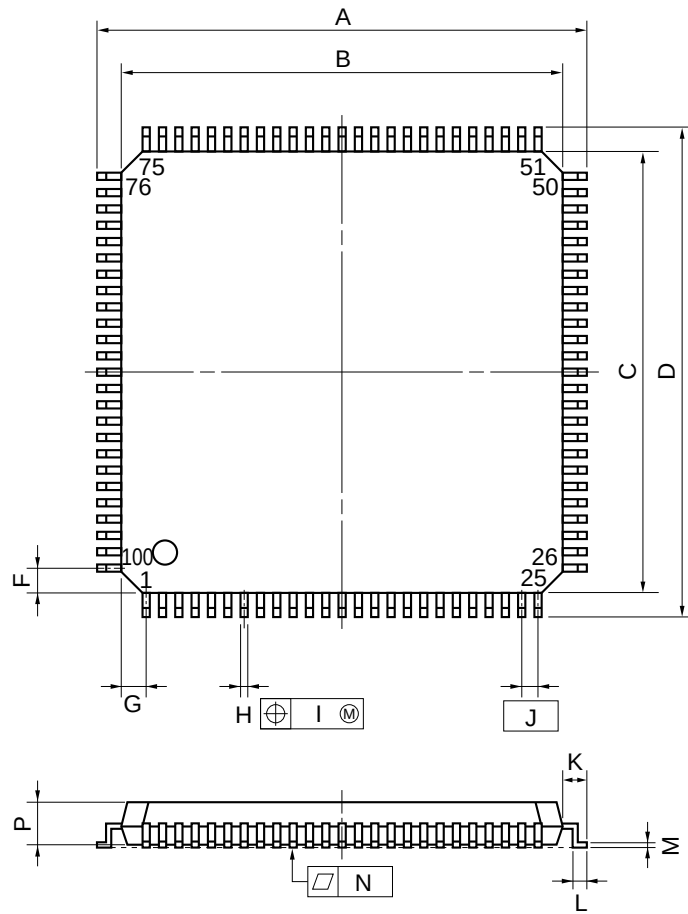
- Notes**
1. When reading within the  $t_{ACC}$  range, the  $\overline{OE}$  input delay time from the  $\overline{CE}$  fall time must be maximum of  $t_{ACC} - t_{OE}$ .
  2.  $t_{DF}$  is the time from the point at which either  $\overline{OE}$  or  $\overline{CE}$  (whichever is first) reaches  $V_{IH}$ .

## PROM Programming Mode Setting Timing

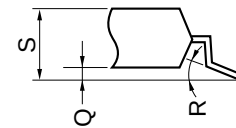


## 7. PACKAGE DRAWINGS

## 100 PIN PLASTIC QFP (FINE PITCH) (□14)



detail of lead end

**NOTE**

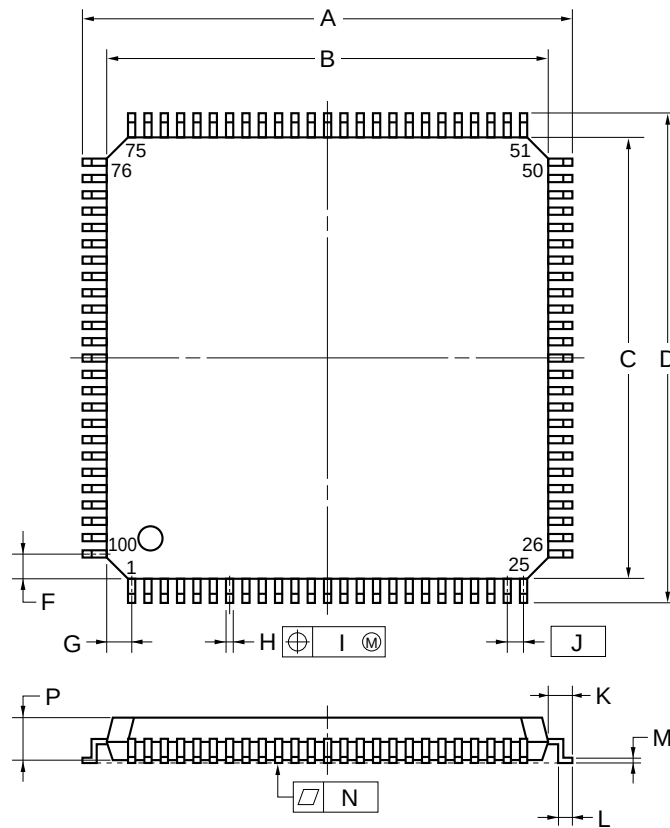
Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

**Remark** Dimensions and materials of ES products are the same as those of the mass production product.

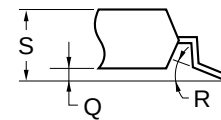
| ITEM | MILLIMETERS                            | INCHES                                    |
|------|----------------------------------------|-------------------------------------------|
| A    | 16.0±0.2                               | 0.630±0.008                               |
| B    | 14.0±0.2                               | 0.551 <sup>+0.009</sup> <sub>-0.008</sub> |
| C    | 14.0±0.2                               | 0.551 <sup>+0.009</sup> <sub>-0.008</sub> |
| D    | 16.0±0.2                               | 0.630±0.008                               |
| F    | 1.0                                    | 0.039                                     |
| G    | 1.0                                    | 0.039                                     |
| H    | 0.22 <sup>+0.05</sup> <sub>-0.04</sub> | 0.009±0.002                               |
| I    | 0.10                                   | 0.004                                     |
| J    | 0.5 (T.P.)                             | 0.020 (T.P.)                              |
| K    | 1.0±0.2                                | 0.039 <sup>+0.009</sup> <sub>-0.008</sub> |
| L    | 0.5±0.2                                | 0.020 <sup>+0.008</sup> <sub>-0.009</sub> |
| M    | 0.17 <sup>+0.03</sup> <sub>-0.07</sub> | 0.007 <sup>+0.001</sup> <sub>-0.003</sub> |
| N    | 0.10                                   | 0.004                                     |
| P    | 1.45                                   | 0.057                                     |
| Q    | 0.125±0.075                            | 0.005±0.003                               |
| R    | 5°±5°                                  | 5°±5°                                     |
| S    | 1.7 MAX.                               | 0.067 MAX.                                |

P100GC-50-7EA-2

## 100 PIN PLASTIC LQFP (FINE PITCH) (14×14)



detail of lead end

**NOTE**

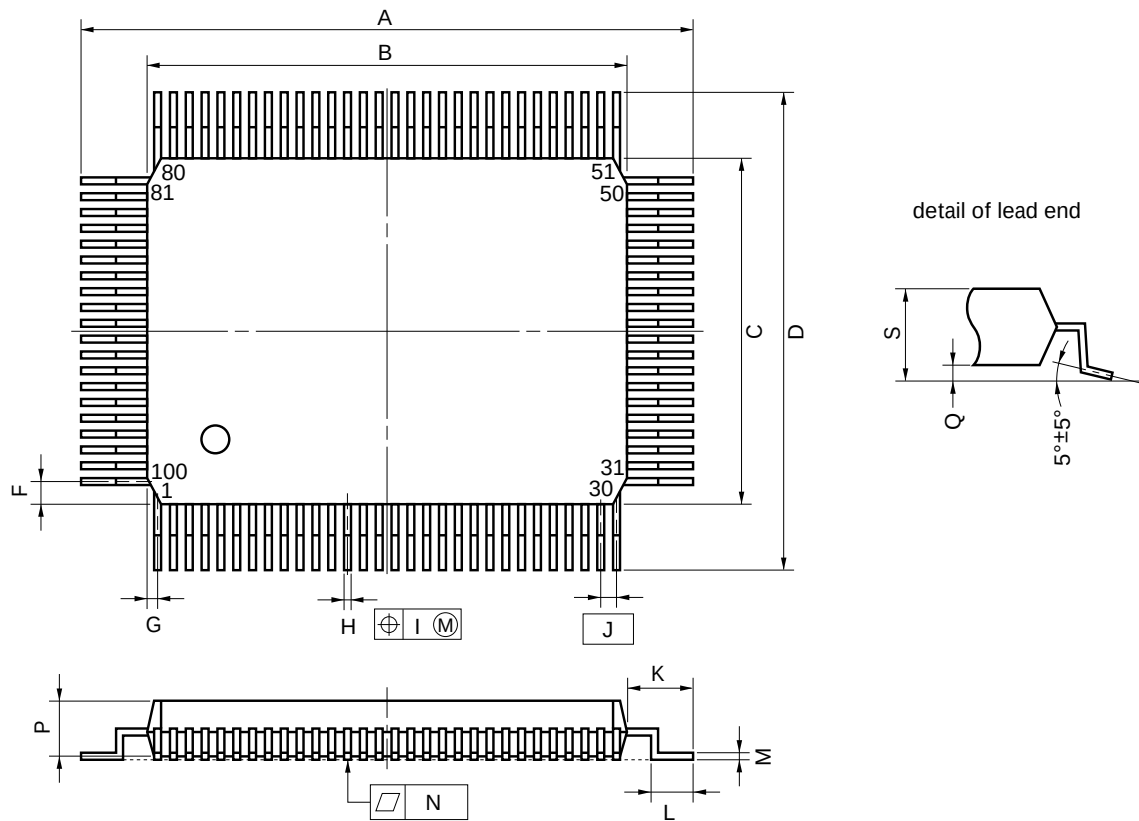
Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

**Remark** Dimensions and materials of ES products are the same as those of the mass production product.

| ITEM | MILLIMETERS                            | INCHES                                    |
|------|----------------------------------------|-------------------------------------------|
| A    | 16.00±0.20                             | 0.630±0.008                               |
| B    | 14.00±0.20                             | 0.551 <sup>+0.009</sup> <sub>-0.008</sub> |
| C    | 14.00±0.20                             | 0.551 <sup>+0.009</sup> <sub>-0.008</sub> |
| D    | 16.00±0.20                             | 0.630±0.008                               |
| F    | 1.00                                   | 0.039                                     |
| G    | 1.00                                   | 0.039                                     |
| H    | 0.22 <sup>+0.05</sup> <sub>-0.04</sub> | 0.009±0.002                               |
| I    | 0.08                                   | 0.003                                     |
| J    | 0.50 (T.P.)                            | 0.020 (T.P.)                              |
| K    | 1.00±0.20                              | 0.039 <sup>+0.009</sup> <sub>-0.008</sub> |
| L    | 0.50±0.20                              | 0.020 <sup>+0.008</sup> <sub>-0.009</sub> |
| M    | 0.17 <sup>+0.03</sup> <sub>-0.07</sub> | 0.007 <sup>+0.001</sup> <sub>-0.003</sub> |
| N    | 0.08                                   | 0.003                                     |
| P    | 1.40±0.05                              | 0.055±0.002                               |
| Q    | 0.10±0.05                              | 0.004±0.002                               |
| R    | 3° <sup>+7°</sup> <sub>-3°</sub>       | 3° <sup>+7°</sup> <sub>-3°</sub>          |
| S    | 1.60 MAX.                              | 0.063 MAX.                                |

S100GC-50-8EU

## 100 PIN PLASTIC QFP (14 × 20)

**NOTE**

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

P100GF-65-3BA1-2

| ITEM | MILLIMETERS                            | INCHES                                    |
|------|----------------------------------------|-------------------------------------------|
| A    | 23.6±0.4                               | 0.929±0.016                               |
| B    | 20.0±0.2                               | 0.795 <sup>+0.009</sup> <sub>-0.008</sub> |
| C    | 14.0±0.2                               | 0.551 <sup>+0.009</sup> <sub>-0.008</sub> |
| D    | 17.6±0.4                               | 0.693±0.016                               |
| F    | 0.8                                    | 0.031                                     |
| G    | 0.6                                    | 0.024                                     |
| H    | 0.30±0.10                              | 0.012 <sup>+0.004</sup> <sub>-0.005</sub> |
| I    | 0.15                                   | 0.006                                     |
| J    | 0.65 (T.P.)                            | 0.026 (T.P.)                              |
| K    | 1.8±0.2                                | 0.071 <sup>+0.008</sup> <sub>-0.009</sub> |
| L    | 0.8±0.2                                | 0.031 <sup>+0.009</sup> <sub>-0.008</sub> |
| M    | 0.15 <sup>+0.10</sup> <sub>-0.05</sub> | 0.006 <sup>+0.004</sup> <sub>-0.003</sub> |
| N    | 0.10                                   | 0.004                                     |
| P    | 2.7                                    | 0.106                                     |
| Q    | 0.1±0.1                                | 0.004±0.004                               |
| S    | 3.0 MAX.                               | 0.119 MAX.                                |

**Remark** Dimensions and materials of ES products are the same as those of the mass production product.

## 8. RECOMMENDED SOLDERING CONDITIONS

The μPD78P064B should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact our sales personnel.

**Table 8-1. Surface Mounting Type Soldering Conditions**

(1) μPD78P064BGC-7EA: 100-pin plastic QFP (fine pitch) (14 × 14 mm)

★ μPD78P064BGC-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14 mm)

| Soldering Method | Soldering Conditions                                                                                                                                                                                                                                                                                                                                                                  | Recommended Soldering Symbols |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------|
| Infrared reflow  | Package peak temperature: 235 °C, Duration: 30 sec. max. (at 210 °C or above),<br>Number of times: Twice max., Time limit: 7 days <sup>Note</sup> (thereafter 10 hours prebaking required at 125 °C)<br><Precaution><br>Products cannot be baked while packed in anything other than in a heat resistant tray (i.e. they cannot be baked in a magazine, taping, or heat-labile tray). | IR35-107-2                    |
| VPS              | Package peak temperature: 235 °C, Duration: 30 sec. max. (at 210 °C or above),<br>Number of times: Twice max., Time limit: 7 days <sup>Note</sup> (thereafter 10 hours prebaking required at 125 °C)<br><Precaution><br>Products cannot be baked while packed in anything other than in a heat resistant tray (i.e. they cannot be baked in a magazine, taping, or heat-labile tray). | VP15-107-2                    |
| Partial heating  | Pin temperature: 300 °C max., Duration: 3 sec. max. (per device side)                                                                                                                                                                                                                                                                                                                 | —                             |

**Note** For the storage period after dry-pack decapsulation, storage conditions are max. 25 °C, 65 % RH.

(2) μPD78P064BGF-3BA: 100-pin plastic QFP (14 × 20 mm)

| Soldering Method | Soldering Conditions                                                                                                                                      | Recommended Soldering Symbols |
|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------|
| Infrared reflow  | Package peak temperature: 235 °C, Duration: 30 sec. max. (at 210 °C or above),<br>Number of times: Three times max.                                       | IR35-00-3                     |
| VPS              | Package peak temperature: 215 °C, Duration: 40 sec. (at 200 °C or above),<br>Number of times: Three times max.                                            | VP15-00-3                     |
| Wave soldering   | Solder bath temperature: 260 °C max., Duration: 10 sec. max., Number of times:<br>Once, Preheating temperature: 120 °C max. (Package surface temperature) | WS60-00-1                     |
| Partial heating  | Pin temperature: 300 °C max., Duration: 3 sec. max. (per device side)                                                                                     | —                             |

**Caution** Use of more than one soldering method should be avoided (except in the case of partial heating).

## APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using μPD78P064B.

### Language Processing Software

|                                      |                                                    |
|--------------------------------------|----------------------------------------------------|
| RA78K/0 <sup>Note 1, 2, 3, 4</sup>   | 78K/0 series common assembler package              |
| CC78K/0 <sup>Note 1, 2, 3, 4</sup>   | 78K/0 series common C compiler package             |
| DF78064 <sup>Note 1, 2, 3, 4</sup>   | μPD78064 subseries common device file              |
| CC78K/0-L <sup>Note 1, 2, 3, 4</sup> | 78K/0 series common C compiler library source file |

### PROM Writing Tools

|                                            |                                          |
|--------------------------------------------|------------------------------------------|
| PG-1500                                    | PROM programmer                          |
| PA-78P064GC                                | Programmer adapters connected to PG-1500 |
| PA-78P064GF                                |                                          |
| PA-PG-1500 controller <sup>Note 1, 2</sup> | PG-1500 control program                  |

### Debugging Tools

|                                          |                                                                                                                                                                                                                         |
|------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IE-78000-R                               | 78K/0 series common in-circuit emulators                                                                                                                                                                                |
| IE-78000-R-A                             | 78K/0 series common in-circuit emulators (for integrated debugger)                                                                                                                                                      |
| IE-78000-R-BK                            | 78K/0 series common break board                                                                                                                                                                                         |
| ★ IE-780308-R-EM                         | μPD780308 subseries common evaluation emulation boards                                                                                                                                                                  |
| EP-78064GC-R                             | μPD78064 subseries common emulation probes                                                                                                                                                                              |
| EP-78064GF-R                             |                                                                                                                                                                                                                         |
| ★ TGC-100SDW                             | Adapter to be mounted on a target system board made for 100-pin plastic QFP (GC-7EA, GC-8EU type)<br>A product of Tokyo Eletech Corp. (Tokyo 03-5295-1661). When purchasing this product, consult your NEC distributor. |
| EV-9200GF-100                            | Socket to be mounted on a target system board made for 100-pin plastic QFP (GF-3BA type)                                                                                                                                |
| SM78K0 <sup>Note 5, 6, 7</sup>           | 78K/0 series common system simulators                                                                                                                                                                                   |
| ID78K0 <sup>Note 4, 5, 6, 7</sup>        | IE-78000-R-A integrated debuggers                                                                                                                                                                                       |
| SD78K/0 <sup>Note 1, 2</sup>             | IE-78000-R screen debuggers                                                                                                                                                                                             |
| DF78064 <sup>Note 1, 2, 4, 5, 6, 7</sup> | μPD78064 subseries common device file                                                                                                                                                                                   |

### Real-Time OS

|                                    |                           |
|------------------------------------|---------------------------|
| RX78K/0 <sup>Note 1, 2, 3, 4</sup> | 78K/0 series real-time OS |
| MX78K/0 <sup>Note 1, 2, 3, 4</sup> | 78K/0 series OS           |



### Fuzzy Inference Development Support System

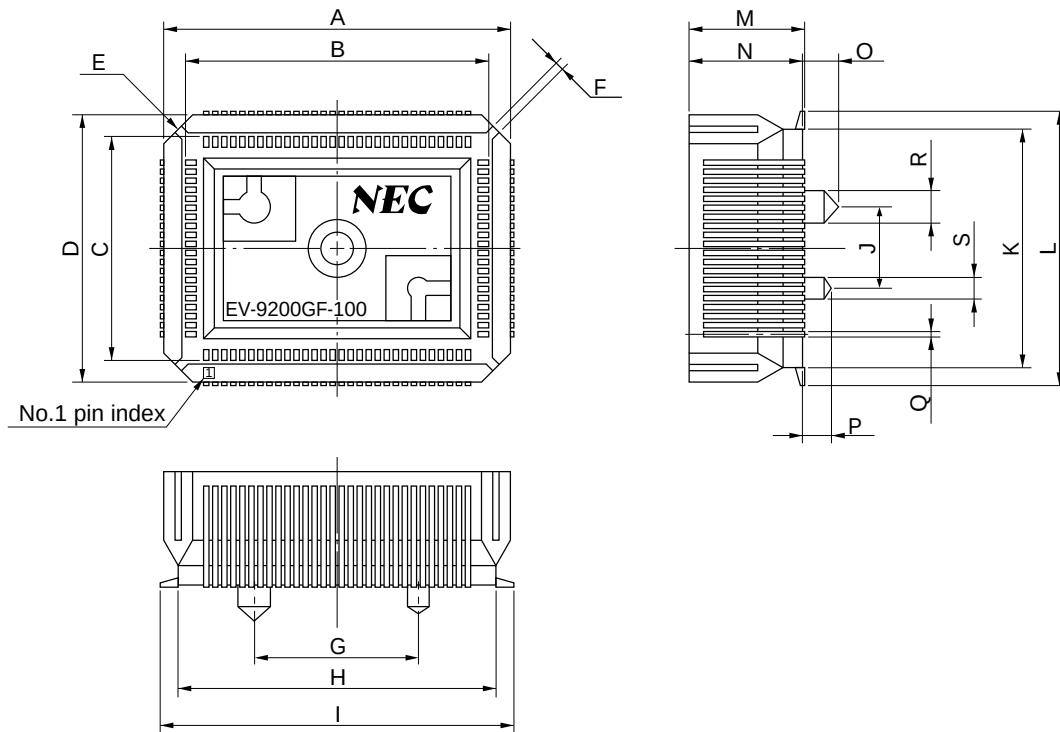
|                                                     |                                    |
|-----------------------------------------------------|------------------------------------|
| FE9000 <sup>Note 1</sup> , FE9200 <sup>Note 6</sup> | Fuzzy knowledge data creation tool |
| FT9080 <sup>Note 1</sup> , FT9085 <sup>Note 2</sup> | Translator                         |
| FI78K/II <sup>Note 1, 2</sup>                       | Fuzzy inference module             |
| FD78K/II <sup>Note 1, 2</sup>                       | Fussy inference debugger           |

- Notes**
1. PC-9800 series (MS-DOS™) based
  2. IBM PC/AT™ and compatible machines (PC DOS™/IBM DOS™/MS-DOS) based
  3. HP9000 series 300™ (HP-UX™) based
  4. HP9000 series 700™ (HP-UX) based, SPARCstation™ (SunOS™) based, EWS4800 series (EWS-UX/V) based
  5. PC-9800 series (MS-DOS + Windows™) based
  6. IBM PC/AT and compatible machines (PC DOS/IBM DOS/MS-DOS + Windows) based
  7. NEWS™ (NEWS-OS™) based

- Remarks**
1. For third party development tools, refer to **78K/0 Series Selection Guide (U11126E)**.
  2. RA78K/0, CC78K/0, SM78K/0, ID78K/0, SD78K/0, and RX78K/0 are used in combination with DF78064.

CONVERSION SOCKET (EV-9200GF-100) PACKAGE DRAWINGS AND  
RECOMMENDED BOARD MOUNTING PATTERN

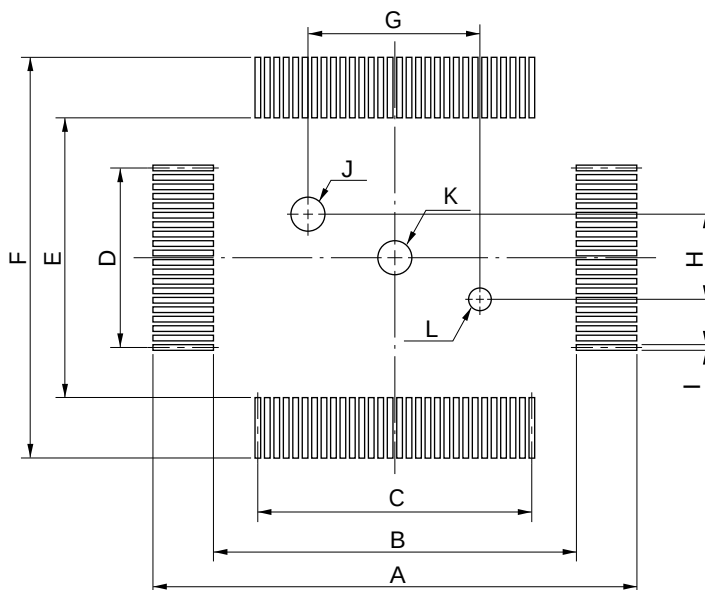
Figure A-1. EV-9200GF-100 Package Drawing



EV-9200GF-100-G0

| ITEM | MILLIMETERS | INCHES    |
|------|-------------|-----------|
| A    | 24.6        | 0.969     |
| B    | 21          | 0.827     |
| C    | 15          | 0.591     |
| D    | 18.6        | 0.732     |
| E    | 4-C 2       | 4-C 0.079 |
| F    | 0.8         | 0.031     |
| G    | 12.0        | 0.472     |
| H    | 22.6        | 0.89      |
| I    | 25.3        | 0.996     |
| J    | 6.0         | 0.236     |
| K    | 16.6        | 0.654     |
| L    | 19.3        | 0.76      |
| M    | 8.2         | 0.323     |
| N    | 8.0         | 0.315     |
| O    | 2.5         | 0.098     |
| P    | 2.0         | 0.079     |
| Q    | 0.35        | 0.014     |
| R    | φ2.3        | φ0.091    |
| S    | φ1.5        | φ0.059    |

Figure A-2. EV-9200GF-100 Board Mounting Pattern



EV-9200GF-100-P0

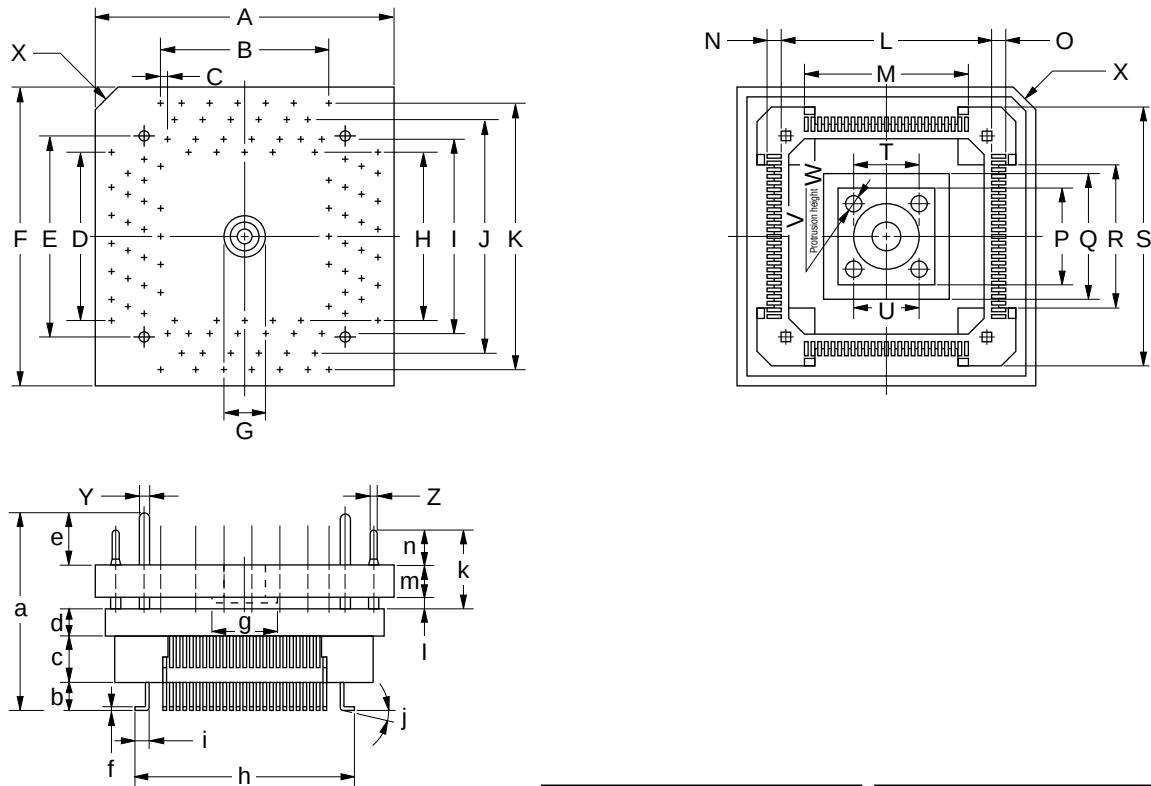
| ITEM | MILLIMETERS                                | INCHES                                                           |
|------|--------------------------------------------|------------------------------------------------------------------|
| A    | 26.3                                       | 1.035                                                            |
| B    | 21.6                                       | 0.85                                                             |
| C    | $0.65 \pm 0.02 \times 29 = 18.85 \pm 0.05$ | $0.026^{+0.001}_{-0.002} \times 1.142 = 0.742^{+0.002}_{-0.002}$ |
| D    | $0.65 \pm 0.02 \times 19 = 12.35 \pm 0.05$ | $0.026^{+0.001}_{-0.002} \times 0.748 = 0.486^{+0.003}_{-0.002}$ |
| E    | 15.6                                       | 0.614                                                            |
| F    | 20.3                                       | 0.799                                                            |
| G    | $12 \pm 0.05$                              | $0.472^{+0.003}_{-0.002}$                                        |
| H    | $6 \pm 0.05$                               | $0.236^{+0.003}_{-0.002}$                                        |
| I    | $0.35 \pm 0.02$                            | $0.014^{+0.001}_{-0.001}$                                        |
| J    | $\phi 2.36 \pm 0.03$                       | $\phi 0.093^{+0.001}_{-0.002}$                                   |
| K    | $\phi 2.3$                                 | $\phi 0.091$                                                     |
| L    | $\phi 1.57 \pm 0.03$                       | $\phi 0.062^{+0.001}_{-0.002}$                                   |

**Caution** Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

## ★ CONVERSION ADAPTER (TGC-100SDW) PACKAGE DRAWINGS

Figure A-3. TGC-100SDW Package Drawing

Reference diagram: TGC-100SDW  
Package dimension (unit: mm)



| ITEM | MILLIMETERS | INCHES            | ITEM           | MILLIMETERS | INCHES       |
|------|-------------|-------------------|----------------|-------------|--------------|
| A    | 21.55       | 0.848             | a              | 14.45       | 0.569        |
| B    | 0.5x24=12   | 0.020x0.945=0.472 | b              | 1.85±0.25   | 0.073±0.010  |
| C    | 0.5         | 0.020             | c              | 3.5         | 0.138        |
| D    | 0.5x24=12   | 0.020x0.945=0.472 | d              | 2.0         | 0.079        |
| E    | 15.0        | 0.591             | e              | 3.9         | 0.154        |
| F    | 21.55       | 0.848             | f              | 0.25        | 0.010        |
| G    | φ3.55       | φ0.140            | g              | φ4.5        | φ0.177       |
| H    | 10.9        | 0.429             | h              | 16.0        | 0.630        |
| I    | 13.3        | 0.524             | i              | 1.125±0.3   | 0.044±0.012  |
| J    | 15.7        | 0.618             | j              | 0~5°        | 0.000~0.197° |
| K    | 18.1        | 0.713             | k              | 5.9         | 0.232        |
| L    | 13.75       | 0.541             | l              | 0.8         | 0.031        |
| M    | 0.5x24=12.0 | 0.020x0.945=0.472 | m              | 2.4         | 0.094        |
| N    | 1.125±0.3   | 0.044±0.012       | n              | 2.7         | 0.106        |
| O    | 1.125±0.2   | 0.044±0.008       | TGC-100SDW-G0E |             |              |
| P    | 7.5         | 0.295             |                |             |              |
| Q    | 10.0        | 0.394             |                |             |              |
| R    | 11.3        | 0.445             |                |             |              |
| S    | 18.1        | 0.713             |                |             |              |
| T    | φ5.0        | φ0.197            |                |             |              |
| U    | 5.0         | 0.197             |                |             |              |
| V    | 4-φ1.3      | 4-φ0.051          |                |             |              |
| W    | 1.8         | 0.071             |                |             |              |
| X    | C 2.0       | C 0.079           |                |             |              |
| Y    | φ0.9        | φ0.035            |                |             |              |
| Z    | φ0.3        | φ0.012            |                |             |              |

**Remark** Manufactured by Tokyo Eletech Corp.

## APPENDIX B. RELATED DOCUMENTS

## Device Related Documents

| Document Name                                       | Document No. |               |
|-----------------------------------------------------|--------------|---------------|
|                                                     | Japanese     | English       |
| μPD78064B Subseries User's Manual                   | U10785J      | U10785E       |
| μPD78064B Data Sheet                                | U11590J      | U11590E       |
| μPD78P064B Data Sheet                               | U11598J      | This document |
| 78K/0 Series User's Manual (Instruction)            | U12326J      | U12326E       |
| 78K/0 Series Instruction List                       | U10903J      | —             |
| 78K/0 Series Instruction Set                        | U10904J      | —             |
| μPD78064B Subseries Special Function Register Table | Planned      | —             |

## Development Tool Related Documents (User's Manual) (1/2)

| Document Name                                    |                              | Document No. |          |
|--------------------------------------------------|------------------------------|--------------|----------|
|                                                  |                              | Japanese     | English  |
| RA78K Series Assembler Package                   | Operation                    | EEU-809      | EEU-1399 |
|                                                  | Language                     | EEU-815      | EEU-1404 |
| RA78K Series Structured Assembler Preprocessor   |                              | EEU-817      | EEU-1402 |
| ★ RA78K0 Assembler Package                       | Operation                    | U11802J      | U11802E  |
|                                                  | Assembly language            | U11801J      | U11801E  |
|                                                  | Structured assembly language | U11789J      | U11789E  |
| CC78K Series C Compiler                          | Operation                    | EEU-656      | EEU-1280 |
|                                                  | Language                     | EEU-655      | EEU-1284 |
| ★ CC78K0 C Compiler                              | Operation                    | U11517J      | U11517E  |
|                                                  | Language                     | U11518J      | U11518E  |
| CC78K/0 C Compiler Application Note              | Programming know-how         | EEA-618      | EEA-1208 |
| CC78K Series Library Source File                 |                              | U12322J      | —        |
| PG-1500 PROM Programmer                          |                              | U11940J      | U11940E  |
| PG-1500 Controller PC-9800 Series (MS-DOS) Based |                              | EEU-704      | EEU-1291 |
| PG-1500 Controller IBM PC Series (PC DOS) Based  |                              | EEU-5008     | U10540E  |
| IE-78000-R                                       |                              | U11376J      | U11376E  |
| IE-78000-R-A                                     |                              | U10057J      | U10057E  |
| IE-78000-R-BK                                    |                              | EEU-867      | EEU-1427 |
| ★ IE-780308-R-EM                                 |                              | U11362J      | U11362E  |
| EP-78064                                         |                              | EEU-934      | EEU-1469 |

## Development Tool Related Documents (User's Manual) (2/2)

| Document Name                              |                                                       | Document No. |          |
|--------------------------------------------|-------------------------------------------------------|--------------|----------|
|                                            |                                                       | Japanese     | English  |
| SM78K0 System Simulator Windows Based      | Reference                                             | EEU-5002     | U10181E  |
| SM78K Series System Simulator              | External components user open interface specification | U10092J      | U10092E  |
| ID78K0 Integrated Debugger EWS Based       | Reference                                             | U11151J      | —        |
| ★ ID78K0 Integrated Debugger PC Based      | Reference                                             | U11539J      | U11539E  |
| ★ ID78K0 Integrated Debugger Windows Based | Guide                                                 | U11649J      | U11649E  |
| SD78K/0 Screen Debugger                    | Introduction                                          | EEU-852      | U10539E  |
| PC-9800 Series (MS-DOS) Based              | Reference                                             | U10952J      | —        |
| SD78K/0 Screen Debugger                    | Introduction                                          | EEU-5024     | EEU-1414 |
| IBM PC/AT (PC DOS) Based                   | Reference                                             | U11279J      | U11279E  |

**Caution** The above related documents are subject to change without notice. For design purpose, etc., be sure to use the latest documents.

## Embedded Software Related Documents (User's Manual)

| Document Name                                                                    |              | Document No. |          |
|----------------------------------------------------------------------------------|--------------|--------------|----------|
|                                                                                  |              | Japanese     | English  |
| 78K/0 Series Real-Time OS                                                        | Basic        | U11537J      | —        |
|                                                                                  | Installation | U11536J      | —        |
| 78K/0 Series OS MX78K0                                                           | Basic        | U12257J      | —        |
| Fuzzy Knowledge Data Creation Tool                                               |              | EEU-829      | EEU-1438 |
| 78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System Translator |              | EEU-862      | EEU-1444 |
| 78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module   |              | EEU-858      | EEU-1441 |
| 78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger |              | EEU-921      | EEU-1458 |

## Other Related Documents

| Document Name                                                         |  | Document No. |          |
|-----------------------------------------------------------------------|--|--------------|----------|
|                                                                       |  | Japanese     | English  |
| IC Package Manual                                                     |  | C10943X      |          |
| Semiconductor Device Mounting Technology Manual                       |  | C10535J      | C10535E  |
| Quality Grades on Semiconductor Devices                               |  | C11531J      | C11531E  |
| NEC Semiconductor Device Reliability and Quality Control              |  | C10983J      | C10983E  |
| Electrostatic Discharge (ESD) Test                                    |  | MEM-539      | —        |
| Semiconductor Devices Quality Guarantee Guide                         |  | C11893J      | MEI-1202 |
| Microcomputer-Related Product Guide (Products by Other Manufacturers) |  | U11416J      | —        |

**Caution** The above related documents are subject to change without notice. For design purpose, etc., be sure to use the latest documents.

[MEMO]

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note:** Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note:** No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

**Note:** Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.



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- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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