Integrated Device Technology, Inc.

64K x 9/128K x 9 CMOS PARALLEL IN-OUT FIFO MODULE

PRELIMINARY
IDT7M208
IDT7M209

FEATURES:

- First-In/First-Out memory module
- 64K x 9 (IDT7M208) or 128K x 9 (IDT7M209)
- High speed: 20ns (max.) access time
- Asynchronous and simultaneous read and write
- Fully expandable: depth and/or width
- MASTER/SLAVE multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and Full warning-flags
- Single 5V (±10%) power supply

DESCRIPTION:

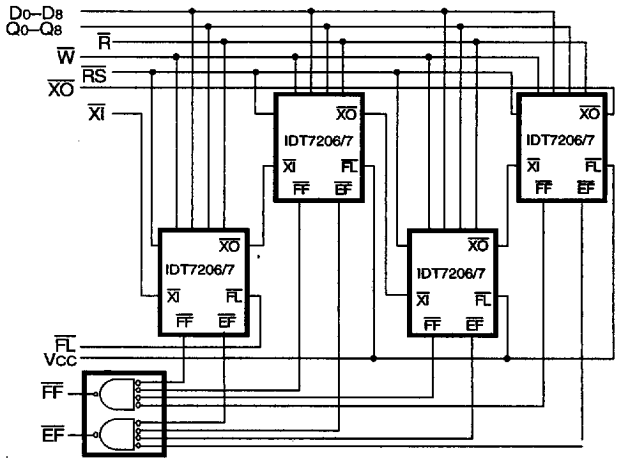
IDT7M208 and IDT7M209 are FIFO memory modules constructed on a multi-layered ceramic substrate using four IDT7206 (16K x 9) or IDT7207 (32K x 9) FIFOs in leadless chip carriers. Extremely high speeds are achieved in this fashion due to the use of IDT7206/7s fabricated in IDT's high performance CMOS technology. These devices utilize an algorithm that loads and empties data on a first-in/first-out basis. The device uses Full and Empty flags as warnings for data overflow and underflow conditions and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The devices have a read/write cycle time of 20ns (min.) for commercial and 30ns (min.) for military temperature ranges.

The devices utilize a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

IDT's Military FIFO modules have semiconductor components manufactued in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

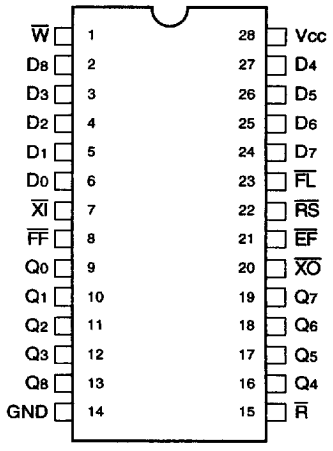
FUNCTIONAL BLOCK DIAGRAM



DUAL 4-INPUT OR GATE

3162 drw 01

PIN CONFIGURATION



DIP
TOP VIEW

3162 drw 02

PIN NAMES

$\overline{W}$ = WRITE	$\overline{FL}$ = FIRST LOAD	$\overline{XI}$ = EXPANSION IN	$\overline{EF}$ = EMPTY FLAG
$\overline{R}$ = READ	D = DATAIN	$\overline{XO}$ = EXPANSION OUT	V_{CC} = 5V
$\overline{RS}$ = RESET	Q = DATAOUT	$\overline{FF}$ = FULL FLAG	GND = GROUND

3162 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE: 3162 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Condition	Max.	Unit
CIN	Input Capacitance	VIN = 0V	50	pF
COUT	Output Capacitance	VOUT = 0V	50	pF

NOTE: 3162 tbl 03

1. This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH(1)	Input High Voltage Commercial	2.0	—	—	V
VIH(1)	Input High Voltage Military	2.2	—	—	V
VIL(2)	Input Low Voltage Commercial and Military	—	—	0.8	V

NOTES: 3162 tbl 04

1. V_{IH} = 2.6V for $\overline{XI}$ input (commercial)
   V_{IH} = 2.8V for $\overline{XI}$ input (military)
2. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; and –55°C to +125°C)

Symbol	Parameter	Commercial Min.	Commercial Max.	Military Min.	Military Max.	Unit
ILI(1)	Input Leakage Current (Any Input)	–5	5	-40	40	µA
ILO(2)	Output Leakage Current	–40	40	-40	40	µA
VOH	Output Logic "1" Voltage IOUT = –2mA	2.4	—	2.4	—	V
VOL	Output Logic "0" Voltage IOUT = 8mA	—	0.4	—	0.4	V
ICC1(3)	VCC Power Supply Current	—	560	—	720	mA
ICC2(3)	Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = VIH)	—	60	—	80	mA
ICC3(3)	Power Down Current (All Input = VCC – 0.2V)	—	32	—	48	mA

NOTES: 3162 tbl 05

1. Measurements with 0.4 ≤ VIN ≤ VCC.
2. R ≥ VIH, 0.4 ≤ VOUT ≤ VCC.
3. ICC measurements are made with outputs open.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1 and 2

3162 tbl 06

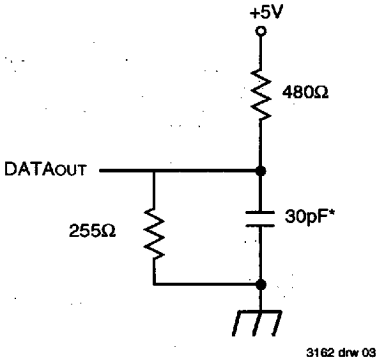


Figure 1. Output Load
*** Includes scope and jig capacitances.**

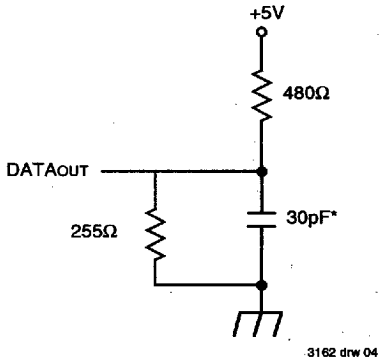


Figure 2. Output Load
(for tRLZ, tWLZ, and tRHZ)

* Includes scope and jig capacitances.

AC ELECTRICAL CHARACTERISTICS

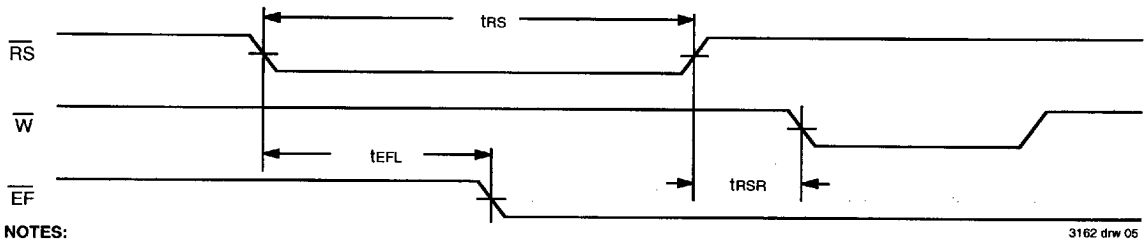
(V_{CC} = 5.0V±10%, T_A = 0°C to +70°C and –55°C to +125°C)

Symbol	Parameter	–20 (Com'l Only)		–25 (Com'l Only)		–30 (Mil Only)		–35 (Mil Only)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_S	Shift Frequency	—	33.3	—	28.6	—	25	—	22.5	MHz
t_{RC}	Read Cycle Time	30	—	35	—	40	—	45	—	ns
t_A	Access Time	—	20	—	25	—	30	—	35	ns
t_{RR}	Read Recovery Time	10	—	10	—	10	—	10	—	ns
t_{RPW}(1)	Read Pulse Width	20	—	25	—	30	—	35	—	ns
t_{RLZ}(2)	Read Pulse Low to Data Bus at Low Z	5	—	5	—	5	—	5	—	ns
t_{WLZ}(2)	Write Pulse High to Data Bus at Low Z	5	—	5	—	5	—	10	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	ns
t_{RHZ}(2)	Read Pulse High to Data Bus at High Z	—	16	—	20	—	20	—	20	ns
t_{WC}	Write Cycle Time	30	—	35	—	40	—	45	—	ns
t_{WPW}(1)	Write Pulse Width	20	—	25	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	10	—	10	—	10	—	10	—	ns
t_{DS}	Data Set-up Time	15	—	18	—	18	—	20	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{RSC}	Reset Cycle Time	30	—	35	—	40	—	45	—	ns
t_{RS}(1)	Reset Pulse Width	20	—	25	—	30	—	35	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	10	—	10	—	ns
t_{EFL}	Reset to Emtpy Flag Low	—	30	—	35	—	40	—	45	ns
t_{REF}	Read Low to Emtpy Flag Low	—	23	—	25	—	30	—	35	ns
t_{RFF}	Read High to Full Flag High	—	23	—	25	—	30	—	35	ns
t_{WEF}	Write High to Empty Flag High	—	23	—	25	—	30	—	35	ns
t_{WFF}	Write Low to Full Flag Low	—	23	—	25	—	30	—	35	ns

NOTES:
1. Pulse widths less than minimum value are not allowed.
2. Values guaranteed by design, not currently tested.

3162 tbl 06

TIMING WAVEFORM OF RESET CYCLE(1,2)



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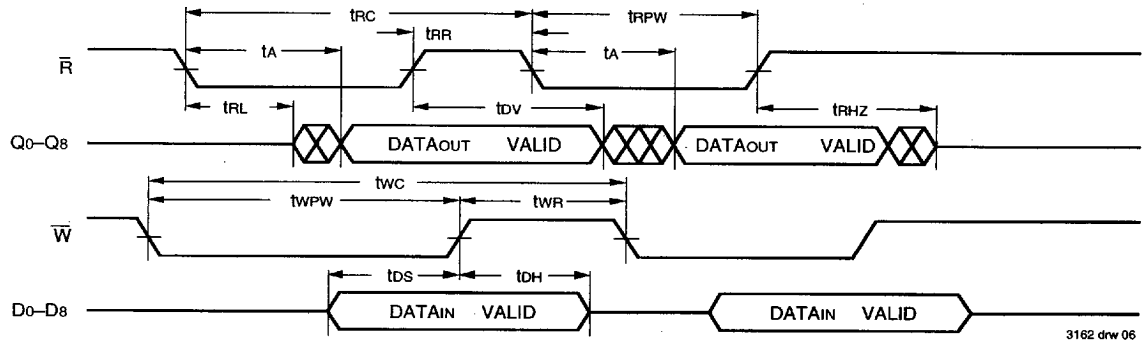
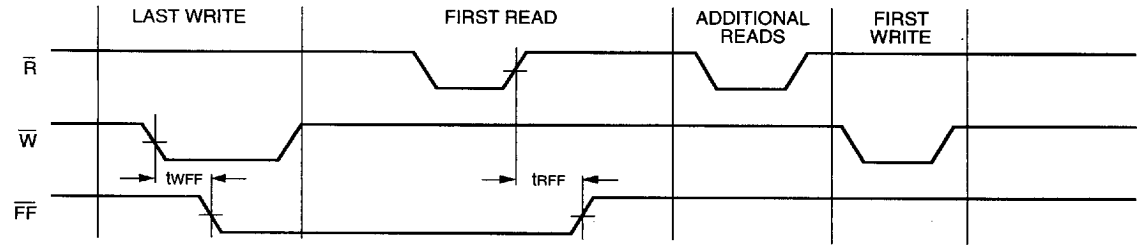
NOTES:
1. $t_{RSC} = t_{RS} + t_{RSR}$
2. $\overline{W}$ and $\overline{R}$ = V_{IH} during RESET.

TIMING WAVEFORM OF ASYNCHRONOUS WRITE AND READ OPERATION



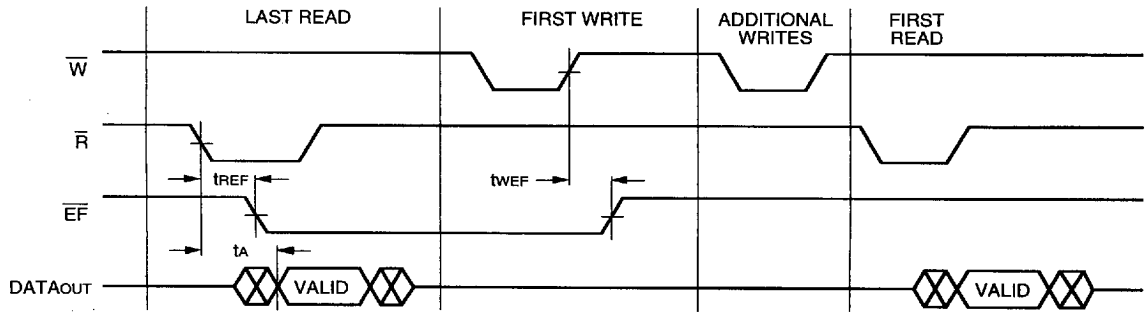
3162 drw 06

TIMING WAVEFORM FOR THE FULL FLAG FROM LAST WRITE TO FIRST READ



3162 drw 07

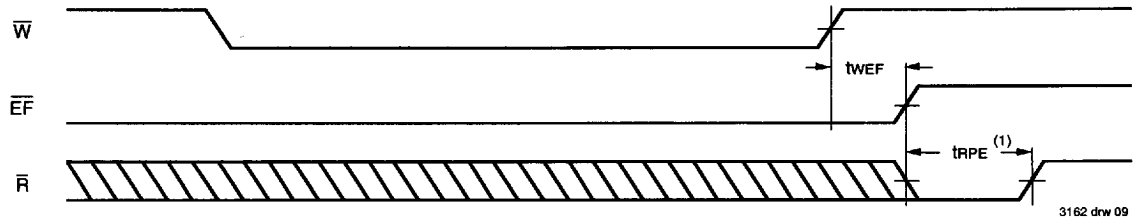
TIMING WAVEFORM FOR THE EMPTY FLAG FROM LAST READ TO FIRST WRITE



3162 drw 08

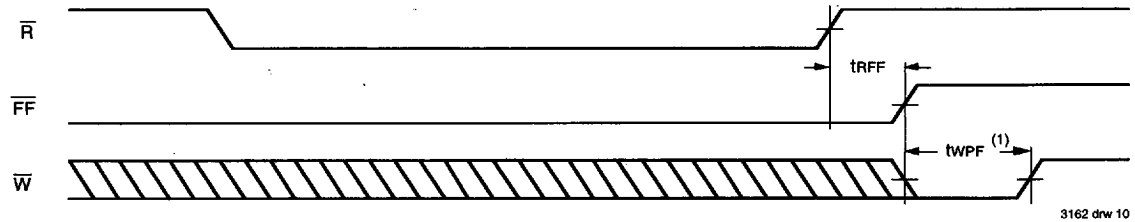
NOTE:
1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM FOR THE EMPTY FLAG CYCLE



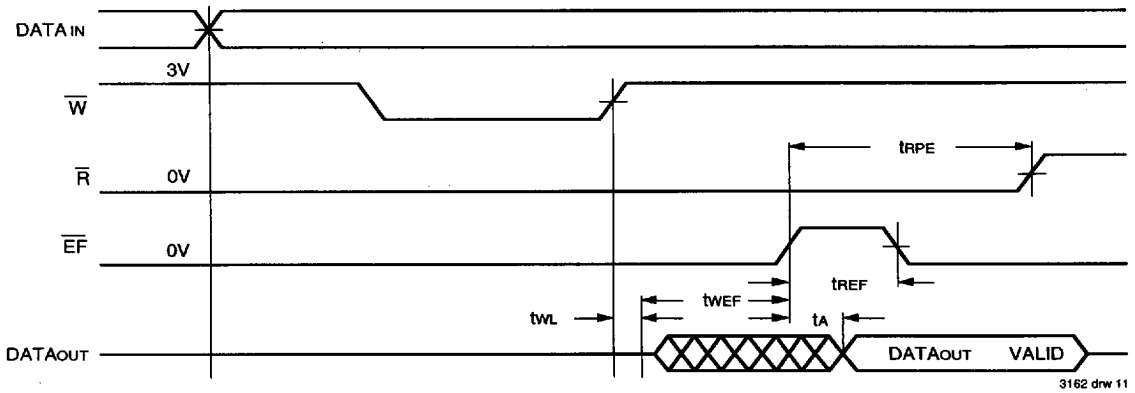
NOTE:
1. t_{RPE} must be ≥ $t_{RPW\ (min)}$. Refer to Technical Note TN-08 for details on this boundary condition.

TIMING WAVEFORM FOR THE FULL FLAG CYCLE

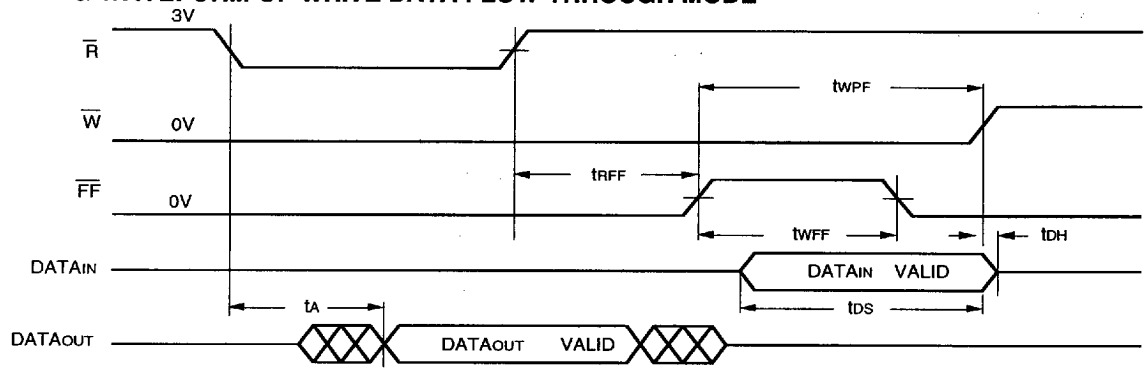


NOTE:
1. t_{WPF} must be ≥ $t_{WPW\ (min)}$. Refer to Technical Note TN-08 for details on this boundary condition.

TIMING WAVEFORM OF READ DATA FLOW-THROUGH MODE



TIMING WAVEFORM OF WRITE DATA FLOW-THROUGH MODE



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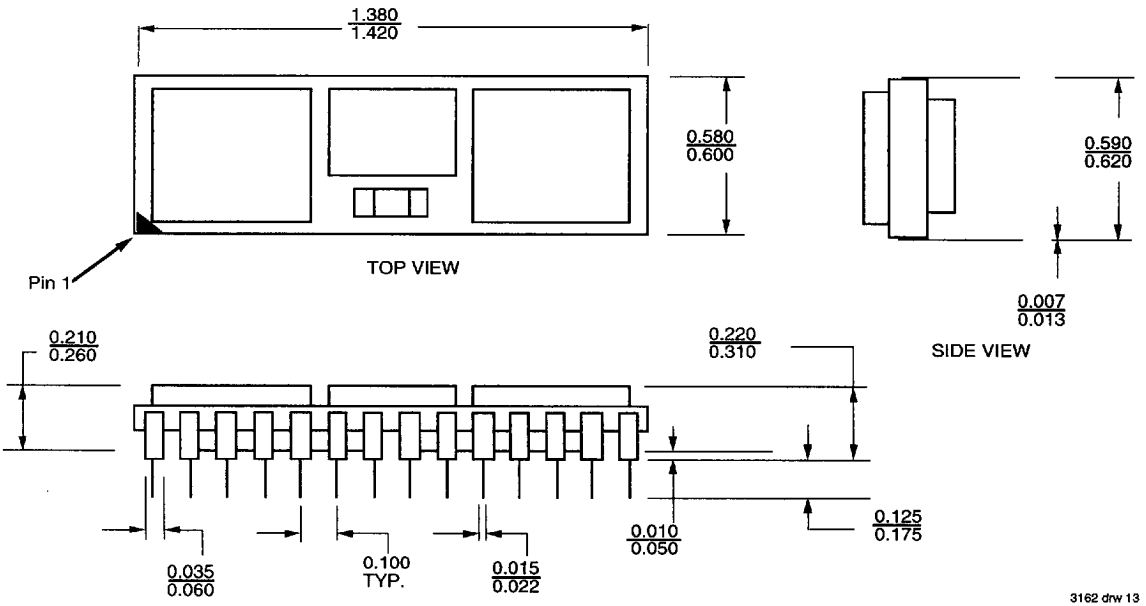
DEPTH/WIDTH EXPANSION & DATA FLOW-THROUGH MODES:

For more details on expanding FIFO modules in depth and/or width, please refer to the IDT7206 or IDT7207 data sheets.

For more details on data flow-through modes (read data fall through and write data fall-through), please refer to the IDT7206 or IDT7207 data sheets.

PACKAGE DIMENSIONS



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ORDERING INFORMATION