CYPRESS SEMICONDUCTOR

CY7C270

Reprogrammable 16K x 16 Processor-Intelligent PROM

Features

- **0.8-micron CMOS for optimum speed/power**
- **High speed (for commercial and military)**
  - **— 25-ns single access time**
  - **— 11-ns burst access time**
- **16-bit-wide words**
- **Input address registered, latched, or transparent**
- **On-chip programmable burst logic**
- **Programmable compatibility with many common microprocessors**
- **Three programmable chip selects**
- **Programmable output enable**
- **44-pin PLCC and 44-pin LCC packages**
- **100% reprogrammable in windowed packages**
- **TTL-compatible I/O**
- **Capable of withstanding greater than 2001V static discharge**

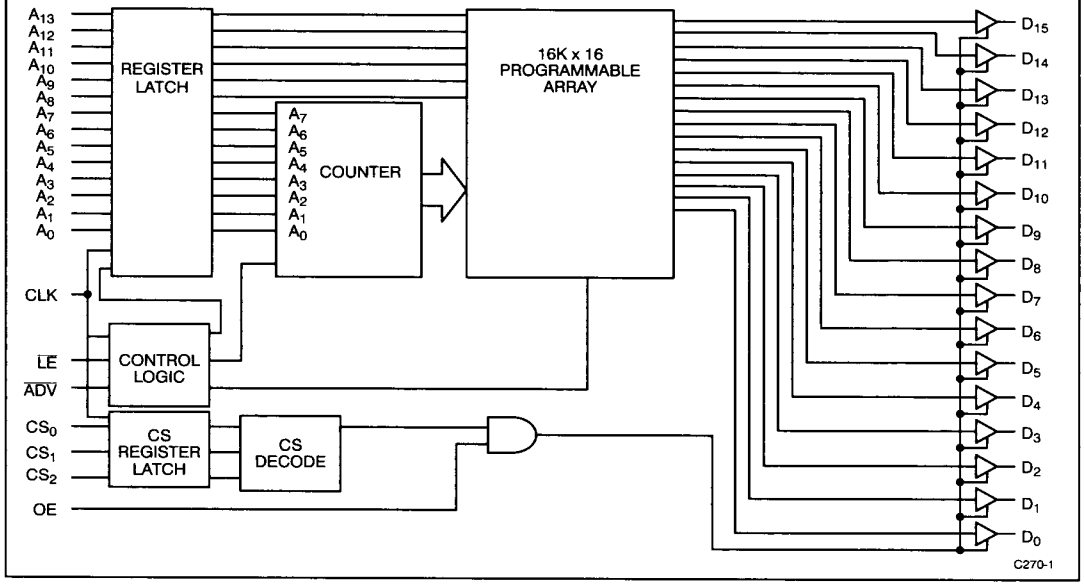
Functional Description

The CY7C270 is a 16K-word by 16-bit PROM designed to support a number of popular microprocessors with little or no "glue" logic. This PROM is packaged in a 44-pin PLCC package and a 44-pin LCC package. The CY7C270 is available in windowed packages for 100% reprogrammability. The memory cells utilize proven EPROM floating-gate technology.

The CY7C270 offers a number of programmable features that allow the user to configure the PROM for use with their chosen microprocessor. The programmable features include a choice between registered and latched modes of operation. The CY7C270 also has an on-board programmable counter for burst reads. The user may select a 2-bit, 4-bit, or 8-bit linear counter, or program the PROM to use the Intel 80486 burst pattern (*Table 2*). A separate control input ($\overline{ADV}$) is used to choose between single reads and bursts. In addition, the burst counter and latch may be bypassed for asynchronous operation to be used with DSP processors.

The CY7C270 allows the user to independently program the polarity of each chip select ($CS_2 - CS_0$). This provides on-chip decoding of up to eight banks of PROM. The polarity of the asynchronous output enable pin (OE) is also programmable.

Logic Block Diagram

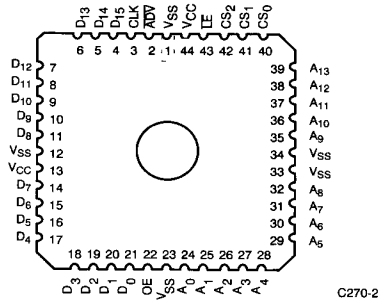


Selection Guide

		CY7C270–15	CY7C270–20	CY7C270–30
Minimum Clock Period (ns)		15	20	30
Maximum Operating Current (mA)	Commercial	175	175	175
	Military	200	200	200

Pin Configuration

LCC/PLCC (Opaque Only)
Top View



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Operating Modes

The CY7C270 can be specifically configured for use with many popular microprocessors. The PROM configuration for some of these processors is detailed in *Table 1*. Note that many of the processors can use either registered or latched mode depending on their speed.

Table 1. Processor-Intelligent PROM Configuration

Processor	Registered/Latched	Burst Counter
SPARC	Registered	—
Intel 486	Latched	Table Logic[1]
80386	Latched	—
Motorola 68040	Latched	2-Bit Counter
Motorola 68030	Latched	2-Bit Counter
Intel 80960KB	Registered	2-Bit Counter
Intel 80960CA	Latched	2-Bit Counter
AMD 29000	Latched	8-Bit Counter
MIPS R3000	Registered	—
MIPS R2000	Registered	—
Motorola 88000	Registered	—

Note:
1. The Intel 486 uses a non-sequential burst. The CY7C270 is equipped with a look-up table (described in *Table 2*) for use with this processor.

Single Read Access in Registered Mode

A read access is initiated in registered mode on the rising edge of CLK if all three chip selects are asserted and $\overline{LE}$ is sampled LOW. The address applied to the input is stored in a register and is delivered to both the PROM core and the counter. The contents of the memory location accessed by the original address are delivered to the outputs. When $\overline{LE}$ is asserted the system ignores the advance enable ($\overline{ADV}$) input.

Single Read Access in Latched Mode

In latched mode, the CY7C270 can take advantage of situations where the address is available well before the rising edge of CLK. A read is initiated when the latch is opened (on the falling edge of $\overline{LE}$). The address is sent directly to the PROM core and to the counter. The contents of the memory location addressed by the original address are delivered to the outputs. The latch is closed when $\overline{LE}$ is deasserted.

Burst Sequence

During a burst, the first read is initiated as a single access read. After the initial read, the $\overline{LE}$ input is held inactive. The advance enable input ($\overline{ADV}$) controls the address sequencing starting with the second read. $\overline{ADV}$ is sampled on the rising edge of the CLK input. If $\overline{ADV}$ is sampled LOW, the address is incremented to the next location. The number of address bits incremented by the counter is programmed by the user. The counter wraps around after reaching the maximum count without affecting other bits in the address.

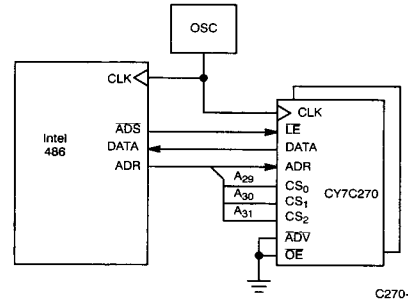
Special burst advancement logic is included in the CY7C270 to support the Intel 80486 burst operation. The 80486 bursts in the non-sequential pattern shown in *Table 2*.

Some processors have the capability to suspend a burst. In order to suspend a burst in the CY7C270 the processor must simply deassert the $\overline{ADV}$ input. When the $\overline{ADV}$ input is reasserted the burst will continue from where it left off. It is not necessary for the processor to send a new address to the PROM.

Table 2. Look-Up Table for Use with Intel 486

First Address		Second Address		Third Address		Fourth Address	
$A_X + 1$	A_X	$A_X + 1$	A_X	$A_X + 1$	A_X	$A_X + 1$	A_X
0	0	0	1	1	0	1	1
0	1	0	0	1	1	1	0
1	0	1	1	0	0	0	1
1	1	1	0	0	1	0	0

Application Example 1



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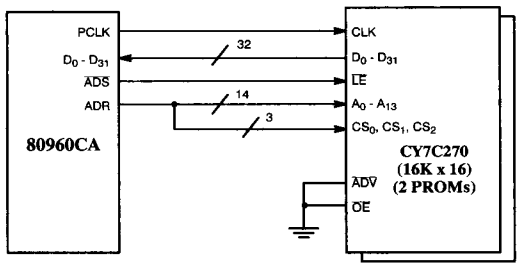
80486 Instruction Memory Using Two CY7C270s

Application Example 2



Intel 80960CA Using Two CY7C270s

Pin Definitions

Signal Name	I/O	Description
$A_{13} - A_0$	I	Address Inputs
CLK	I	Clock
$\overline{LE}$	I	Latch Enable
$\overline{ADV}$	I	Advance Enable
$CS_2 - CS_0$	I	Programmable Chip Selects
OE	I	Programmable Output Enable
$D_{15} - D_0$	O	Data Outputs
V_{CC}	–	Power Supply
V_{SS}	–	Ground

Pin Descriptions

Input Signals

$A_{13} - A_0$ (Address lines). The address inputs are stored in a register at the rising edge of CLK if the device is programmed in registered mode. If the device is programmed in latched mode, the address inputs flow into the PROM while $\overline{LE}$ is active and are captured at the rising edge of $\overline{LE}$. For asynchronous operation, the device should be programmed in the latch mode with $\overline{LE}$ tied LOW.

CLK (Clock line). The clock is used to sample the $\overline{ADV}$ input. In registered mode, the clock is also used to sample $\overline{LE}$, $CS_2 - CS_0$, and the address.

$\overline{LE}$ (Latch Enable). In registered mode, this input is sampled on the rising edge of CLK. If it is active, the address and chip selects are stored in a register. In latched mode, the address and chip selects are latched on the rising edge of this signal.

$\overline{ADV}$ (Advance Enable). This signal is used for burst reads. If $\overline{LE}$ is inactive, $\overline{ADV}$ is sampled on the rising edge of CLK. If $\overline{ADV}$ is LOW, the counter will be incremented and the next address will be delivered to the PROM core. $\overline{ADV}$ should be tied HIGH, and in the programming mode, the burst enable (BE) should be disabled for asynchronous operation.

$CS_2 - CS_0$ (Synchronous Chip Selects). The polarity of each chip select is programmed by the user. The inputs from these pins are stored in a register on the rising edge of CLK in registered mode. In latched mode, the inputs are latched on the rising edge of $\overline{LE}$. All three chip selects must be active in order to select the device.

OE (Asynchronous Output Enable). The polarity of this pin is programmable. The outputs are active when OE is asserted and tri-stated when OE is deasserted.

Output Signals

$D_{15} - D_0$ (Data Outputs). Data from the array location addressed on inputs $A_{13} - A_0$ will appear on these pins. The outputs will be tri-stated if OE is deasserted or if the chip is not selected.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

DC Program Voltage 13.0V

UV Erasure ..... 7258 Wsec/cm^2

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... >2001V

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[2]	– 40°C to +85°C	5V ±10%
Military[3]	– 55°C to +125°C	5V ±10%

Notes:

2. Contact a Cypress representative for industrial temperature range specifications.
3. T_A is the "instant on" case temperature.

Electrical Characteristics[4, 5]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 2.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA (6.0 mA Mil)			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs		− 3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		− 10	+10	μA
V_{CD}	Input Clamp Diode Voltage	Note 4				μA
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{OL} ≤ V_{OUT} ≤ V_{OH}, Output Disabled		− 40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[6]		− 20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0.0 mA	Com'l		175	mA
			Military		200	mA

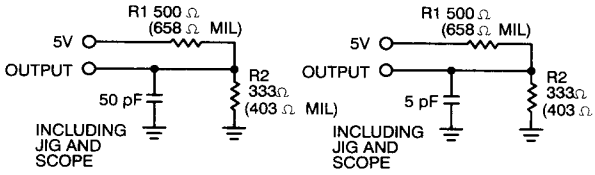
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

4. See Introduction to CMOS PROMs in this Data Book for general information on testing.
5. See the last page of this specification for Group A subgroup testing information.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

AC Test Loads and Waveforms



(a) Normal Load (b) High Z Load

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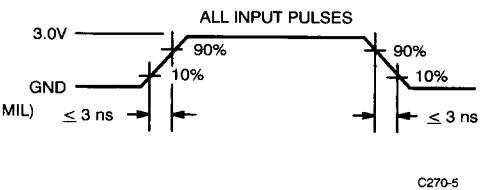

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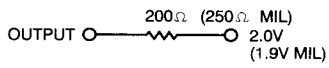
Equivalent to: THÉVENIN EQUIVALENT



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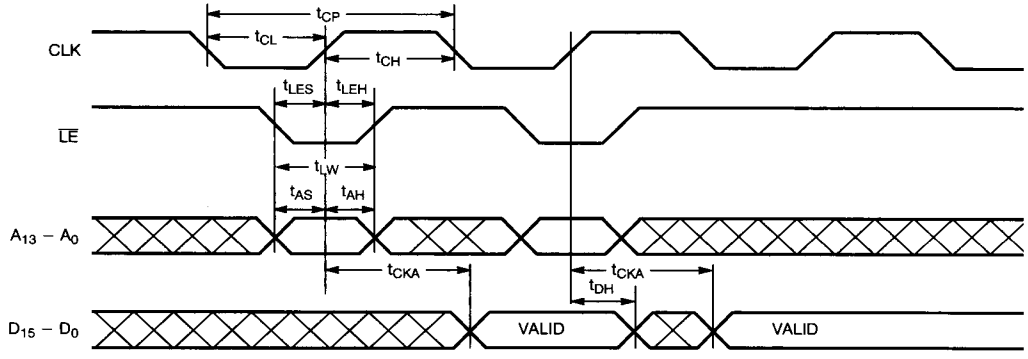
Switching Characteristics Over the Operating Range[5]

Parameter	Description	Commercial and Military						Unit
		CY7C270–15		CY7C270–20		CY7C270–30		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CP}	Clock Period	15		20		30		ns
t_{CH}	Clock HIGH Pulse Width	6		8		13		ns
t_{CL}	Clock LOW Pulse Width	6		8		13		ns
t_{AS}	Address Set-Up to CLK Rise	3		4		4		ns
t_{AH}	Address Hold from CLK Rise	2		3		4		ns
t_{LES}	$\overline{LE}$ Set-Up to CLK Rise	3		4		4		ns
t_{LEH}	$\overline{LE}$ Hold from CLK Rise	2		3		4		ns
t_{LW}	Latch Pulse Width	7		10		12		ns
t_{ADVS}	$\overline{ADV}$ Set-Up to CLK Rise	3		4		4		ns
t_{ADVH}	$\overline{ADV}$ Hold from CLK Rise	2		3		4		ns
t_{ASL}	Address Set-Up to Latch Close	3		4		4		ns
t_{AHL}	Address Hold from Latch Close	2		3		4		ns
t_{DH}	Data Hold	3		3		3		ns
t_{AA}	Address to Data for Single Read		25		28		35	ns
t_{LEA}	$\overline{LE}$ Low to Data Valid for Single Read		25		28		35	ns
t_{CKA}	Clock to Data for Single Read		25		28		35	ns
t_{CKB}	CLK Rise to Data for Burst Read		11		12		15	ns
t_{CSS}	CS Set-Up to CLK Rise	3		4		4		ns
t_{CSH}	CS Hold from CLK Rise	2		3		4		ns
t_{COV}	CLK Rise to Output Valid		11		12		15	ns
t_{COZ}	CLK Rise to High Z Output		11		12		15	ns
t_{CSOV}	CS Asserted to Output Valid		13		15		18	ns
t_{CSOZ}	CS Deasserted to High Z Output		13		15		18	ns
t_{CSSL}	CS Set-Up to Latch Close	3		4		4		ns
t_{CSHL}	CS Hold from Latch Close	2		3		4		ns
t_{LOV}	Latch Open to Output Valid		13		15		18	ns
t_{LOZ}	Latch Open to High Z Output		13		15		18	ns
t_{OEV}	OE Asserted to Output Valid		11		12		15	ns
t_{OEZ}	OE Deasserted to High Z Output		11		12		15	ns

Switching Waveforms

Single Reads – Registered Mode[7, 8]



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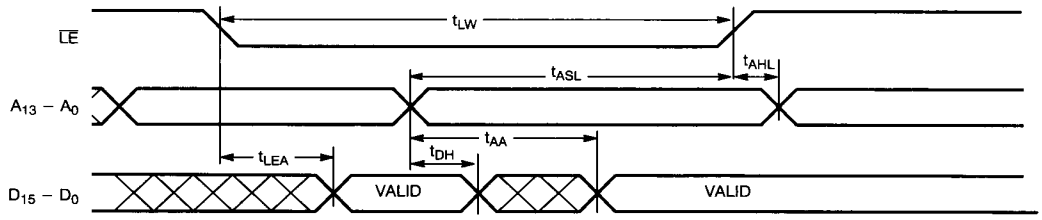
Single Reads – Latched Mode[8]



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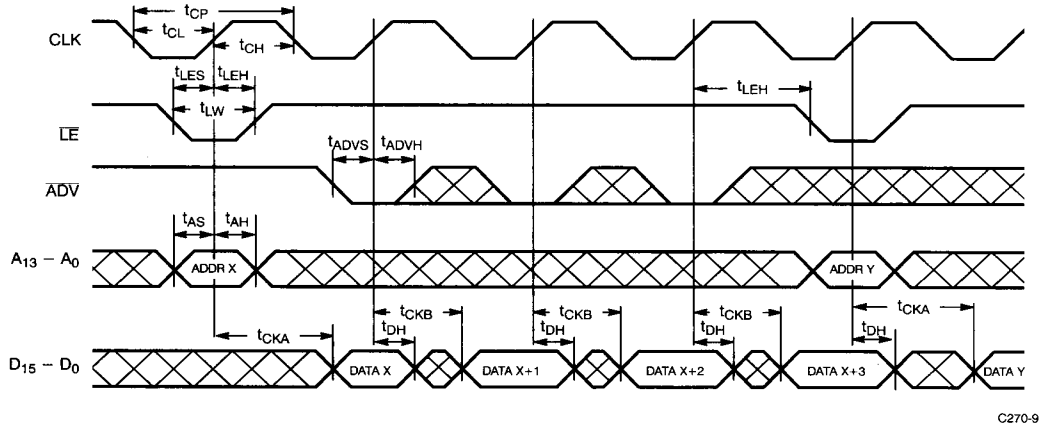
4-Word Burst Followed by Single Read – Registered Mode[8]



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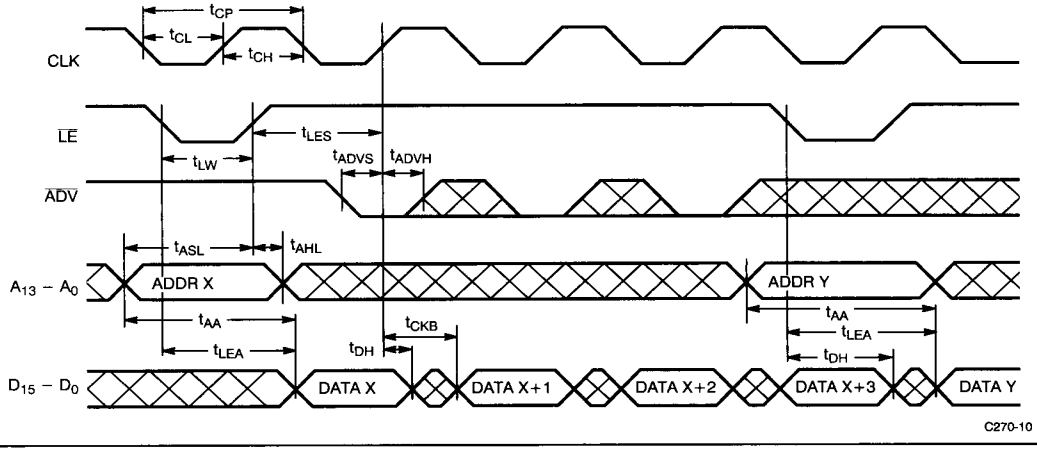
Notes:

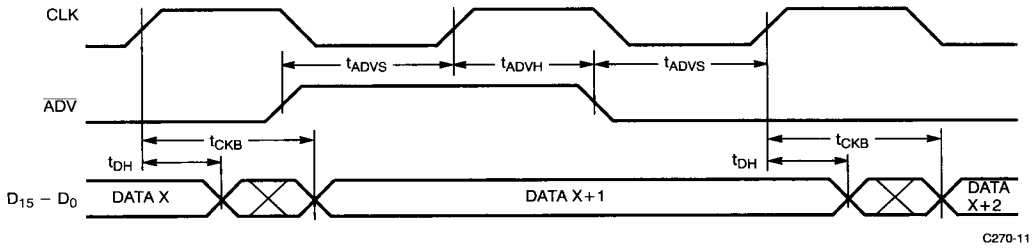
7. $\overline{ADV}$ is assumed HIGH.
8. $CS_2 - CS_0$, OE are assumed active.

Switching Waveforms (continued)

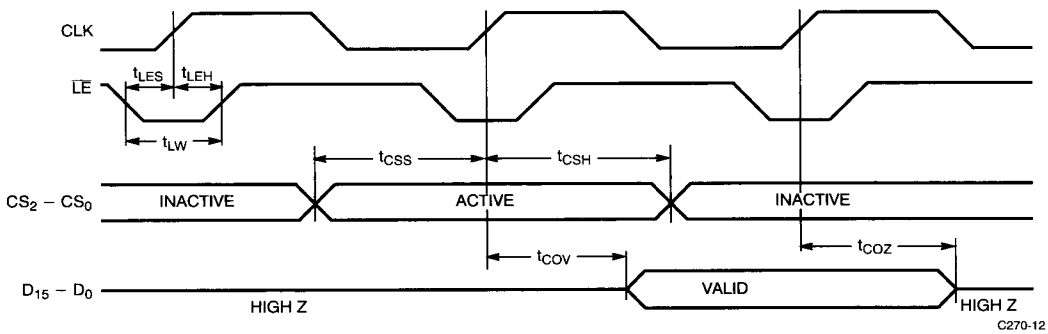
4-Word Burst Followed by Single Read – Latched Mode[8]



Suspended Burst[8, 9]



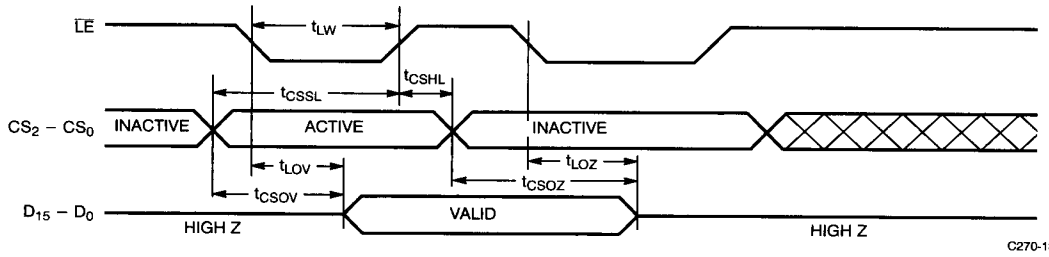
Output Controlled by CS and CLK – Registered Mode[10]



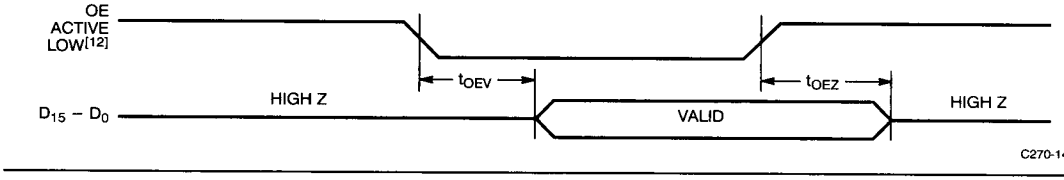
Notes:
9. Burst in progress.
10. OE assumed active.

Switching Waveforms (continued)

Outputs Controlled by CS and $\overline{LE}$ – Latched Mode



Outputs Controlled by OE[11]



Notes:
11. $CS_2 - CS_0$ are assumed active.
12. OE active HIGH is a programmable option.

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the CY7C270. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose for erasure of ultraviolet light is a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 35 minutes. The 7C270 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Architecture Configuration Bits

The CY7C270 is configured by programming the Control Word located at the end of the programmable array (4000H). *Table 3* gives the specific information for configuring the architecture.

To use the CY7C270 as a purely asynchronous PROM, tie the $\overline{ADV}$ signal to V_{CC}, the CLK and $\overline{LE}$ signal to V_{SS}, and program the control word for No Burst and Latched mode of operation ($D_3 = 1$, $D_{15} = 0$).

Table 3. Control Word for Architecture Configuration

Control Option	Control Word		Function
	Bit	Programmed Level	
OE Output Enable	D_0	0 = Default 1 = Programmed	OE Active LOW OE Active HIGH
C_1 C_0 (Counter Configuration)	D_2 D_1	00 = Default 01 = Programmed 10 = Programmed 11 = Programmed	486 2-Bit Counter Linear 2-Bit Counter Linear 4-Bit Counter Linear 8-Bit Counter
R/L Registered/Latched	D_3	0 = Default 1 = Programmed	Registered Mode Latched Mode
CS_0 Chip Select 0	D_{12}	0 = Default 1 = Programmed	CS_0 Active LOW CS_0 Active HIGH
CS_1 Chip Select 1	D_{13}	0 = Default 1 = Programmed	CS_1 Active LOW CS_1 Active HIGH
CS_2 Chip Select 2	D_{14}	0 = Default 1 = Programmed	CS_2 Active LOW CS_2 Active HIGH
BE (Burst Enable)	D_{15}	0 = Default 1 = Programmed	No Burst Burst (follow C_1 C_0)

Bit Map

Programmer Address (Hex)	RAM Data
0000	Data
.	.
.	.
.	.
3FFF	Data
4000	Control Word

Control Word (4000H – default state is 00H)

D_{15} D_0

BE CS_2 CS_1 CS_0 X X X X X X X X R/L C_1 C_0 OE

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 4. Program Mode Table

Mode	V_{PP}	$\overline{PGM}$	$\overline{VFY}$	$D_0 - D_{15}$
Program Inhibit	V_{PP}	V_{IHP}	V_{IHP}	High Z
Program Enable	V_{PP}	V_{ILP}	V_{IHP}	Data
Program Verify	V_{PP}	V_{IHP}	V_{ILP}	Data

Table 5. Configuration Mode Table

Mode	V_{PP}	$\overline{PGM}$	$\overline{VFY}$	A_2	$D_0 - D_{15}$
Program Inhibit	V_{PP}	V_{IHP}	V_{IHP}	V_{PP}	High Z
Program Control Word	V_{PP}	V_{ILP}	V_{IHP}	V_{PP}	Control Word
Verify Control Word	V_{PP}	V_{IHP}	V_{ILP}	V_{PP}	Control Word

Table 6. Signature Mode Table

Signature Mode	A_0	A_9	$D_0 - D_{15}$
Cypress Code	V_{ILP}	V_{PP}	0034H
Device Code	V_{IHP}	V_{PP}	0013H

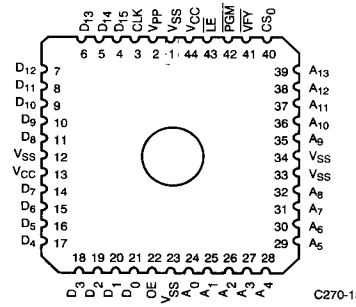
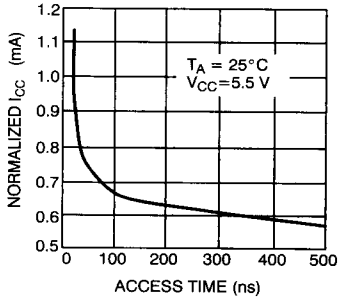


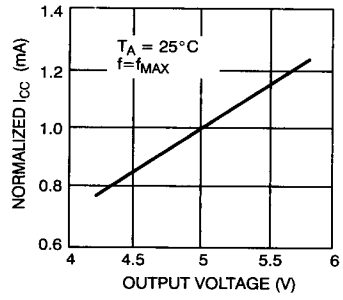
Figure 1. Programming Pinout

Typical DC and AC Characteristics

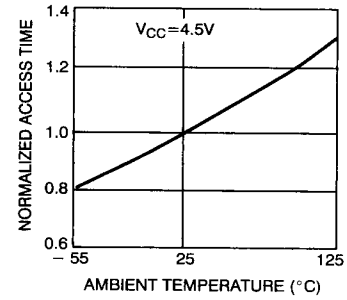
NORMALIZED I_{CC} vs. t_{CKA} CYCLE



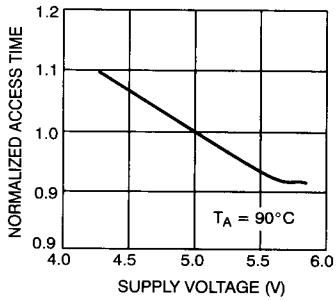
NORMALIZED I_{CC} vs. OUTPUT VOLTAGE



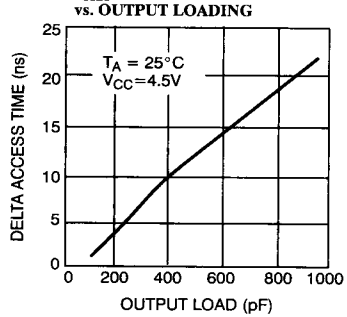
NORMALIZED t_{CKA} vs. TEMPERATURE



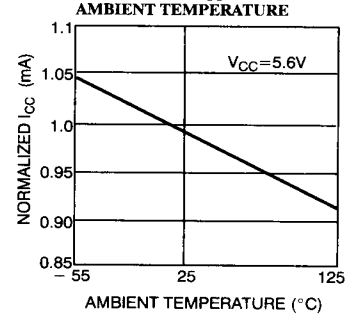
NORMALIZED t_{CKA} vs. SUPPLY VOLTAGE



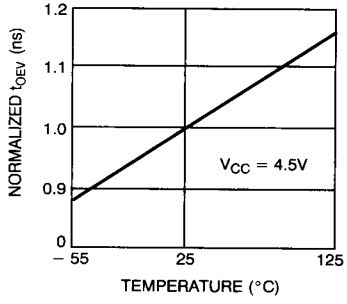
t_{CKA} CHANGE vs. OUTPUT LOADING



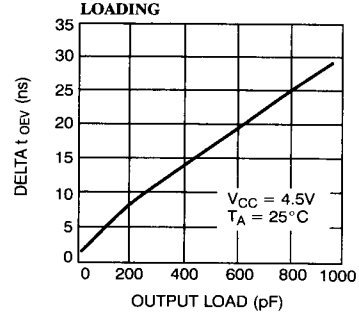
NORMALIZED I_{CC} vs. AMBIENT TEMPERATURE



NORMALIZED t_{OEV} vs. TEMPERATURE



t_{OEV} CHANGE vs. OUTPUT LOADING



C270-16

Ordering Information[13]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C270–15HC	H67	44-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C270–15JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C270–15HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C270–15QMB	Q67	44-Pin Windowed Leadless Chip Carrier	
20	CY7C270–20HC	H67	44-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C270–20JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C270–20HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C270–20QMB	Q67	44-Pin Windowed Leadless Chip Carrier	
30	CY7C270–30HC	H67	44-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C270–30JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C270–30HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C270–30QMB	Q67	44-Pin Windowed Leadless Chip Carrier	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Note:

13. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

Switching Characteristics

Parameter	Subgroups
t_{AS}	7, 8, 9, 10, 11
t_{AH}	7, 8, 9, 10, 11
t_{LES}	7, 8, 9, 10, 11
t_{LEH}	7, 8, 9, 10, 11
t_{ADVS}	7, 8, 9, 10, 11
t_{ADVH}	7, 8, 9, 10, 11
t_{DH}	7, 8, 9, 10, 11
t_{CKA}	7, 8, 9, 10, 11
t_{CSS}	7, 8, 9, 10, 11
t_{CSH}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{CKB}	7, 8, 9, 10, 11
t_{LEA}	7, 8, 9, 10, 11
t_{OEV}	7, 8, 9, 10, 11
t_{LW}	7, 8, 9, 10, 11
t_{ASL}	7, 8, 9, 10, 11
t_{CSSL}	7, 8, 9, 10, 11
t_{AHL}	7, 8, 9, 10, 11
t_{CSHL}	7, 8, 9, 10, 11
t_{CSOV}	7, 8, 9, 10, 11
t_{LOV}	7, 8, 9, 10, 11
t_{COV}	7, 8, 9, 10, 11

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