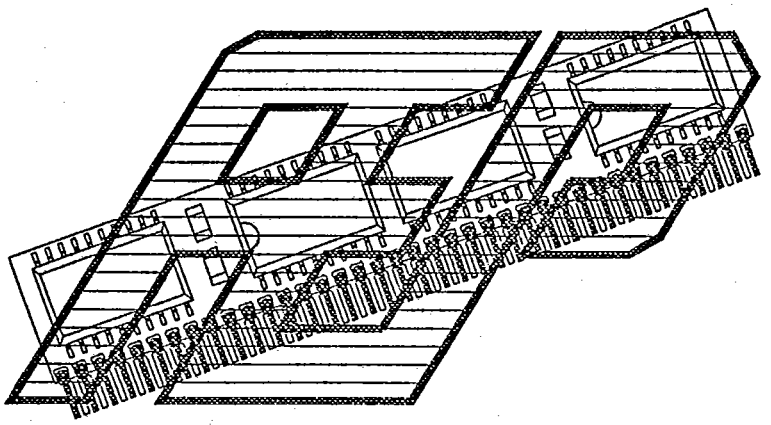
T-52-09

- >> *32 line bus interface*
- >> *Individual control of each 8 line group.*
- >> *High density .070 center spaced ZIP leads for maximum I/O in minimum area.*
- >> *Space saving vertical mounting orientation.*
- >> *Convenient "in one side, out the other" broadside pin-out.*
- >> *TTL compatible*
- >> *Uses single +5V power supply*



32 LINE BUFFER MODULE

DESCRIPTION:

The AEPBZ32 is a high density 32 line buffer module ideal for driving 16 or 32 bit wide bus lines as well as general purpose applications. The vertical mounting orientation and compact I/O pin footprint make it superb for projects with tight space constraints.

Physically the module consists of an FR4 PC material substrate surface mounted with four 244 type buffer ICs, four 0.10 microfarad decoupling capacitors, and 75 I/O pins in a staggered ZIP package format. It can be ordered with any 244 type buffer from any family of IC manufacturing technology (such as LS, F, FCT or equivalent) that is available in a 20 pin SOP package. The module features four active low Output Enables, each controlling eight outputs.

Performance specifications and electrical characteristics are determined by the IC devices used. These items can vary according to the type and manufacturer of the components. The necessary information is obtained from the IC vendors' data sheets, like those attached, or from their data books.

Mechanical dimensions are 0.505 in. high by 2.66 in. long by 0.22 in. wide. The I/O pins are in two rows which are 0.1 inch apart and offset longitudinally 0.035 inch. In each row the pins are on 0.070 inch center spacing. See included specification drawing.

The AEPBZ32 is one of a family of digital circuit support function modules which includes a 32 line transceiver, a 32 line register, and a 32 line latch module. These are natural companions for AEP memory modules.

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EXAMPLE PART NUMBERING CHART

BZ32 with	
74F244 buffer	AEPBZ32-F244
74FCT244 buffer	AEPBZ32-FCT244
74ACT244 buffer	AEPBZ32-ACT244
74LS244 buffer	AEPBZ32-LS244

Buffer notes:
The standard buffer device used is the 74FCT244/A. Please contact AEP if a type that is not listed above is desired. If the pin out configuration is the same as the 74FCT244 and the desired type is available in a standard 20 pin SOP, there should be no problem using it on the module.

The "/A" at the end of the standard IC number is a "High Performance" speed indicator. AEP may use the "A" version of a device even if it is not explicitly specified unless requested not to. An exact specification (type and manufacturer) of the IC device desired is recommended. Please contact AEP for assistance if needed.

Vendor notes:
The IC device specification information which may be included is typical and does not limit AEP to that vendor. The actual devices used will be equivalent depending on price, availability, and customer requirements. AEP will gladly use or exclude particular manufacturers upon request. However, this might affect module price.

Disclaimers:
The information in this document has been carefully checked and is believed to be reliable. However, Advanced Electronic Packaging Inc. assumes no responsibility for inaccuracies. AEP also reserves the right to change products or specifications without notice.

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AEPBZ32-244

32 LINE BUFFER MODULE

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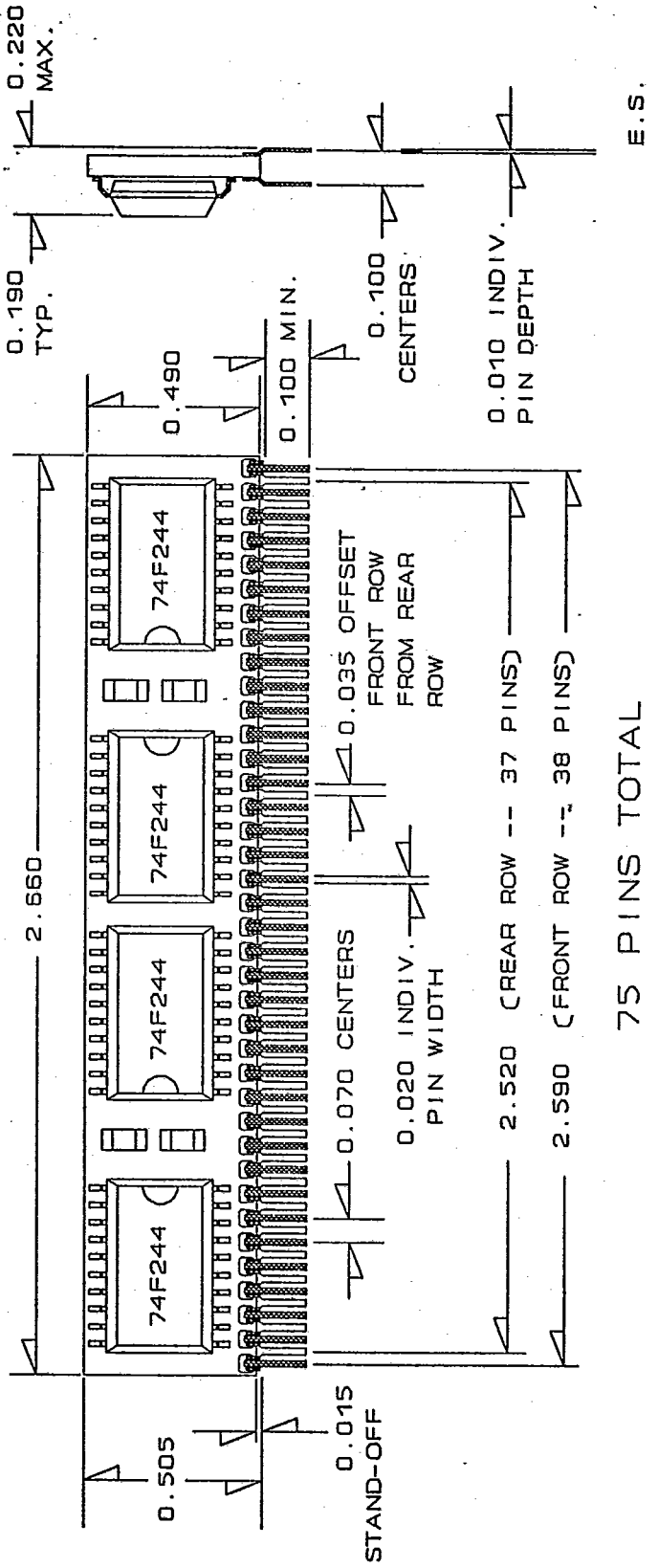
DIMENSIONS IN INCHES. TOLERANCE: ±0.010 UNLESS SPECIFIED.



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32 LINE BUFFER MODULE
PIN CONFIGURATION (TOP VIEW)

	PIN #s		
(DATA INPUTS)	I_0 – 1	2 – Y_0	(DATA OUTPUTS)
	I_1 – 3	4 – Y_1	
	I_2 – 5	6 – Y_2	
	I_3 – 7	8 – Y_3	
	I_4 – 9	10 – Y_4	
	I_5 – 11	12 – Y_5	
	I_6 – 13	14 – Y_6	
	I_7 – 15	16 – Y_7	
(GROUND)	Vss – 17	18 – OE_1	(OUTPUT ENABLE 1)
(OUTPUT ENABLE 2)	OE_2 – 19	20 – Vss	(GROUND)
(DATA INPUTS)	I_8 – 21	22 – Y_8	(DATA OUTPUTS)
	I_9 – 23	24 – Y_9	
	I_{10} – 25	26 – Y_{10}	
	I_{11} – 27	28 – Y_{11}	
	I_{12} – 29	30 – Y_{12}	
	I_{13} – 31	32 – Y_{13}	
	I_{14} – 33	34 – Y_{14}	
	I_{15} – 35	36 – Y_{15}	
(POWER)	Vcc – 37	38 – Vcc	(POWER)
(DATA INPUTS)	I_{16} – 39	40 – Y_{16}	(DATA OUTPUTS)
	I_{17} – 41	42 – Y_{17}	
	I_{18} – 43	44 – Y_{18}	
	I_{19} – 45	46 – Y_{19}	
	I_{20} – 47	48 – Y_{20}	
	I_{21} – 49	50 – Y_{21}	
	I_{22} – 51	52 – Y_{22}	
	I_{23} – 53	54 – Y_{23}	
(GROUND)	Vss – 55	56 – OE_3	(OUTPUT ENABLE 3)
(OUTPUT ENABLE 4)	OE_4 – 57	58 – Vss	(GROUND)
(DATA INPUTS)	I_{24} – 59	60 – Y_{24}	(DATA OUTPUTS)
	I_{25} – 61	62 – Y_{25}	
	I_{26} – 63	64 – Y_{26}	
	I_{27} – 65	66 – Y_{27}	
	I_{28} – 67	68 – Y_{28}	
	I_{29} – 69	70 – Y_{29}	
	I_{30} – 71	72 – Y_{30}	
	I_{31} – 73	74 – Y_{31}	
(NO CONNECT)	N/C – 75		

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32 LINE BUFFER MODULE FUNCTIONAL DIAGRAM