

FEATURES

- Controls and monitors up to 4 fans**
- High and low frequency fan drive signal**
- 1 on-chip and 2 remote temperature sensors**
- Series resistance cancellation on the remote channel**
- Extended temperature measurement range, up to 191°C**
- Dynamic T_{MIN} control mode optimizes system acoustics intelligently**
- Automatic fan speed control mode controls system cooling based on measured temperature**
- Enhanced acoustic mode dramatically reduces user perception of changing fan speeds**
- Thermal protection feature via \overline{THERM} output**
- Monitors performance impact of Intel® Pentium™ 4 processor**
- Thermal control circuit via \overline{THERM} input**
- 2-wire, 3-wire, and 4-wire fan speed measurement**
- Limit comparison of all monitored values**
- Meets SMBus 2.0 electrical specifications (fully SMBus 1.1 compliant)**

GENERAL DESCRIPTION

The ADT7467 dBCOOL™ controller is a thermal monitor and multiple PWM fan controller for noise-sensitive or power-sensitive applications requiring active system cooling. The ADT7467 can drive a fan using either a low or high frequency drive signal, monitor the temperature of up to two remote sensor diodes plus its own internal temperature, and measure and control the speed of up to four fans, so that they operate at the lowest possible speed for minimum acoustic noise.

The automatic fan speed control loop optimizes fan speed for a given temperature. A unique dynamic T_{MIN} control mode enables the system thermals/acoustics to be intelligently managed. The effectiveness of the system's thermal solution can be monitored using the \overline{THERM} input. The ADT7467 also provides critical thermal protection to the system using the bidirectional \overline{THERM} pin as an output to prevent system or component overheating.

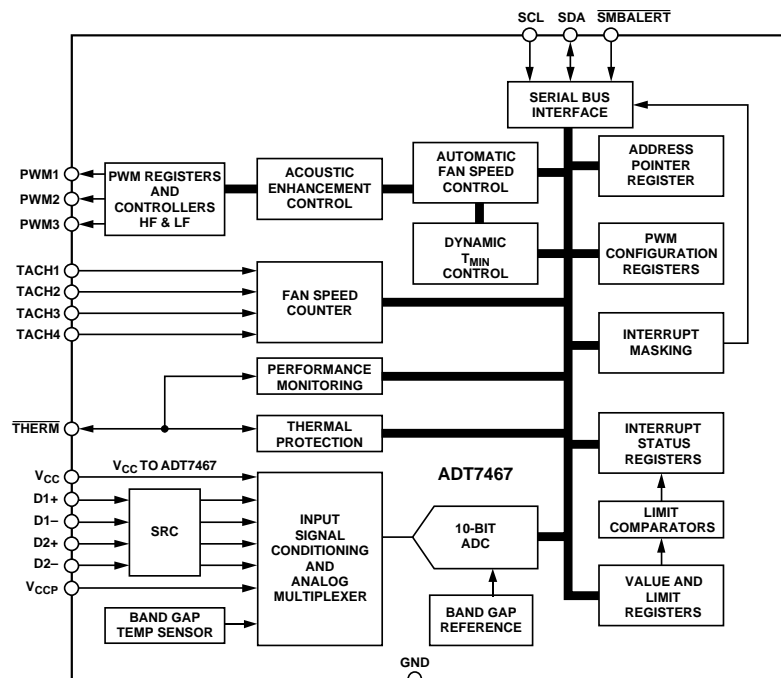
FUNCTIONAL BLOCK DIAGRAM


Figure 1.

Rev. 0

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REVISION HISTORY

Revision 0: Initial Version

SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX} , $V_{CC} = V_{MIN}$ to V_{MAX} , unless otherwise noted.

All voltages are measured with respect to GND, unless otherwise specified. Typicals are at $T_A = 25^\circ\text{C}$ and represent most likely parametric norm. Logic inputs accept input high voltages up to V_{MAX} even when device is operating down to V_{MIN} . Timing specifications are tested at logic levels of $V_{IL} = 0.8\text{ V}$ for a falling edge and $V_{IH} = 2.0\text{ V}$ for a rising edge. SMBus timing specifications are guaranteed by design and are not production tested.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					
Supply Voltage	3.0	3.3	5.5	V	
Supply Current, I_{CC}			3	mA	Interface inactive, ADC active
			20	μA	Standby mode
TEMP-TO-DIGITAL CONVERTER					
Local Sensor Accuracy			± 1.5	$^\circ\text{C}$	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$
	-3.5		+2	$^\circ\text{C}$	$-40^\circ\text{C} \leq T_A \leq +100^\circ\text{C}$
	-4		+2	$^\circ\text{C}$	$-40^\circ\text{C} \leq T_A \leq +120^\circ\text{C}$
Resolution		0.25		$^\circ\text{C}$	
Remote Diode Sensor Accuracy		± 0.5	± 1.5	$^\circ\text{C}$	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$; $0^\circ\text{C} \leq T_D \leq 120^\circ\text{C}$
	-3.5		+2	$^\circ\text{C}$	$0^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$; $0^\circ\text{C} \leq T_D \leq 120^\circ\text{C}$
	-4.5		+2	$^\circ\text{C}$	$-40^\circ\text{C} \leq T_A \leq +120^\circ\text{C}$; $0^\circ\text{C} \leq T_D \leq +120^\circ\text{C}$
Resolution		0.25		$^\circ\text{C}$	
Remote Sensor Source Current		6		μA	First current
		36		μA	Second current
		96		μA	Third current
ANALOG-TO-DIGITAL CONVERTER (INCLUDING MUX AND ATTENUATORS)					
Total Unadjusted Error (TUE)			± 1.5	%	
Differential Nonlinearity (DNL)			± 1	LSB	8 bits
Power Supply Sensitivity		± 0.1		%/V	
Conversion Time (Voltage Input)		11		ms	Averaging enabled
Conversion Time (Local Temperature)		12		ms	Averaging enabled
Conversion Time (Remote Temperature)		38		ms	Averaging enabled
Total Monitoring Cycle Time		145		ms	Averaging enabled
Total Monitoring Cycle Time		19		ms	Averaging disabled
Input Resistance	40	80	100	$\text{k}\Omega$	For V_{CC} channel
	80	140	200	$\text{k}\Omega$	For all other channels
FAN RPM-TO-DIGITAL CONVERTER					
Accuracy			± 5	%	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, 3.3 V
			± 7	%	$-40^\circ\text{C} \leq T_A \leq +120^\circ\text{C}$, 3.3 V
			± 10	%	$-40^\circ\text{C} \leq T_A \leq +120^\circ\text{C}$, 5.5 V
Full-Scale Count			65,535		
Nominal Input RPM		109		RPM	Fan count = 0xBFFF
		329		RPM	Fan count = 0x3FFF
		5000		RPM	Fan count = 0x0438
		10000		RPM	Fan count = 0x021C
Internal Clock Frequency	85.5	90	94.5	kHz	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, $V_{CC} = 3.3\text{ V}$
	83.7	90	96.3	kHz	$-40^\circ\text{C} \leq T_A \leq +120^\circ\text{C}$, $V_{CC} = 3.3\text{ V}$
	81	90	99	kHz	$-40^\circ\text{C} \leq T_A \leq +120^\circ\text{C}$, $V_{CC} = 5.5\text{ V}$

ADT7467

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments	
OPEN-DRAIN DIGITAL OUTPUTS, PWM1 to PWM3, XTO						
Current Sink, I_{OL}			8.0	mA	$I_{OUT} = -8.0 \text{ mA}, V_{CC} = +3.3 \text{ V}$ $V_{OUT} = V_{CC}$	
Output Low Voltage, V_{OL}			0.4	V		
High Level Output Current, I_{OH}		0.1	1.0	μA		
OPEN-DRAIN SERIAL DATA BUS OUTPUT (SDA)						
Output Low Voltage, V_{OL}			0.4	V	$I_{OUT} = -4.0 \text{ mA}, V_{CC} = +3.3 \text{ V}$ $V_{OUT} = V_{CC}$	
High Level Output Current, I_{OH}		0.1	1.0	μA		
SMBUS DIGITAL INPUTS (SCL, SDA)						
Input High Voltage, V_{IH}	2.0			V		
Input Low Voltage, V_{IL}			0.4	V		
Hysteresis		500		mV		
DIGITAL INPUT LOGIC LEVELS (TACH INPUTS)						
Input High Voltage, V_{IH}	2.0			V	Maximum input voltage	
Input Low Voltage, V_{IL}			0.8	V		
Hysteresis		0.5		V p-p	Minimum input voltage	
DIGITAL INPUT LOGIC LEVELS (THERM) ADTL+						
Input High Voltage, V_{IH}		$0.75 \times V_{CCP}$		V		
Input Low Voltage, V_{IL}			0.4	V		
DIGITAL INPUT CURRENT						
Input High Current, I_{IH}	-1			μA	$V_{IN} = V_{CC}$	
Input Low Current, I_{IL}			1	μA	$V_{IN} = 0$	
Input Capacitance, C_{IN}		5		pF		
SERIAL BUS TIMING ⁵						
Clock Frequency, f_{SCLK}	10		400	kHz	See Figure 2	
Glitch Immunity, t_{SW}			50	ns		
Bus Free Time, t_{BUF}	4.7			μs		
Start Setup Time, $t_{SU;STA}$	4.7			μs		
Start Hold Time, $t_{HD;STA}$	4.0			μs		
SCL Low Time, t_{LOW}	4.7			μs		
SCL High Time, t_{HIGH}	4.0		50	μs		
SCL, SDA Rise Time, t_R			1000	ns		
SCL, SDA Fall Time, t_F			300	μs		
Data Setup Time, $t_{SU;DAT}$	250			ns		
Data Hold Time, $t_{HD;DAT}$	300			ns		
Detect Clock Low Timeout, $t_{TIMEOUT}$	15		35	ms		
						Can be optionally disabled

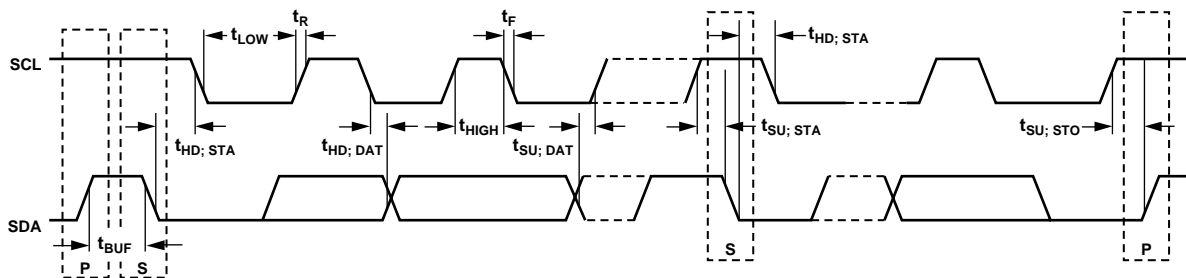


Figure 2. Serial Bus Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Positive Supply Voltage (V_{CC})	5.5 V
Voltage on Any Input or Output Pin	-0.3 V to +6.5 V
Input Current at Any Pin	± 5 mA
Package Input Current	± 20 mA
Maximum Junction Temperature (T_{JMAX})	150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature, Soldering	
IR Reflow Peak Temperature	220°C
Lead Temperature (Soldering 10 s)	300°C
ESD Rating	1000 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

16-lead QSOP package:

$$\theta_{JA} = 150^{\circ}\text{C}/\text{W}$$

$$\theta_{JC} = 39^{\circ}\text{C}/\text{W}$$

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

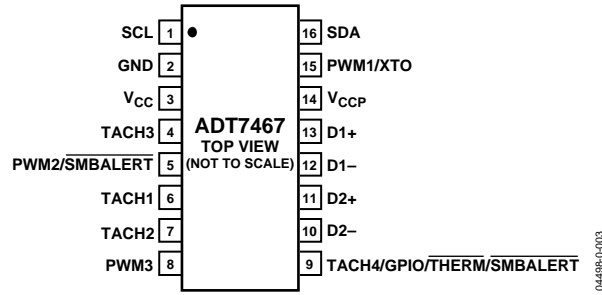
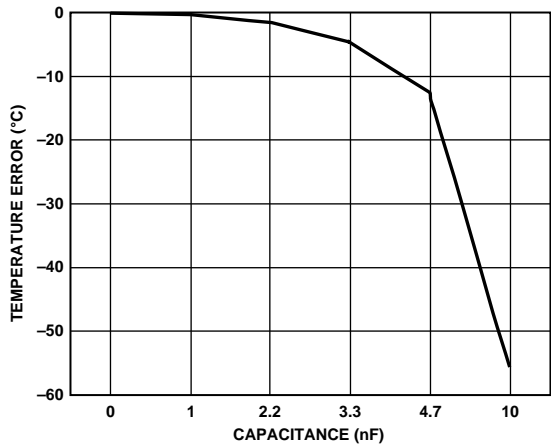


Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

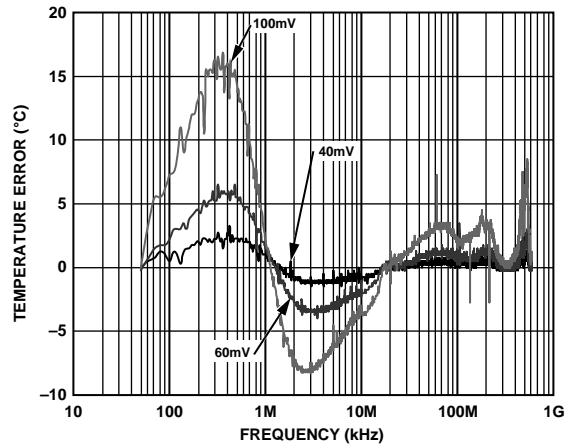
Pin No.	Mnemonic	Description
1	SCL	Digital Input (Open Drain). SMBus serial clock input. Requires SMBus pull-up.
2	GND	Ground Pin for the ADT7467.
3	V _{CC}	Power Supply. Can be powered by 3.3 V standby, if monitoring in low power states is required. V _{CC} is also monitored through this pin. The ADT7467 can also be powered from a 5 V supply. Setting Bit 7 of Configuration Register 1 (Reg. 0x40) rescales the V _{CC} input attenuators to correctly measure a 5 V supply.
4	TACH3	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 3. Can be reconfigured as an analog input (AIN3) to measure the speed of 2-wire fans (low frequency mode only).
5	PWM2 SMBALERT	Digital Output (Open Drain). Requires 10 kΩ typical pull-up. Pulse width modulated output to control Fan 2 speed. Can be configured as a high or low frequency drive. Digital Output (Open Drain). This pin can be reconfigured as an SMBALERT interrupt output to signal out-of-limit conditions.
6	TACH1	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 1. Can be reconfigured as an analog input (AIN1) to measure the speed of 2-wire fans (low frequency mode only).
7	TACH2	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 2. Can be reconfigured as an analog input (AIN2) to measure the speed of 2-wire fans (low frequency mode only).
8	PWM3	Digital I/O (Open Drain). Pulse width modulated output to control the speed of Fan 3 and Fan 4. Requires 10 kΩ typical pull-up. Can be configured as a high or low frequency drive.
9	TACH4 GPIO THERM SMBALERT	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 4. Can be reconfigured as an analog input (AIN4) to measure the speed of 2-wire fans (low frequency mode only). General Purpose Open Drain Digital I/O. Alternatively, the pin can be reconfigured as a bidirectional THERM pin, which can be used to time and monitor assertions on the THERM input. For example, the pin can be connected to the PROCHOT output of an Intel Pentium 4 processor or to the output of a trip point temperature sensor. This pin can be used as an output to signal overtemperature conditions. Digital Output (Open Drain). This pin can be reconfigured as an SMBALERT interrupt output to signal out-of-limit conditions.
10	D2-	Cathode Connection to Second Thermal Diode.
11	D2+	Anode Connection to Second Thermal Diode.
12	D1-	Cathode Connection to First Thermal Diode.
13	D1+	Anode Connection to First Thermal Diode.
14	V _{CCP}	Analog Input. Monitors processor core voltage (0 V – 3 V).
15	PWM1 XTO	Digital Output (Open Drain). Pulse-width modulated output to control Fan 1 speed. Requires 10 kΩ typical pull-up. Also functions as the output from the XNOR tree in XNOR test mode.
16	SDA	Digital I/O (Open Drain). SMBus bidirectional serial data. Requires 10 kΩ typical pull-up.

TYPICAL PERFORMANCE CHARACTERISTICS



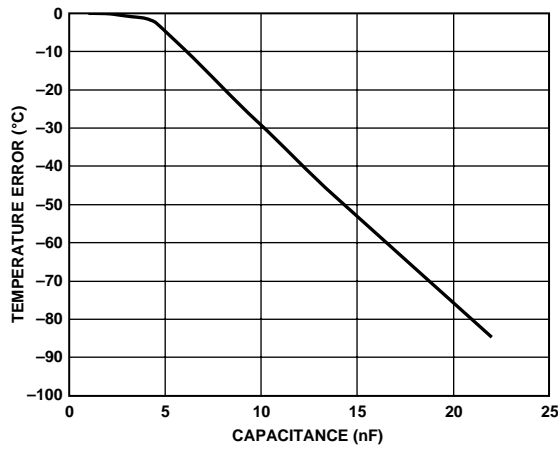
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Figure 4. Temperature Error vs. Capacitance between D+ and D-



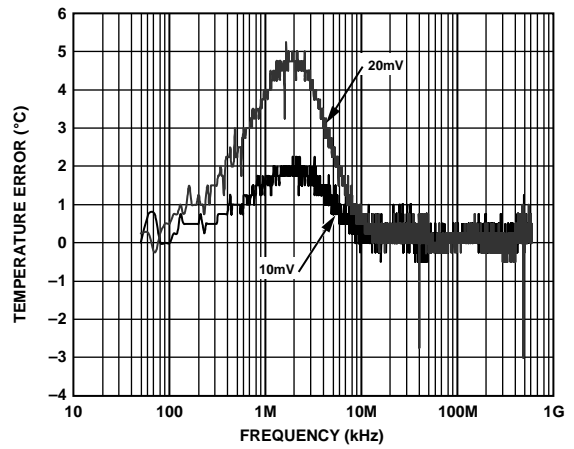
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Figure 7. Remote Temperature Error vs. Common Mode Noise Frequency



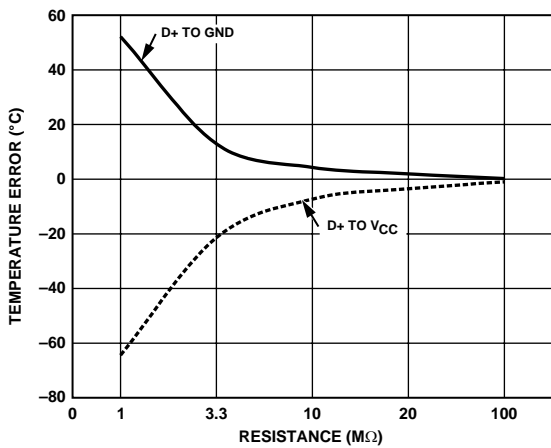
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Figure 5. External Temperature Error vs. D+/D- Capacitance



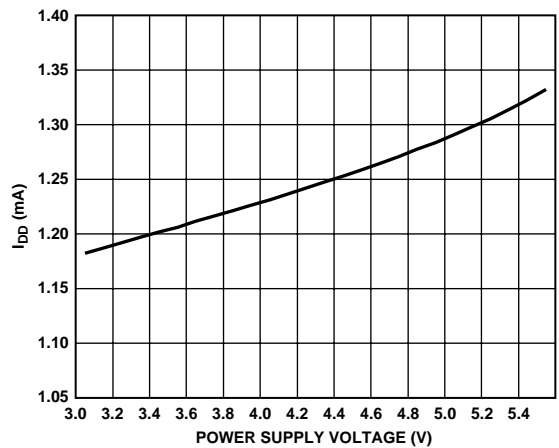
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Figure 8. Remote Temperature Error vs. Differential Mode Noise Frequency



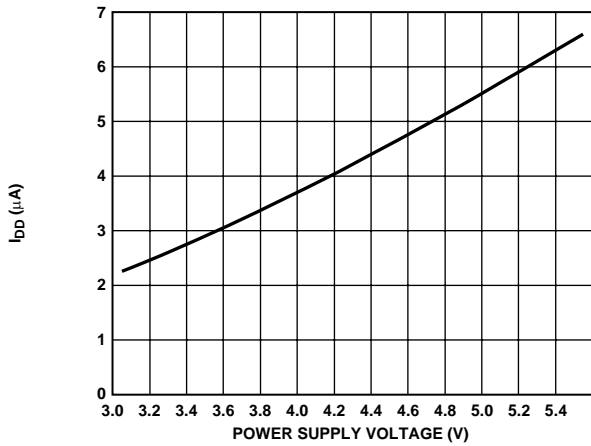
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Figure 6. Temperature Error vs. PCB Resistance



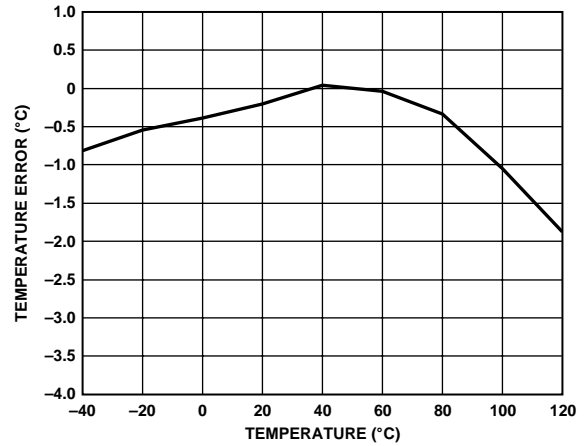
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Figure 9. Normal I_{DD} vs. Power Supply



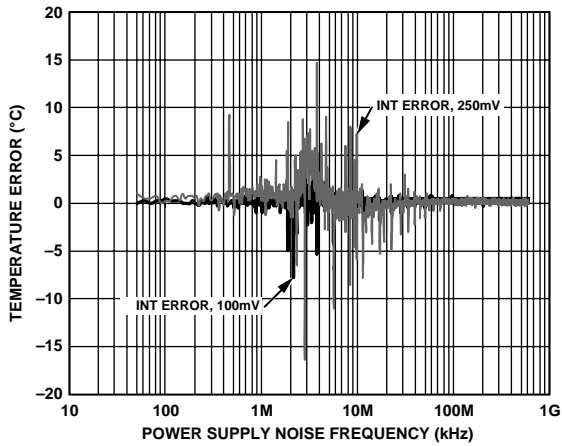
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Figure 10. Shutdown I_{DD} vs. Power Supply



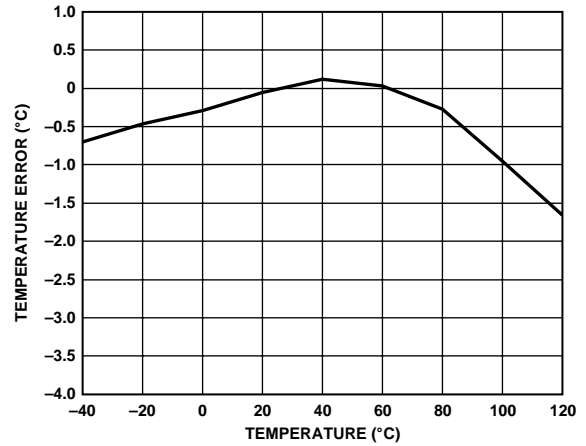
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Figure 13. Internal Temperature Error vs. ADT7467 Temperature



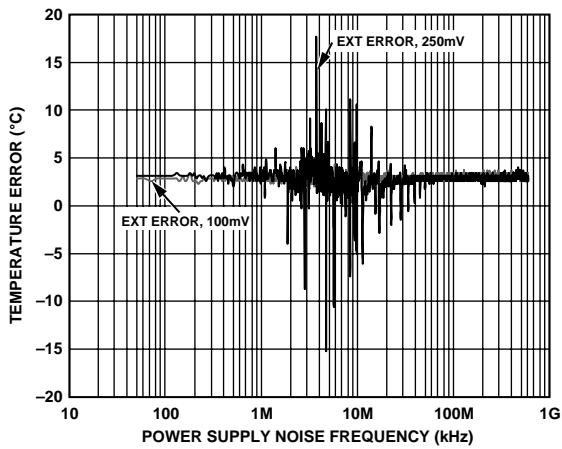
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Figure 11. Internal Temperature Error vs. Power Supply



04488-0-092

Figure 14. Remote Temperature Error vs. ADT7467 Temperature



04488-0-053

Figure 12. Remote Temperature Error vs. Power Supply Noise Frequency

PRODUCT DESCRIPTION

The ADT7467 is a complete thermal monitor and multiple fan controller for any system requiring thermal monitoring and cooling. The device communicates with the system via a serial system management bus. The serial bus controller has a serial data line for reading and writing addresses and data (Pin 16), and an input line for the serial clock (Pin 1). All control and programming functions for the ADT7467 are performed over the serial bus. In addition, a pin can be reconfigured as an SMBALERT output to signal out-of-limit conditions.

COMPARISON BETWEEN ADT7460 AND ADT7467

The ADT7467 is an upgrade to the ADT7460. The ADT7467 and ADT7460 are almost pin and register map compatible. The ADT7467 and ADT7460 have the following differences:

1. On the ADT7467, the PWM drive signals can be configured as either high frequency or low frequency drives. The low frequency option is programmable between 10 Hz and 100 Hz. The high frequency option is 22.5 kHz. On the ADT7460, only the low frequency option is available.
2. Once V_{CC} is powered up, monitoring of temperature and fan speeds is enabled on the ADT7467 when V_{CCP} is powered up, or if V_{CCP} is never powered up, when the first SMBus transaction with the ADT7467 is completed. On the ADT7460, the STRT bit in Configuration Register 1 must be set to enable monitoring.
3. The fans are switched off by default on power-up on the ADT7467. On the ADT7460, the fans run at full speed on power-up.

Fail-safe cooling is provided on the ADT7467 in that, if the measured temperature exceeds the THERM limit (100°C), the fans run at full speed.

Fail-safe cooling is also provided 4.6 s after V_{CCP} is powered up. The fans go to full speed, if the ADT7467 has not been addressed via the SMBus within 4.6 s of when the V_{CCP} is powered up. This protects the system in the event that the SMBus fails. The ADT7467 can be programmed at any time, either before or after the 4.6 s has elapsed, and it behaves as programmed. If V_{CCP} is never powered up, fail-safe cooling is effectively disabled. If V_{CCP} is disabled, writing to the ADT7467 at any time causes the ADT7467 to operate normally.

4. Series resistance cancellation (SRC) is provided on the remote temperature channels on the ADT7467, but not on the ADT7460. SRC automatically cancels linear offset introduced by a series resistance between the thermal diode and the sensor.

5. The ADT7467 has an extended temperature measurement range. The measurement range goes from -64°C to $+191^{\circ}\text{C}$. On the ADT7460, the measurement range is from -127°C to $+127^{\circ}\text{C}$. This means that the ADT7467 can measure higher temperatures. The ADT7467 also includes the ADT7460 temperature range; the temperature measurement range can be switched by setting Bit 0 of Configuration Register 5.
6. The ADT7467 maximum fan speed (% duty cycle) in the automatic fan speed control loop can be programmed. The maximum fan speed is 100% duty cycle on the ADT7460 and is not programmable.
7. The offset register in the ADT7467 is programmable up to $\pm 64^{\circ}\text{C}$ with 0.50°C resolution. The offset register of the ADT7460 is programmable up to $\pm 32^{\circ}\text{C}$ with 0.25°C resolution.
8. V_{CCP} is monitored on Pin 14 of the ADT7467 and can be used to set the threshold for THERM (PROCHOT) ($2/3$ of V_{CCP}). 2.5 V is monitored on Pin 14 of the ADT7460. The threshold for THERM (PROCHOT) is set at $V_{IH} = 1.7\text{ V}$ and $V_{IL} = 0.8\text{ V}$ on the ADT7460.
9. On the ADT7460, Pin 14 could be reconfigured as SMBus ALERT. This is not available on the ADT7467. SMBus ALERT can be enabled instead on Pin 9.
10. A GPIO can also be made available on Pin 9 on the ADT7467. This is not available on the ADT7460. Set the GPIO polarity and direction in Configuration Register 5. The GPIO status bit is Bit 5 of Status Register 2 (shared with TACH4 and THERM, because only one can be enabled at a time).
11. The ADT7460 has three possible SMBus addresses, which are selectable using the address select and address enable pins. The ADT7467 has one SMBus address available at Address 0x2E.

Due to the inclusion of extra functionality, the register map has changed, including an additional configuration register: Configuration Register 5 at Address 0x7C.

ADT7467

Configuration Register 5

Bit 0: If Bit 0 is set to 1, the ADT7467 is backward compatible temperature-wise with the ADT7460. Measurements, T_{MIN} calibration circuit, fan control, etc., work in the range -127°C to $+127^{\circ}\text{C}$. Also, care should be taken in reprogramming the temperature limits (T_{MIN} , operating point, $THERM$ limits) to their desired twos complement value, because the power-on default for them is at Offset 64. The extended temperature range is -64°C to 191°C . The default is 1, which is in the -64°C to $+191^{\circ}\text{C}$ temperature range.

Bit 1 = 0 is the high frequency (22.5 kHz) fan drive signal.

Bit 1 = 1 switches the fan drive to low frequency PWM, programmable between 10 Hz and 100 Hz, the same as the ADT7460. The default = 0 = HF PWM.

Bit 2 sets the direction for the GPIO: 0 = input, 1 = output.

Bit 3 sets the GPIO polarity: 0 = active low, 1 = active high.

How to Set the Functionality of Pin 9

Pin 9 on the ADT7467 has four possible functions: $\overline{\text{SMBALERT}}$, $\overline{\text{THERM}}$, GPIO, and TACH4. The user chooses the required functionality by setting Bit 0 and Bit 1 of Configuration Register 4 at Address 0x7D.

Table 4. Pin 9 Settings

Bit 0	Bit 1	Function
00		TACH4
01		THERM
10		SMBALERT
11		GPIO

RECOMMENDED IMPLEMENTATION

Configuring the ADT7467 as in Figure 15 allows the system designer to use the following features:

- Two PWM outputs for fan control of up to three fans (the front and rear chassis fans are connected in parallel).
- Three TACH fan speed measurement inputs.
- V_{CC} measured internally through Pin 3.
- CPU temperature measured using Remote 1 temperature channel.
- Ambient temperature measured through Remote 2 temperature channel.
- Bidirectional $\overline{\text{THERM}}$ pin. This feature allows Intel Pentium 4 PROCHOT monitoring and can function as an overtemperature $\overline{\text{THERM}}$ output. It can alternatively be programmed as an $\overline{\text{SMBALERT}}$ system interrupt output.

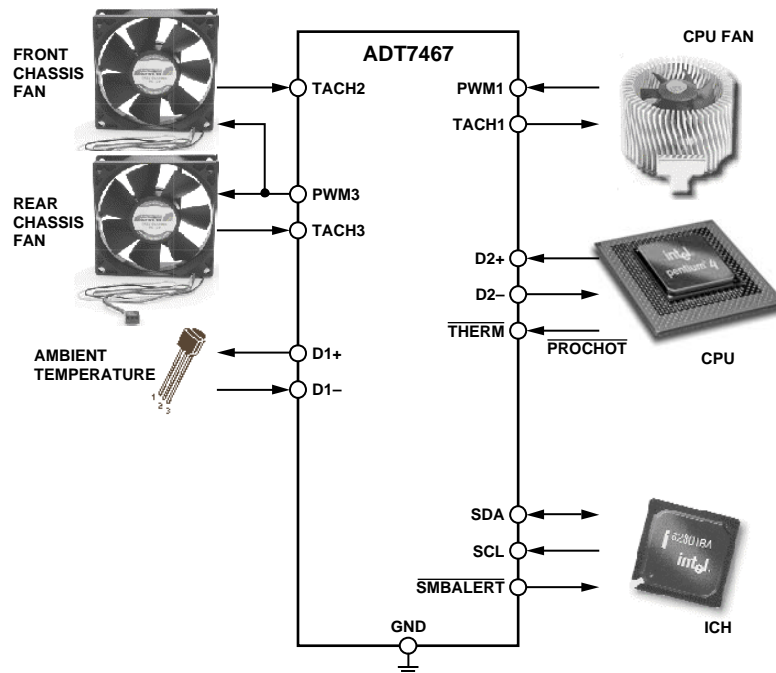


Figure 15. ADT7467 Configuration

SERIAL BUS INTERFACE

On PCs and servers, control of the ADT7467 is carried out using the serial system management bus (SMBus). The ADT7467 is connected to this bus as a slave device, under the control of a master controller, which is usually (but not necessarily) the ICH.

The ADT7467 has a fixed 7-bit serial bus address of 0101110 or 0x2E. The read/write bit must be added to get the 8-bit address (01011100 or 0x5C). Data is sent over the serial bus in sequences of nine clock pulses: eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low-to-high transition when the clock is high might be interpreted as a stop signal. The number of data bytes that can be transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.

When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the tenth clock pulse to assert a stop condition. In read mode, the master device overrides the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as No Acknowledge. The master then takes the data line low during the low period before the tenth clock pulse, and then high during the tenth clock pulse to assert a stop condition.

Any number of bytes of data can be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation, because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

In the ADT7467, write operations contain either one or two bytes, and read operations contain one byte and perform the following functions. To write data to one of the device data registers or read data from it, the address pointer register must be set so that the correct data register is addressed, then data can be written into that register or read from it. The first byte of a write operation always contains an address that is stored in the address pointer register. If data is to be written to the device, then the write operation contains a second data byte that is written to the register selected by the address pointer register.

This write operation is illustrated in Figure 16. The device address is sent over the bus, and then R/W is set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second data byte is the data to be written to the internal data register.

When reading data from a register, there are two possibilities:

- If the ADT7467's address pointer register value is unknown or not the desired value, it must first be set to the correct value before data can be read from the desired data register. This is done by performing a write to the ADT7467 as before, but only the data byte containing the register address is sent, because no data is written to the register. This is shown in Figure 17.

A read operation is then performed consisting of the serial bus address, R/W bit set to 1, followed by the data byte read from the data register. This is shown in Figure 18.

- If the address pointer register is known to be already at the desired address, data can be read from the corresponding data register without first writing to the address pointer register, as shown in Figure 18.

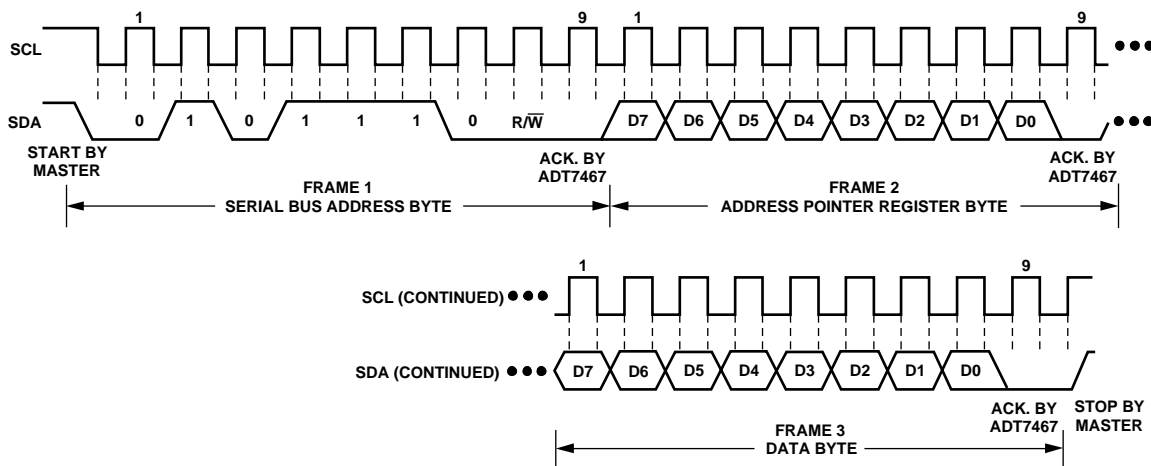


Figure 16. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

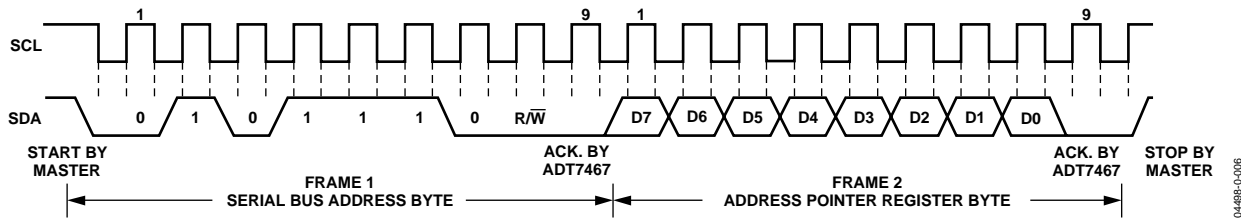


Figure 17. Writing to the Address Pointer Register Only

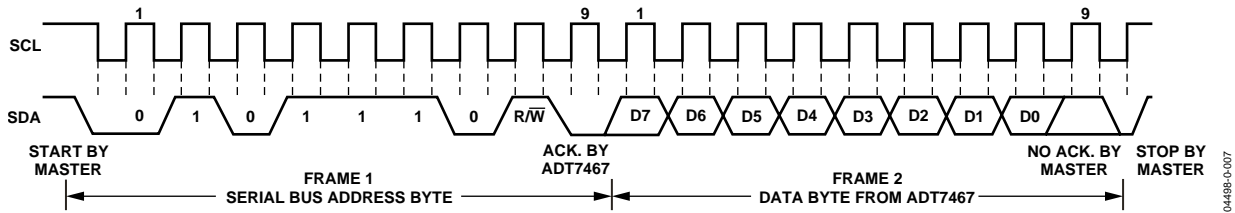


Figure 18. Reading Data from a Previously Selected Register

It is possible to read a data byte from a data register without first writing to the address pointer register, if the address pointer register is already at the correct value. However, it is not possible to write data to a register without writing to the address pointer register, because the first data byte of a write is always written to the address pointer register.

In addition to supporting the send byte and receive byte protocols, the ADT7467 also supports the read byte protocol. (See *System Management Bus Specifications Rev. 2* for more information. This document is available from Intel.)

If several read or write operations must be performed in succession, the master can send a repeat start condition instead of a stop condition to begin a new operation.

WRITE OPERATIONS

The SMBus specification defines several protocols for different types of read and write operations. The ones used in the ADT7467 are discussed below. The following abbreviations are used in the diagrams:

- S – START
- P – STOP
- R – READ
- W – WRITE
- A – ACKNOWLEDGE
- A – NO ACKNOWLEDGE

The ADT7467 uses the following SMBus write protocols.

Send Byte

In this operation, the master device sends a single command byte to a slave device as follows:

1. The master device asserts a start condition on SDA.

2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master asserts a stop condition on SDA and the transaction ends.

For the ADT7467, the send byte protocol is used to write a register address to RAM for a subsequent single byte read from the same address. This operation is illustrated in Figure 19.

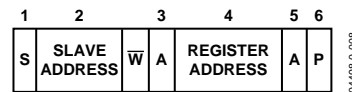


Figure 19. Setting a Register Address for Subsequent Read

If the master is required to read data from the register immediately after setting up the address, it can assert a repeat start condition immediately after the final ACK and carry out a single byte read without asserting an intermediate stop condition.

Write Byte

In this operation, the master device sends a command byte and one data byte to the slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.

- The slave asserts ACK on SDA.
- The master sends a data byte.
- The slave asserts ACK on SDA.
- The master asserts a stop condition on SDA to end the transaction.

This operation is illustrated in Figure 20.

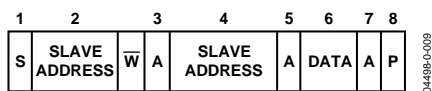


Figure 20. Single Byte Write to a Register

READ OPERATIONS

The ADT7467 uses the following SMBus read protocols.

Receive Byte

This operation is useful when repeatedly reading a single register. The register address must have been set up previously. In this operation, the master device receives a single byte from a slave device, as follows:

- The master device asserts a start condition on SDA.
- The master sends the 7-bit slave address followed by the read bit (high).
- The addressed slave device asserts ACK on SDA.
- The master receives a data byte.
- The master asserts NO ACK on SDA.
- The master asserts a stop condition on SDA and the transaction ends.

In the ADT7467, the receive byte protocol is used to read a single byte of data from a register whose address has previously been set by a send byte or write byte operation. This operation is illustrated in Figure 21.

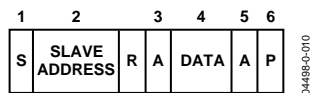


Figure 21. Single Byte Read from a Register

Alert Response Address

Alert response address (ARA) is a feature of SMBus devices that allows an interrupting device to identify itself to the host when multiple devices exist on the same bus.

The $\overline{\text{SMBALERT}}$ output can be used as either an interrupt output or an $\overline{\text{SMBALERT}}$. One or more outputs can be connected to a common $\overline{\text{SMBALERT}}$ line connected to the

master. If a device's $\overline{\text{SMBALERT}}$ line goes low, the following procedure occurs:

- $\overline{\text{SMBALERT}}$ is pulled low.
- The master initiates a read operation and sends the alert response address (ARA = 0001 100). This is a general call address that must not be used as a specific device address.
- The device whose $\overline{\text{SMBALERT}}$ output is low responds to the alert response address, and the master reads its device address. The address of the device is now known and can be interrogated in the usual way.
- If more than one device's $\overline{\text{SMBALERT}}$ output is low, the one with the lowest device address has priority in accordance with normal SMBus arbitration.
- Once the ADT7467 has responded to the alert response address, the master must read the status registers and the $\overline{\text{SMBALERT}}$ is cleared only if the error condition has gone away.

SMBUS TIMEOUT

The ADT7467 includes an SMBus timeout feature. If there is no SMBus activity for 35 ms, the ADT7467 assumes that the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus expecting data. Some SMBus controllers cannot handle the SMBus timeout feature, so it can be disabled.

Configuration Register 1 (Reg. 0x40)

<6> TODIS = 0, SMBus timeout enabled (default).

<6> TODIS = 1, SMBus timeout disabled.

VOLTAGE MEASUREMENT INPUT

The ADT7467 has one external voltage measurement channel. It can also measure its own supply voltage, V_{CC} . Pin 14 can measure V_{CCP} . The V_{CC} supply voltage measurement is carried out through the V_{CC} pin (Pin 3). Setting Bit 7 of Configuration Register 1 (Reg. 0x40) allows a 5 V supply to power the ADT7467 and be measured without overranging the V_{CC} measurement channel. The V_{CCP} input can be used to monitor a chipset supply voltage in computer systems.

ANALOG-TO-DIGITAL CONVERTER

All analog inputs are multiplexed into the on-chip, successive approximation, analog-to-digital converter. This has a resolution of 10 bits. The basic input range is 0 V to 2.25 V, but the input has built-in attenuators to allow measurement of V_{CCP} without any external components. To allow for the tolerance of the supply voltage, the ADC produces an output of 3/4 full scale (decimal 768 or 300 hex) for the nominal input voltage and so has adequate headroom to deal with overvoltages.

INPUT CIRCUITRY

The internal structure for the V_{CCP} analog input is shown in Figure 22. The input circuit consists of an input protection diode, an attenuator, plus a capacitor to form a first-order low-pass filter that gives the input immunity to high frequency noise.

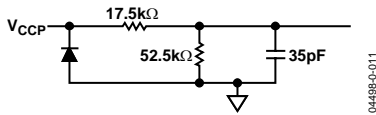


Figure 22. Structure of Analog Inputs

VOLTAGE MEASUREMENT REGISTERS

Reg. 0x21 V_{CCP} Reading = 0x00 default

Reg. 0x22 V_{CC} Reading = 0x00 default

V_{CCP} LIMIT REGISTERS

Associated with the V_{CCP} and V_{CC} measurement channels is a high and low limit register. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts.

Reg. 0x46 V_{CCP} Low Limit = 0x00 default

Reg. 0x47 V_{CCP} High Limit = 0xFF default

Reg. 0x48 V_{CC} Low Limit = 0x00 default

Reg. 0x49 V_{CC} High Limit = 0xFF default

Table 5 shows the input ranges of the analog inputs and output codes of the 10-bit ADC.

When the ADC is running, it samples and converts a voltage input in 0.7 ms and averages 16 conversions to reduce noise; a measurement takes nominally 11 ms.

ADDITIONAL ADC FUNCTIONS FOR VOLTAGE MEASUREMENTS

A number of other functions are available on the ADT7467 to offer the system designer increased flexibility.

Turn-Off Averaging

For each voltage measurement read from a value register, 16 readings have actually been made internally and the results averaged before being placed into the value register. For instances where faster conversions are needed, setting Bit 4 of Configuration Register 2 (Reg. 0x73) turns averaging off. This effectively gives a reading 16 times faster (0.7 ms), but the reading may be noisier.

Bypass Voltage Input Attenuator

Setting Bit 5 of Configuration Register 2 (Reg. 0x73) removes the attenuation circuitry from the V_{CCP} input. This allows the user to directly connect external sensors or to rescale the analog voltage measurement inputs for other applications. The input range of the ADC without the attenuators is 0 V to 2.25 V.

Single-Channel ADC Conversion

Setting Bit 6 of Configuration Register 2 (Reg. 0x73) places the ADT7467 into single-channel ADC conversion mode. In this mode, the ADT7467 can be made to read a single voltage channel only. If the internal ADT7467 clock is used, the selected input is read every 0.7 ms. The appropriate ADC channel is selected by writing to Bits <7:5> of the TACH1 minimum high byte register (0x55).

Bits <7:5> Reg. 0x55	Channel Selected
001	V_{CCP}
010	V_{CC}
101	Remote 1 Temperature
110	Local Temperature
111	Remote 2 Temperature

Configuration Register 2 (Reg. 0x73)

<4> = 1, averaging off.

<5> = 1, bypass input attenuators.

<6> = 1, single-channel convert mode.

TACH1 Minimum High Byte (Reg. 0x55)

<7:5> selects ADC channel for single-channel convert mode.

Table 5. 10-Bit A/D Output Code vs. V_{IN}

Input Voltage			A/D Output	
$V_{CC} (+5 V_{IN})$	$V_{CC} (3.3 V_{IN})$	V_{CCP}	Decimal	Binary (10 Bits)
<0.0065	<0.0042	<0.00293	0	00000000 00
0.0065–0.0130	0.0042–0.0085	0.0293–0.0058	1	00000000 01
0.0130–0.0195	0.0085–0.0128	0.0058–0.0087	2	00000000 10
0.0195–0.0260	0.0128–0.0171	0.0087–0.0117	3	00000000 11
0.0260–0.0325	0.0171–0.0214	0.0117–0.0146	4	00000001 00
0.0325–0.0390	0.0214–0.0257	0.0146–0.0175	5	00000001 01
0.0390–0.0455	0.0257–0.0300	0.0175–0.0205	6	00000001 10
0.0455–0.0521	0.0300–0.0343	0.0205–0.0234	7	00000001 11
0.0521–0.0586	0.0343–0.0386	0.0234–0.0263	8	00000010 00
			.	
			.	
			.	
1.6675–1.6740	1.100–1.1042	0.7500–0.7529	256 (1/4-scale)	01000000 00
			.	
			.	
			.	
3.330–3.3415	2.200–2.2042	1.5000–1.5029	512 (1/2-scale)	10000000 00
			.	
			.	
			.	
5.0025–5.0090	3.300–3.3042	2.2500–2.2529	768 (3/4 scale)	11000000 00
			.	
			.	
			.	
6.5983–6.6048	4.3527–4.3570	2.9677–2.9707	1013	11111101 01
6.6048–6.6113	4.3570–4.3613	2.9707–2.9736	1014	11111101 10
6.6113–6.6178	4.3613–4.3656	2.9736–2.9765	1015	11111101 11
6.6178–6.6244	4.3656–4.3699	2.9765–2.9794	1016	11111110 00
6.6244–6.6309	4.3699–4.3742	2.9794–2.9824	1017	11111110 01
6.6309–6.6374	4.3742–4.3785	2.9824–2.9853	1018	11111110 10
6.6374–6.4390	4.3785–4.3828	2.9853–2.9882	1019	11111110 11
6.6439–6.6504	4.3828–4.3871	2.9882–2.9912	1020	11111111 00
6.6504–6.6569	4.3871–4.3914	2.9912–2.9941	1021	11111111 01
6.6569–6.6634	4.3914–4.3957	2.9941–2.9970	1022	11111111 10
>6.6634	>4.3957	>2.9970	1023	11111111 11

TEMPERATURE MEASUREMENT METHOD

A simple method of measuring temperature is to exploit the negative temperature coefficient of a diode, measuring the base-emitter voltage (V_{BE}) of a transistor, operated at constant current. Unfortunately, this technique requires calibration to null out the effect of the absolute value of V_{BE} , which varies from device to device.

The technique used in the ADT7467 is to measure the change in V_{BE} when the device is operated at three different currents. Previous devices have used only two operating currents, but the use of a third current allows automatic cancellation of resistances in series with the external temperature sensor.

Figure 24 shows the input signal conditioning used to measure the output of an external temperature sensor. This figure shows the external sensor as a substrate transistor, but it could equally be a discrete transistor. If a discrete transistor is used, the collector is not grounded and should be linked to the base. To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode at the D– input. C1 can optionally be added as a noise filter (recommended maximum value 1000 pF). However, a better option in noisy environments is to add a filter, as described in the Noise Filtering section.

Local Temperature Measurement

The ADT7467 contains an on-chip band gap temperature sensor whose output is digitized by the on-chip 10-bit ADC. The 8-bit MSB temperature data is stored in the local temperature register (Address 26h). Because both positive and negative temperatures can be measured, the temperature data is stored in Offset 64 format or twos complement format, as shown in Table 6 and Table 7. Theoretically, the temperature sensor and ADC can measure temperatures from -128°C to $+127^{\circ}\text{C}$ (or -61°C to $+191^{\circ}\text{C}$ in the extended temperature range) with a resolution of 0.25°C . However, this exceeds the operating temperature range of the device, so local temperature measurements outside the ADT7467 operating temperature range are not possible.

Remote Temperature Measurement

The ADT7467 can measure the temperature of two remote diode sensors or diode-connected transistors connected to Pins 10 and 11, or 12 and 13.

The forward voltage of a diode or diode-connected transistor operated at a constant current exhibits a negative temperature coefficient of about $-2\text{ mV}/^{\circ}\text{C}$. Unfortunately, the absolute value of V_{BE} varies from device to device and individual calibration is required to null this out, so the technique is unsuitable for mass production. The technique used in the ADT7467 is to measure the change in V_{BE} when the device is operated at three different currents. This is given by

$$\Delta V_{\text{BE}} = KT / q \times \ln(N)$$

where:

K is Boltzmann's constant.

q is the charge on the carrier.

T is the absolute temperature in Kelvin.

N is the ratio of the two currents.

Figure 23 shows the input signal conditioning used to measure the output of a remote temperature sensor. This figure shows the external sensor as a substrate transistor, provided for temperature monitoring on some microprocessors. It could also be a discrete transistor such as a 2N3904/2N3906.

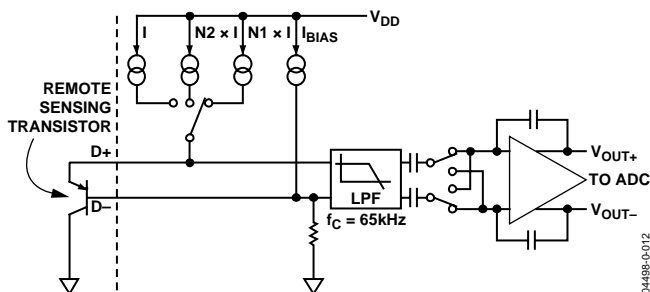


Figure 23. Signal Conditioning for Remote Diode Temperature Sensors

If a discrete transistor is used, the collector is not grounded and should be linked to the base. If a PNP transistor is used, the base is connected to the D- input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D- input and the base to the D+ input. Figure 25 and Figure 26 show how to connect the ADT7467 to an NPN or PNP transistor for temperature measurement. To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode at the D- input.

To measure ΔV_{BE} , the operating current through the sensor is switched among three related currents. Shown in Figure 23, $N1 \times I$ and $N2 \times I$ are different multiples of the current I . The currents through the temperature diode are switched between I and $N1 \times I$, giving $\Delta V_{\text{BE}1}$, and then between I and $N2 \times I$, giving $\Delta V_{\text{BE}2}$. The temperature can then be calculated using the two ΔV_{BE} measurements. This method can also cancel the effect of any series resistance on the temperature measurement.

The resulting ΔV_{BE} waveforms are passed through a 65 kHz low-pass filter to remove noise and then to a chopper-stabilized amplifier. This amplifies and rectifies the waveform to produce a dc voltage proportional to ΔV_{BE} . The ADC digitizes this voltage, and a temperature measurement is produced. To reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles.

The results of remote temperature measurements are stored in 10-bit, twos complement format, as listed in Table 6. The extra resolution for the temperature measurements is held in the Extended Resolution Register 2 (Reg. 0x77). This gives temperature readings with a resolution of 0.25°C .

Noise Filtering

For temperature sensors operating in noisy environments, previous practice was to place a capacitor across the D+ and D- pins to help combat the effects of noise. However, large capacitances affect the accuracy of the temperature measurement, leading to a recommended maximum capacitor value of 1000 pF. This capacitor reduces the noise, but does not eliminate it, making use of the sensor difficult in a very noisy environment.

The ADT7467 has a major advantage over other devices for eliminating the effects of noise on the external sensor. Using the series resistance cancellation feature, a filter can be constructed between the external temperature sensor and the part. The effect of any filter resistance seen in series with the remote sensor is automatically canceled from the temperature result.

The construction of a filter allows the ADT7467 and the remote temperature sensor to operate in noisy environments. Figure 24 shows a low-pass R-C-R filter, with the following values:

$$R = 100 \Omega, C = 1 \text{ nF}$$

This filtering reduces both common-mode noise and differential noise.

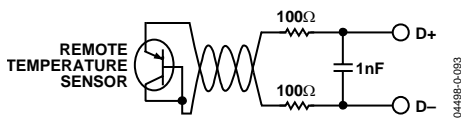


Figure 24. Filter between Remote Sensor and ADT7467

SERIES RESISTANCE CANCELLATION

Parasitic resistance to the ADT7467 D+ and D- inputs (seen in series with the remote diode) is caused by a variety of factors including PCB track resistance and track length. This series resistance appears as a temperature offset in the remote sensor's temperature measurement. This error typically causes a 0.5°C offset per 1 Ω of parasitic resistance in series with the remote diode.

The ADT7467 automatically cancels out the effect of this series resistance on the temperature reading, giving a more accurate result without the need for user characterization of this resistance. The ADT7467 is designed to automatically cancel, typically, up to 3 kΩ of resistance. By using an advanced temperature measurement method, this is transparent to the user. This feature allows resistances to be added to the sensor path to produce a filter, allowing the part to be used in noisy environments. See the Noise Filtering section for details.

FACTORS AFFECTING DIODE ACCURACY

Remote Sensing Diode

The ADT7467 is designed to work with either substrate transistors built into processors or discrete transistors. Substrate transistors are generally PNP types with the collector connected to the substrate. Discrete types can be either PNP or NPN transistors connected as a diode (base-shortened to the collector). If an NPN transistor is used, the collector and base are connected to D+ and the emitter is connected to D-. If a PNP transistor is used, the collector and base are connected to D- and the emitter is connected to D+.

To reduce the error due to variations in both substrate and discrete transistors, a number of factors should be taken into consideration:

- The ideality factor, n_f , of the transistor is a measure of the deviation of the thermal diode from ideal behavior. The ADT7467 is trimmed for an n_f value of 1.008. Use the following equation to calculate the error introduced at a temperature T (°C), when using a transistor whose n_f does not equal 1.008. See the processor data sheet for the n_f values.

$$\Delta T = (n_f - 1.008) / 1.008 \times (273.15 \text{ K} + T)$$

To factor this in, the user can write the ΔT value to the offset register. The ADT7467 then automatically adds it to or subtracts it from the temperature measurement.

- Some CPU manufacturers specify the high and low current levels of the substrate transistors. The high current level of the ADT7467, I_{HIGH} , is 96 μA and the low level current, I_{LOW} , is 6 μA. If the ADT7467 current levels do not match the current levels specified by the CPU manufacturer, it might be necessary to remove an offset. The CPU's data sheet advises whether this offset needs to be removed and how to calculate it. This offset can be programmed to the offset register. It is important to note that, if more than one offset must be considered, the algebraic sum of these offsets must be programmed to the offset register.

If a discrete transistor is used with the ADT7467, the best accuracy is obtained by choosing devices according to the following criteria:

- Base-emitter voltage greater than 0.25 V at 6 μA, at the highest operating temperature.
- Base-emitter voltage less than 0.95 V at 100 μA, at the lowest operating temperature.
- Base resistance less than 100 Ω.
- Small variation in h_{FE} (say 50 to 150) that indicates tight control of V_{BE} characteristics.

Transistors, such as 2N3904, 2N3906, or equivalents in SOT-23 packages, are suitable devices to use.

ADT7467

Table 6. Temperature Data Format

Temperature	Digital Output (10-Bit) ¹
-128°C	1000 0000 00
-125°C	1000 0011 00
-100°C	1001 1100 00
-75°C	1011 0101 00
-50°C	1100 1110 00
-25°C	1110 0111 00
-10°C	1111 0110 00
0°C	0000 0000 00
10.25°C	0000 1010 01
25.5°C	0001 1001 10
50.75°C	0011 0010 11
75°C	0100 1011 00
100°C	0110 0100 00
125°C	0111 1101 00
127°C	0111 1111 00

¹Bold numbers denote 2 LSB of measurement in Extended Resolution Register 2 (Reg. 0x77) with 0.25°C resolution.

Table 7. Extended Range, Temperature Data Format

Temperature	Digital Output (10-Bit) ¹
-64°C	0000 0000 00
-1°C	0011 1111 00
0°C	0100 0000 00
1°C	0100 0001 00
10°C	0100 1010 00
25°C	0101 1001 00
50°C	0111 0010 00
75°C	1000 1001 00
100°C	1010 0100 00
125°C	1011 1101 00
191°C	1111 1111 00

¹ Bold numbers denote 2 LSB of measurement in Extended Resolution Register 2 (Reg. 0x77) with 0.25°C resolution.

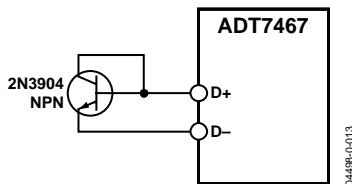


Figure 25. Measuring Temperature Using an NPN Transistor

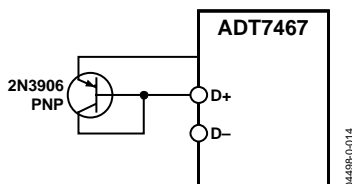


Figure 26. Measuring Temperature Using a PNP Transistor

Nulling Out Temperature Errors

As CPUs run faster, it is getting more difficult to avoid high frequency clocks when routing the D+/D- traces around a system board. Even when recommended layout guidelines are followed, some temperature errors may still be attributable to noise coupled onto the D+/D- lines. Constant high frequency noise usually attenuates or increases temperature measurements by a linear, constant value.

The ADT7467 has temperature offset registers at Addresses 0x70, 0x72 for the Remote 1 and Remote 2 temperature channels. By doing a one-time calibration of the system, the user can determine the offset caused by system board noise and null it out using the offset registers. The offset registers automatically add an Offset 64/twos complement 8-bit reading to every temperature measurement. The LSBs add 0.5°C offset to the temperature reading so the 8-bit register effectively allows temperature offsets of up to ±64°C with a resolution of 0.5°C. This ensures that the readings in the temperature measurement registers are as accurate as possible.

Temperature Offset Registers

Reg. 0x70 **Remote 1 Temperature Offset** = 0x00 (0°C default)

Reg. 0x71 **Local Temperature Offset** = 0x00 (0°C default)

Reg. 0x72 **Remote 2 Temperature Offset** = 0x00 (0°C default)

ADT7460/ADT7467 Backwards Compatible Mode

By setting Bit 1 of Configuration Register 5 (0x7C), all temperature measurements are stored in the Zone Temp value registers (0x25, 0x26, and 0x27) in twos complement in the range -64°C to +127°C. (The ADT7468 still makes calculations based on the Offset64 extended range and clamps the results, if necessary.) The temperature limits must be reprogrammed in twos complement. If a twos complement temperature below -63°C is entered, the temperature is clamped to -63°C. In this mode, the diode fault condition remains -128°C = 1000 0000, while in the extended temperature range (-64°C to +191°C), the fault condition is represented by -64°C = 0000 0000.

Temperature Measurement Registers

Reg. 0x25 **Remote 1 Temperature**

Reg. 0x26 **Local Temperature**

Reg. 0x27 **Remote 2 Temperature**

Reg. 0x77 **Extended Resolution 2** = 0x00 default

<7:6> **TDM2**, Remote 2 temperature LSBs.

<5:4> **LTMP**, local temperature LSBs.

<3:2> **TDM1**, Remote 1 temperature LSBs.

Temperature Measurement Limit Registers

Associated with each temperature measurement channel are high and low limit registers. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate SMBALERT interrupts.

Reg. 0x4E **Remote 1 Temperature Low Limit** = 0x01 default

Reg. 0x4F **Remote 1 Temperature High Limit** = 0x7F default

Reg. 0x50 **Local Temperature Low Limit** = 0x01 default

Reg. 0x51 **Local Temperature High Limit** = 0x7F default

Reg. 0x52 **Remote 2 Temperature Low Limit** = 0x01 default

Reg. 0x53 **Remote 2 Temperature High Limit** = 0x7F default

Reading Temperature from the ADT7467

It is important to note that temperature can be read from the ADT7467 as an 8-bit value (with 1°C resolution) or as a 10-bit value (with 0.25°C resolution). If only 1°C resolution is required, the temperature readings can be read back at any time and in no particular order.

If the 10-bit measurement is required, this involves a 2-register read for each measurement. The extended resolution register (Reg. 0x77) should be read first. This causes all temperature reading registers to be frozen until all temperature reading registers have been read from. This prevents an MSB reading from being updated while its two LSBs are being read and vice versa.

ADDITIONAL ADC FUNCTIONS FOR TEMPERATURE MEASUREMENT

A number of other functions are available on the ADT7467 to offer the system designer increased flexibility.

Turn-Off Averaging

For each temperature measurement read from a value register, 16 readings have actually been made internally and the results averaged before being placed into the value register. Sometimes it is necessary to take a very fast measurement. Setting Bit 4 of Configuration Register 2 (Reg. 0x73) turns averaging off.

Table 8. Conversion Time with Averaging Disabled

Channel	Measurement Time
Voltage Channel	0.7 ms
Remote Temperature 1	7 ms
Remote Temperature 2	7 ms
Local Temperature	1.3 ms

Table 9. Conversion Time with Averaging Enabled

Channel	Measurement Time
Voltage Channels	11 ms
Remote Temperature	39 ms
Local Temperature	12 ms

Single-Channel ADC Conversions

Setting Bit 6 of Configuration Register 2 (Reg. 0x73) places the ADT7467 into single-channel ADC conversion mode. In this mode, the ADT7467 can be made to read a single temperature channel only. The appropriate ADC channel is selected by writing to Bits <7:5> of the TACH1 minimum high byte register (0x55).

Table 10. Channel Selection

Bits <7:5> Reg. 0x55	Channel Selected
101	Remote 1 temperature
110	Local temperature
111	Remote 2 temperature

Configuration Register 2 (Reg. 0x73)

<4> = 1, averaging off.

<6> = 1, single-channel convert mode,

TACH1 Minimum High Byte (Reg. 0x55)

<7:5> selects ADC channel for single-channel convert mode.

Overtemperature Events

Overtemperature events on any of the temperature channels can be detected and dealt with automatically in automatic fan speed control mode. Reg. 0x6A to Reg. 0x6C are the THERM temperature limits. When a temperature exceeds its THERM temperature limit, all PWM outputs run at the maximum PWM duty cycle (Reg. 0x38, Reg. 0x39, Reg. 0x3A). This effectively runs the fans at the fastest allowed speed. The fans stay running at this speed until the temperature drops below THERM minus hysteresis. (This can be disabled by setting the boost bit in Configuration Register 3, Bit 2, Reg. 0x78.) The hysteresis value for that THERM temperature limit is the value programmed into Reg. 0x6D and Reg. 0x6E (hysteresis registers). The default hysteresis value is 4°C.

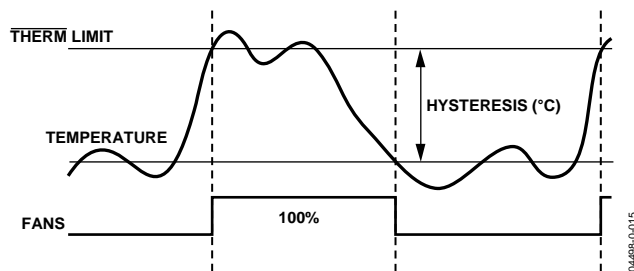


Figure 27. THERM Temperature Limit Operation

LIMITS, STATUS REGISTERS, AND INTERRUPTS

LIMIT VALUES

Associated with each measurement channel on the ADT7467 are high and low limits. These can form the basis of system status monitoring; a status bit can be set for any out-of-limit condition and detected by polling the device. Alternatively, SMBALERT interrupts can be generated to flag a processor or microcontroller of out-of-limit conditions.

8-Bit Limits

The following is a list of 8-bit limits on the ADT7467.

Voltage Limit Registers

Reg. 0x46 V_{CCP} **Low Limit** = 0x00 default

Reg. 0x47 V_{CCP} **High Limit** = 0xFF default

Reg. 0x48 V_{CC} **Low Limit** = 0x00 default

Reg. 0x49 V_{CC} **High Limit** = 0xFF default

Temperature Limit Registers

Reg. 0x4E **Remote 1 Temperature Low Limit** = 0x01 default

Reg. 0x4F **Remote 1 Temperature High Limit** = 0x7F default

Reg. 0x6A **Remote 1 $\overline{\text{THERM}}$ Limit** = 0x64 default

Reg. 0x50 **Local Temperature Low Limit** = 0x01 default

Reg. 0x51 **Local Temperature High Limit** = 0x7F default

Reg. 0x6B **Local $\overline{\text{THERM}}$ Limit** = 0x64 default

Reg. 0x52 **Remote 2 Temperature Low Limit** = 0x01 default

Reg. 0x53 **Remote 2 Temperature High Limit** = 0x7F default

Reg. 0x6C **Remote 2 $\overline{\text{THERM}}$ Limit** = 0x64 default

$\overline{\text{THERM}}$ Limit Register

Reg. 0x7A $\overline{\text{THERM}}$ **Limit** = 0x00 default

16-Bit Limits

The fan TACH measurements are 16-bit results. The fan TACH limits are also 16 bits, consisting of a high byte and low byte. Because fans running under speed or stalled are normally the only conditions of interest, only high limits exist for fan TACHs. Because the fan TACH period is actually being measured, exceeding the limit indicates a slow or stalled fan.

Fan Limit Registers

Reg. 0x54 **TACH1 Minimum Low Byte** = 0x00 default

Reg. 0x55 **TACH1 Minimum High Byte** = 0x00 default

Reg. 0x56 **TACH2 Minimum Low Byte** = 0x00 default

Reg. 0x57 **TACH2 Minimum High Byte** = 0x00 default

Reg. 0x58 **TACH3 Minimum Low Byte** = 0x00 default

Reg. 0x59 **TACH3 Minimum High Byte** = 0x00 default

Reg. 0x5A **TACH4 Minimum Low Byte** = 0x00 default

Reg. 0x5B **TACH4 Minimum High Byte** = 0x00 default

Out-of-Limit Comparisons

Once all limits have been programmed, the ADT7467 can be enabled for monitoring. The ADT7467 measures all voltage and temperature measurements in round-robin format and sets the appropriate status bit for out-of-limit conditions. TACH measurements are not part of this round-robin cycle. Comparisons are done differently depending on whether the measured value is being compared to a high or low limit.

High Limit: > Comparison Performed

Low Limit: \leq Comparison Performed

Voltage and temperature channels use a window comparator for error detecting and, therefore, have high and low limits. Fan speed measurements use only a low limit. This fan limit is needed only in manual fan control mode.

Analog Monitoring Cycle Time

The analog monitoring cycle begins when a 1 is written to the start bit (Bit 0) of Configuration Register 1 (Reg. 0x40). By default, the ADT7463 powers up with this bit set. The ADC measures each analog input in turn and, as each measurement is completed, the result is automatically stored in the appropriate value register. This round-robin monitoring cycle continues unless disabled by writing a 0 to Bit 0 of Configuration Register 1.

As the ADC is normally left to free-run in this manner, the time taken to monitor all the analog inputs is normally not of interest, because the most recently measured value of any input can be read out at any time.

For applications where the monitoring cycle time is important, it can easily be calculated. The total number of channels measured is

- One dedicated supply voltage input (V_{CCP})
- Supply voltage (V_{CC} pin)
- Local temperature
- Two remote temperatures

As mentioned previously, the ADC performs round-robin conversions. The total monitoring cycle time for averaged voltage and temperature monitoring is 145 ms. The total monitoring cycle time for voltage and temperature monitoring with averaging disabled is 19 ms. The ADT7467 is a derivative of the ADT7468. As a result, the total conversion time in the ADT7467 is the same as the total conversion time of the ADT7468, even though the ADT7467 has less monitored channels.

Fan TACH measurements are made in parallel and are not synchronized with the analog measurements in any way.

STATUS REGISTERS

The results of limit comparisons are stored in Status Registers 1 and 2. The status register bit for each channel reflects the status of the last measurement and limit comparison on that channel. If a measurement is within limits, the corresponding status register bit is cleared to 0. If the measurement is out-of-limits, the corresponding status register bit is set to 1.

The state of the various measurement channels can be polled by reading the status registers over the serial bus. In Bit 7 (OOL) of Status Register 1 (Reg. 0x41), 1 means that an out-of-limit event has been flagged in Status Register 2. This means that the user also needs to read Status Register 2. Alternatively, Pin 5 or Pin 9 can be configured as an $\overline{\text{SMBALERT}}$ output. This hardware interrupt automatically notifies the system supervisor of an out-of-limit condition. Reading the status registers clears the appropriate status bit as long as the error condition that caused the interrupt has cleared. Status register bits are “sticky.” Whenever a status bit is set, indicating an out-of-limit condition, it remains set even if the event that caused it has gone away (until read). The only way to clear the status bit is to read the status register after the event has gone away. Interrupt status mask registers (Reg. 0x74, 0x75) allow individual interrupt sources to be masked from causing an $\overline{\text{SMBALERT}}$. However, if one of these masked interrupt sources goes out-of-limit, its associated status bit is set in the interrupt status registers.

Status Register 1 (Reg. 0x41)

Bit 7 (OOL) = 1, denotes a bit in Status Register 2 is set and Status Register 2 should be read.

Bit 6 (R2T) = 1, Remote 2 temperature high or low limit has been exceeded.

Bit 5 (LT) = 1, local temperature high or low limit has been exceeded.

Bit 4 (R1T) = 1, Remote 1 temperature high or low limit has been exceeded.

Bit 2 (V_{CC}) = 1, V_{CC} high or low limit has been exceeded.

Bit 1 (V_{CCP}) = 1, V_{CCP} high or low limit has been exceeded.

Status Register 2 (Reg. 0x42)

Bit 7 (D2) = 1, indicates an open or short on D2+/D2- inputs.

Bit 6 (D1) = 1, indicates an open or short on D1+/D1- inputs.

Bit 5 (F4P) = 1, indicates Fan 4 has dropped below minimum speed. Alternatively, indicates that the THERM limit has been exceeded, if the THERM function is used.

Bit 4 (FAN3) = 1, indicates Fan 3 has dropped below minimum speed.

Bit 3 (FAN2) = 1, indicates Fan 2 has dropped below minimum speed.

Bit 2 (FAN1) = 1, indicates Fan 1 has dropped below minimum speed.

Bit 1 (OVT) = 1, indicates a THERM overtemperature limit has been exceeded.

$\overline{\text{SMBALERT}}$ Interrupt Behavior

The ADT7467 can be polled for status, or an $\overline{\text{SMBALERT}}$ interrupt can be generated for out-of-limit conditions. It is important to note how the $\overline{\text{SMBALERT}}$ output and status bits behave when writing interrupt handler software.

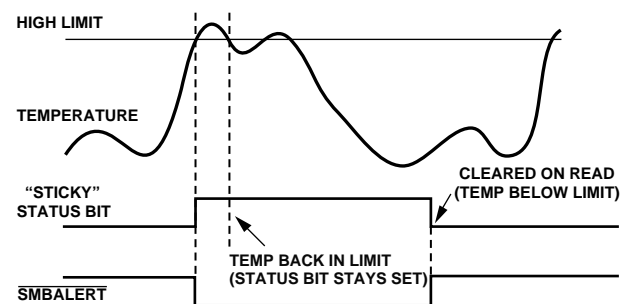


Figure 28. $\overline{\text{SMBALERT}}$ and Status Bit Behavior

Figure 28 shows how the $\overline{\text{SMBALERT}}$ output and “sticky” status bits behave. Once a limit is exceeded, the corresponding status bit is set to 1. The status bit remains set until the error condition subsides and the status register is read. The status bits are referred to as “sticky,” because they remain set until read by software. This ensures that an out-of-limit event cannot be missed, if software is polling the device periodically. Note that the $\overline{\text{SMBALERT}}$ output remains low for the entire duration that a reading is out-of-limit and until the status register has been read. This has implications on how software handles the interrupt.

Handling $\overline{\text{SMBALERT}}$ Interrupts

To prevent the system from being tied up servicing interrupts, it is recommended to handle the $\overline{\text{SMBALERT}}$ interrupt as follows:

1. Detect the $\overline{\text{SMBALERT}}$ assertion.
2. Enter the interrupt handler.
3. Read the status registers to identify the interrupt source.
4. Mask the interrupt source by setting the appropriate mask bit in the interrupt mask registers (Reg. 0x74, Reg. 0x75).
5. Take the appropriate action for a given interrupt source.
6. Exit the interrupt handler.
7. Periodically poll the status registers. If the interrupt status bit has cleared, reset the corresponding interrupt mask bit to 0. This causes the $\overline{\text{SMBALERT}}$ output and status bits to behave as shown in Figure 29.

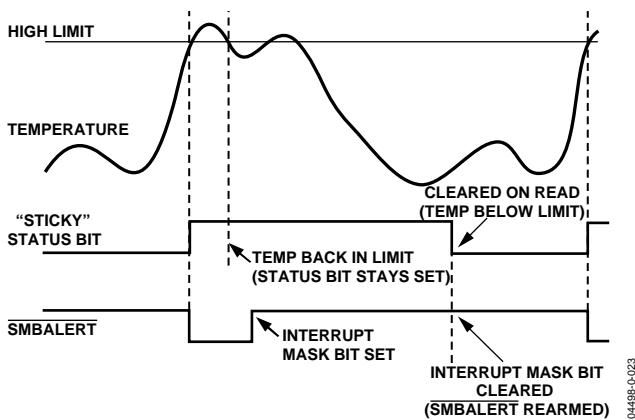


Figure 29. How Masking the Interrupt Source Affects $\overline{\text{SMBALERT}}$ Output

Masking Interrupt Sources

Interrupt Mask Registers 1 and 2 are located at Addresses 0x74 and 0x75. These allow individual interrupt sources to be masked out to prevent $\overline{\text{SMBALERT}}$ interrupts. Note that masking an interrupt source prevents only the $\overline{\text{SMBALERT}}$ output from being asserted; the appropriate status bit is set normally.

Interrupt Mask Register 1 (Reg. 0x74)

- Bit 7 (OOL) = 1**, masks $\overline{\text{SMBALERT}}$ for any alert condition flagged in Status Register 2.
- Bit 6 (R2T) = 1**, masks $\overline{\text{SMBALERT}}$ for Remote 2 temperature.
- Bit 5 (LT) = 1**, masks $\overline{\text{SMBALERT}}$ for local temperature.
- Bit 4 (R1T) = 1**, masks $\overline{\text{SMBALERT}}$ for Remote 1 temperature.

Bit 2 (V_{CC}) = 1, masks $\overline{\text{SMBALERT}}$ for V_{CC} channel.

Bit 0 (V_{CCP}) = 1, masks $\overline{\text{SMBALERT}}$ for V_{CCP} channel.

Interrupt Mask Register 2 (Reg. 0x75)

Bit 7 (D2) = 1, masks $\overline{\text{SMBALERT}}$ for Diode 2 errors.

Bit 6 (D1) = 1, masks $\overline{\text{SMBALERT}}$ for Diode 1 errors.

Bit 5 (FAN4) = 1, masks $\overline{\text{SMBALERT}}$ for Fan 4 failure.

If the TACH4 pin is being used as the $\overline{\text{THERM}}$ input, this bit masks $\overline{\text{SMBALERT}}$ for a $\overline{\text{THERM}}$ event.

Bit 4 (FAN3) = 1, masks $\overline{\text{SMBALERT}}$ for Fan 3.

Bit 3 (FAN2) = 1, masks $\overline{\text{SMBALERT}}$ for Fan 2.

Bit 2 (FAN1) = 1, masks $\overline{\text{SMBALERT}}$ for Fan 1.

Bit 1 (OVT) = 1, masks $\overline{\text{SMBALERT}}$ for overtemperature (exceeding $\overline{\text{THERM}}$ temperature limits).

Enabling the $\overline{\text{SMBALERT}}$ Interrupt Output

The $\overline{\text{SMBALERT}}$ interrupt function is disabled by default. Pin 5 or Pin 9 can be reconfigured as an $\overline{\text{SMBALERT}}$ output to signal out-of-limit conditions.

Table 11. Configuring Pin 5 as $\overline{\text{SMBALERT}}$ Output

Register	Bit Setting
Configuration Register 3 (Reg. 0x78)	<0> ALERT = 1

Assigning $\overline{\text{THERM}}$ Functionality to a Pin

Pin 9 on the ADT7467 has four possible functions: SMBus ALERT, $\overline{\text{THERM}}$, GPIO, and TACH4. The user chooses the required functionality by setting Bit 0 and Bit 1 of Configuration Register 4 at Address 0x7D.

Table 12. Configuring Pin 9

Bit 0	Bit 1	Function
00		TACH4
01		$\overline{\text{THERM}}$
10		SMBus ALERT
11		GPIO

Once Pin 9 is configured as $\overline{\text{THERM}}$, it must be enabled (Bit 1, Configuration Register 3 at Address 0x78).

$\overline{\text{THERM}}$ as an Input

When $\overline{\text{THERM}}$ is configured as an input, the user can time assertions on the $\overline{\text{THERM}}$ pin. This can be useful for connecting to the PROCHOT output of a CPU to gauge system performance.

The user can also set up the ADT7467 so that, when the $\overline{\text{THERM}}$ pin is driven low externally, the fans run at 100%. The fans run at 100% for the duration of the time that the $\overline{\text{THERM}}$ pin is pulled low. This is done by setting the BOOST bit (Bit 2) in Configuration Register 3 (Address = 0x78) to 1. This works only if the fan is already running, for example, in manual mode when the current duty cycle is above 0x00, or in automatic mode when the temperature is above T_{MIN} . If the temperature is below T_{MIN} or if the duty cycle in manual mode is set to 0x00, then pulling the $\overline{\text{THERM}}$ low externally has no effect. See Figure 30 for more information.

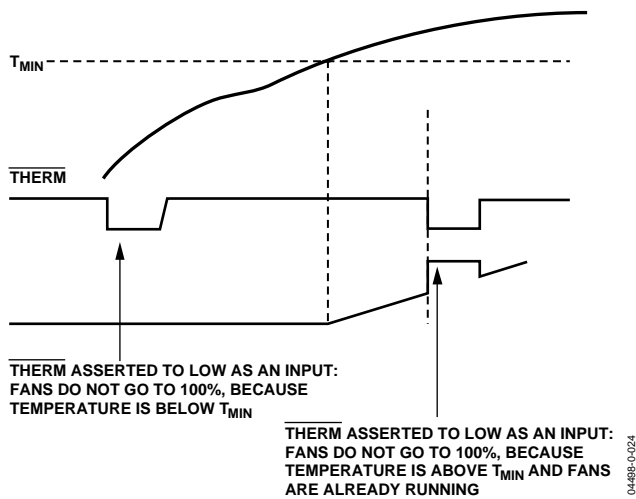


Figure 30. Asserting $\overline{\text{THERM}}$ Low as an Input in Automatic Fan Speed Control Mode

THERM TIMER

The ADT7467 has an internal timer to measure $\overline{\text{THERM}}$ assertion time. For example, the $\overline{\text{THERM}}$ input can be connected to the PROCHOT output of a Pentium 4 CPU to measure system performance. The $\overline{\text{THERM}}$ input can also be connected to the output of a trip point temperature sensor.

The timer is started on the assertion of the ADT7467's $\overline{\text{THERM}}$ input and stopped when $\overline{\text{THERM}}$ is unasserted. The timer counts $\overline{\text{THERM}}$ times cumulatively, that is, the timer resumes counting on the next $\overline{\text{THERM}}$ assertion. The $\overline{\text{THERM}}$ timer continues to accumulate $\overline{\text{THERM}}$ assertion times until the timer is read (it is cleared on read) or until it reaches full scale. If the counter reaches full scale, it stops at that reading until cleared.

The 8-bit $\overline{\text{THERM}}$ timer register (Reg. 0x79) is designed such that Bit 0 is set to 1 on the first $\overline{\text{THERM}}$ assertion. Once the cumulative $\overline{\text{THERM}}$ assertion time has exceeded 45.52 ms, Bit 1 of the $\overline{\text{THERM}}$ timer is set and Bit 0 now becomes the LSB of the timer with a resolution of 22.76 ms (see Figure 31).

When using the $\overline{\text{THERM}}$ timer, be aware of the following.

After a $\overline{\text{THERM}}$ timer read (Reg. 0x79):

1. The contents of the timer are cleared on read.
2. The F4P bit (Bit 5) of Status Register 2 needs to be cleared (assuming that the $\overline{\text{THERM}}$ timer limit has been exceeded).

If the $\overline{\text{THERM}}$ timer is read during a $\overline{\text{THERM}}$ assertion, then the following happens:

1. The contents of the timer are cleared.
2. Bit 0 of the $\overline{\text{THERM}}$ timer is set to 1 (because a $\overline{\text{THERM}}$ assertion is occurring).
3. The $\overline{\text{THERM}}$ timer increments from zero.
4. If the $\overline{\text{THERM}}$ timer limit (Reg. 0x7A) = 0x00, then the F4P bit is set.

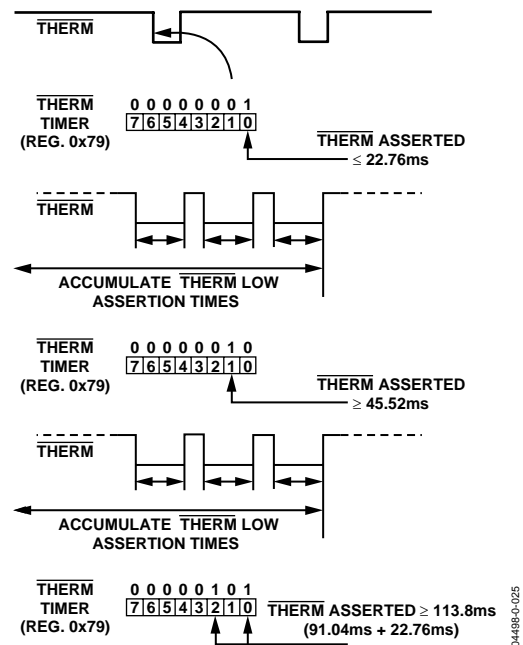


Figure 31. Understanding the $\overline{\text{THERM}}$ Timer

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Generating SMBALERT Interrupts from THERM Timer Events

The ADT7467 can generate SMBALERTs when a programmable THERM timer limit has been exceeded. This allows the system designer to ignore brief, infrequent THERM assertions, while capturing longer THERM timer events. Register 0x7A is the THERM timer limit register. This 8-bit register allows a limit from 0 s (first THERM assertion) to 5.825 s to be set before an SMBALERT is generated. The THERM timer value is compared with the contents of the THERM timer limit register. If the THERM timer value exceeds the THERM timer limit

value, then the F4P bit (Bit 5) of Status Register 2 is set, and an SMBALERT is generated. Note that the F4P bit (Bit 5) of Mask Register 2 (Reg. 0x75) masks out SMBALERTs, if this bit is set to 1; although the F4P bit of Interrupt Status Register 2 still is set, if the THERM timer limit is exceeded.

Figure 32 is a functional block diagram of the THERM timer, limit, and associated circuitry. Writing a value of 0x00 to the THERM timer limit register (Reg. 0x7A) causes SMBALERT to be generated on the first THERM assertion. A THERM timer limit value of 0x01 generates an SMBALERT, once cumulative THERM assertions exceed 45.52 ms.

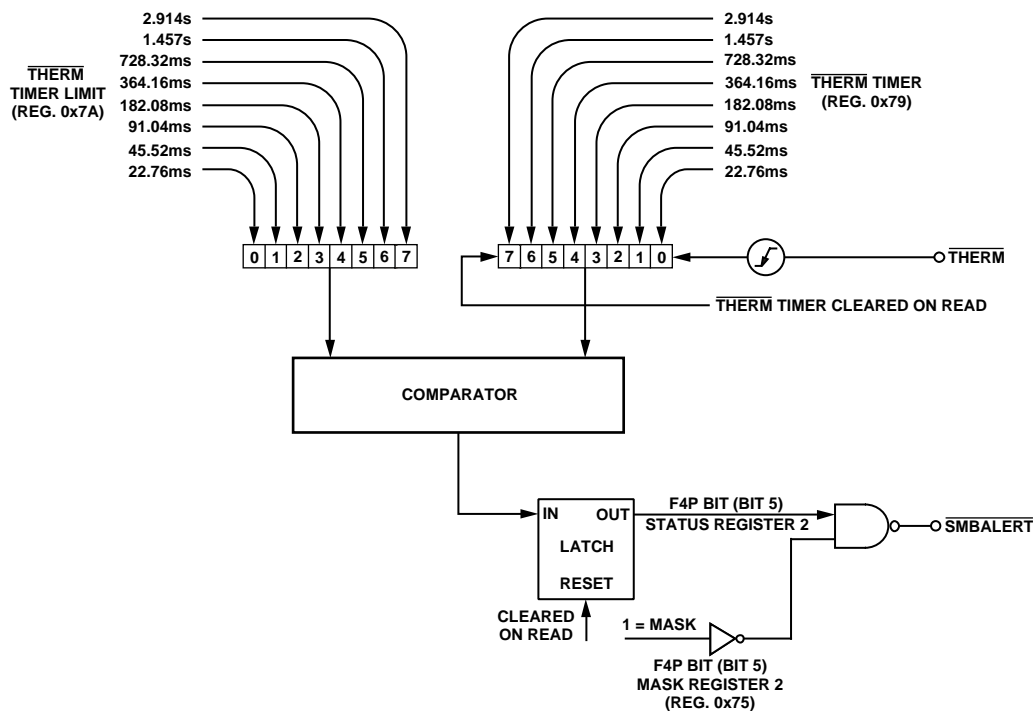


Figure 32. Functional Block Diagram of ADT7467's THERM Monitoring Circuitry

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Configuring the $\overline{\text{THERM}}$ Behavior

1. Configure the relevant pin as the $\overline{\text{THERM}}$ timer input.

Setting Bit 1 ($\overline{\text{THERM}}$ timer enable) of Configuration Register 3 (Reg. 0x78) enables the $\overline{\text{THERM}}$ timer monitoring functionality. This is disabled on Pin 9 by default.

Setting Bits 0 and 1 (PIN9FUNC) of Configuration Register 4 (Reg. 0x7D) enables $\overline{\text{THERM}}$ timer/output functionality on Pin 9 (Bit 1 of Configuration Register 3, $\overline{\text{THERM}}$, must also be set). Pin 9 can also be used as TACH4.

2. Select the desired fan behavior for $\overline{\text{THERM}}$ timer events.

Assuming that the fans are running, setting Bit 2 (BOOST bit) of Configuration Register 3 (Reg. 0x78) causes all fans to run at 100% duty cycle whenever $\overline{\text{THERM}}$ gets asserted. This allows fail-safe system cooling. If this bit is 0, the fans run at their current settings and are not affected by $\overline{\text{THERM}}$ events. If the fans are not already running when $\overline{\text{THERM}}$ is asserted, the fans do not run to full speed.

3. Select whether $\overline{\text{THERM}}$ timer events should generate SMBALERT interrupts.

Bit 5 (F4P) of Mask Register 2 (Reg. 0x75), when set, masks out SMBALERTs when the $\overline{\text{THERM}}$ timer limit value gets exceeded. This bit should be cleared if SMBALERTs based on $\overline{\text{THERM}}$ events are required.

4. Select a suitable $\overline{\text{THERM}}$ limit value.

This value determines whether an SMBALERT is generated on the first $\overline{\text{THERM}}$ assertion, or only if a cumulative $\overline{\text{THERM}}$ assertion time limit is exceeded. A value of 0x00 causes an SMBALERT to be generated on the first $\overline{\text{THERM}}$ assertion.

5. Select a $\overline{\text{THERM}}$ monitoring time.

This value specifies how often OS or BIOS level software checks the $\overline{\text{THERM}}$ timer. For example, BIOS could read the $\overline{\text{THERM}}$ timer once an hour to determine the cumulative $\overline{\text{THERM}}$ assertion time. If, for example, the total $\overline{\text{THERM}}$ assertion time is <22.76 ms in Hour 1, >182.08 ms in Hour 2, and >5.825 s in Hour 3, this can indicate that system performance is degrading significantly because $\overline{\text{THERM}}$ is asserting more frequently on an hourly basis.

Alternatively, OS or BIOS level software can timestamp when the system is powered on. If an SMBALERT is generated due to the $\overline{\text{THERM}}$ timer limit being exceeded, another timestamp can be taken. The difference in time can be calculated for a fixed $\overline{\text{THERM}}$ timer limit time. For example, if it takes one week for a $\overline{\text{THERM}}$ timer limit of 2.914 s to be exceeded and the next time it takes only 1 hour, then this is an indication of a serious degradation in system performance.

Configuring the $\overline{\text{THERM}}$ Pin as an Output

In addition to monitoring $\overline{\text{THERM}}$ as an input, the ADT7467 can optionally drive $\overline{\text{THERM}}$ low as an output. In cases where $\overline{\text{PROCHOT}}$ is bidirectional, $\overline{\text{THERM}}$ can be used to throttle the processor by asserting $\overline{\text{PROCHOT}}$. The user can preprogram system-critical thermal limits. If the temperature exceeds a thermal limit by 0.25°C, $\overline{\text{THERM}}$ asserts low. If the temperature is still above the thermal limit on the next monitoring cycle, $\overline{\text{THERM}}$ stays low. $\overline{\text{THERM}}$ remains asserted low until the temperature is equal to or below the thermal limit. Because the temperature for that channel is measured only once for every monitoring cycle, after $\overline{\text{THERM}}$ asserts it is guaranteed to remain low for at least one monitoring cycle.

The $\overline{\text{THERM}}$ pin can be configured to assert low, if the Remote 1, local, or Remote 2 $\overline{\text{THERM}}$ temperature limits are exceeded by 0.25°C. The $\overline{\text{THERM}}$ temperature limit registers are at Registers 0x6A, 0x6B, and 0x6C, respectively. Setting Bit 3 of Registers 0x5F, 0x60, and 0x61 enables the $\overline{\text{THERM}}$ output feature for the Remote 1, local, and Remote 2 temperature channels, respectively. Figure 33 shows how the $\overline{\text{THERM}}$ pin asserts low as an output in the event of a critical overtemperature.

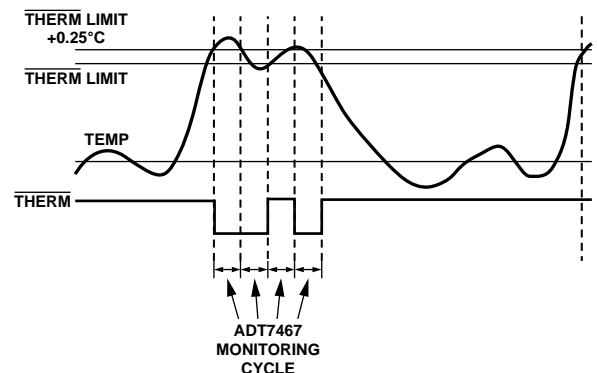


Figure 33. Asserting $\overline{\text{THERM}}$ as an Output, Based on Tripping $\overline{\text{THERM}}$ Limits

An alternative method of disabling $\overline{\text{THERM}}$ is to program the $\overline{\text{THERM}}$ temperature limit to -64°C or less in Offset 64 mode, or -128°C or less in twos complement mode; that is, for $\overline{\text{THERM}}$ temperature limit values less than -63°C or -128°C , respectively, $\overline{\text{THERM}}$ is disabled.

FAN DRIVE USING PWM CONTROL

The ADT7467 uses pulse-width modulation (PWM) to control fan speed. This relies on varying the duty cycle (or on/off ratio) of a square wave applied to the fan to vary the fan speed. The external circuitry required to drive a fan using PWM control is extremely simple. For 4-wire fans, the PWM drive might need only a pull-up resistor. In many cases, the 4-wire fan PWM input has a built-in pull-up resistor.

The ADT7467 PWM frequency can be set to a selection of low frequencies or a single high PWM frequency. The low frequency options are usually used for 2-wire and 3-wire fans, while the high frequency option is usually used with 4-wire fans.

For 2-wire or 3-wire fans, a single N-channel MOSFET is the only drive device required. The specifications of the MOSFET depend on the maximum current required by the fan being driven. Typical notebook fans draw a nominal 170 mA, and so SOT devices can be used where board space is a concern. In desktops, fans can typically draw 250 mA to 300 mA each. If you drive several fans in parallel from a single PWM output or drive larger server fans, the MOSFET must handle the higher current requirements. The only other stipulation is that the MOSFET should have a gate voltage drive, $V_{GS} < 3.3$ V, for direct interfacing to the PWM_OUT pin. V_{GS} can be greater than 3.3 V as long as the pull-up on the gate is tied to 5 V. The MOSFET should also have a low on resistance to ensure that there is not significant voltage drop across the FET, which would reduce the voltage applied across the fan and, therefore, the maximum operating speed of the fan.

Figure 34 shows how to drive a 3-wire fan using PWM control.

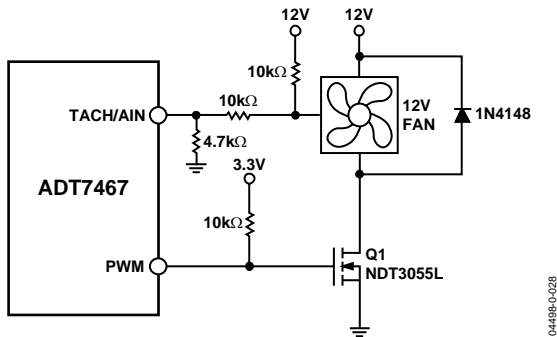


Figure 34. Driving a 3-Wire Fan Using an N-Channel MOSFET

Figure 34 uses a 10 kΩ pull-up resistor for the TACH signal. This assumes that the TACH signal is an open-collector from the fan. In all cases, the TACH signal from the fan must be kept below 5 V maximum to prevent damaging the ADT7467. If in doubt as to whether the fan used has an open-collector or totem pole TACH output, use one of the input signal conditioning circuits shown in the Fan Speed Measurement section.

Figure 35 shows a fan drive circuit using an NPN transistor such as a general-purpose MMBT2222. While these devices are inexpensive, they tend to have much lower current handling capabilities and higher on resistance than MOSFETs. When choosing a transistor, care should be taken to ensure that it meets the fan's current requirements.

Ensure that the base resistor is chosen such that the transistor is saturated when the fan is powered on.

Because 4-wire fans are powered continuously, the fan speed is not switched on or off as with previous PWM driven/powered fans. This enables it to perform better than 3-wire fans, especially for high frequency applications. Figure 36 shows a typical drive circuit for 4-wire fans.

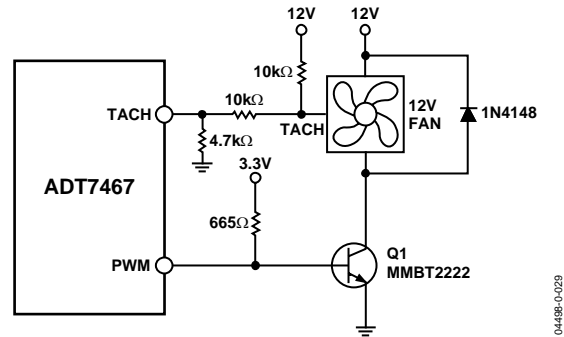


Figure 35. Driving a 3-Wire Fan Using an NPN Transistor

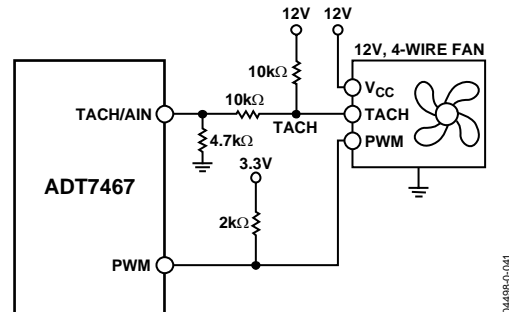


Figure 36. Driving a 4-Wire Fan

Driving Two Fans from PWM3

The ADT7467 has four TACH inputs available for fan speed measurement, but only three PWM drive outputs. If a fourth fan is being used in the system, it should be driven from the PWM3 output in parallel with the third fan. Figure 37 shows how to drive two fans in parallel using low cost NPN transistors. Figure 38 shows the equivalent circuit using a MOSFET.

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Note that when the voltage spikes (either negative going or positive going) are more than 40 mV in amplitude, the fan speed can be reliably determined.

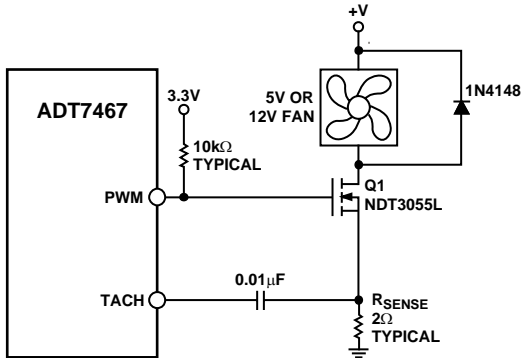


Figure 39. Driving a 2-Wire Fan

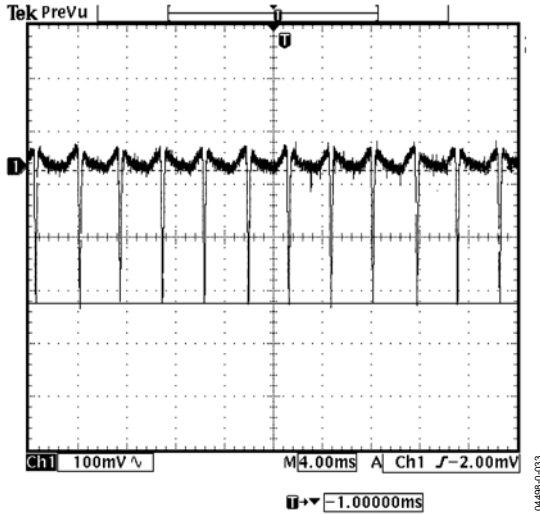


Figure 40. Fan Speed Sensing Waveform at TACH/AIN Pin

LAYING OUT 2-WIRE AND 3-WIRE FANS

Figure 41 shows how to lay out a common circuit arrangement for 2-wire and 3-wire fans. Some components are not populated, depending on whether a 2-wire or 3-wire fan is used.

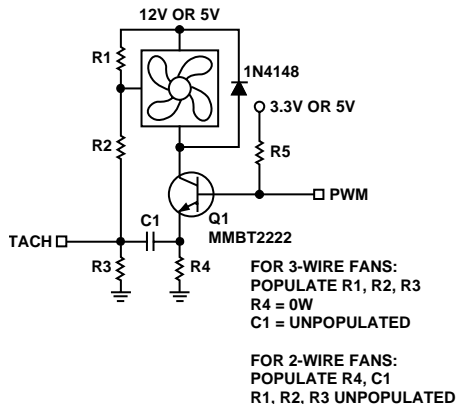


Figure 41. Planning for 2-Wire or 3-Wire Fans on a PCB

TACH Inputs

Pins 4, 6, 7, and 9 (when configured as TACH inputs) are open-drain TACH inputs intended for fan speed measurement.

Signal conditioning in the ADT7467 accommodates the slow rise and fall times typical of fan tachometer outputs. The maximum input signal range is 0 V to 5 V, even when V_{CC} is less than 5 V. In the event that these inputs are supplied from fan outputs that exceed 0 V to 5 V, either resistive attenuation of the fan signal or diode clamping must be included to keep inputs within an acceptable range.

Figure 42 to Figure 45 show circuits for most common fan TACH outputs.

If the fan TACH output has a resistive pull-up to V_{CC} , it can be connected directly to the fan input, as shown in Figure 42.

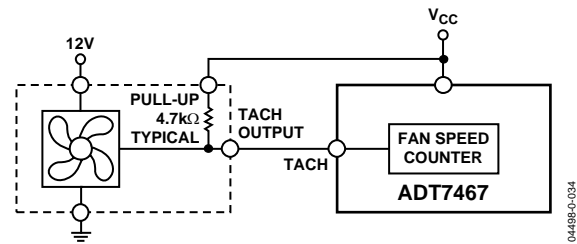


Figure 42. Fan with TACH Pull-Up to V_{CC}

If the fan output has a resistive pull-up to 12 V (or other voltage greater than 5 V) then the fan output can be clamped with a Zener diode, as shown in Figure 43. The Zener diode voltage should be chosen so that it is greater than V_{IH} of the TACH input but less than 5 V, allowing for the voltage tolerance of the Zener. A value of between 3 V and 5 V is suitable.

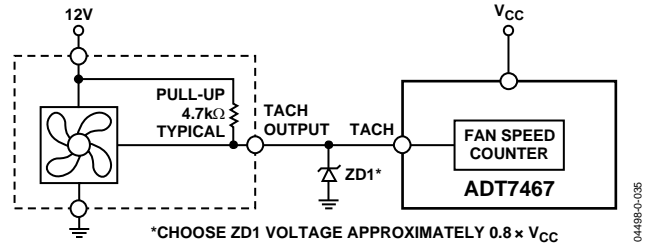


Figure 43. Fan with TACH Pull-Up to Voltage > 5 V. (for example, 12 V) Clamped with Zener Diode

If the fan has a strong pull-up (less than 1 kΩ) to 12 V or a totem-pole output, then a series resistor can be added to limit the Zener current, as shown in Figure 44.

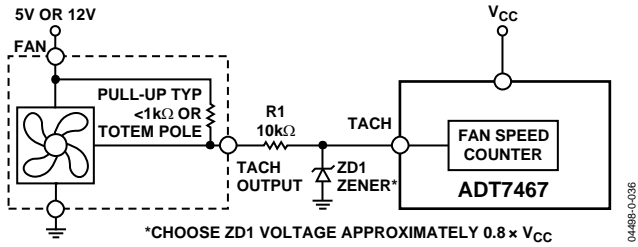


Figure 44. Fan with Strong TACH Pull-Up to $> V_{CC}$ or Totem-Pole Output, Clamped with Zener and Resistor

$$2V < V_{PULL-UP} \times R2 / (R_{PULL-UP} + R1 + R2) < 5V$$

Alternatively, a resistive attenuator can be used, as shown in Figure 45. $R1$ and $R2$ should be chosen such that

The fan inputs have an input resistance of nominally 160 kΩ to ground, which should be taken into account when calculating resistor values. With a pull-up voltage of 12 V and pull-up resistor less than 1 kΩ, suitable values for $R1$ and $R2$ would be 100 kΩ and 47 kΩ, respectively. This gives a high input voltage of 3.83 V.

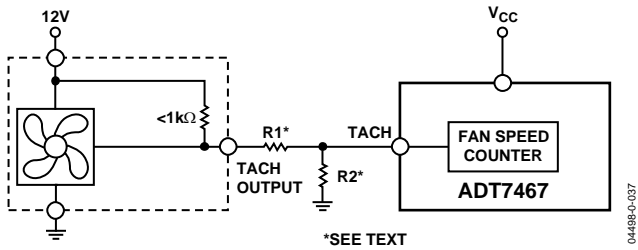


Figure 45. Fan with Strong TACH Pull-Up to $> V_{CC}$ or Totem-Pole Output, Attenuated with $R1/R2$

Fan Speed Measurement

The fan counter does not count the fan TACH output pulses directly, because the fan speed could be less than 1,000 RPM and it would take several seconds to accumulate a reasonably large and accurate count. Instead, the period of the fan revolution is measured by gating an on-chip 90 kHz oscillator into the input of a 16-bit counter for N periods of the fan TACH output (Figure 46), so the accumulated count is actually proportional to the fan tachometer period and inversely proportional to the fan speed.

N , the number of pulses counted, is determined by the settings of Register 0x7B (TACH pulses per revolution register). This register contains two bits for each fan, allowing one, two (default), three, or four TACH pulses to be counted.

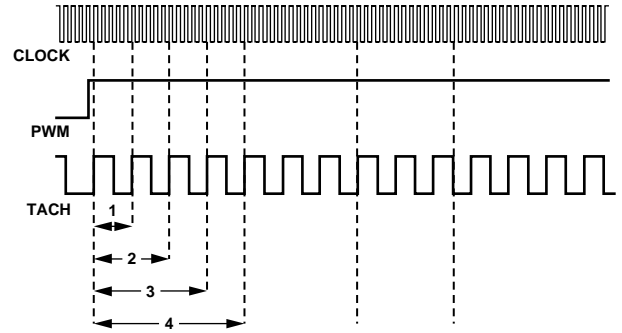


Figure 46. Fan Speed Measurement

Fan Speed Measurement Registers

The fan tachometer readings are 16-bit values consisting of a 2-byte read from the ADT7467.

Reg. 0x28 TACH1 Low Byte = 0x00 default

Reg. 0x29 TACH1 High Byte = 0x00 default

Reg. 0x2A TACH2 Low Byte = 0x00 default

Reg. 0x2B TACH2 High Byte = 0x00 default

Reg. 0x2C TACH3 Low Byte = 0x00 default

Reg. 0x2D TACH3 High Byte = 0x00 default

Reg. 0x2E TACH4 Low Byte = 0x00 default

Reg. 0x2F TACH4 High Byte = 0x00 default

Reading Fan Speed from the ADT7467

The measurement of fan speeds involves a 2-register read for each measurement. The low byte should be read first. This causes the high byte to be frozen until both high and low byte registers have been read, preventing erroneous TACH readings. The fan tachometer reading registers report back the number of 11.11 μs period clocks (90 kHz oscillator) gated to the fan speed counter, from the rising edge of the first fan TACH pulse to the rising edge of the third fan TACH pulse (assuming two pulses per revolution are being counted). Because the device is essentially measuring the fan TACH period, the higher the count value, the slower the fan is actually running. A 16-bit fan tachometer reading of 0xFFFF indicates either that the fan has stalled or is running very slowly (<100 RPM).

High Limit: > Comparison Performed

Because the actual fan TACH period is being measured, falling below a fan TACH limit by 1 sets the appropriate status bit and can be used to generate an SMBALERT.

Fan TACH Limit Registers

The fan TACH limit registers are 16-bit values consisting of two bytes.

Reg. 0x54 TACH1 Minimum Low Byte = 0xFF default

Reg. 0x55 TACH1 Minimum High Byte = 0xFF default

Reg. 0x56 TACH2 Minimum Low Byte = 0xFF default

Reg. 0x57 TACH2 Minimum High Byte = 0xFF default

Reg. 0x58 TACH3 Minimum Low Byte = 0xFF default

Reg. 0x59 TACH3 Minimum High Byte = 0xFF default

Reg. 0x5A TACH4 Minimum Low Byte = 0xFF default

Reg. 0x5B TACH4 Minimum High Byte = 0xFF default

Fan Speed Measurement Rate

The fan TACH readings are normally updated once every second.

The FAST bit (Bit 3) of Configuration Register 3 (Reg. 0x78), when set, updates the fan TACH readings every 250 ms.

If any of the fans are not being driven by a PWM channel but are powered directly from 5 V or 12 V, their associated dc bit in Configuration Register 3 should be set. This allows TACH readings to be taken on a continuous basis for fans connected directly to a dc source. For optimal results, the associated dc bit should always be set when using 4-wire fans.

Calculating Fan Speed

Assuming a fan with a two pulses per revolution (and two pulses per revolution being measured) fan speed is calculated by

$$\text{Fan Speed (RPM)} = (90,000 \times 60) / \text{Fan TACH Reading}$$

where *Fan TACH Reading* is the 16-bit fan tachometer reading.

Example:

TACH1 High Byte (Reg. 0x29) = 0x17

TACH1 Low Byte (Reg. 0x28) = 0xFF

What is Fan 1 speed in RPM?

Fan 1 TACH Reading = 0x17FF = 6143 (decimal)

$RPM = (f \times 60) / \text{Fan 1 TACH Reading}$

$RPM = (90000 \times 60) / 6143$

Fan Speed = 879 RPM

Fan Pulses per Revolution

Different fan models can output either 1, 2, 3, or 4 TACH pulses per revolution. Once the number of fan TACH pulses has been determined, it can be programmed into the fan pulses per revolution register (Reg. 0x7B) for each fan. Alternatively, this register can be used to determine the number of pulses per revolution output by a given fan. By plotting fan speed measurements at 100% speed with different pulses per revolution setting, the smoothest graph with the lowest ripple determines the correct pulses per revolution value.

Fan Pulses per Revolution Register

<1:0> Fan 1 default = 2 pulses per revolution.

<3:2> Fan 2 default = 2 pulses per revolution.

<5:4> Fan 3 default = 2 pulses per revolution.

<7:6> Fan 4 default = 2 pulses per revolution.

00 = 1 pulse per revolution.

01 = 2 pulses per revolution.

10 = 3 pulses per revolution.

11 = 4 pulses per revolution.

2-Wire Fan Speed Measurements (Low Frequency Mode Only)

The ADT7467 is capable of measuring the speed of 2-wire fans, that is, fans without TACH outputs. To do this, the fan must be interfaced as shown in the Driving 2-Wire Fans section. In this case, the TACH inputs should be reprogrammed as analog inputs, AIN.

Configuration Register 2 (Reg. 0x73)

Bit 3 (AIN4) = 1, Pin 9 is reconfigured to measure the speed of a 2-wire fan using an external sensing resistor and coupling capacitor.

Bit 2 (AIN3) = 1, Pin 4 is reconfigured to measure the speed of a 2-wire fan using an external sensing resistor and coupling capacitor.

Bit 1 (AIN2) = 1, Pin 7 is reconfigured to measure the speed of a 2-wire fan using an external sensing resistor and coupling capacitor.

Bit 0 (AIN1) = 1, Pin 6 is reconfigured to measure the speed of a 2-wire fan using an external sensing resistor and coupling capacitor.

AIN Switching Threshold

Having configured the TACH inputs as AIN inputs for 2-wire measurements, a user can select the sensing threshold for the AIN signal.

Configuration Register 4 (Reg. 0x7D)

<3:2> AINL, input threshold for 2-wire fan speed measurements.

00 = ±20 mV

01 = ±40 mV

10 = ±80 mV

11 = ±130 mV

Fan Spin-Up

The ADT7467 has a unique fan spin-up function. It spins the fan at 100% PWM duty cycle until two TACH pulses are detected on the TACH input. Once two TACH pulses have been detected, the PWM duty cycle goes to the expected running value, for example, 33%. The advantage is that fans have different spin-up characteristics and take different times to overcome inertia. The ADT7467 runs the fans just fast enough to overcome inertia and is quieter on spin-up than fans programmed to spin up for a given spin-up time.

Fan Startup Timeout

To prevent the generation of false interrupts as a fan spins up (because it is below running speed), the ADT7467 includes a fan startup timeout function. During this time, the ADT7467 looks for two TACH pulses. If two TACH pulses are not detected, then an interrupt is generated. Using Configuration Register 4 (0x40) Bit 5 (FSPDIS), this functionality can be changed (see the Disabling Fan Startup Timeout section).

PWM1 Configuration (Reg. 0x5C)

<2:0> SPIN, startup timeout for PWM1.

000 = no startup timeout

001 = 100 ms

010 = 250 ms default

011 = 400 ms

100 = 667 ms

101 = 1 s

110 = 2 s

111 = 4 s

PWM2 Configuration (Reg. 0x5D)

<2:0> SPIN, startup timeout for PWM2.

000 = no startup timeout

001 = 100 ms

010 = 250 ms default

011 = 400 ms

100 = 667 ms

101 = 1 s

110 = 2 s

111 = 4 s

PWM3 Configuration (Reg. 0x5E)

<2:0> SPIN, start-up timeout for PWM3.

000 = no startup timeout

001 = 100 ms

010 = 250 ms default

011 = 400 ms

100 = 667 ms

101 = 1 s

110 = 2 s

111 = 4 s

Disabling Fan Startup Timeout

Although fan startup makes fan spin-ups much quieter than fixed-time spin-ups, the option exists to use fixed spin-up times. Setting Bit 5 (FSPDIS) to 1 in Configuration Register 1 (Reg. 0x40) disables the spin-up for two TACH pulses. Instead, the fan spins up for the fixed time as selected in Reg. 0x5C to Reg. 0x5E.

PWM Logic State

The PWM outputs can be programmed high for 100% duty cycle (noninverted) or low for 100% duty cycle (inverted).

PWM1 Configuration (Reg. 0x5C)

<4> INV.

0 = Logic high for 100% PWM duty cycle.

1 = Logic low for 100% PWM duty cycle.

PWM2 Configuration (Reg. 0x5D)

<4> INV.

0 = Logic high for 100% PWM duty cycle.

1 = Logic low for 100% PWM duty cycle.

PWM3 Configuration (Reg. 0x5E)

<4> INV.

0 = Logic high for 100% PWM duty cycle.

1 = Logic low for 100% PWM duty cycle.

Low Frequency Mode PWM Drive Frequency

The PWM drive frequency can be adjusted for the application. Reg. 0x5F to Reg. 0x61 configure the PWM frequency for PWM1 to PWM3, respectively. In high frequency mode, the PWM drive frequency is always 22.5 kHz and cannot be changed.

PWM1 Frequency Registers (Reg. 0x5F to Reg. 0x61)

<2:0> **FREQ.**

000	= 11.0 Hz
001	= 14.7 Hz
010	= 22.1 Hz
011	= 29.4 Hz
100	= 35.3 Hz default
101	= 44.1 Hz
110	= 58.8 Hz
111	= 88.2 Hz

Fan Speed Control

The ADT7467 controls fan speed using two modes: automatic and manual.

In automatic fan speed control mode, fan speed is automatically varied with temperature and without CPU intervention, once initial parameters are set up. The advantage of this is that, if the system hangs, the user is guaranteed that the system is protected from overheating. The automatic fan speed control incorporates a feature called dynamic T_{MIN} calibration. This feature reduces the design effort required to program the automatic fan speed control loop. For more information and how to program the automatic fan speed control loop and dynamic T_{MIN} calibration, see the Programming the Automatic Fan Speed Control Loop section.

In manual fan speed control mode, the ADT7467 allows the duty cycle of any PWM output to be manually adjusted. This can be useful, if the user wants to change fan speed in software or adjust PWM duty cycle output for test purposes. Bits <7:5> of Reg. 0x5C to Reg. 0x5E (PWM Configuration) control the behavior of each PWM output.

PWM Configuration Register (Reg. 0x5C to Reg. 0x5E)

<7:5> **BHVR.**

111 = manual mode.

Once under manual control, each PWM output can be manually updated by writing to Reg. 0x30 to Reg. 0x32 (PWMx current duty cycle registers).

Programming the PWM Current Duty Cycle Registers

The PWM current duty cycle registers are 8-bit registers that allow the PWM duty cycle for each output to be set anywhere from 0% to 100% in steps of 0.39%.

The value to be programmed into the PWM_{MIN} register is given by

$$Value \text{ (decimal)} = PWM_{MIN}/0.39$$

Example 1: For a PWM duty cycle of 50%,

$$Value \text{ (decimal)} = 50/0.39 = 128 \text{ (decimal)}$$

$$Value = 128 \text{ (decimal) or } 0x80 \text{ (hex)}$$

Example 2: For a PWM duty cycle of 33%,

$$Value \text{ (decimal)} = 33/0.39 = 85 \text{ (decimal)}$$

$$Value = 85 \text{ (decimal) or } 0x54 \text{ (hex)}$$

PWM Duty Cycle Registers

Reg. 0x30 **PWM1 Duty Cycle** = 0x00 (0% default)

Reg. 0x31 **PWM2 Duty Cycle** = 0x00 (0% default)

Reg. 0x32 **PWM3 Duty Cycle** = 0x00 (0% default)

By reading the PWMx current duty cycle registers, the user can keep track of the current duty cycle on each PWM output, even when the fans are running in automatic fan speed control mode or acoustic enhancement mode. See the Programming the Automatic Fan Speed Control Loop section for details.

OPERATING FROM 3.3 V STANDBY

The ADT7467 has been specifically designed to operate from a 3.3 V STBY supply. In computers that support S3 and S5 states, the core voltage of the processor is lowered in these states. If using the dynamic T_{MIN} mode, lowering the core voltage of the processor changes the CPU temperature and changes the dynamics of the system under dynamic T_{MIN} control. Likewise, when monitoring THERM, the THERM timer should be disabled during these states.

Dynamic T_{MIN} Control Register 1 (Reg. 0x36) <1> $V_{CCP} = 1$

When the power is supplied from 3.3 V STBY and the V_{CCP} voltage drops below the V_{CCP} low limit, the following occurs:

1. Status Bit 1 (V_{CCP}) in Status Register 1 is set.
2. $\overline{SMBALERT}$ is generated if enabled.
3. \overline{THERM} monitoring is disabled. The \overline{THERM} timer should hold its value prior to the S3 or S5 state.
4. Dynamic T_{MIN} control is disabled. This prevents T_{MIN} from being adjusted due to an S3 or S5 state.
5. The ADT7467 is prevented from entering the shutdown state.

Once the core voltage, V_{CCP} , goes above the V_{CCP} low limit, everything is re-enabled and the system resumes normal operation.

XNOR TREE TEST MODE

The ADT7467 includes an XNOR tree test mode. This mode is useful for in-circuit test equipment at board-level testing. By applying stimulus to the pins included in the XNOR tree, it is possible to detect opens or shorts on the system board.

Figure 47 shows the signals that are exercised in the XNOR tree test mode. The XNOR tree test is invoked by setting Bit 0 (XEN) of the XNOR tree test enable register (Reg. 0x6F).

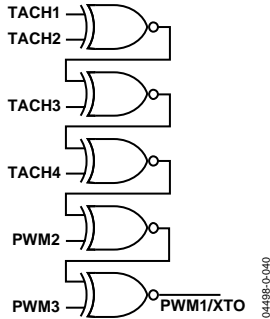


Figure 47. XNOR Tree Test

POWER-ON DEFAULT

When the ADT7467 is powered up, it polls the V_{CCP} input.

If V_{CCP} stays below 0.75 V (the system CPU power rail is not powered up), then the ADT7467 assumes the functionality of the default registers after the ADT7467 is addressed via any valid SMBus transaction.

If V_{CC} goes high (the system processor power rail is powered up), then a fail-safe timer begins to count down. If the ADT7467 is not addressed by any valid SMBus transaction before the fail-safe timeout (4.6 s) lapses, then the ADT7467 drives the fans to full speed. If the ADT7467 is addressed by a valid SMBus transaction after this point, the fans stop, and the ADT7467 assumes its default settings and begins normal operation.

If V_{CCP} goes high (the system processor power rail is powered up), then a fail-safe timer begins to count down. If the ADT7467 is addressed by a valid SMBus transaction before the fail-safe timeout (4.6 s) lapses, then the ADT7467 operates normally, assuming the functionality of all the default registers. See the flow chart in Figure 48.

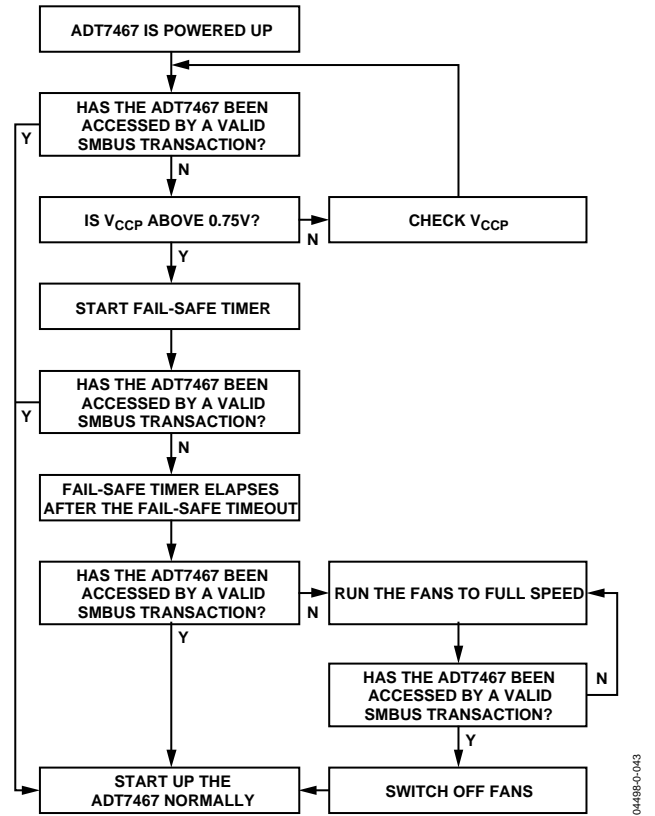


Figure 48. Power-On Flow Chart

PROGRAMMING THE AUTOMATIC FAN SPEED CONTROL LOOP

Note: To more efficiently understand the automatic fan speed control loop, it is strongly recommended to use the ADT7467 evaluation board and software while reading this section.

This section provides the system designer with an understanding of the automatic fan control loop, and provides step-by-step guidance on effectively evaluating and selecting critical system parameters. To optimize the system characteristics, the designer needs to give some thought to system configuration, including the number of fans, where they are located, and what temperatures are being measured in the particular system.

The mechanical or thermal engineer who is tasked with the system thermal characterization should also be involved at the beginning of the process.

AUTOMATIC FAN CONTROL OVERVIEW

The ADT7467 can automatically control the speed of fans based upon the measured temperature. This is done independently of CPU intervention once initial parameters are set up.

The ADT7467 has a local temperature sensor and two remote temperature channels that can be connected to a CPU on-chip thermal diode (available on Intel Pentium class and other CPUs). These three temperature channels can be used as the basis for automatic fan speed control to drive fans using pulse-width modulation (PWM).

Automatic fan speed control reduces acoustic noise by optimizing fan speed according to accurately measured

temperature. Reducing fan speed can also decrease system current consumption. The automatic fan speed control mode is very flexible owing to the number of programmable parameters, including T_{MIN} and T_{RANGE} . The T_{MIN} and T_{RANGE} values for a temperature channel and, therefore, for a given fan are critical, because they define the thermal characteristics of the system. The thermal validation of the system is one of the most important steps in the design process, so these values should be selected carefully.

Figure 49 gives a top-level overview of the automatic fan control circuitry on the ADT7467. From a systems-level perspective, up to three system temperatures can be monitored and used to control three PWM outputs. The three PWM outputs can be used to control up to four fans. The ADT7467 allows the speed of four fans to be monitored. Each temperature channel has a thermal calibration block, allowing the designer to individually configure the thermal characteristics of each temperature channel. For example, one can decide to run the CPU fan when CPU temperature increases above 60°C and a chassis fan when the local temperature increases above 45°C. At this stage, the designer has not assigned these thermal calibration settings to a particular fan drive (PWM) channel. The right side of Figure 49 shows controls that are fan-specific. The designer has individual control over parameters such as minimum PWM duty cycle, fan speed failure thresholds, and even ramp control of the PWM outputs. Automatic fan control, then, ultimately allows graceful fan speed changes that are less perceptible to the system user.

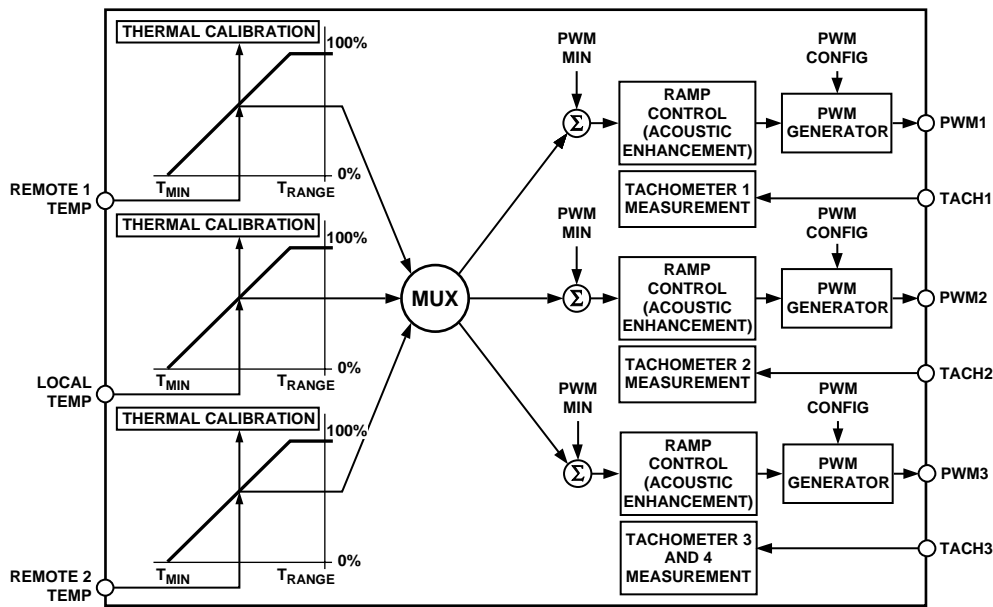


Figure 49. Automatic Fan Control Block Diagram

STEP 1: HARDWARE CONFIGURATION

During system design, the motherboard sensing and control capabilities should be addressed early in the design stages. Decisions about how these capabilities are used should involve the system thermal/mechanical engineer. Ask the following questions:

1. What ADT7467 functionality will be used?
 - PWM2 or SMBALERT?
 - TACH4 fan speed measurement or overtemperature THERM function?
 - 5 V voltage monitoring or overtemperature THERM function?
 - 12 V voltage monitoring or VID5 input?

2. How many fans will be supported in system, three or four?
This influences the choice of whether to use the TACH4 pin or to reconfigure it for the THERM function.
3. Is the CPU fan to be controlled using the ADT7467 or will it run at full speed 100% of the time?
If run at 100%, this frees up a PWM output, but the system is louder.
4. Where will the ADT7467 be physically located in the system?

This influences the assignment of the temperature measurement channels to particular system thermal zones. For example, locating the ADT7467 close to the VRM controller circuitry allows the VRM temperature to be monitored using the local temperature channel.

The ADT7467 offers multifunctional pins that can be reconfigured to suit different system requirements and physical layouts. These multifunction pins are software programmable.

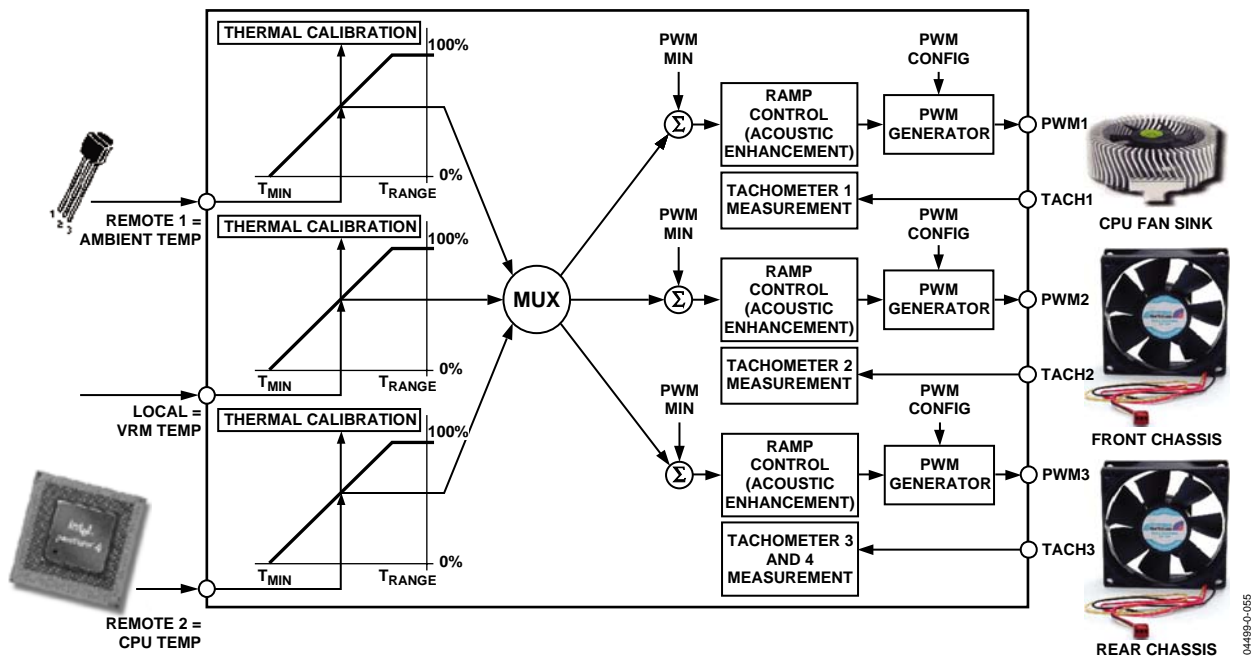


Figure 50. Hardware Configuration Example

ADT7467

RECOMMENDED IMPLEMENTATION 1

Configuring the ADT7467 as in Figure 51 provides the system designer with the following features:

1. Six VID inputs (VID0 to VID5) for VRM10 support.
2. Two PWM outputs for fan control of up to three fans. (The front and rear chassis fans are connected in parallel.)
3. Three TACH fan speed measurement inputs.
4. V_{CC} measured internally through Pin 4.
5. CPU core voltage measurement (V_{CORE}).
6. 2.5 V measurement input used to monitor CPU current (connected to V_{COMP} output of ADP316x VRM controller). This is used to determine CPU power consumption.
7. 5 V measurement input.
8. VRM temperature using local temperature sensor.
9. CPU temperature measured using the Remote 1 temperature channel.
10. Ambient temperature measured through the Remote 2 temperature channel.
11. If not using VID5, this pin can be reconfigured as the 12 V monitoring input.
12. Bidirectional \overline{THERM} pin allows the monitoring of $\overline{PROCHOT}$ output from an Intel® P4 processor, for example, or can be used as an overtemperature \overline{THERM} output.
13. $\overline{SMBALERT}$ system interrupt output.

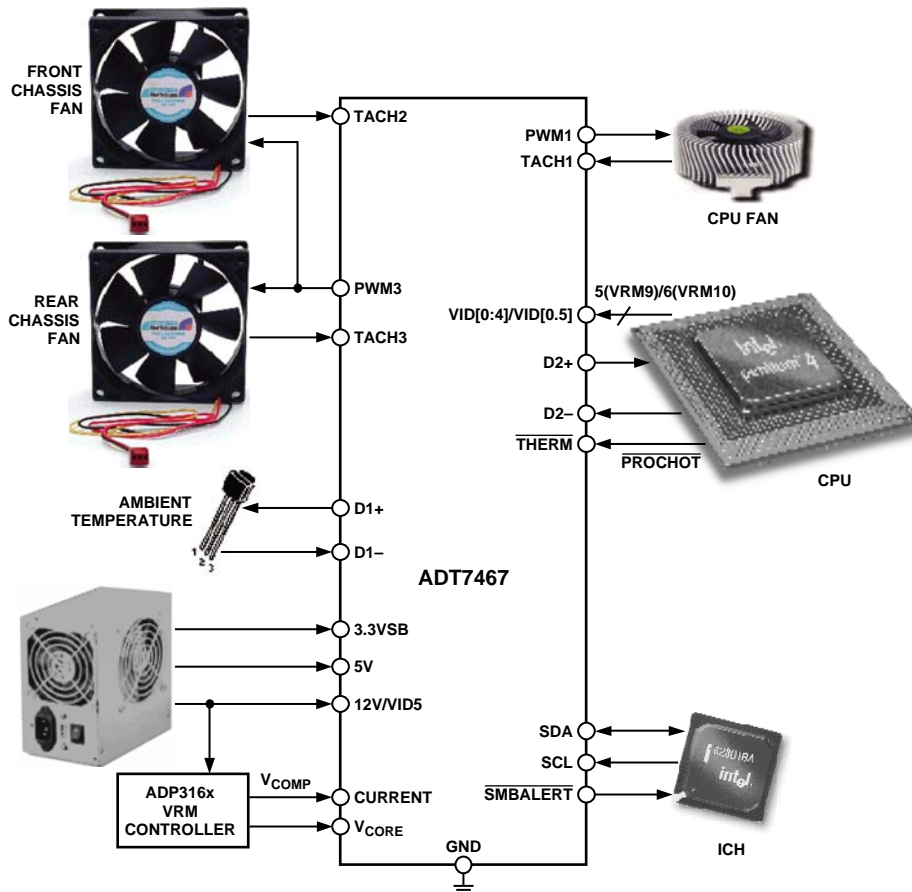


Figure 51. Recommended Implementation 1

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RECOMMENDED IMPLEMENTATION 2

Configuring the ADT7467 as in Figure 52 provides the system designer with the following features:

1. Six VID inputs (VID0 to VID5) for VRM10 support.
2. Three PWM outputs for fan control of up to three fans. (All three fans can be individually controlled.)
3. Three TACH fan speed measurement inputs.
4. V_{CC} measured internally through Pin 4.
5. CPU core voltage measurement (V_{CORE}).
6. 2.5 V measurement input used to monitor CPU current (connected to V_{COMP} output of ADP316x VRM controller). This is used to determine CPU power consumption.
7. 5 V measurement input.
8. VRM temperature using local temperature sensor.
9. CPU temperature measured using the Remote 1 temperature channel.
10. Ambient temperature measured through the Remote 2 temperature channel.
11. If not using VID5, this pin can be reconfigured as the 12 V monitoring input.
12. Bidirectional \overline{THERM} pin allows the monitoring of $\overline{PROCHOT}$ output from an Intel P4 processor, for example, or can be used as an overtemperature \overline{THERM} output.

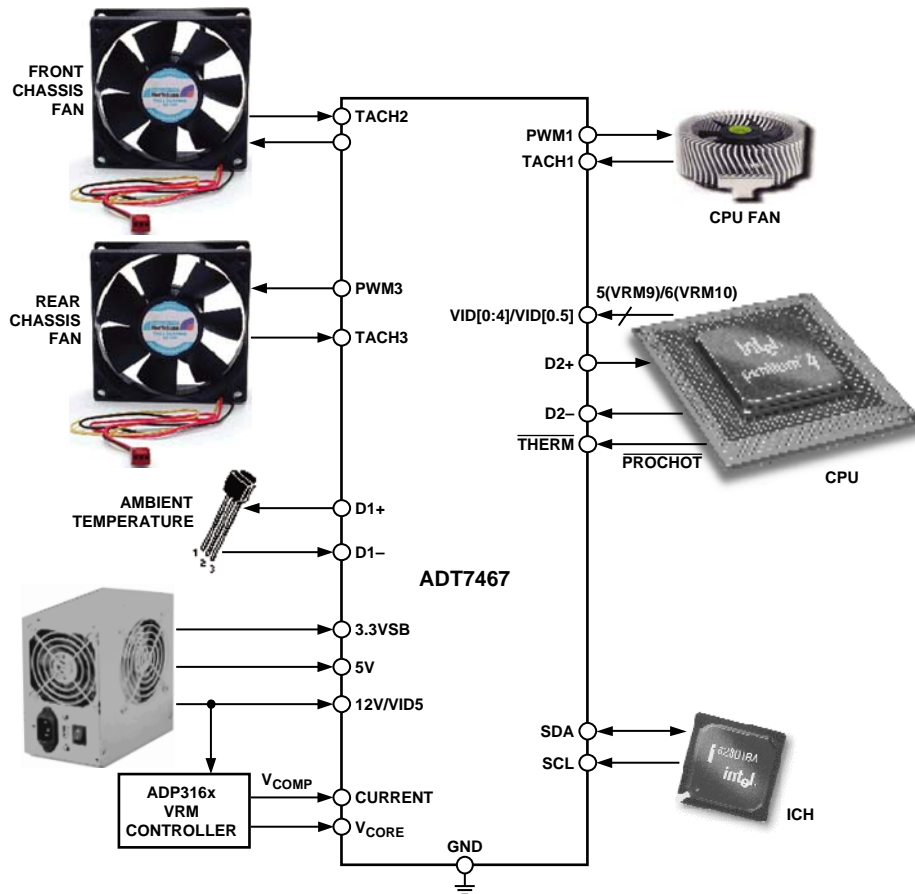


Figure 52. Recommended Implementation 2

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STEP 2: CONFIGURING THE MUX

After the system hardware configuration is determined, the fans can be assigned to particular temperature channels. Not only can fans be assigned to individual channels, but the behavior of the fans is also configurable. For example, fans can be run under automatic fan control, can be run manually (under software control), or can be run at the fastest speed calculated by multiple temperature channels. The MUX is the bridge between temperature measurement channels and the three PWM outputs.

Bits <7:5> (BHVR) of Registers 0x5C, 0x5D, and 0x5E (PWM configuration registers) control the behavior of the fans connected to the PWM1, PWM2, and PWM3 outputs. The values selected for these bits determine how the MUX connects a temperature measurement channel to a PWM output.

Automatic Fan Control MUX Options

<7:5> (BHVR), Registers 0x5C, 0x5D, 0x5E.

- 000 = Remote 1 temperature controls PWMx
- 001 = local temperature controls PWMx
- 010 = Remote 2 temperature controls PWMx

101 = Fastest speed calculated by local and Remote 2 temperature controls PWMx

110 = Fastest speed calculated by all three temperature channels controls PWMx

The Fastest Speed Calculated options pertain to controlling one PWM output based on multiple temperature channels. The thermal characteristics of the three temperature zones can be set to drive a single fan. An example would be the fan turning on when Remote 1 temperature exceeds 60°C or if the local temperature exceeds 45°C.

Other MUX Options

<7:5> (BHVR), Registers 0x5C, 0x5D, 0x5E.

011 = PWMx runs full speed

100 = PWMx disabled (default)

111 = manual mode. PWMx is runner under software control. In this mode, PWM duty cycle registers (Registers 0x30 to 0x32) are writable and control the PWM outputs.

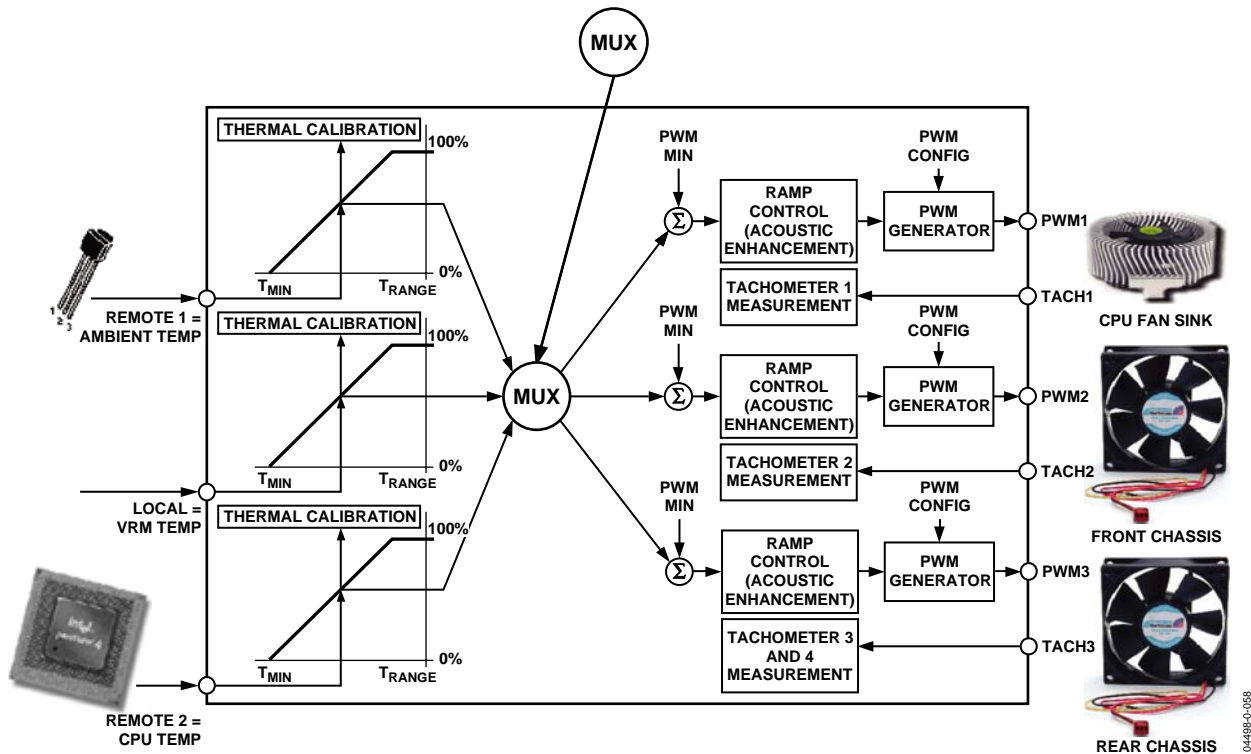


Figure 53. Assigning Temperature Channels to Fan Channels

MUX Configuration Example

This is an example of how to configure the MUX in a system using the ADT7467 to control three fans. The CPU fan sink is controlled by PWM1, the front chassis fan is controlled by PWM2, and the rear chassis fan is controlled by PWM3. The MUX is configured for the following fan control behavior:

- PWM1 (CPU fan sink) is controlled by the fastest speed calculated by the local (VRM temperature) and Remote 2 (processor) temperature. In this case, the CPU fan sink is also being used to cool the VRM.
- PWM2 (front chassis fan) is controlled by the Remote 1 temperature (ambient).
- PWM3 (rear chassis fan) is controlled by the Remote 1 temperature (ambient).

Example MUX Settings

<7:5> (BHVR), PWM1 Configuration Register 0x5C.

101 = Fastest speed calculated by local and Remote 2 temperature controls PWM1

<7:5> (BHVR), PWM2 Configuration Register 0x5D.

000 = Remote 1 temperature controls PWM2

<7:5> (BHVR), PWM3 Configuration Register 0x5E.

000 = Remote 1 temperature controls PWM3

These settings configure the MUX, as shown in Figure 54.

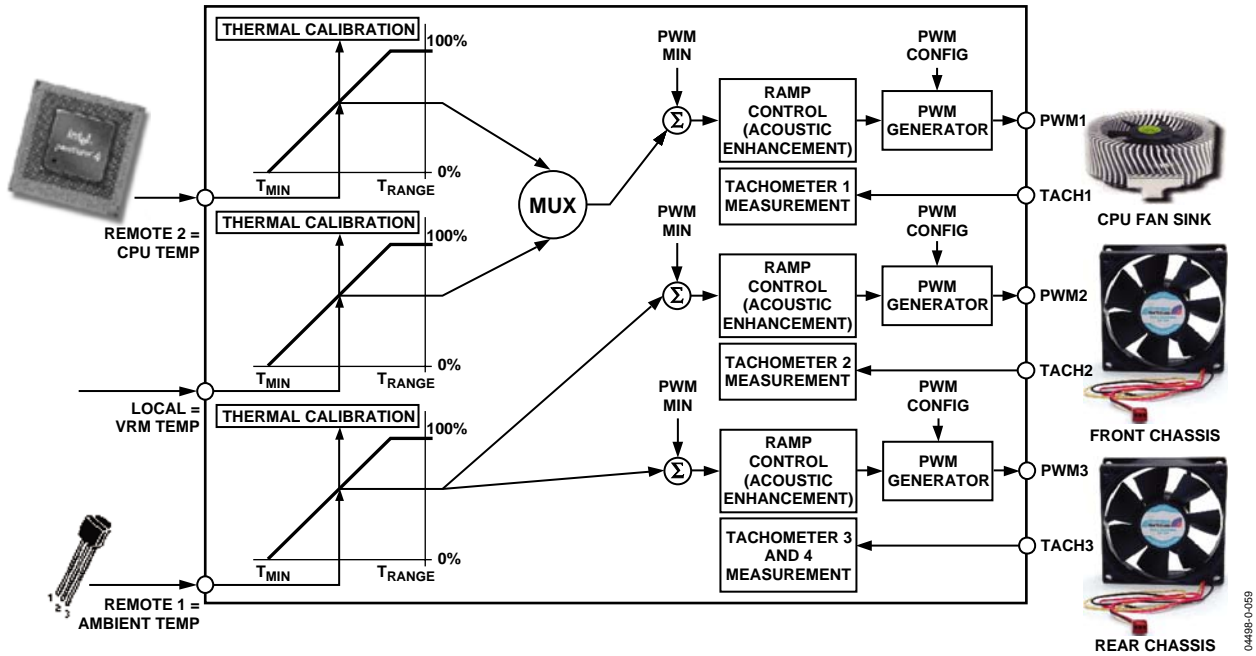


Figure 54. MUX Configuration Example

STEP 3: T_{MIN} SETTINGS FOR THERMAL CALIBRATION CHANNELS

T_{MIN} is the temperature at which the fans start to turn on under automatic fan control. The speed at which the fan runs at T_{MIN} is programmed later. The T_{MIN} values chosen are temperature channel specific, for example, 25°C for ambient channel, 30°C for VRM temperature, and 40°C for processor temperature.

T_{MIN} is an 8-bit value, either twos complement or Offset 64, that can be programmed in 1°C increments. There is a T_{MIN} register associated with each temperature measurement channel: Remote 1 Local, and Remote 2 Temp. Once the T_{MIN} value is exceeded, the fan turns on and runs at the minimum PWM duty cycle. The fan turns off once the temperature has dropped below $T_{MIN} - T_{HYST}$.

To overcome fan inertia, the fan is spun up until two valid TACH rising edges are counted. See the Fan Startup Timeout section for more details. In some cases, primarily for psycho-acoustic reasons, it is desirable that the fan never switch off below T_{MIN} . Bits <7:5> of Enhanced Acoustics Register 1 (Reg. 0x62), when set, keep the fans running at the PWM minimum duty cycle, if the temperature should fall below T_{MIN} .

T_{MIN} Registers

Reg. 0x67, Remote 1 Temperature $T_{MIN} = 0x9A$ (90°C)

Reg. 0x68, Local Temperature $T_{MIN} = 0x9A$ (90°C)

Reg. 0x69, Remote 2 Temperature $T_{MIN} = 0x9A$ (90°C)

Enhance Acoustics Register 1 (Reg. 0x62)

Bit 7 (MIN3) = 0, PWM3 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 7 (MIN3) = 1, PWM3 runs at PWM3 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 0, PWM2 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 1, PWM2 runs at PWM2 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 0, PWM1 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 1, PWM1 runs at PWM1 minimum duty cycle below $T_{MIN} - T_{HYST}$.

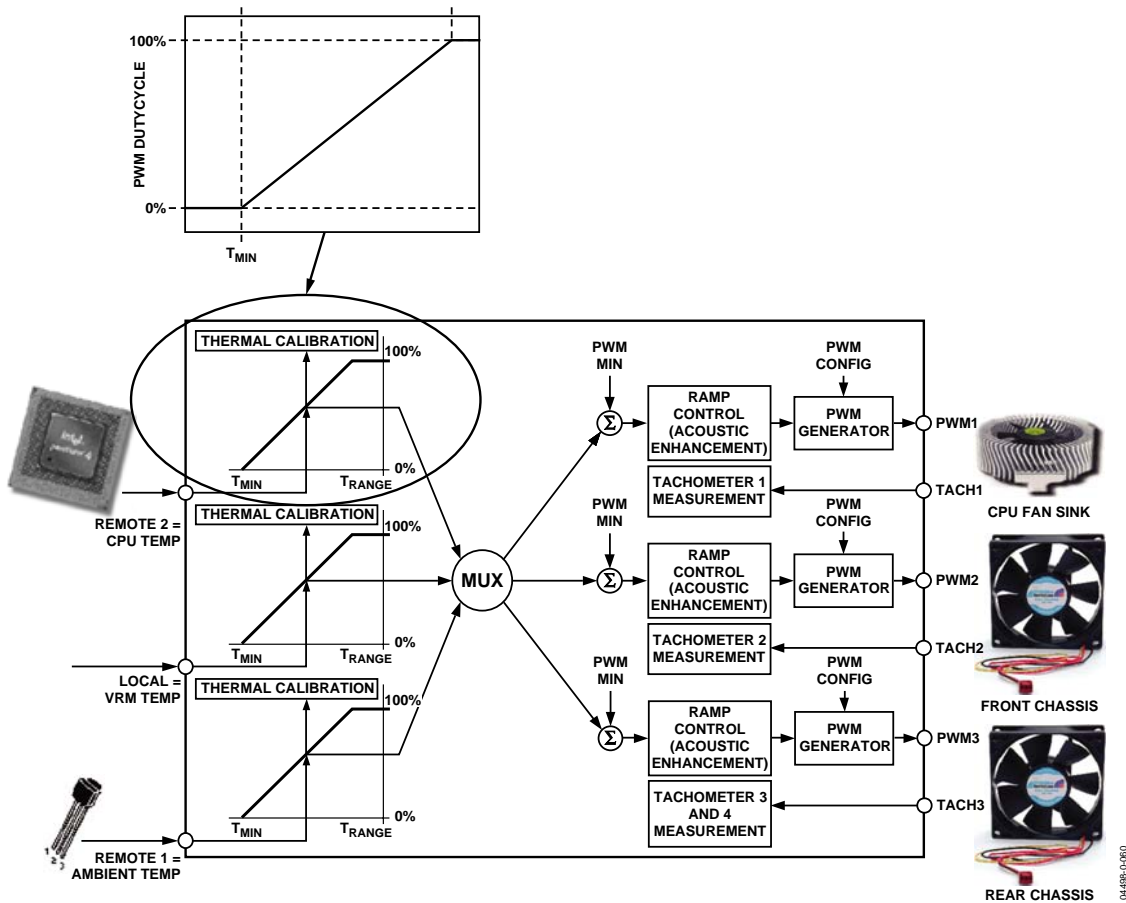


Figure 55. Understanding the T_{MIN} Parameter

STEP 4: PWM_{MIN} FOR EACH PWM (FAN) OUTPUT

PWM_{MIN} is the minimum PWM duty cycle at which each fan in the system runs. It is also the start speed for each fan under automatic fan control once the temperature rises above T_{MIN}. For maximum system acoustic benefit, PWM_{MIN} should be as low as possible. Depending on the fan used, the PWM_{MIN} setting is usually in the 20% to 33% duty cycle range. This value can be found through fan validation.

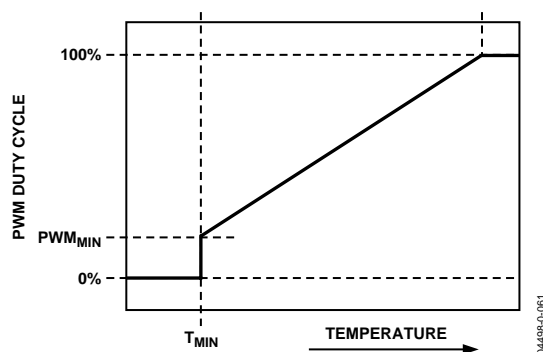


Figure 56. PWM_{MIN} Determines Minimum PWM Duty Cycle

More than one PWM output can be controlled from a single temperature measurement channel. For example, Remote 1 temperature can control PWM1 and PWM2 outputs. If two different fans are used on PWM1 and PWM2, then the fan characteristics can be set up differently. As a result, Fan 1 driven by PWM1 can have a different PWM_{MIN} value than that of Fan 2 connected to PWM2. Figure 57 illustrates this as PWM1_{MIN} (front fan) is turned on at a minimum duty cycle of 20%, while PWM2_{MIN} (rear fan) turns on at a minimum of 40% duty cycle. Note, however, that both fans turn on at exactly the same temperature, defined by T_{MIN}.

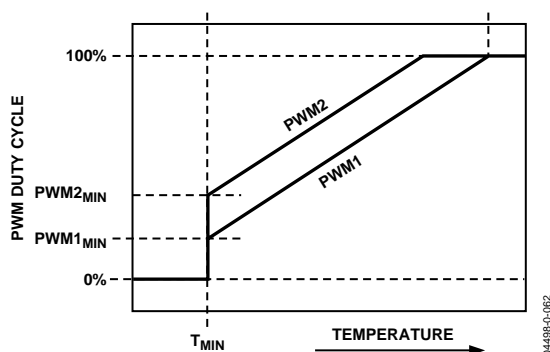


Figure 57. Operating Two Different Fans from a Single Temperature Channel

Programming the PWM_{MIN} Registers

The PWM_{MIN} registers are 8-bit registers that allow the minimum PWM duty cycle for each output to be configured anywhere from 0% to 100%. This allows the minimum PWM duty cycle to be set in steps of 0.39%.

The value to be programmed into the PWM_{MIN} register is given by

$$\text{Value (decimal)} = \text{PWM}_{\text{MIN}}/0.39$$

Example 1: For a minimum PWM duty cycle of 50%,

$$\text{Value (decimal)} = 50/0.39 = 128 \text{ (decimal)}$$

$$\text{Value} = 128 \text{ (decimal) or } 80 \text{ (hex)}$$

Example 2: For a minimum PWM duty cycle of 33%,

$$\text{Value (decimal)} = 33/0.39 = 85 \text{ (decimal)}$$

$$\text{Value} = 85 \text{ (decimal) or } 54 \text{ (hex)}$$

PWM_{MIN} Registers

Reg. 0x64, PWM1 Minimum Duty Cycle = 0x80 (50% default)

Reg. 0x65 PWM2 Minimum Duty Cycle = 0x80 (50% default)

Reg. 0x66, PWM3 Minimum Duty Cycle = 0x80 (50% default)

Note on Fan Speed and PWM Duty Cycle

The PWM duty cycle does not directly correlate to fan speed in RPM. Running a fan at 33% PWM duty cycle does not equate to running the fan at 33% speed. Driving a fan at 33% PWM duty cycle actually runs the fan at closer to 50% of its full speed. This is because fan speed in %RPM generally relates to the square root of PWM duty cycle. Given a PWM square wave as the drive signal, fan speed in RPM approximates to

$$\% \text{ fanspeed} = \sqrt{\text{PWM duty cycle} \times 10}$$

STEP 5: PWM_{MAX} FOR PWM (FAN) OUTPUTS

PWM_{MAX} is the maximum duty cycle that each fan in the system runs at under the automatic fan speed control loop. For maximum system acoustic benefit, PWM_{MAX} should be as low as possible, but should be capable of maintaining the processor temperature limit at an acceptable level. If the THERM temperature limit is exceeded, the fans are still boosted to 100% for fail-safe cooling.

There is a PWM_{MAX} limit for each fan channel. The default value of this register is 0xFF and so has no effect unless it is programmed.

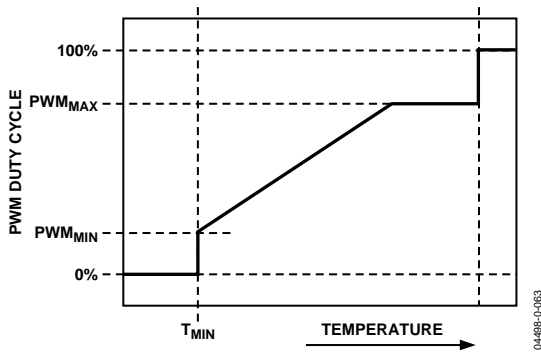


Figure 58. PWM_{MAX} Determines Maximum PWM Duty Cycle below the $THERM$ Temperature Limit

Programming the PWM_{MAX} Registers

The PWM_{MAX} registers are 8-bit registers that allow the maximum PWM duty cycle for each output to be configured anywhere from 0% to 100%. This allows the maximum PWM duty cycle to be set in steps of 0.39%.

The value to be programmed into the PWM_{MAX} register is given by

$$\text{Value (decimal)} = PWM_{MAX}/0.39$$

Example 1: For a maximum PWM duty cycle of 50%,

$$\begin{aligned} \text{Value (decimal)} &= 50/0.39 = 128 \text{ (decimal)} \\ \text{Value} &= 128 \text{ (decimal) or } 80 \text{ (hex)} \end{aligned}$$

Example 2: For a minimum PWM duty cycle of 75%,

$$\begin{aligned} \text{Value (decimal)} &= 75/0.39 = 85 \text{ (decimal)} \\ \text{Value} &= 192 \text{ (decimal) or } C0 \text{ (hex)} \end{aligned}$$

PWM_{MAX} Registers

Reg. 0x38, **PWM1 Maximum Duty Cycle** = 0xFF (100% default)

Reg. 0x39, **PWM2 Maximum Duty Cycle** = 0xFF (100% default)

Reg. 0x3A, **PWM3 Maximum Duty Cycle** = 0xFF (100% default)

See the Note on Fan Speed and PWM Duty Cycle on Page 41.

STEP 6: T_{RANGE} FOR TEMPERATURE CHANNELS

T_{RANGE} is the range of temperature over which automatic fan control occurs once the programmed T_{MIN} temperature has been exceeded. T_{RANGE} is a temperature slope, not an arbitrary value, that is, a T_{RANGE} of 40°C holds true only for $PWM_{MIN} = 33\%$. If PWM_{MIN} is increased or decreased, the effective T_{RANGE} changes.

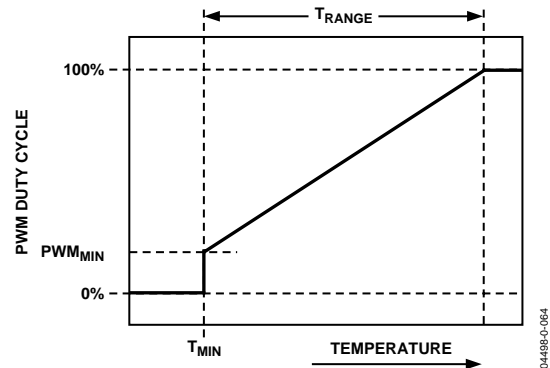


Figure 59. T_{RANGE} Parameter Affects Cooling Slope

The T_{RANGE} or fan control slope is determined by the following procedure:

1. Determine the maximum operating temperature for that channel (for example, 70°C).
2. Determine experimentally the fan speed (PWM duty cycle value) that does not exceed the temperature at the worst-case operating points. (For example, 70°C is reached when the fans are running at 50% PWM duty cycle.)
3. Determine the slope of the required control loop to meet these requirements.
4. Using the ADT7467 evaluation software, can graphically program and visualize this functionality. Ask your local Analog Devices representative for details.

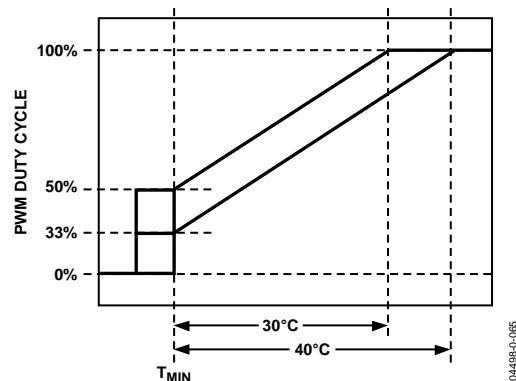


Figure 60. Adjusting PWM_{MIN} Affects T_{RANGE}

T_{RANGE} is implemented as a slope, which means that as PWM_{MIN} is changed, T_{RANGE} changes, but the actual slope remains the same. The higher the PWM_{MIN} value, the smaller the effective T_{RANGE} , that is, the fan reaches full speed (100%) at a lower temperature.

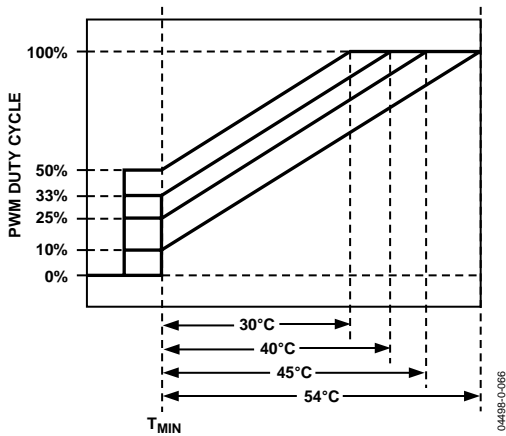


Figure 61. Increasing PWM_{MIN} Changes Effective T_{RANGE}

For a given T_{RANGE} value, the temperature at which the fan runs at full speed for different PWM_{MIN} values can be easily calculated:

$$T_{MAX} = T_{MIN} + (Max\ DC - Min\ DC) \times T_{RANGE} / 170$$

where:

- T_{MAX} is the temperature at which the fan runs full speed.
- T_{MIN} is the temperature at which the fan turns on.
- $Max\ DC$ is the maximum duty cycle (100%) = 255 decimal.
- $Min\ DC$ is equal to PWM_{MIN} .
- T_{RANGE} is the duty PWM duty cycle vs. temperature slope.

Example: Calculate T , given that $T_{MIN} = 30^{\circ}C$, $T_{RANGE} = 40^{\circ}C$, and $PWM_{MIN} = 10\%$ duty cycle = 26 (decimal).

$$\begin{aligned} T_{MAX} &= T_{MIN} + (Max\ DC - Min\ DC) \times T_{RANGE} / 170 \\ T_{MAX} &= 30^{\circ}C + (100\% - 10\%) \times 40^{\circ}C / 170 \\ T_{MAX} &= 30^{\circ}C + (255 - 26) \times 40^{\circ}C / 170 \\ T_{MAX} &= 84^{\circ}C \text{ (effective } T_{RANGE} = 54^{\circ}C) \end{aligned}$$

Example: Calculate T_{MAX} , given that $T_{MIN} = 30^{\circ}C$, $T_{RANGE} = 40^{\circ}C$, and $PWM_{MIN} = 25\%$ duty cycle = 64 (decimal).

$$\begin{aligned} T_{MAX} &= T_{MIN} + (Max\ DC - Min\ DC) \times T_{RANGE} / 170 \\ T_{MAX} &= 30^{\circ}C + (100\% - 25\%) \times 40^{\circ}C / 170 \\ T_{MAX} &= 30^{\circ}C + (255 - 64) \times 40^{\circ}C / 170 \\ T_{MAX} &= 75^{\circ}C \text{ (effective } T_{RANGE} = 45^{\circ}C) \end{aligned}$$

Example: Calculate T_{MAX} , given that $T_{MIN} = 30^{\circ}C$, $T_{RANGE} = 40^{\circ}C$, and $PWM_{MIN} = 33\%$ duty cycle = 85 (decimal).

$$\begin{aligned} T_{MAX} &= T_{MIN} + (Max\ DC - Min\ DC) \times T_{RANGE} / 170 \\ T_{MAX} &= 30^{\circ}C + (100\% - 33\%) \times 40^{\circ}C / 170 \\ T_{MAX} &= 30^{\circ}C + (255 - 85) \times 40^{\circ}C / 170 \\ T_{MAX} &= 70^{\circ}C \text{ (effective } T_{RANGE} = 40^{\circ}C) \end{aligned}$$

Example: Calculate T_{MAX} , given that $T_{MIN} = 30^{\circ}C$, $T_{RANGE} = 40^{\circ}C$, and $PWM_{MIN} = 50\%$ duty cycle = 128 (decimal).

$$\begin{aligned} T_{MAX} &= T_{MIN} + (Max\ DC - Min\ DC) \times T_{RANGE} / 170 \\ T_{MAX} &= 30^{\circ}C + (100\% - 50\%) \times 40^{\circ}C / 170 \\ T_{MAX} &= 30^{\circ}C + (255 - 128) \times 40^{\circ}C / 170 \\ T_{MAX} &= 60^{\circ}C \text{ (effective } T_{RANGE} = 30^{\circ}C) \end{aligned}$$

Selecting a T_{RANGE} Slope

The T_{RANGE} value can be selected for each temperature channel: Remote 1, local, and Remote 2 temperature. Bits <7:4> (T_{RANGE}) of Registers 0x5F to 0x61 define the T_{RANGE} value for each temperature channel.

Table 13. Selecting a T_{RANGE} Value

Bits <7:4> ¹	T_{RANGE} (°C)
0000	2
0001	2.5
0010	3.33
0011	4
0100	5
0101	6.67
0110	8
0111	10
1000	13.33
1001	16
1010	20
1011	26.67
1100	32 (default)
1101	40
1110	53.33
1111	80

¹ Register 0x5F configures Remote 1 T_{RANGE} .
 Register 0x60 configures Local T_{RANGE} .
 Register 0x61 configures Remote 2 T_{RANGE} .

Summary of T_{RANGE} Function

When using the automatic fan control function, the temperature at which the fan reaches full speed can be calculated by

$$T_{MAX} = T_{MIN} + T_{RANGE} \tag{1}$$

Equation 1 holds true only when PWM_{MIN} is equal to 33% PWM duty cycle.

Increasing or decreasing PWM_{MIN} changes the effective T_{RANGE}, although the fan control still follows the same PWM duty cycle to temperature slope. The effective T_{RANGE} for different PWM_{MIN} values can be calculated using Equation 2:

$$T_{MAX} = T_{MIN} + (Max DC - Min DC) \times T_{RANGE}/170 \quad (2)$$

where:

$(Max DC - Min DC) \times T_{RANGE}/170$ is the effective T_{RANGE} value.

See the Note on Fan Speed and PWM Duty Cycle.

Figure 62 shows PWM duty cycle versus temperature for each T_{RANGE} setting. The lower graph shows how each T_{RANGE} setting affects fan speed versus temperature. As can be seen from the graph, the effect on fan speed is nonlinear.

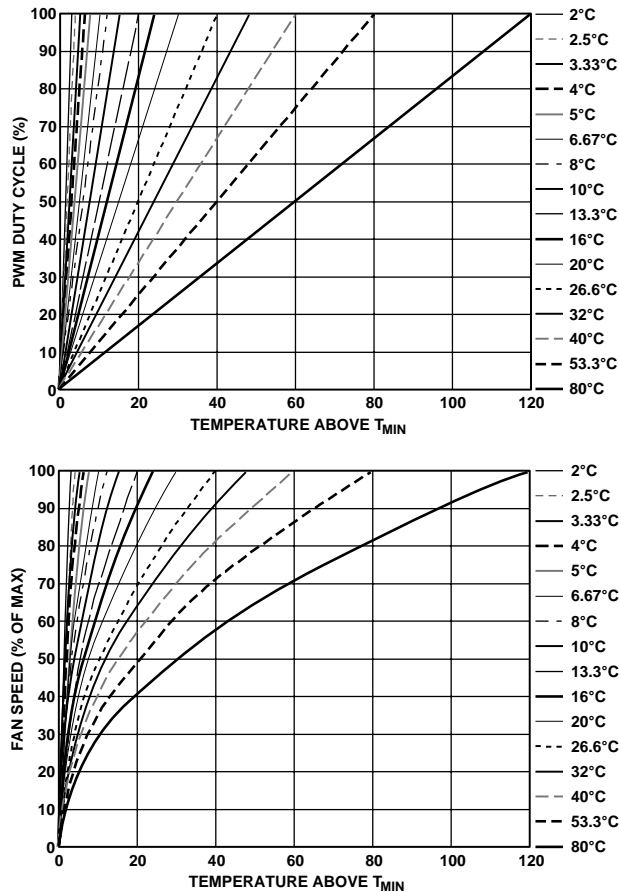


Figure 62. T_{RANGE} VS. Actual Fan Speed Profile

The graphs in Figure 62 assume that the fan starts from 0% PWM duty cycle. Clearly, the minimum PWM duty cycle, PWM_{MIN}, needs to be factored in to see how the loop actually performs in the system. Figure 63 shows how T_{RANGE} is affected when the PWM_{MIN} value is set to 20%. It can be seen that the fan actually runs at about 45% fan speed when the temperature exceeds T_{MIN}.

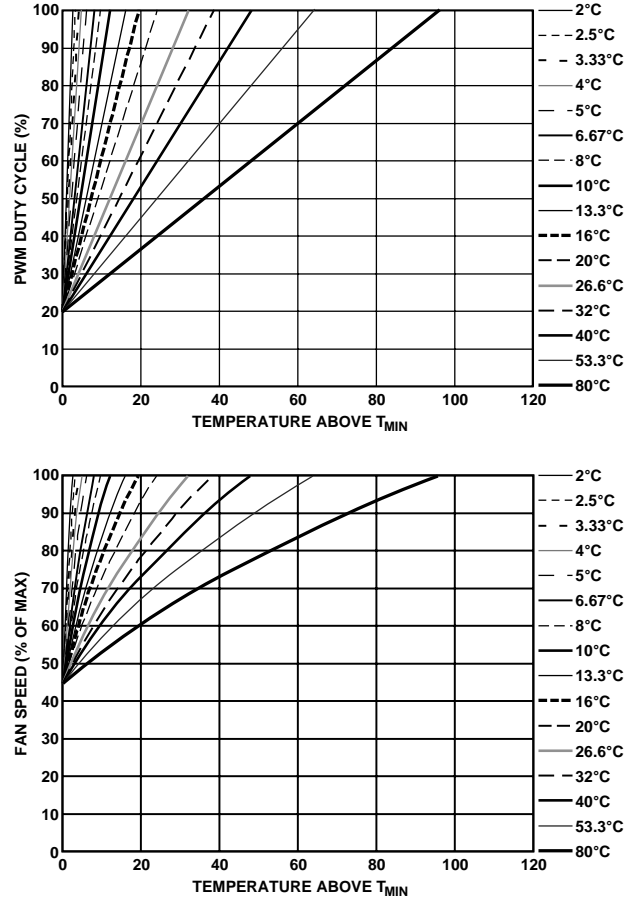


Figure 63. T_{RANGE} and % Fan Speed Slopes with PWM_{MIN} = 20%

Example: Determining T_{RANGE} for Each Temperature Channel

The following example shows how the different T_{MIN} and T_{RANGE} settings can be applied to three different thermal zones. In this example, the following T_{RANGE} values apply:

- T_{RANGE} = 80°C for ambient temperature
- T_{RANGE} = 53.3°C for CPU temperature
- T_{RANGE} = 40°C for VRM temperature

This example uses the MUX configuration described in Step 2, with the ADT7467 connected as shown in Figure 54. Both CPU temperature and VRM temperature drive the CPU fan connected to PWM1. Ambient temperature drives the front chassis fan and rear chassis fan connected to PWM2 and PWM3. The front chassis fan is configured to run at PWM_{MIN} = 20%. The rear chassis fan is configured to run at PWM_{MIN} = 30%. The CPU fan is configured to run at PWM_{MIN} = 10%.

Note on 4-Wire Fans

The control range for 4-wire fans is much wider than that of 2 wire or 3 wire fans. In many cases, 4-wire fans can start with a PWM drive of as little as 20%.

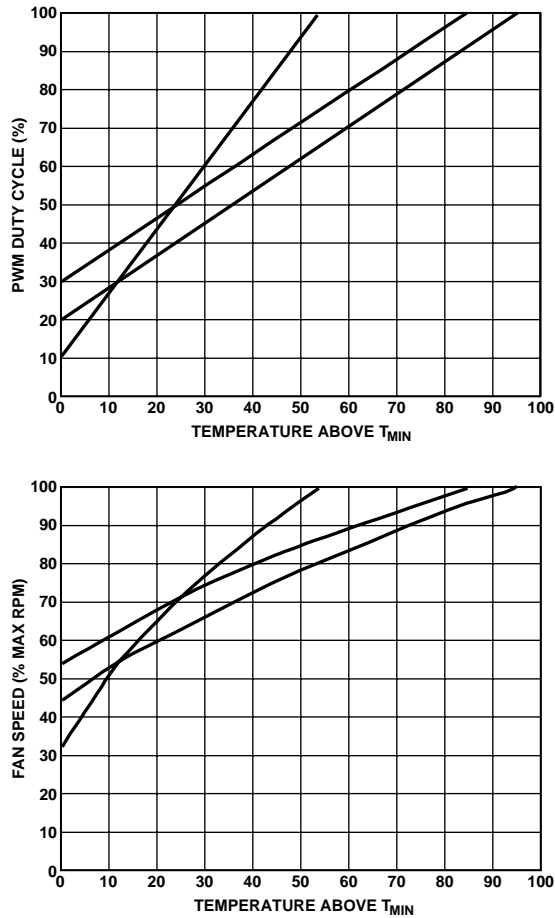


Figure 64. T_{RANGE} and % Fan Speed Slopes for VRM, Ambient, and CPU Temperature Channels

STEP 7: T_{THRESHOLD} FOR TEMPERATURE CHANNELS

T_{THRESHOLD} is the absolute maximum temperature allowed on a temperature channel. Above this temperature, a component such as the CPU or VRM might be operating beyond its safe operating limit. When the temperature measured exceeds T_{THRESHOLD}, all fans are driven at 100% PWM duty cycle (full speed) to provide critical system cooling.

The fans remain running at 100% until the temperature drops below T_{THRESHOLD} minus *hysteresis*, where *hysteresis* is the number programmed into the Hysteresis Registers 0x6D and 0x6E. The default hysteresis value is 4°C.

The T_{THRESHOLD} limit should be considered the maximum worst-case operating temperature of the system. Because exceeding any T_{THRESHOLD} limit runs all fans at 100%, it has very negative acoustic effects. Ultimately, this limit should be set up as a fail-safe, and one should ensure that it is not exceeded under normal system operating conditions.

Note that the T_{THRESHOLD} limits are nonmaskable and affect the fan speed no matter how automatic fan control settings are configured. This allows some flexibility, because a T_{RANGE} value can be selected based on its slope, while a hard limit (such as 70°C), can be programmed as T_{MAX} (the temperature at which the fan reaches full speed) by setting T_{THRESHOLD} to that limit (for example, 70°C).

THERM Registers

Reg. 0x6A, Remote 1 THERM limit = 0xA4 (100°C default)

Reg. 0x6B, Local THERM limit = 0xA4 (100°C default)

Reg. 0x6C, Remote 2 THERM limit = 0xA4 (100°C default)

Hysteresis Registers

Reg. 0x6D, Remote 1, Local Hysteresis Register

<7:4>, Remote 1 temperature hysteresis (4°C default).

<3:0>, Local temperature hysteresis (4°C default).

Reg. 0x6E, Remote 2 Temperature Hysteresis Register

<7:4>, Remote 2 temperature hysteresis (4°C default).

Because each hysteresis setting is four bits, hysteresis values are programmable from 1°C to 15°C. It is not recommended that hysteresis values ever be programmed to 0°C, because this disables hysteresis. In effect, this would cause the fans to cycle between normal speed and 100% speed, creating unsettling acoustic noise.

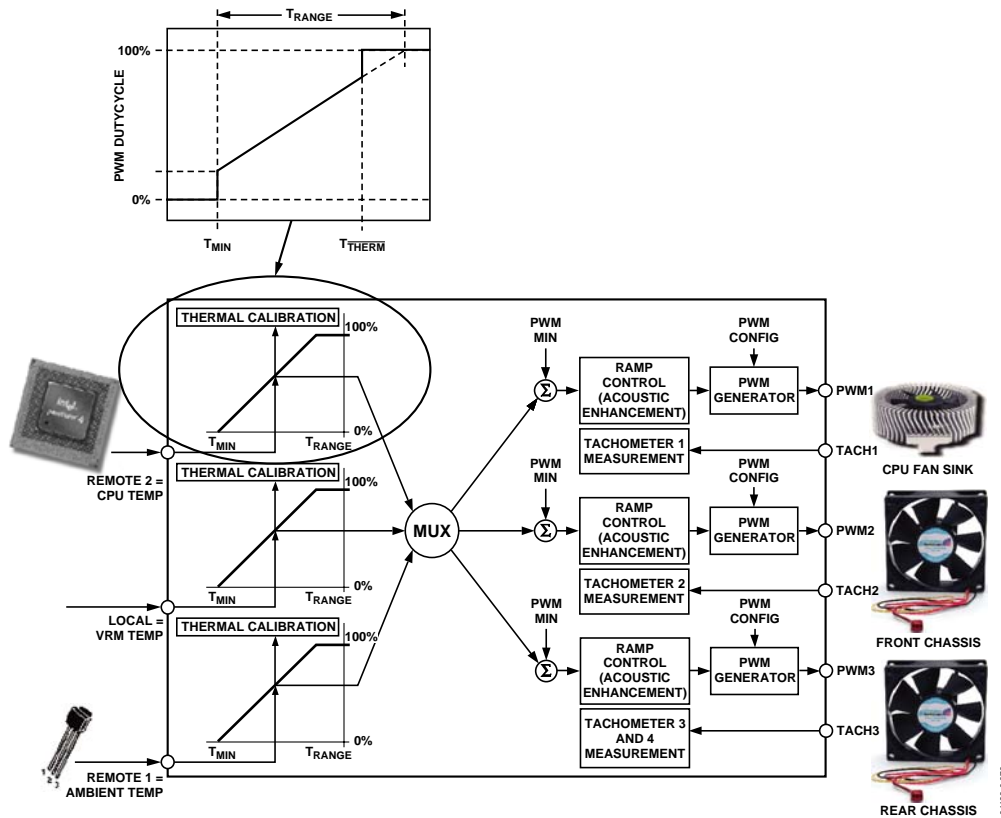


Figure 65. How T_{THERM} Relates to Automatic Fan Control

STEP 8: T_{HYST} FOR TEMPERATURE CHANNELS

T_{HYST} is the amount of extra cooling a fan provides after the temperature measured has dropped back below T_{MIN} before the fan turns off. The premise for temperature hysteresis (T_{HYST}) is that, without it, the fan would merely chatter or cycle on and off regularly whenever temperature is hovering at about the T_{MIN} setting.

The T_{HYST} value chosen determines the amount of time needed for the system to cool down or heat up as the fan is turning on and off. Values of hysteresis are programmable in the range 1°C to 15°C. Larger values of T_{HYST} prevent the fans from chattering on and off. The T_{HYST} default value is set at 4°C.

The T_{HYST} setting applies not only to the temperature hysteresis for fan on/off, but the same setting is used for the T_{THERM} hysteresis value, described in Step 6. Therefore, programming Registers 0x6D and 0x6E sets the hysteresis for both fan on/off and the T_{THERM} function.

Hysteresis Registers

Reg. 0x6D, **Remote 1, Local Hysteresis Register**

<7:4>, Remote 1 temperature hysteresis (4°C default).

<3:0>, local temperature hysteresis (4°C default).

Reg. 0x6E, **Remote 2 Temp Hysteresis Register**

<7:4>, Remote 2 temperature hysteresis (4°C default).

In some applications, it is required that fans not turn off below T_{MIN} , but remain running at PWM_{MIN} . Bits <7:5> of Enhanced Acoustics Register 1 (Reg. 0x62) allow the fans to be turned off or to be kept spinning below T_{MIN} . If the fans are always on, the T_{HYST} value has no effect on the fan when the temperature drops below T_{MIN} .

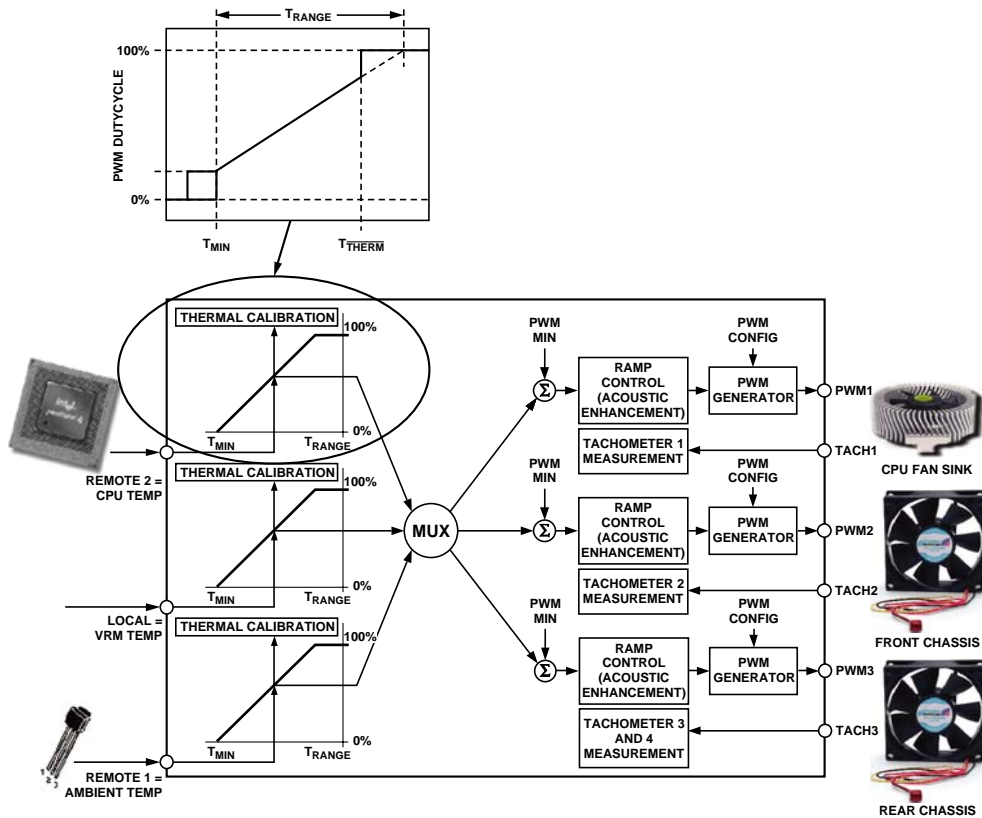


Figure 66. The T_{HYST} Value Applies to Fan On/Off Hysteresis and \overline{THERM} Hysteresis

Enhance Acoustics Register 1 (Reg. 0x62)

Bit 7 (MIN3) = 0, PWM3 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 7 (MIN3) = 1, PWM3 runs at PWM3 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 0, PWM2 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 1, PWM2 runs at PWM2 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 0, PWM1 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 1, PWM1 runs at PWM1 minimum duty cycle below $T_{MIN} - T_{HYST}$.

DYNAMIC T_{MIN} CONTROL MODE

In addition to the automatic fan speed control mode described in the Automatic Fan Control Overview section, the ADT7467 has a mode that extends the basic automatic fan speed control loop. Dynamic T_{MIN} control allows the ADT7467 to intelligently adapt the system's cooling solution for best system performance or lowest possible system acoustics, depending on user or design requirements. Use of dynamic T_{MIN} control alleviates the need to design for worst-case conditions and significantly reduces system design and validation time.

Designing for Worst-Case Conditions

System design must always allow for worst-case conditions. In PC design, the worst-case conditions include, but are not limited to the following:

- Worst-Case Altitude**
 A computer can be operated at different altitudes. The altitude affects the relative air density, which alters the effectiveness of the fan cooling solution. For example, comparing 40°C air temperature at 10,000 ft. to 20°C air temperature at sea level, relative air density is increased by 40%. This means that the fan can spin 40% slower and make less noise at sea level than at 10,000 ft. while keeping the system at the same temperature at both locations.
- Worst-Case Fan**
 Due to manufacturing tolerances, fan speeds in RPM are normally quoted with a tolerance of $\pm 20\%$. The designer needs to assume that the fan RPM can be 20% below tolerance. This translates to reduced system airflow and elevated system temperature. Note that fans 20% out of tolerance can negatively impact system acoustics, because they run faster and generate more noise.
- Worst-Case Chassis Airflow**
 The same motherboard can be used in a number of different chassis configurations. The design of the chassis and the physical location of fans and components determine the system thermal characteristics. Moreover, for a given chassis, the addition of add-in cards, cables, or other system configuration options can alter the system airflow and reduce the effectiveness of the system cooling solution. The cooling solution can also be inadvertently altered by the end user. (For example, placing a computer against a wall can block the air ducts and reduce system airflow.)

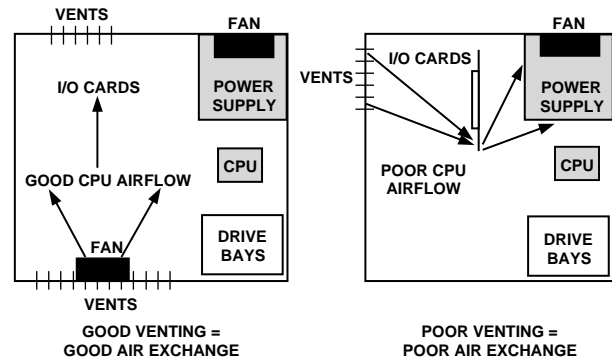


Figure 67. Chassis Airflow Issues

- Worst-Case Processor Power Consumption**
 This data sheet maximum does not necessarily reflect the true processor power consumption. Designing for worst-case CPU power consumption can result in a processor becoming overcooled (generating excess system noise).
- Worst-Case Peripheral Power Consumption**
 The tendency is to design to data sheet maximums for peripheral components (again overcooling the system).
- Worst-Case Assembly**
 Every system manufactured is unique because of manufacturing variations. Heat sinks may be loose fitting or slightly misaligned. Too much or too little thermal grease might be used, or variations in application pressure for thermal interface material could affect the efficiency of the thermal solution. Accounting for manufacturing variations in every system is difficult; therefore, the system must be designed for the worst case.

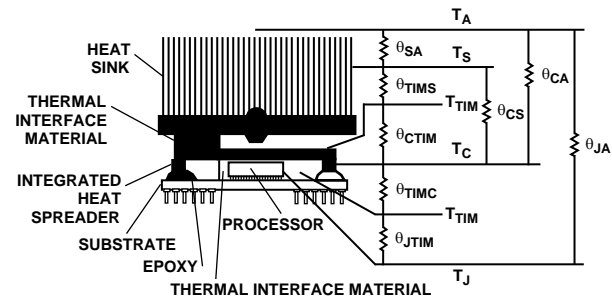


Figure 68. Thermal Model

Although a design usually accounts for worst-case conditions in all these cases, the actual system is almost never operated at worst-case conditions. The alternative to designing for the worst case is to use the dynamic T_{MIN} control function.

Dynamic T_{MIN} Control Overview

Dynamic T_{MIN} control mode builds upon the basic automatic fan control loop by adjusting the T_{MIN} value based on system performance and measured temperature. This is important, because, instead of designing for the worst case, the system thermals can be defined as operating zones. ADT7467 can self-adjust its fan control loop to maintain either an operating zone temperature or a system target temperature. For example, one can specify that the ambient temperature in a system should be maintained at 50°C. If the temperature is below 50°C, the fans might not need to run or might run very slowly. If the temperature is higher than 50°C, the fans need to throttle up.

The challenge presented by any thermal design is finding the right settings to suit the system's fan control solution. This can involve designing for the worst case, followed by weeks of system thermal characterization, and finally fan acoustic optimization (for psycho-acoustic reasons). Getting the most benefit from the automatic fan control mode involves characterizing the system to find the best T_{MIN} and T_{RANGE} settings for the control loop, and the best PWM_{MIN} value for the quietest fan speed setting. Using the ADT7467's dynamic T_{MIN} control mode, however, shortens the characterization time and alleviates tweaking the control loop settings, because the device can self-adjust during system operation.

Dynamic T_{MIN} control mode is operated by specifying the operating zone temperatures required for the system. Associated with this control mode are three operating point registers, one for each temperature channel. This allows the system thermal solution to be broken down into distinct thermal zones. For example, CPU operating temperature is 70°C, VRM operating temperature is 80°C, and ambient operating temperature is 50°C. The ADT7467 dynamically alters the control solution to maintain each zone temperature as closely as possible to its target operating point.

Operating Point Registers

Reg. 0x33, **Remote 1 Operating Point** = 0xA4 (100°C default)

Reg. 0x34, **Local Operating Point** = 0xA4 (100°C default)

Reg. 0x35, **Remote 2 Operating Point** = 0xA4 (100°C default)

Figure 69 shows an overview of the parameters that affect the operation of the dynamic T_{MIN} control loop.

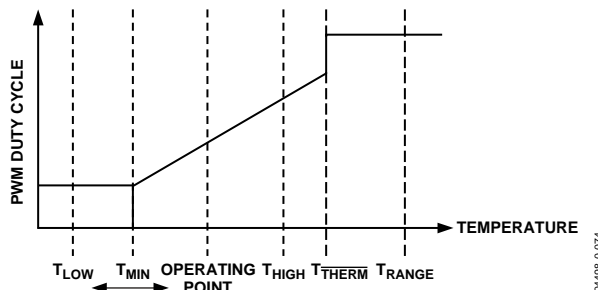


Figure 69. Dynamic T_{MIN} Control Loop

Table 14 provides a brief description of each parameter.

Table 14. T_{MIN} Control Loop Parameters

Parameter	Description
T_{LOW}	If the temperature drops below the T_{LOW} limit, an <u>error flag</u> is set in a status register and an SMBALERT interrupt can be generated.
T_{HIGH}	If the temperature exceeds the T_{HIGH} limit, an <u>error flag</u> is set in a status register and an SMBALERT interrupt can be generated.
T_{MIN}	The temperature at which the fan turns on under automatic fan speed control.
Operating point	The target temperature for a particular temperature zone. The ADT7467 attempts to maintain system temperature at about the operating point by adjusting the T_{MIN} parameter of the control loop.
T_{THERM}	If the temperature exceeds this critical limit, the fans can be run at 100% for maximum cooling.
T_{RANGE}	Programs the PWM duty cycle vs. temperature control slope.

Dynamic T_{MIN} Control Programming

Because the dynamic T_{MIN} control mode is a basic extension of the automatic fan control mode, program the automatic fan control mode parameters first, as described in Step 1 to Step 8, then proceed with dynamic T_{MIN} control mode programming.

STEP 9: OPERATING POINTS FOR TEMPERATURE CHANNELS

The operating point for each temperature channel is the optimal temperature for that thermal zone. The hotter each zone is allowed to be, the quieter the system, because the fans are not required to run as fast. The ADT7467 increases or decreases fan speeds as necessary to maintain the operating point temperature, allowing for system-to-system variation and removing the need for worst-case design. If a sensible operating point value is chosen, any T_{MIN} value can be selected in the system characterization. If the T_{MIN} value is too low, the fans run sooner than required, and the temperature is below the operating point. In response, the ADT7467 increases T_{MIN} to keep the fans off longer and to allow the temperature zone to get closer to the operating point. Likewise, too high a T_{MIN} value causes

the operating point to be exceeded, and in turn, the ADT7467 reduces T_{MIN} to turn the fans on sooner to cool the system.

Programming Operating Point Registers

There are three operating point registers, one for each temperature channel. These 8-bit registers allow the operating point temperatures to be programmed with 1°C resolution.

Operating Point Registers

Reg. 0x33, **Remote 1 Operating Point** = 0xA4 (100°C default)

Reg. 0x34, **Local Operating Point** = 0xA4 (100°C default)

Reg. 0x35, **Remote 2 Operating Point** = 0xA4 (100°C default)

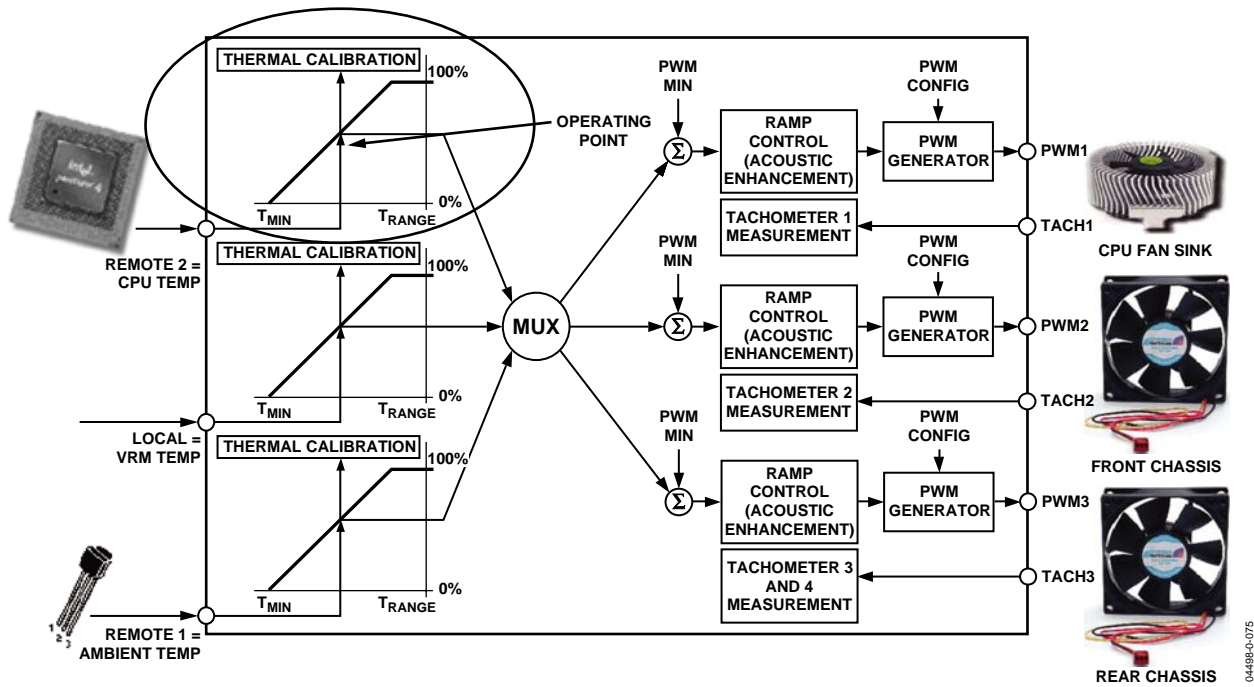


Figure 70. Operating Point Value Dynamically Adjusts Automatic Fan Control Settings

STEP 10: HIGH AND LOW LIMITS FOR TEMPERATURE CHANNELS

The low limit defines the temperature at which the T_{MIN} value starts to be increased, if temperature falls below this value. This has the net effect of reducing the fan speed, allowing the system to get hotter. An interrupt can be generated when the temperature drops below the low limit.

The high limit defines the temperature at which the T_{MIN} value starts to be reduced, if temperature increases above this value. This has the net effect of increasing fan speed to cool down the system. An interrupt can be generated when the temperature rises above the high limit.

Programming High and Low Limits

There are six limit registers; a high limit and low limit are associated with each temperature channel. These 8-bit registers allow the high and low limit temperatures to be programmed with 1°C resolution.

Temperature Limit Registers

Reg. 0x4E, Remote 1 Temperature Low Limit = 0x01

Reg. 0x4F, Remote 1 Temperature High Limit = 0x7F

Reg. 0x50, Local Temperature Low Limit = 0x01

Reg. 0x51, Local Temperature High Limit = 0x7F

Reg. 0x52, Remote 2 Temperature Low Limit = 0x01

Reg. 0x53, Remote 2 Temperature High Limit = 0x7F

How Dynamic T_{MIN} Control Works

The basic premise is as follows:

1. Set the target temperature for the temperature zone, which could be, for example, the Remote 1 thermal diode. This value is programmed to the Remote 1 operating temperature register.
2. As the temperature in that zone (Remote 1 temperature) rises toward and exceeds the operating point temperature, T_{MIN} is reduced and the fan speed increases.
3. As the temperature drops below the operating point temperature, T_{MIN} is increased and the fan speed is reduced.

However, the loop operation is not as simple as described in these steps. A number of conditions govern the situations in which T_{MIN} can increase or decrease.

Short Cycle and Long Cycle

The ADT7467 implements two loops: a short cycle and a long cycle. The short cycle takes place every n monitoring cycles. The long cycle takes place every $2n$ monitoring cycles. The value of n is programmable for each temperature channel. The bits are located at the following register locations:

Remote 1 = CYR1 = Bits <2:0> of Calibration Control Register 2 (Address = 0x37).

Local = CYL = Bits <5:3> of Calibration Control Register 2 (Address = 0x37).

Remote 2 = CYR2 = Bits <7:6> of Calibration Control Register 2 and Bit 0 of Calibration Control Register 1 (Address = 0x36).

Table 15. Cycle Bit Assignments

Code	Short Cycle		Long Cycle	
000	8 cycles	(1 s)	16 cycles	(2 s)
001	16 cycles	(2 s)	32 cycles	(4 s)
010	32 cycles	(4 s)	64 cycles	(8 s)
011	64 cycles	(8 s)	128 cycles	(16 s)
100	128 cycles	(16 s)	256 cycles	(32 s)
101	256 cycles	(32 s)	512 cycles	(64 s)
110	512 cycles	(64 s)	1024 cycles	(128 s)
111	1024 cycles	(128 s)	2048 cycles	(256 s)

Care should be taken when choosing the cycle time. A long cycle time means that T_{MIN} is updated less often. If your system has very fast temperature transients, the dynamic T_{MIN} control loop will always be lagging. If you choose a cycle time that is too fast, the full benefit of changing T_{MIN} might not be realized and needs to change again on the next cycle; in effect, it is over-shooting. It is necessary to carry out some calibration to identify the most suitable response time.

Figure 71 shows the steps taken during the short cycle.

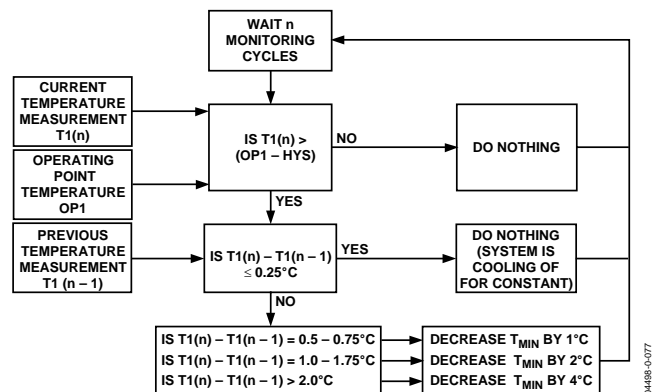


Figure 71. Short Cycle Steps

Figure 72 shows the steps taken during the long cycle.

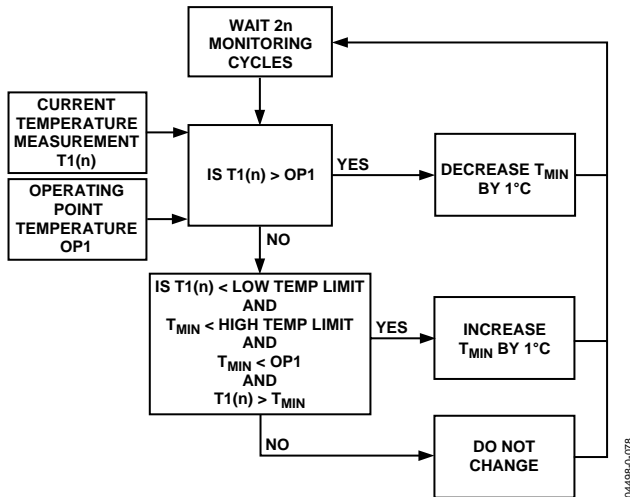


Figure 72. Long Cycle Steps

The following examples illustrate some of the circumstances that might cause T_{MIN} to increase, decrease, or stay the same.

Example: Normal Operation—No T_{MIN} Adjustment

1. If measured temperature never exceeds the programmed operating point minus the hysteresis temperature, then T_{MIN} is not adjusted, that is, remains at its current setting.
2. If measured temperature never drops below the low temperature limit, then T_{MIN} is not adjusted.

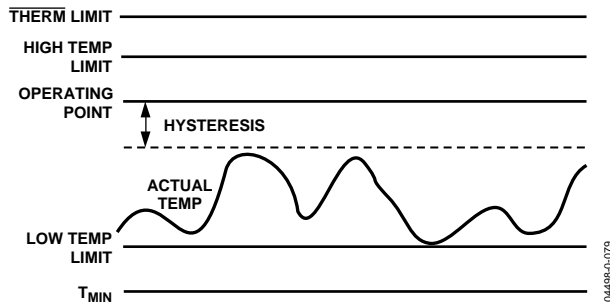


Figure 73. Temperature between Operating Point and Low Temperature Limit

Because neither the operating point minus the hysteresis temperature nor the low temperature limit has been exceeded, the T_{MIN} value is not adjusted, and the fan runs at a speed determined by the fixed T_{MIN} and T_{RANGE} values defined in the automatic fan speed control mode.

Example: Operating Point Exceeded— T_{MIN} Reduced

When the measured temperature is below the operating point temperature minus the hysteresis, T_{MIN} remains the same.

Once the temperature exceeds the operating temperature minus the hysteresis ($OP - Hyst$), T_{MIN} starts to decrease. This occurs during the short cycle (see Figure 71). The rate at which T_{MIN} decreases depends on the programmed value of n . It also

depends on how much the temperature has increased between this monitoring cycle and the last monitoring cycle, that is, if the temperature has increased by $1^{\circ}C$, then T_{MIN} is reduced by $2^{\circ}C$. Decreasing T_{MIN} has the effect of increasing the fan speed, thus providing more cooling to the system.

If the temperature is slowly increasing only in the range ($OP - Hyst$), that is, $\leq 0.25^{\circ}C$ per short monitoring cycle, then T_{MIN} does not decrease. This allows small changes in temperature in the desired operating zone without changing T_{MIN} . The long cycle makes no change to T_{MIN} in the temperature range ($OP - Hyst$), because the temperature has not exceeded the operating temperature.

Once the temperature exceeds the operating temperature, the long cycle causes T_{MIN} to be reduced by $1^{\circ}C$ every long cycle while the temperature remains above the operating temperature. This takes place in addition to the decrease in T_{MIN} that would occur due to the short cycle. In Figure 74, because the temperature is increasing at a rate $\leq 0.25^{\circ}C$ per short cycle, no reduction in T_{MIN} takes place during the short cycle.

Once the temperature has fallen below the operating temperature, T_{MIN} stays the same. Even when the temperature starts to increase slowly, T_{MIN} stays the same, because the temperature increases at a rate $\leq 0.25^{\circ}C$ per cycle.

Example: Increase T_{MIN} Cycle

When the temperature drops below the low temperature limit, T_{MIN} can increase in the long cycle. Increasing T_{MIN} has the effect of running the fan slower and, therefore, quieter. The long cycle diagram in Figure 25 shows the conditions that need to be true for T_{MIN} to increase. Here is a quick summary of those conditions and the reasons they need to be true.

T_{MIN} can increase, if

1. The measured temperature has fallen below the low temperature limit. This means the user must choose the low limit carefully. It should not be so low that the temperature never falls below it, because T_{MIN} would never increase and the fans would run faster than necessary.
2. T_{MIN} is below the high temperature limit. T_{MIN} is never allowed to increase above the high temperature limit. As a result, the high limit should be sensibly chosen, because it determines how high T_{MIN} can go.
3. T_{MIN} is below the operating point temperature. T_{MIN} should never be allowed to increase above the operating point temperature, because the fans would not switch on until the temperature rose above the operating point.
4. The temperature is above T_{MIN} . The dynamic T_{MIN} control is turned off below T_{MIN} .

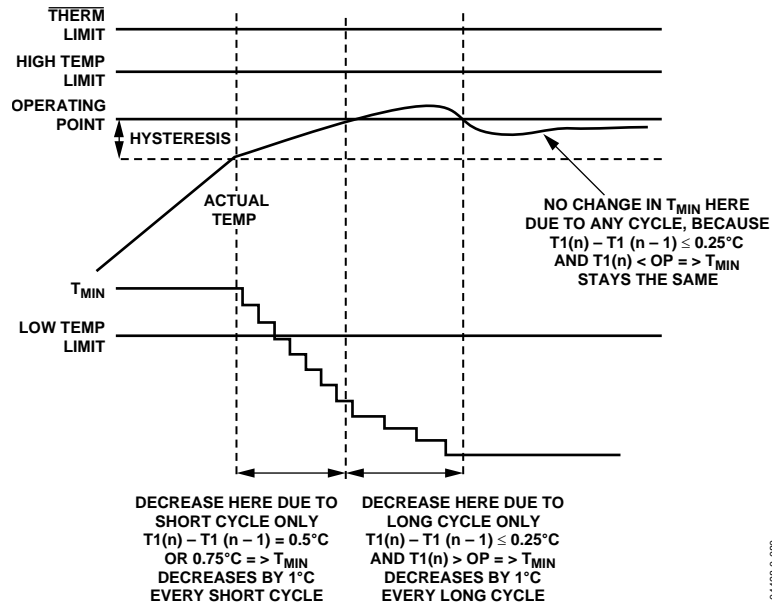


Figure 74. Effect of Exceeding Operating Point Minus Hysteresis Temperature

Figure 75 shows how T_{MIN} increases when the current temperature is above T_{MIN} and below the low temperature limit, and T_{MIN} is below the high temperature limit and below the operating point. Once the temperature rises above the low temperature limit, T_{MIN} stays the same.

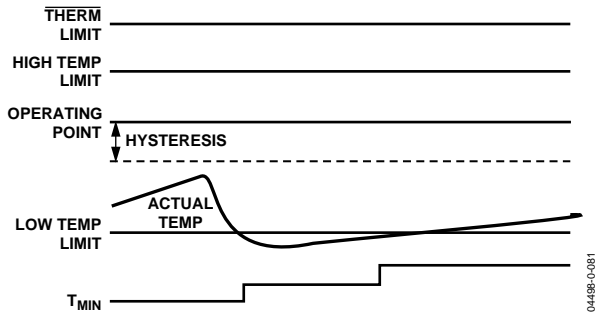


Figure 75. Increasing T_{MIN} for Quieter Operation

Example: Preventing T_{MIN} from Reaching Full Scale

Because T_{MIN} is dynamically adjusted, it is undesirable for T_{MIN} to reach full scale (127°C), because the fan would never switch on. As a result, T_{MIN} is allowed to vary only within a specified range:

1. The lowest possible value for T_{MIN} is -127°C (twos complement mode) or -64°C (Offset 64 mode).
2. T_{MIN} cannot exceed the high temperature limit.
3. If the temperature is below T_{MIN} , the fan is switched off or is running at minimum speed and dynamic T_{MIN} control is disabled.

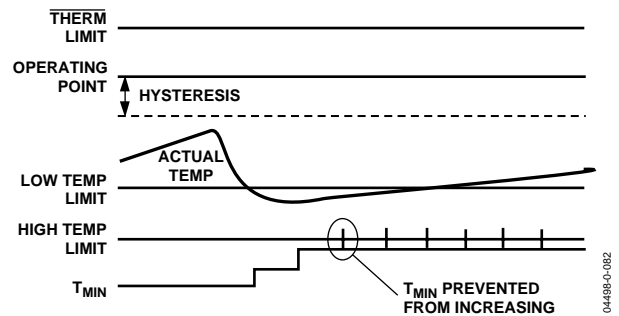


Figure 76. T_{MIN} Adjustments Limited by the High Temperature Limit

STEP 11: MONITORING THERM

Using the operating point limit ensures that the dynamic T_{MIN} control mode is operating in the best possible acoustic position while ensuring that the temperature never exceeds the maximum operating temperature. Using the operating point limit allows T_{MIN} to be independent of system-level issues because of its self-corrective nature. In PC design, the operating point for the chassis is usually the worst-case internal chassis temperature.

The optimal operating point for the processor is determined by monitoring the thermal monitor in the Intel Pentium 4 processor. To do this, the PROCHOT output of the Pentium 4 is connected to the THERM input of the ADT7467.

The operating point for the processor can be determined by allowing the current temperature to be copied to the operating point register when the PROCHOT output pulls the THERM input low on the ADT7467. This gives the maximum temperature at which the Pentium 4 can run before clock modulation occurs.

Enabling the $\overline{\text{THERM}}$ Trip Point as the Operating Point

Bits <4:2> of dynamic T_{MIN} control Register 1 (Reg. 0x36) enable/disable $\overline{\text{THERM}}$ monitoring to program the operating point.

Dynamic T_{MIN} Control Register 1 (0x36)

<2> **PHTR2 = 1**, copies the Remote 2 current temperature to the Remote 2 operating point register, if $\overline{\text{THERM}}$ is asserted. The operating point contains the temperature at which $\overline{\text{THERM}}$ is asserted. This allows the system to run as quietly as possible without affecting system performance.

PHTR2 = 0, ignores any $\overline{\text{THERM}}$ assertions. The Remote 2 operating point register reflects its programmed value.

<3> **PHTL = 1**, copies the local current temperature to the local temperature operating point register, if $\overline{\text{THERM}}$ is asserted. The operating point contains the temperature at which $\overline{\text{THERM}}$ is asserted. This allows the system to run as quietly as possible without affecting system performance.

PHTL = 0, ignores any $\overline{\text{THERM}}$ assertions. The local temperature operating point register reflects its programmed value.

<4> **PHTR1 = 1**, copies the Remote 1 current temperature to the Remote 1 operating point register, if $\overline{\text{THERM}}$ is asserted. The operating point contains the temperature at which $\overline{\text{THERM}}$ is asserted. This allows the system to run as quietly as possible without affecting system performance.

PHTR1 = 0, ignores any $\overline{\text{THERM}}$ assertions. The Remote 1 operating point register reflects its programmed value.

Enabling Dynamic T_{MIN} Control Mode

Bits <7:5> of dynamic T_{MIN} control Register 1 (Reg. 0x36) enable/disable dynamic T_{MIN} control on the temperature channels.

Dynamic T_{MIN} Control Register 1 (0x36)

<5> **R2T = 1**, enables dynamic T_{MIN} control on the Remote 2 temperature channel. The chosen T_{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for this zone.

R2T = 0, disables dynamic T_{MIN} control. The T_{MIN} value chosen is not adjusted and the channel behaves as described in the Automatic Fan Control Overview section.

<6> **LT = 1**, enables dynamic T_{MIN} control on the local temperature channel. The chosen T_{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for this zone.

LT = 0, disables dynamic T_{MIN} control. The T_{MIN} value chosen is not adjusted and the channel behaves as described in the Automatic Fan Control Overview section.

<7> **R1T = 1**, enables dynamic T_{MIN} control on the Remote 1 temperature channel. The chosen T_{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for this zone.

R1T = 0, disables dynamic T_{MIN} control. The T_{MIN} value chosen is not adjusted and the channel behaves as described in the Automatic Fan Control Overview section.

ENHANCING SYSTEM ACOUSTICS

Automatic fan speed control mode reacts instantaneously to changes in temperature, that is, the PWM duty cycle responds immediately to temperature change. Any impulses in temperature can cause an impulse in fan noise. For psycho-acoustic reasons, the ADT7467 can prevent the PWM output from reacting instantaneously to temperature changes. Enhanced acoustic mode controls the maximum change in PWM duty cycle at a given time. The objective is to prevent the fan from cycling up and down, annoying the user.

Acoustic Enhancement Mode Overview

Figure 77 gives a top-level overview of the automatic fan control circuitry on the ADT7467 and shows where acoustic enhancement fits in. Acoustic enhancement is intended as a postdesign tweak made by a system or mechanical engineer evaluating best settings for the system. Having determined the optimal settings for the thermal solution, the engineer can adjust the system acoustics. The goal is to implement a system that is acoustically pleasing without causing user annoyance due to fan cycling. It is important to realize that although a system might pass an acoustic noise requirement specification (for example, 36 dB), if the fan is annoying, it fails the consumer test.

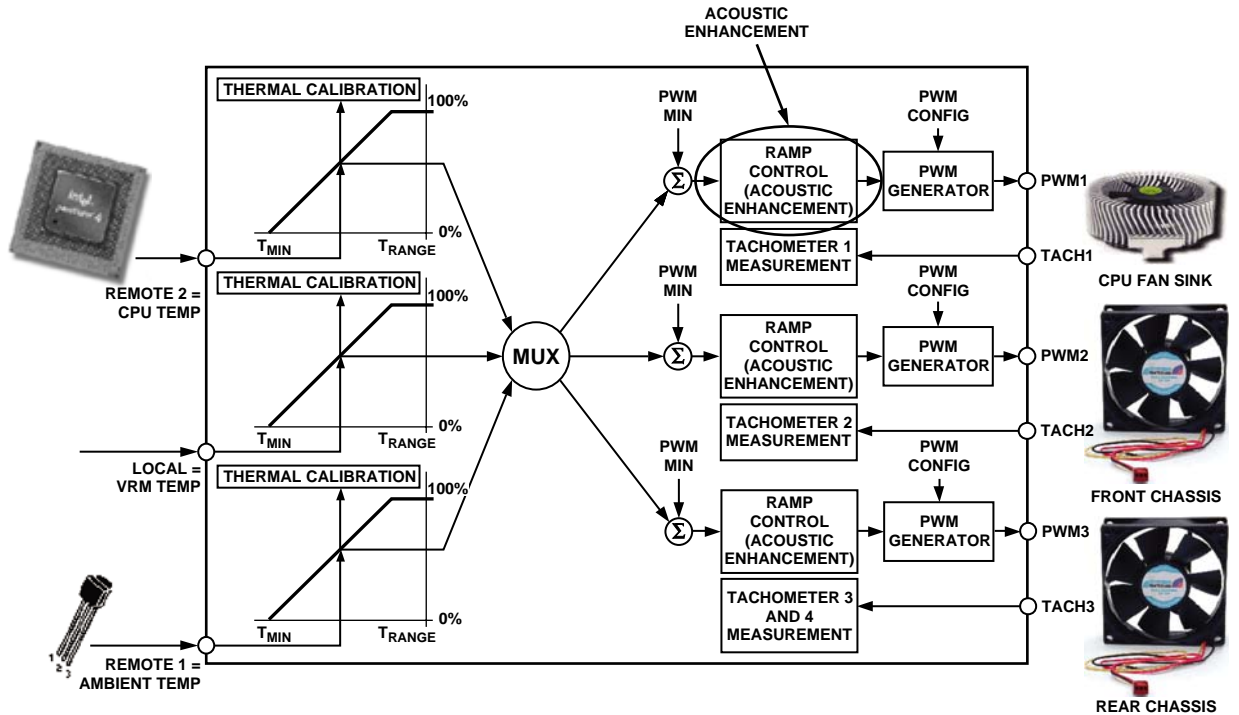


Figure 77. Acoustic Enhancement Smooths Fan Speed Variations under Automatic Fan Speed Control

Approaches to System Acoustic Enhancement

There are two different approaches to implementing system acoustic enhancement: temperature-centric and fan-centric.

The temperature-centric approach involves smoothing transient temperatures as they are measured by a temperature source (for example, Remote 1 temperature). The temperature values used to calculate the PWM duty cycle values are smoothed, reducing fan speed variation. However, this approach causes an inherent delay in updating fan speed and causes the thermal characteristics of the system to change. It also causes the system fans to stay on longer than necessary, because the fan's reaction is merely delayed. The user has no control over noise from different fans driven by the same temperature source. Consider, for example, a system in which control of a CPU cooler fan (on PWM1) and a chassis fan (on PWM2) use Remote 1 temperature. Because the Remote 1 temperature is smoothed, both fans are updated at exactly the same rate. If the chassis fan is much louder than the CPU fan, there is no way to improve its acoustics without changing the thermal solution of the CPU cooling fan.

The fan-centric approach to system acoustic enhancement controls the PWM duty cycle, driving the fan at a fixed rate (for example, 6%). Each time the PWM duty cycle is updated, it is incremented by a fixed 6%. As a result, the fan ramps smoothly to its newly calculated speed. If the temperature starts to drop, the PWM duty cycle immediately decreases by 6% at every update. Therefore, the fan ramps smoothly up or down without

inherent system delay. Consider, for example, controlling the same CPU cooler fan (on PWM1) and chassis fan (on PWM2) using Remote 1 temperature. The T_{MIN} and T_{RANGE} settings have already been defined in automatic fan speed control mode, that is, thermal characterization of the control loop has been optimized. Now the chassis fan is noisier than the CPU cooling fan. Using the fan-centric approach, PWM2 can be placed into acoustic enhancement mode independently of PWM1. The acoustics of the chassis fan can, therefore, be adjusted without affecting the acoustic behavior of the CPU cooling fan, even though both fans are controlled by Remote 1 temperature. The fan-centric approach is how acoustic enhancement works on the ADT7467.

Enabling Acoustic Enhancement for Each PWM Output

Enhance Acoustics Register 1 (Reg. 0x62)

<3> = 1, enables acoustic enhancement on PWM1 output.

Enhance Acoustics Register 2 (Reg. 0x63)

<7> = 1, enables acoustic enhancement on PWM2 output.

<3> = 1, enables acoustic enhancement on PWM3 output.

Effect of Ramp Rate on Enhanced Acoustics Mode

The PWM signal driving the fan has a period, T , given by the PWM drive frequency, f , because $T = 1/f$. For a given PWM period, T , the PWM period is subdivided into 255 equal time slots. One time slot corresponds to the smallest possible increment in the PWM duty cycle. A PWM signal of 33% duty

cycle is, therefore, high for $1/3 \times 255$ time slots and low for $2/3 \times 255$ time slots. Therefore, a 33% PWM duty cycle corresponds to a signal that is high for 85 time slots and low for 170 time slots.

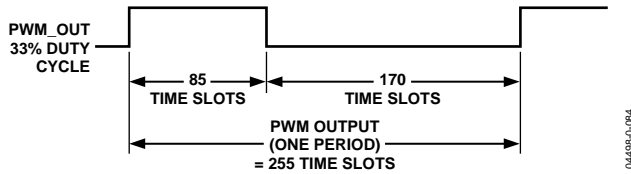


Figure 78. 33% PWM Duty Cycle Represented in Time Slots

The ramp rates in the enhanced acoustics mode are selectable from the values 1, 2, 3, 5, 8, 12, 24, and 48. The ramp rates are discrete time slots. For example, if the ramp rate is 8, then eight time slots are added to the PWM high duty cycle each time the PWM duty cycle needs to be increased. If the PWM duty cycle value needs to be decreased, it is decreased by eight time slots. Figure 79 shows how the enhanced acoustics mode algorithm operates.

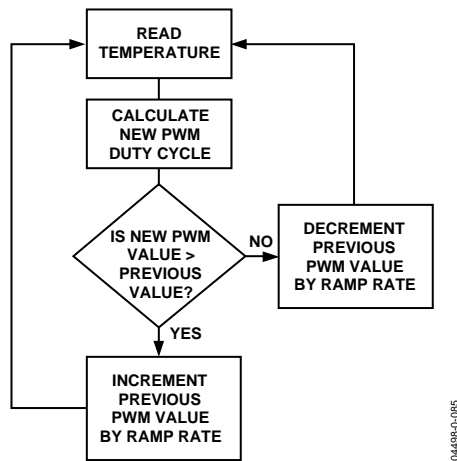


Figure 79. Enhanced Acoustics Algorithm

The enhanced acoustics mode algorithm calculates a new PWM duty cycle based on the temperature measured. If the new PWM duty cycle value is greater than the previous PWM value, then the previous PWM duty cycle value is incremented by either 1, 2, 3, 5, 8, 12, 24, or 48 time slots, depending on the settings of the enhance acoustics registers. If the new PWM duty cycle value is less than the previous PWM value, then the previous PWM duty cycle is decremented by 1, 2, 3, 5, 8, 12, 24, or 48 time slots. Each time the PWM duty cycle is incremented or decremented, its value is stored as the previous PWM duty cycle for the next comparison. A ramp rate of 1 corresponds to one time slot, which is $1/255$ of the PWM period. In enhanced acoustics mode, incrementing or decrementing by 1 changes the PWM output by $1/255 \times 100\%$.

STEP 12: RAMP RATE FOR ACOUSTIC ENHANCEMENT

The optimal ramp rate for acoustic enhancement can be found through system characterization after the thermal optimization has been finished. The effect of each ramp rate should be logged, if possible, to determine the best setting for a given solution.

Enhanced Acoustics Register 1 (Reg. 0x62)

<2:0> ACOU, selects the ramp rate for PWM1.

- 000 = 1 time slot = 35 s
- 001 = 2 time slots = 17.6 s
- 010 = 3 time slots = 11.8 s
- 011 = 5 time slots = 7 s
- 100 = 8 time slots = 4.4 s
- 101 = 12 time slots = 3 s
- 110 = 24 time slots = 1.6 s
- 111 = 48 time slots = 0.8 s

Enhance Acoustics Register 2 (Reg. 0x63)

<2:0> ACOU3, selects the ramp rate for PWM3.

- 000 = 1 time slot = 35 s
- 001 = 2 time slots = 17.6 s
- 010 = 3 time slots = 11.8 s
- 011 = 5 time slots = 7 s
- 100 = 8 time slots = 4.4 s
- 101 = 12 time slots = 3 s
- 110 = 24 time slots = 1.6 s
- 111 = 48 time slots = 0.8 s

<6:4> ACOU2, selects the ramp rate for PWM2.

- 000 = 1 time slot = 35 s
- 001 = 2 time slots = 17.6 s
- 010 = 3 time slots = 11.8 s
- 011 = 5 time slots = 7 s
- 100 = 8 time slots = 4.4 s
- 101 = 12 time slots = 3 s
- 110 = 24 time slots = 1.6 s
- 111 = 48 time slots = 0.8 s

Another way to view the ramp rates is to measure the time it takes for the PWM output to ramp up from 0% to 100% duty cycle for an instantaneous change in temperature. This can be tested by putting the ADT7467 into manual mode and changing the PWM output from 0% to 100% PWM duty cycle. The PWM output takes 35 s to reach 100%, when a ramp rate of 1 time slot is selected.

Figure 80 shows remote temperature plotted against PWM duty cycle for enhanced acoustics mode. The ramp rate is set to 48, which corresponds to the fastest ramp rate. Assume that a new temperature reading is available every 115 ms. With these settings, it takes approximately 0.76 s to go from 33% duty cycle to 100% duty cycle (full speed). Even though the temperature increases very rapidly, the fan ramps up to full speed gradually.

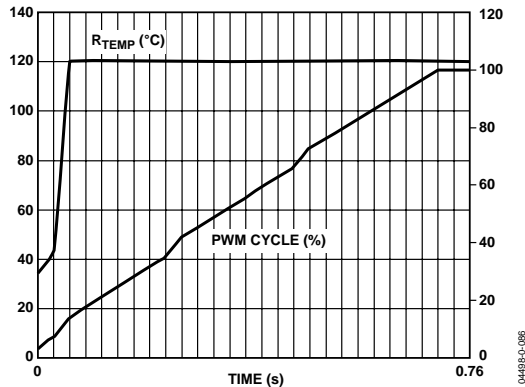


Figure 80. Enhanced Acoustics Mode with Ramp Rate = 48

Figure 81 shows how changing the ramp rate from 48 to 8 affects the control loop. The overall response of the fan is slower. Because the ramp rate is reduced, it takes longer for the fan to achieve full running speed. In this case, it takes approximately 4.4 s for the fan to reach full speed.

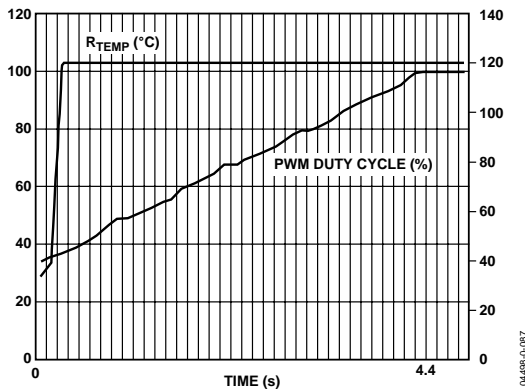


Figure 81. Enhanced Acoustics Mode with Ramp Rate = 8

Figure 82 shows the PWM output response for a ramp rate of 2. In this instance, the fan took about 17.6 s to reach full running speed.

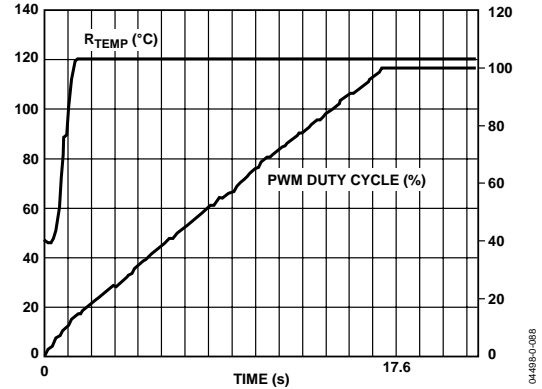


Figure 82. Enhanced Acoustics Mode with Ramp Rate = 2

Figure 83 shows how the control loop reacts to temperature with the slowest ramp rate. The ramp rate is set to 1, while all other control parameters remain the same. With the slowest ramp rate selected, it takes 35 s for the fan to reach full speed.

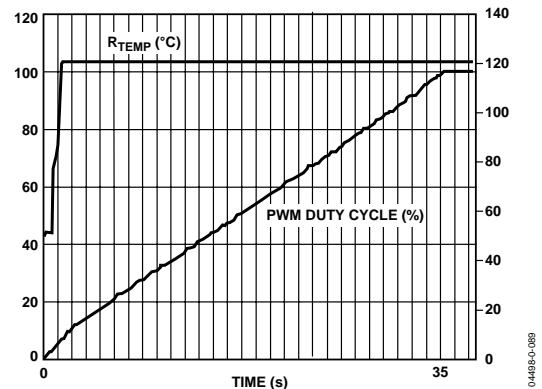


Figure 83. Enhanced Acoustics Mode with Ramp Rate = 1

As Figure 80 to Figure 83 show, the rate at which the fan reacts to temperature change is dependent on the ramp rate selected in the enhanced acoustics registers. The higher the ramp rate, the faster the fan reaches the newly calculated fan speed.

Figure 84 shows the behavior of the PWM output as temperature varies. As the temperature increases, the fan speed ramps up. Small drops in temperature do not affect the ramp-up function, because the newly calculated fan speed is still higher than the previous PWM value. Enhanced acoustics mode allows the PWM output to be made less sensitive to temperature variations. This is dependent on the ramp rate selected and programmed into the enhanced acoustics registers.

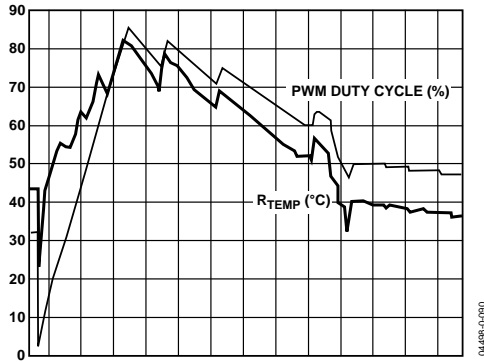


Figure 84. How Fan Reacts to Temperature Variation in Enhanced Acoustics Mode

Slower Ramp Rates

The ADT7467 can be programmed for much longer ramp times by slowing the ramp rates. Each ramp rate can be slowed by a factor of 4.

PWM1 Configuration Register (Reg. 0x5C)

<3> SLOW, 1 slows the ramp rate for PWM1 by 4.

PWM2 Configuration Register (Reg. 0x5D)

<3> SLOW, 1 slows the ramp rate for PWM2 by 4.

PWM3 Configuration Register (Reg. 0x5E)

<3> SLOW, 1 slows the ramp rate for PWM3 by 4.

The following sections list the ramp-up times when the SLOW bit is set for each PWM output.

Enhanced Acoustics Register 1 (Reg. 0x62)

<2:0> ACOU, selects the ramp rate for PWM1.

- 000 = 140 s
- 001 = 70.4 s
- 010 = 47.2 s
- 011 = 28 s
- 100 = 17.6 s
- 101 = 12 s
- 110 = 6.4 s
- 111 = 3.2 s

Enhance Acoustics Register 2 (Reg. 0x63)

<2:0> ACOU3, selects the ramp rate for PWM3.

- 000 = 140 s
- 001 = 70.4 s
- 010 = 47.2 s
- 011 = 28 s
- 100 = 17.6 s
- 101 = 12 s
- 110 = 6.4 s
- 111 = 3.2 s

<6:4> ACOU2, selects the ramp rate for PWM2.

- 000 = 140 s
- 001 = 70.4 s
- 010 = 47.2 s
- 011 = 28 s
- 100 = 17.6 s
- 101 = 12 s
- 110 = 6.4 s
- 111 = 3.2 s

REGISTER TABLES

Table 16. ADT7467 Registers

Address	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Lockable?
0x21	R	V _{ccp} Reading	9	8	7	6	5	4	3	2	0x00	
0x22	R	V _{cc} Reading	9	8	7	6	5	4	3	2	0x00	
0x25	R	Remote 1 Temperature	9	8	7	6	5	4	3	2	0x01	
0x26	R	Local Temperature	9	8	7	6	5	4	3	2	0x01	
0x27	R	Remote 2 Temperature	9	8	7	6	5	4	3	2	0x01	
0x28	R	TACH1 Low Byte	7	6	5	4	3	2	1	0	0x00	
0x29	R	TACH1 High Byte	15	14	13	12	11	10	9	8	0x00	
0x2A	R	TACH2 Low Byte	7	6	5	4	3	2	1	0	0x00	
0x2B	R	TACH2 High Byte	15	14	13	12	11	10	9	8	0x00	
0x2C	R	TACH3 Low Byte	7	6	5	4	3	2	1	0	0x00	
0x2D	R	TACH3 High Byte	15	14	13	12	11	10	9	8	0x00	
0x2E	R	TACH4 Low Byte	7	6	5	4	3	2	1	0	0x00	
0x2F	R	TACH4 High Byte	15	14	13	12	11	10	9	8	0x00	
0x30	R/W	PWM1 Current Duty Cycle	7	6	5	4	3	2	1	0	0x00	
0x31	R/W	PWM2 Current Duty Cycle	7	6	5	4	3	2	1	0	0x00	
0x32	R/W	PWM3 Current Duty Cycle	7	6	5	4	3	2	1	0	0x00	
0x33	R/W	Remote 1 Operating Point	7	6	5	4	3	2	1	0	0xA4	Yes
0x34	R/W	Local Temp Operating Point	7	6	5	4	3	2	1	0	0xA4	Yes
0x35	R/W	Remote 2 Operating Point	7	6	5	4	3	2	1	0	0xA4	Yes
0x36	R/W	Dynamic T _{MIN} Control Reg. 1	R2T	LT	R1T	PHTR2	PHTL	PHTR1	V _{ccp} LO	CYR2	0x00	Yes
0x37	R/W	Dynamic T _{MIN} Control Reg. 2	CYR2	CYR2	CYL	CYL	CYL	CYR1	CYR1	CYR1	0x00	Yes
0x38	R/W	Max PWM 1 Duty Cycle	7	6	5	4	3	2	1	0	0xFF	
0x39	R/W	Max PWM 2 Duty Cycle	7	6	5	4	3	2	1	0	0xFF	
0x3A	R/W	Max PWM 3 Duty Cycle	7	6	5	4	3	2	1	0	0xFF	
0x3D	R	Device ID Register	7	6	5	4	3	2	1	0	0x68	
0x3E	R	Company ID Number	7	6	5	4	3	2	1	0	0x41	
0x3F	R	Revision Number	VER	VER	VER	VER	STP	STP	STP	STP	0x70	
0x40	R/W	Configuration Register 1	V _{cc}	TODIS	FSPDIS	Vxl	FSPD	RDY	LOCK	STRT	0x01	Yes

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Address	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Lockable?
0x41	R	Interrupt Status Register 1	OOL	R2T	LT	R1T	RES	V _{CC}	V _{CCP}	RES	0x00	
0x42	R	Interrupt Status Register 2	D2	D1	F4P	FAN3	FAN2	FAN1	OVT	RES	0x00	
0x46	R/W	V _{CCP} Low Limit	7	6	5	4	3	2	1	0	0x00	
0x47	R/W	V _{CCP} High Limit	7	6	5	4	3	2	1	0	0xFF	
0x48	R/W	V _{CC} Low Limit	7	6	5	4	3	2	1	0	0x00	
0x49	R/W	V _{CC} High Limit	7	6	5	4	3	2	1	0	0xFF	
0x4E	R/W	Remote 1 Temp Low Limit	7	6	5	4	3	2	1	0	0x01	
0x4F	R/W	Remote 1 Temp High Limit	7	6	5	4	3	2	1	0	0x7F	
0x50	R/W	Local Temp Low Limit	7	6	5	4	3	2	1	0	0x01	
0x51	R/W	Local Temp High Limit	7	6	5	4	3	2	1	0	0x7F	
0x52	R/W	Remote 2 Temp Low Limit	7	6	5	4	3	2	1	0	0x01	
0x53	R/W	Remote 2 Temp High Limit	7	6	5	4	3	2	1	0	0x7F	
0x54	R/W	TACH1 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	
0x55	R/W	TACH1 Minimum High Byte	15	14	13	12	11	10	9	8	0xFF	
0x56	R/W	TACH2 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	
0x57	R/W	TACH2 Minimum High Byte	15	14	13	12	11	10	9	8	0xFF	
0x58	R/W	TACH3 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	
0x59	R/W	TACH3 Minimum High Byte	15	14	13	12	11	10	9	8	0xFF	
0x5A	R/W	TACH4 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	
0x5B	R/W	TACH4 Minimum High Byte	15	14	13	12	11	10	9	8	0xFF	
0x5C	R/W	PWM1 Configuration Register	BHVR	BHVR	BHVR	INV	SLOW	SPIN	SPIN	SPIN	0x82	Yes
0x5D	R/W	PWM2 Configuration Register	BHVR	BHVR	BHVR	INV	SLOW	SPIN	SPIN	SPIN	0x82	Yes
0x5E	R/W	PWM3 Configuration Register	BHVR	BHVR	BHVR	INV	SLOW	SPIN	SPIN	SPIN	0x82	Yes
0x5F	R/W	Remote 1 T _{RANGE} /PWM1 Frequency	RANGE	RANGE	RANGE	RANGE	THRM	FREQ	FREQ	FREQ	0XC4	Yes
0x60	R/W	Local T _{RANGE} /PWM2 Frequency	RANGE	RANGE	RANGE	RANGE	THRM	FREQ	FREQ	FREQ	0XC4	Yes

Address	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Lockable?
0x61	R/W	Remote 2 T _{RANGE} /PWM3 Frequency	RANGE	RANGE	RANGE	RANGE	THRM	FREQ	FREQ	FREQ	0XC4	Yes
0x62	R/W	Enhance Acoustics Reg 1	MIN3	MIN2	MIN1	SYNC	EN1	ACOU	ACOU	ACOU	0X00	Yes
0x63	R/W	Enhance Acoustics Reg 2	EN2	ACOU2	ACOU2	ACOU2	EN3	ACOU3	ACOU3	ACOU3	0X00	Yes
0x64	R/W	PWM1 Min Duty Cycle	7	6	5	4	3	2	1	0	0X80	Yes
0x65	R/W	PWM2 Min Duty Cycle	7	6	5	4	3	2	1	0	0X80	Yes
0x66	R/W	PWM3 Min Duty Cycle	7	6	5	4	3	2	1	0	0X80	Yes
0x67	R/W	Remote 1 Temp T _{MIN}	7	6	5	4	3	2	1	0	0X9A	Yes
0x68	R/W	Local Temp T _{MIN}	7	6	5	4	3	2	1	0	0X9A	Yes
0x69	R/W	Remote 2 Temp T _{MIN}	7	6	5	4	3	2	1	0	0X9A	Yes
0x6A	R/W	Remote 1 THERM Temp Limit	7	6	5	4	3	2	1	0	0XA4	Yes
0x6B	R/W	Local THERM Temp Limit	7	6	5	4	3	2	1	0	0XA4	Yes
0x6C	R/W	Remote 2 THERM Temp Limit	7	6	5	4	3	2	1	0	0XA4	Yes
0x6D	R/W	Remote 1 and Local Temp/T _{MIN} Hysteresis	HYSR1	HYSR1	HYSR1	HYSR1	HYSL	HYSL	HYSL	HYSL	0X44	Yes
0x6E	R/W	Remote 2 Temp/T _{MIN} Hysteresis	HYSR2	HYSR2	HYSR2	HYRS	RES	RES	RES	RES	0X40	Yes
0x6F	R/W	XNOR Tree Test Enable	RES	RES	RES	RES	RES	RES	RES	XEN	0X00	Yes
0x70	R/W	Remote 1 Temperature Offset	7	6	5	4	3	2	1	0	0X00	Yes
0x71	R/W	Local Temperature Offset	7	6	5	4	3	2	1	0	0X00	Yes
0x72	R/W	Remote 2 Temperature Offset	7	6	5	4	3	2	1	0	0X00	Yes
0x73	R/W	Configuration Register 2	SHDN	CONV	ATTN	AVG	AIN4	AIN3	AIN2	AIN1	0X00	Yes
0x74	R/W	Interrupt Mask 1 Register	OOL	R2T	LT	RIT	RES	V _{CC}	V _{CCP}	RES	0X00	
0x75	R/W	Interrupt Mask 2 Register	D2	D1	F4P	FAN3	FAN2	FAN1	OVT	RES	0X00	
0x76	R/W	Extended Resolution 1	RES	RES	V _{CC}	V _{CC}	V _{CCP}	V _{CCP}	RES	RES	0X00	
0x77	R/W	Extended Resolution 2	TDM2	TDM2	LTMP	LTMP	TDM1	TDM1	RES	RES	0X00	
0x78	R/W	Configuration Register 3	DC4	DC3	DC2	DC1	FAST	BOOST	THERM	ALERT Enable	0X00	Yes
0x79	R	THERM Timer Status Register	TMR	TMR	TMR	TMR	TMR	TMR	TMR	ASRT/T MRO	0X00	
0x7A	R/W	THERM Timer Limit Register	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	0X00	
0x7B	R/W	TACH Pulses per Revolution	FAN4	FAN4	FAN3	FAN3	FAN2	FAN2	FAN1	FAN1	0X55	

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Address	RW	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Lockable?
0x7C	R/W	Configuration Register 5	RES	RES	RES	RES	GPIOP	GPIOD	LF/HF	Twos Compl	0X00	Yes
0x7D	R/W	Configuration Register 4	RES	RES	BpAtt V _{CCP}	RES	AINL	AINL	Pin 9 Func	Pin 9 Func	0X00	Yes
0x7E	R	Test Register 1	DO NOT WRITE TO THESE REGISTERS								0X00	Yes
0x7F	R	Test Register 2	DO NOT WRITE TO THESE REGISTERS								0X00	Yes

Table 17. Voltage Reading Registers (Power-On Default = 0x00)¹

Register Address	R/W	Description
0x21	Read-only	Reflects the voltage measurement ² at the V _{CCP} input on Pin 14 (8 MSBs of reading).
0x22	Read-only	Reflects the voltage measurement ³ at the V _{CC} input on Pin 3 (8 MSBs of reading).

¹If the extended resolution bits of these readings are also being read, the extended resolution registers (Reg. 0x76, 0x77) must be read first. Once the extended resolution registers have been read, the associated MSB reading registers are frozen until read. Both the extended resolution registers and the MSB registers are frozen.

²If V_{CCP}Low (Bit 1 of the Dynamic T_{MIN} Control Register 1, 0x36) is set, V_{CCP} can control the sleep state of the ADT7467.

³V_{CC} (Pin 3) is the supply voltage for the ADT7467.

Table 18. Temperature Reading Registers (Power-On Default = 0x01)^{1,2}

Register Address	R/W	Description
0x25	Read-only	Remote 1 temperature reading ^{3,4} (8 MSB of reading).
0x26	Read-only	Local temperature reading (8 MSB of reading).
0x27	Read-only	Remote 2 temperature reading (8 MSB of reading).

¹These temperature readings can be in twos complement or Offset 64 format; this interpretation is determined by Bit 0 of Configuration Register 5 (0x7C).

²If the extended resolution bits of these readings are also being read, the extended resolution registers (Reg. 0x76, 0x77) must be read first. Once the extended resolution registers have been read, all associated MSB reading registers get frozen until read. Both the extended resolution registers and the MSB registers are frozen.

³In twos complement mode, a temperature reading of -128°C (0x80) indicates a diode fault (open or short) on that channel.

⁴In Offset 64 mode, a temperature reading of -64°C (0x00) indicates a diode fault (open or short) on that channel.

Table 19. Fan Tachometer Reading Registers (Power-On Default = 0x00)¹

Register Address	R/W	Description
0x28	Read-only	TACH1 low byte.
0x29	Read-only	TACH1 high byte.
0x2A	Read-only	TACH2 low byte.
0x2B	Read-only	TACH2 high byte.
0x2C	Read-only	TACH3 low byte.
0x2D	Read-only	TACH3 high byte.
0x2E	Read-only	TACH4 low byte.
0x2F	Read-only	TACH4 high byte.

¹These registers count the number of 11.11 μs periods (based on an internal 90 kHz clock) that occur between a number of consecutive fan TACH pulses (default = 2). The number of TACH pulses used to count can be changed using the fan pulses per revolution register (Reg. 0x7B). This allows the fan speed to be accurately measured. Because a valid fan tachometer reading requires that two bytes are read, the low byte *must* be read first. Both the low and high bytes are then frozen until read. At power-on, these registers contain 0x0000 until such time as the first valid fan TACH measurement is read into these registers. This prevents false interrupts from occurring while the fans are spinning up.

A count of 0xFFFF indicates that a fan is one of the following:

- Stalled or blocked (object jamming the fan).
- Failed (internal circuitry destroyed).
- Not populated. (The ADT7467 expects to see a fan connected to each TACH. If a fan is not connected to that TACH, its TACH minimum high and low bytes should be set to 0xFFFF.)
- Alternate function, for example, TACH4 reconfigured as THERM pin.
- 2-wire instead of 3-wire fan.

Table 20. Current PWM Duty Cycle Registers (Power-On Default = 0x00)¹

Register Address	R/W	Description
0x30	Read/write	PWM1 current duty cycle (0% to 100% duty cycle = 0x00 to 0xFF).
0x31	Read/write	PWM2 current duty cycle (0% to 100% duty cycle = 0x00 to 0xFF).
0x32	Read/write	PWM3 current duty cycle (0% to 100% duty cycle = 0x00 to 0xFF).

¹These registers reflect the PWM duty cycle driving each fan at any given time. When in automatic fan speed control mode, the ADT7467 reports the PWM duty cycles back through these registers. The PWM duty cycle values vary according to temperature in automatic fan speed control mode. During fan startup, these registers report back 0x00. In software mode, the PWM duty cycle outputs can be set to any duty cycle value by writing to these registers.

Table 21. Operating Point Registers (Power-On Default = 0x64)^{1,2,3}

Register Address	R/W ³	Description
0x33	Read/write	Remote 1 operating point register (default = 100°C).
0x34	Read/write	Local temperature operating point register (default = 100°C).
0x35	Read/write	Remote 2 operating point register (default = 100°C).

¹These registers set the target operating point for each temperature channel when the dynamic T_{MIN} control feature is enabled.

²The fans being controlled are adjusted to maintain temperature about an operating point.

³These registers become read-only when the Configuration Register 1 lock bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 22. Register 0x36—Dynamic T_{MIN} Control Register 1 (Power-On Default = 0x00)¹

Bit	Name	R/W	Description
<0>	CYR2	Read/write	MSB of 3-Bit Remote 2 Cycle Value. The other two bits of the code reside in Dynamic T _{MIN} Control Register 2 (Reg. 0x37). These three bits define the delay time between making subsequent T _{MIN} adjustments in the control loop, in terms of the number of monitoring cycles. The system has associated thermal time constants that need to be found to optimize the response of fans and the control loop.
<1>	V _{CCP} LO	Read/write	V _{CCP} LO = 1. When the power is supplied from 3.3 V STANDBY and the core voltage (V _{CCP}) drops below its V _{CCP} low limit value (Reg. 0x46), the following occurs: <ul style="list-style-type: none"> • Status Bit 1 in Status Register 1 is set. • SMBALERT is generated, if enabled. • PROCHOT monitoring is disabled. • Dynamic T_{MIN} control is disabled. • The device is prevented from entering shutdown. • Everything is re-enabled once V_{CCP} increases above the V_{CCP} low limit.
<2>	PHTR1	Read/write	PHTR1 = 1 copies the Remote 1 current temperature to the Remote 1 operating point register, if $\overline{\text{THERM}}$ is asserted. The operating point contains the temperature at which $\overline{\text{THERM}}$ is asserted, allowing the system to run as quietly as possible without affecting system performance. PHTR1 = 0 ignores any $\overline{\text{THERM}}$ assertions on the $\overline{\text{THERM}}$ pin. The Remote 1 operating point register reflects its programmed value.
<3>	PHTL	Read/write	PHTL = 1 copies the local channel's current temperature to the local operating point register, if $\overline{\text{THERM}}$ is asserted. The operating point contains the temperature at which $\overline{\text{THERM}}$ is asserted. This allows the system to run as quietly as possible without affecting system performance. PHTL = 0 ignores any $\overline{\text{THERM}}$ assertions on the $\overline{\text{THERM}}$ pin. The local temperature operating point register reflects its programmed value.
<4>	PHTR2	Read/write	PHTR2 = 1 copies the Remote 2 current temperature to the Remote 2 operating point register, if $\overline{\text{THERM}}$ is asserted. The operating point contains the temperature at which $\overline{\text{THERM}}$ is asserted, allowing the system to run as quietly as possible without affecting system performance. PHTR2 = 0 ignores any $\overline{\text{THERM}}$ assertions on the $\overline{\text{THERM}}$ pin. The Remote 2 operating point register reflects its programmed value.
<5>	R1T	Read/write	R1T = 1 enables dynamic T _{MIN} control on the Remote 1 temperature channel. The chosen T _{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for this zone. R1T = 0 disables dynamic T _{MIN} control. The T _{MIN} value chosen is not adjusted, and the channel behaves as described in the Fan Speed Control section.
<6>	LT	Read/write	LT=1 enables dynamic T _{MIN} control on the local temperature channel. The chosen T _{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for this zone. LT = 0 disables dynamic T _{MIN} control. The T _{MIN} value chosen is not adjusted, and the channel behaves as described in the Fan Speed Control section.
<7>	R2T	Read/write	R2T = 1 enables dynamic T _{MIN} control on the Remote 2 temperature channel. The chosen T _{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for this zone. R2T = 0 disables dynamic T _{MIN} control. The T _{MIN} value chosen is not adjusted and the channel behaves as described in the Fan Speed Control section.

¹This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any subsequent attempts to write to this register fail.

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Table 23. Register 0x37—Dynamic T_{MIN} Control Register 2 (Power-On Default = 0x00)¹

Bit	Name	R/W	Description		
<2:0>	CYR1	Read/write	3-Bit Remote 1 Cycle Value. These three bits define the delay time between making subsequent T _{MIN} adjustments in the control loop for the Remote 1 channel, in terms of number of monitoring cycles. The system has associated thermal time constants that need to be found to optimize the response of fans and the control loop.		
			Bits	Decrease Cycle	Increase Cycle
			000	8 cycles (1 s)	16 cycles (2 s)
			001	16 cycles (2 s)	32 cycles (4 s)
			010	32 cycles (4 s)	64 cycles (8 s)
			011	64 cycles (8 s)	128 cycles (16 s)
			100	128 cycles (16 s)	256 cycles (32 s)
			101	256 cycles (32 s)	512 cycles (64 s)
			110	512 cycles (64 s)	1024 cycles (128 s)
111	1024 cycles (128 s)	2048 cycles (256 s)			
<5:3>	CYL	Read/write	3-Bit Local Temperature Cycle Value. These three bits define the delay time between making subsequent T _{MIN} adjustments in the control loop for the local temperature channel, in terms of number of monitoring cycles. The system has associated thermal time constants that need to be found to optimize the response of fans and the control loop.		
			Bits	Decrease Cycle	Increase Cycle
			000	8 cycles (1 s)	16 cycles (2 s)
			001	16 cycles (2 s)	32 cycles (4 s)
			010	32 cycles (4 s)	64 cycles (8 s)
			011	64 cycles (8 s)	128 cycles (16 s)
			100	128 cycles (16 s)	256 cycles (32 s)
			101	256 cycles (32 s)	512 cycles (64 s)
			110	512 cycles (64 s)	1024 cycles (128 s)
111	1024 cycles (128 s)	2048 cycles (256 s)			
<7:6>	CYR2	Read/write	2 LSBs of 3-Bit Remote 2 Cycle Value. The MSB of the 3-bit code resides in Dynamic T _{MIN} Control Register 1 (Reg. 0x36). These three bits define the delay time between making subsequent T _{MIN} adjustments in the control loop for the Remote 2 channel, in terms of number of monitoring cycles. The system has associated thermal time constants that need to be found to optimize the response of fans and the control loop.		
			Bits	Decrease Cycle	Increase Cycle
			000	8 cycles (1 s)	16 cycles (2 s)
			001	16 cycles (2 s)	32 cycles (4 s)
			010	32 cycles (4 s)	64 cycles (8 s)
			011	64 cycles (8 s)	128 cycles (16 s)
			100	128 cycles (16 s)	256 cycles (32 s)
			101	256 cycles (32 s)	512 cycles (64 s)
			110	512 cycles (64 s)	1024 cycles (128 s)
111	1024 cycles (128 s)	2048 cycles (256 s)			

¹This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any subsequent attempts to write to this register fail.

Table 24. Maximim PWM Duty Cycle (Power-On Default = 0xFF)^{1,2}

Register Address	R/W ²	Description
0x38	Read/write	Maximum duty cycle for PWM1 output, default = 100% (0xFF).
0x39	Read/write	Maximum duty cycle for PWM2 output, default = 100% (0xFF).
0x3A	Read/write	Maximum duty cycle for PWM3 output, default = 100% (0xFF).

¹These registers set the maximum PWM duty cycle of the PWM output.

²This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any subsequent attempts to write to this register fail.

Table 25. Register 0x40—Configuration Register 1 (Power-On Default = 0x01)

Bit	Name	R/W	Description
<0>	STRT	Read/write	Logic 1 enables monitoring and PWM control outputs based on the limit settings programmed. Logic 0 disables monitoring and PWM control based on the default power-up limit settings. Note that the limit values programmed are preserved even if a Logic 0 is written to this bit and the default settings are enabled. This bit becomes read-only and cannot be changed once Bit 1 (LOCK bit) has been written. All limit registers should be programmed by BIOS before setting this bit to 1. (Lockable.)
<1>	LOCK	Write once	Logic 1 locks all limit values to their current settings. Once this bit is set, all lockable registers become read-only and cannot be modified until the ADT7467 is powered down and powered up again. This prevents rogue programs such as viruses from modifying critical system limit settings. (Lockable.)
<2>	RDY	Read-only	This bit is set to 1 by the ADT7467 to indicate only that the device is fully powered up and ready to begin system monitoring.
<3>	FSPD	Read/write	When set to 1, this bit runs all fans at full speed. Power-on default = 0. This bit does not get locked at any time.
<4>	Vxl	Read/write	BIOS should set this bit to a 1 when the ADT7467 is configured to measure current from an ADI ADOPT™ VRM controller and to measure the CPU's core voltage. This bit allows monitoring software to display CPU watts usage. (Lockable.)
<5>	FSPDIS	Read/write	Logic 1 disables fan spin-up for two TACH pulses. Instead, the PWM outputs go high for the entire fan spin-up timeout selected.
<6>	TODIS	Read/write	When this bit is set to 1, the SMBus timeout feature is enabled. This allows the ADT7467 to be used with SMBus controllers that cannot handle SMBus timeouts. (Lockable.)
<7>	V _{CC}	Read/write	When this bit is set to 1, the ADT7467 rescales its V _{CC} pin to measure 5 V supply. If this bit is 0, the ADT7467 measures V _{CC} as a 3.3 V supply. (Lockable.)

Table 26. Register 0x41—Interrupt Status Register 1 (Power-On Default = 0x00)

Bit	Name	R/W	Description
<1>	V _{CCP}	Read-only	V _{CCP} = 1 indicates that the V _{CCP} high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<2>	V _{CC}	Read-only	V _{CC} = 1 indicates that the V _{CC} high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<4>	R1T	Read-only	R1T = 1 indicates that the Remote 1 low or high temperature has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<5>	LT	Read-only	LT = 1 indicates that the local low or high temperature has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<6>	R2T	Read-only	R2T = 1 indicates that the Remote 2 low or high temperature has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<7>	OOL	Read-only	OOL = 1 indicates that an out-of-limit event has been latched in Status Register 2. This bit is a logical OR of all status bits in Status Register 2. Software can test this bit in isolation to determine whether any of the voltage, temperature, or fan speed readings represented by Status Register 2 are out-of-limit, which saves the need to read Status Register 2 every interrupt or polling cycle.

Table 27. Register 0x42—Interrupt Status Register 2 (Power-On Default = 0x00)

Bit	Name	R/W	Description
<1>	OVT	Read-only	OVT = 1 indicates that one of the $\overline{\text{THERM}}$ overtemperature limits has been exceeded. This bit is cleared on a read of the status register when the temperature drops below $\overline{\text{THERM}} - T_{\text{HYST}}$.
<2>	FAN1	Read-only	FAN1 = 1 indicates that Fan 1 has dropped below minimum speed or has stalled. This bit is <i>not</i> set when the PWM1 output is off.
<3>	FAN2	Read-only	FAN2 = 1 indicates that Fan 2 has dropped below minimum speed or has stalled. This bit is <i>not</i> set when the PWM2 output is off.
<4>	FAN3	Read-only	FAN3 = 1 indicates that Fan 3 has dropped below minimum speed or has stalled. This bit is <i>not</i> set when the PWM3 output is off.
<5>	F4P	Read-only Read/write Read-only	F4P = 1 indicates that Fan 4 has dropped below minimum speed or has stalled. This bit is <i>not</i> set when the PWM3 output is off. When Pin 9 is programmed as a GPIO output, writing to this bit determines the logic output of the GPIO. If Pin 9 is configured as the $\overline{\text{THERM}}$ timer input for $\overline{\text{THERM}}$ monitoring, then this bit is set when the $\overline{\text{THERM}}$ assertion time exceeds the limit programmed in the $\overline{\text{THERM}}$ limit register (Reg. 0x7A).
<6>	D1	Read-only	D1 = 1 indicates either an open or short circuit on the Thermal Diode 1 inputs.
<7>	D2	Read-only	D2 = 1 indicates either an open or short circuit on the Thermal Diode 2 inputs.

Table 28. Voltage Limit Registers¹

Register Address	R/W	Description ²	Power-On Default
0x46	Read/write	V _{CCP} low limit.	0x00
0x47	Read/write	V _{CCP} high limit.	0xFF
0x48	Read/write	V _{CC} low limit.	0x00
0x49	Read/write	V _{CC} high limit.	0xFF

¹Setting the Configuration Register 1 lock bit has no effect on these registers.

²High Limits: An interrupt is generated when a value exceeds its high limit (> comparison). Low Limits: An interrupt is generated when a value is equal to or below its low limit (≤ comparison).

Table 29. Temperature Limit Registers¹

Register Address	R/W	Description ²	Power-On Default
0x4E	Read/write	Remote 1 temperature low limit.	0x81
0x4F	Read/write	Remote 1 temperature high limit.	0x7F
0x50	Read/write	Local temperature low limit.	0x81
0x51	Read/write	Local temperature high limit.	0x7F
0x52	Read/write	Remote 2 temperature low limit.	0x81
0x53	Read/write	Remote 2 temperature high limit.	0x7F

¹Exceeding any of these temperature limits by 1°C causes the appropriate status bit to be set in the interrupt status register. Setting the Configuration Register 1 lock bit has no effect on these registers.

²High Limits: An interrupt is generated when a value exceeds its high limit (> comparison). Low Limits: An interrupt is generated when a value is equal to or below its low limit (≤ comparison).

Table 30. Fan Tachometer Limit Registers¹

Register Address	R/W	Description	Power-On Default
0x54	Read/write	TACH1 minimum low byte.	0xFF
0x55	Read/write	TACH1 minimum high byte/single channel ADC channel select.	0xFF
0x56	Read/write	TACH2 minimum low byte.	0xFF
0x57	Read/write	TACH2 minimum high byte.	0xFF
0x58	Read/write	TACH3 minimum low byte.	0xFF
0x59	Read/write	TACH3 minimum high byte.	0xFF
0x5A	Read/write	TACH4 minimum low byte.	0xFF
0x5B	Read/write	TACH4 minimum high byte.	0xFF

¹Exceeding any of the TACH limit registers by 1 indicates that the fan is running too slowly or has stalled. The appropriate status bit is set in Interrupt Status Register 2 to indicate the fan failure. Setting the Configuration Register 1 lock bit has no effect on these registers.

Table 31. Register 0x55—TACH 1 Minimum High Byte (Power-On Default = 0xFF)

Bit	Name	R/W	Description
<4:0>	Reserved	Read-only	These bits are reserved when Bit 6 of Config 2 Register (0x73) is set (single-channel ADC mode). Otherwise, these bits represent Bits <4:0> of the TACH1 minimum high byte.
<7:5>	SCADC	Read/write	When Bit 6 of Config 2 Register (0x73) is set (single-channel ADC mode), these bits are used to select the only channel from which the ADC makes measurements. Otherwise, these bits represent Bits <7:5> of the TACH1 minimum high byte.

Table 32. PWM Configuration Registers

Register Address	R/W ¹	Description	Power-On Default
0x5C	Read/write	PWM1 configuration.	0x82
0x5D	Read/write	PWM2 configuration.	0x82
0x5E	Read/write	PWM3 configuration.	0x82

Bit	Name	R/W	Description
<2:0>	SPIN	Read/write	These bits control the startup timeout for PWMx. The PWM output stays high until two valid TACH rising edges are seen from the fan. If there is not a valid TACH signal during the fan TACH measurement directly after the fan startup timeout period, then the TACH measurement reads 0xFFFF and Status Register 2 reflects the fan fault. If the TACH minimum high and low bytes contain 0xFFFF or 0x0000, then the status register 2 bit is not set, even if the fan has not started. 000 = No startup timeout 001 = 100 ms 010 = 250 ms (default) 011 = 400 ms 100 = 667 ms 101 = 1 s 110 = 2 s 111 = 4 s
<3>	SLOW	Read/write	SLOW = 1 makes the ramp rates for acoustic enhancement four times longer.
<4>	INV	Read/write	This bit inverts the PWM output. The default is 0, which corresponds to a logic high output for 100% duty cycle. Setting this bit to 1 inverts the PWM output, so 100% duty cycle corresponds to a logic low output.
<7:5>	BHVR	Read/write	These bits assign each fan to a particular temperature sensor for localized cooling. 000 = Remote 1 temperature controls PWMx (automatic fan control mode). 001 = local temperature controls PWMx (automatic fan control mode). 010 = Remote 2 temperature controls PWMx (automatic fan control mode). 011 = PWMx runs full speed. 100 = PWMx disabled (default). 101 = fastest speed calculated by local and Remote 2 temperature controls PWMx. 110 = fastest speed calculated by all three temperature channel controls PWMx. 111 = manual mode. PWM duty cycle registers (Reg. 0x30 to Reg. 0x32) become writable.

¹These registers become read-only when the Configuration Register 1 lock bit is set to 1. Any subsequent attempts to write to these registers fail.

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Table 33. TEMP T_{RANGE}/PWM Frequency Registers

Register Address	R/W ¹	Description	Power-On Default
0x5F	Read/write	Remote 1 T _{RANGE} /PWM1 frequency.	0xC4
0x60	Read/write	Local temperature T _{RANGE} /PWM2 frequency.	0xC4
0x61	Read/write	Remote 2 T _{RANGE} /PWM3 frequency.	0xC4
Bit	Name	R/W	Description
<2:0>	FREQ	Read/write	These bits control the PWMx frequency. 000 = 11.0 Hz 001 = 14.7 Hz 010 = 22.1 Hz 011 = 29.4 Hz 100 = 35.3 Hz (default) 101 = 44.1 Hz 110 = 58.8 Hz 111 = 88.2 Hz
<3>	THRM	Read/write	THRM = 1 causes the <u>THERM</u> pin (Pin 9) to assert low as an output when this temperature channel's <u>THERM</u> limit has been exceeded by 0.25°C. The <u>THERM</u> pin remains asserted until the temperature is equal to or below the <u>THERM</u> limit. The minimum time that <u>THERM</u> asserts is one monitoring cycle. This allows clock modulation of devices that incorporate this feature. <u>THRM</u> = 0 makes the <u>THERM</u> pin act as an input only, for example, for Pentium 4 <u>PROCHOT</u> monitoring, when Pin 9 is configured as <u>THERM</u> .
<7:4>	RANGE	Read/write	These bits determine the PWM duty cycle vs. the temperature slope for automatic fan control. 0000 = 2°C 0001 = 2.5°C 0010 = 3.33°C 0011 = 4°C 0100 = 5°C 0101 = 6.67°C 0110 = 8°C 0111 = 10°C 1000 = 13.33°C 1001 = 16°C 1010 = 20°C 1011 = 26.67°C 1100 = 32°C (default) 1101 = 40°C 1110 = 53.33°C 1111 = 80°C

¹These registers become read-only when the Configuration Register 1 lock bit is set. Any further attempts to write to these registers have no effect.

Table 34. Register 0x62—Enhanced Acoustics Register 1 (Power-On Default = 0x00)

Bit	Name	R/W ¹	Description															
<2:0>	ACOU	Read/write	These bits select the ramp rate applied to the PWM1 output. Instead of PWM1 jumping instantaneously to its newly calculated speed, PWM1 ramps gracefully at the rate determined by these bits. This feature enhances the acoustics of the fan being driven by the PWM1 output.															
			<table border="1"> <thead> <tr> <th>Time Slot Increase</th> <th>Time for 33% to 100%</th> </tr> </thead> <tbody> <tr> <td>000 = 1</td> <td>35 s</td> </tr> <tr> <td>001 = 2</td> <td>17.6 s</td> </tr> <tr> <td>010 = 3</td> <td>11.8 s</td> </tr> <tr> <td>011 = 4</td> <td>7 s</td> </tr> <tr> <td>100 = 8</td> <td>4.4 s</td> </tr> <tr> <td>101 = 12</td> <td>3 s</td> </tr> <tr> <td>110 = 24</td> <td>1.6 s</td> </tr> <tr> <td>111 = 48</td> <td>0.8 s</td> </tr> </tbody> </table>	Time Slot Increase	Time for 33% to 100%	000 = 1	35 s	001 = 2	17.6 s	010 = 3	11.8 s	011 = 4	7 s	100 = 8	4.4 s	101 = 12	3 s	110 = 24
Time Slot Increase	Time for 33% to 100%																	
000 = 1	35 s																	
001 = 2	17.6 s																	
010 = 3	11.8 s																	
011 = 4	7 s																	
100 = 8	4.4 s																	
101 = 12	3 s																	
110 = 24	1.6 s																	
111 = 48	0.8 s																	
<3>	EN1	Read/write	When this bit is 1, acoustic enhancement is enabled on PWM1 output.															
<4>	SYNC	Read/write	<p>SYNC = 1 synchronizes fan speed measurements on TACH2, TACH3, and TACH4 to PWM3. This allows up to three fans to be driven from PWM3 output and their speeds to be measured.</p> <p>SYNC = 0 synchronizes only TACH3 and TACH4 to PWM3 output.</p>															
<5>	MIN1	Read/write	<p>When the ADT7467 is in automatic fan control mode, this bit defines whether PWM1 is off (0% duty cycle) or at PWM1 minimum duty cycle when the controlling temperature is below its T_{MIN} – hysteresis value.</p> <p>0 = 0% duty cycle below T_{MIN} – hysteresis.</p> <p>1 = PWM1 minimum duty cycle below T_{MIN} – hysteresis.</p>															
<6>	MIN2	Read/write	<p>When the ADT7467 is in automatic fan speed control mode, this bit defines whether PWM2 is off (0% duty cycle) or at PWM2 minimum duty cycle when the controlling temperature is below its T_{MIN} – hysteresis value.</p> <p>0 = 0% duty cycle below T_{MIN} – hysteresis.</p> <p>1 = PWM 2 minimum duty cycle below T_{MIN} – hysteresis.</p>															
<7>	MIN3	Read/write	<p>When the ADT7467 is in automatic fan speed control mode, this bit defines whether PWM3 is off (0% duty cycle) or at PWM3 minimum duty cycle when the controlling temperature is below its T_{MIN} – hysteresis value.</p> <p>0 = 0% duty cycle below T_{MIN} – hysteresis.</p> <p>1 = PWM3 minimum duty cycle below T_{MIN} – hysteresis.</p>															

¹This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

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Table 35. Register 0x63—Enhanced Acoustics Register 2 (Power-On Default = 0x00)

Bit	Name	R/W ¹	Description	
<2:0>	ACOU3	Read/write	These bits select the ramp rate applied to the PWM3 output. Instead of PWM3 jumping instantaneously to its newly calculated speed, PWM3 ramps gracefully at the rate determined by these bits. This effect enhances the acoustics of the fan being driven by the PWM3 output.	
			Time Slot Increase	Time for 33% to 100%
			000 = 1	35 s
			001 = 2	17.6 s
			010 = 3	11.8 s
			011 = 5	7 s
			100 = 8	4.4 s
			101 = 12	3 s
			110 = 24	1.6 s
			111 = 48	0.8 s
< 3 >	EN3	Read/write	When this bit is 1, acoustic enhancement is enabled on PWM3 output.	
<6:4>	ACOU2	Read/write	These bits select the ramp rate applied to the PWM2 output. Instead of PWM2 jumping instantaneously to its newly calculated speed, PWM2 ramps gracefully at the rate determined by these bits. This effect enhances the acoustics of the fans being driven by the PWM2 output.	
			Time Slot Increase	Time for 33% to 100%
			000 = 1	35 s
			001 = 2	17.6 s
			010 = 3	11.8 s
			011 = 5	7 s
			100 = 8	4.4 s
			101 = 12	3 s
			110 = 24	1.6 s
			<7>	EN2

¹This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 36. PWM Minimum Duty Cycle Registers

Register Address	R/W ¹	Description	Power-On Default
0x64	Read/write	PWM1 minimum duty cycle.	0x80 (50% duty cycle)
0x65	Read/write	PWM2 minimum duty cycle.	0x80 (50% duty cycle)
0x66	Read/write	PWM3 minimum duty cycle.	0x80 (50% duty cycle)
Bit	Name	R/W ¹	Description
<7:0>	PWM duty cycle	Read/write	These bits define the PWM _{MIN} duty cycle for PWMx. 0x00 = 0% duty cycle (fan off). 0x40 = 25% duty cycle. 0x80 = 50% duty cycle. 0xFF = 100% duty cycle (fan full speed).

¹These registers become read-only when the ADT7467 is in automatic fan control mode.

Table 37. T_{MIN} Registers¹

Register Address	R/W ²	Description	Power-On Default
0x67	Read/write	Remote 1 temperature T _{MIN} .	0x5A (90°C)
0x68	Read/write	Local temperature T _{MIN} .	0x5A (90°C)
0x69	Read/write	Remote 2 temperature T _{MIN} .	0x5A (90°C)

¹These are the T_{MIN} registers for each temperature channel. When the temperature measured exceeds T_{MIN}, the appropriate fan runs at minimum speed and increases with temperature according to T_{RANGE}.

²These registers become read-only when the Configuration Register 1 lock bit is set. Any further attempts to write to these registers have no effect.

Table 38. THERM Limit Registers¹

Register Address	R/W ²	Description	Power-On Default
0x6A	Read/write	Remote 1 THERM limit.	0x64 (100°C)
0x6B	Read/write	Local THERM limit.	0x64 (100°C)
0x6C	Read/write	Remote 2 THERM limit.	0x64 (100°C)

¹If any temperature measured exceeds its THERM limit, all PWM outputs drive their fans at 100% duty cycle. This is a fail-safe mechanism incorporated to cool the system in the event of a critical overtemperature. It also ensures some level of cooling in the event that software or hardware locks up. If set to 0x80, this feature is disabled. The PWM output remains at 100% until the temperature drops below THERM Limit – Hysteresis. If the THERM pin is programmed as an output, then exceeding these limits by 0.25°C can cause the THERM pin to assert low as an output.

²These registers become read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to these registers have no effect.

Table 39. Temperature/T_{MIN} Hysteresis Registers¹

Register Address	R/W ²	Description	Power-On Default
0x6D <3:0>	Read/write HYSL	Remote 1 and local temperature hysteresis. Local temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the local temperature AFC and dynamic T _{MIN} control loops.	0x44
<7:4>	HYSR1	Remote 1 temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the Remote 1 temperature AFC and dynamic T _{MIN} control loops.	
0x6E <7:4>	Read/write HYSR2	Remote 2 temperature hysteresis. Local temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the local temperature AFC and dynamic T _{MIN} control loops.	0x40

¹Each 4-bit value controls the amount of temperature hysteresis applied to a particular temperature channel. Once the temperature for that channel falls below its T_{MIN} value, the fan remains running at PWM_{MIN} duty cycle until the temperature = T_{MIN} – hysteresis. Up to 15°C of hysteresis can be assigned to any temperature channel. The hysteresis value chosen also applies to that temperature channel, if its THERM limit is exceeded. The PWM output being controlled goes to 100%, if the THERM limit is exceeded and remains at 100% until the temperature drops below THERM – hysteresis. For acoustic reasons, it is recommended that the hysteresis value not be programmed less than 4°C. Setting the hysteresis value lower than 4°C causes the fan to switch on and off regularly when the temperature is close to T_{MIN}.

²These registers become read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to these registers have no effect.

Table 40. XNOR Tree Test Enable

Register Address	R/W ¹	Description	Power-On Default
0x6F <0>	Read/write XEN	XNOR tree test enable register. If the XEN bit is set to 1, the device enters the XNOR tree test mode. Clearing the bit removes the device from the XNOR tree test mode.	0x00
<7:1>	Reserved	Unused. Do not write to these bits.	

¹This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 41. Remote 1 Temperature Offset

Register Address	R/W ¹	Description	Power-On Default
0x70 <7:0>	Read/write Read/write	Remote 1 temperature offset. Allows a twos complement offset value to be automatically added to or subtracted from the Remote 1 temperature reading. This is to compensate for any inherent system offsets such as PCB trace resistance. LSB value = 0.5°C.	0x00

¹This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

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Table 42. Local Temperature Offset

Register Address	R/W ¹	Description	Power-On Default
0x71 <7:0>	Read/write Read/write	Local temperature offset. Allows a twos complement offset value to be automatically added to or subtracted from the local temperature reading. LSB value = 0.5°C.	0x00

¹This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 43. Remote 2 Temperature Offset

Register Address	R/W ¹	Description	Power-On Default
0x72 <7:0>	Read/write Read/write	Remote 2 temperature offset. Allows a twos complement offset value to be automatically added to or subtracted from the Remote 2 temperature reading. This is to compensate for any inherent system offsets such as PCB trace resistance. LSB value = 0.5°C.	0x00

¹This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 44. Register 0x73—Configuration Register 2 (Power-On Default = 0x00)

Bit	Name	R/W ¹	Description
0	AIN1	Read/write	AIN1 = 0, speed of 3-wire fans measured using the TACH output from the fan. AIN1 = 1, Pin 6 is reconfigured to measure the speed of 2-wire fans using an external sensing resistor and coupling capacitor. AIN voltage threshold is set via Configuration Register 4 (Reg. 0x7D). Only relevant in low frequency mode.
1	AIN2	Read/write	AIN2 = 0, speed of 3-wire fans measured using the TACH output from the fan. AIN2 = 1, Pin 7 is reconfigured to measure the speed of 2-wire fans using an external sensing resistor and coupling capacitor. AIN voltage threshold is set via Configuration Register 4 (Reg. 0x7D). Only relevant in low frequency mode.
2	AIN3	Read/write	AIN3 = 0, speed of 3-wire fans measured using the TACH output from the fan. AIN3 = 1, Pin 4 is reconfigured to measure the speed of 2-wire fans using an external sensing resistor and coupling capacitor. AIN voltage threshold is set via Configuration Register 4 (Reg. 0x7D). Only relevant in low frequency mode.
3	AIN4	Read/write	AIN4 = 0, speed of 3-wire fans measured using the TACH output from the fan. AIN4 = 1, Pin 9 is reconfigured to measure the speed of 2-wire fans using an external sensing resistor and coupling capacitor. AIN voltage threshold is set via Configuration Register 4 (Reg. 0x7D). Only relevant in low frequency mode.
4	AVG	Read/write	AVG = 1, averaging on the temperature and voltage measurements is turned off. This allows measurements on each channel to be made much faster.
5	ATTN	Read/write	ATTN = 1, the ADT7467 removes the attenuators from the V _{CCP} input. The V _{CCP} input can be used for other functions such as connecting up external sensors.
6	CONV	Read/write	CONV = 1, the ADT7467 is put into a single-channel ADC conversion mode. In this mode, the ADT7467 can be made to read continuously from one input only, for example, Remote 1 temperature. The appropriate ADC channel is selected by writing to bits <7:5> of TACH1 minimum high byte register (0x55).
			Bits <7:5> Reg. 0x55
			000 Reserved
			001 V _{CCP}
			010 V _{CC} (3.3 V)
			011 Reserved
			100 Reserved
			101 Remote 1 temperature
			110 Local temperature
			111 Remote 2 temperature
7	SHDN	Read/write	SHDN = 1, ADT7467 goes into shutdown mode. All PWM outputs assert low (or high depending on state of INV bit) to switch off all fans. The PWM current duty cycle registers read 0x00 to indicate that the fans are not being driven.

¹This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 45. Register 0x74—Interrupt Mask Register 1 (Power-On Default <7:0> = 0x00)

Bit	Name	R/W	Description
1	V _{CCP}	Read/write	V _{CCP} = 1, masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the V _{CCP} channel.
2	V _{CC}	Read/write	V _{CC} = 1, masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the V _{CC} channel.
4	R1T	Read/write	R1T = 1, masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the Remote 1 temperature channel.
5	LT	Read/write	LT = 1, masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the local temperature channel.
6	R2T	Read/write	R2T = 1, masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the Remote 2 temperature channel.
7	OOL	Read/write	OOL = 1, masks $\overline{\text{SMBALERT}}$ for any out-of-limit condition in Status Register 2.

Table 46. Register 0x75—Interrupt Mask Register 2 (Power-On Default <7:0> = 0x00)

Bit	Name	R/W	Description
1	OVT	Read only	OVT = 1, masks $\overline{\text{SMBALERT}}$ for overtemperature $\overline{\text{THERM}}$ conditions.
2	FAN1	Read/write	FAN1 = 1, masks $\overline{\text{SMBALERT}}$ for a Fan 1 fault.
3	FAN2	Read/write	FAN2 = 1, masks $\overline{\text{SMBALERT}}$ for a Fan 2 fault.
4	FAN3	Read/write	FAN3 = 1, masks $\overline{\text{SMBALERT}}$ for a Fan 3 fault.
5	F4P	Read/write	F4P = 1, masks $\overline{\text{SMBALERT}}$ for a Fan 4 fault. If the TACH4 pin is being used as the $\overline{\text{THERM}}$ input, this bit masks $\overline{\text{SMBALERT}}$ for a $\overline{\text{THERM}}$ timer event.
6	D1	Read/write	D1 = 1, masks $\overline{\text{SMBALERT}}$ for a diode open or short on a Remote 1 channel.
7	D2	Read/write	D2 = 1, masks $\overline{\text{SMBALERT}}$ for a diode open or short on a Remote 2 channel.

Table 47. Register 0x76—Extended Resolution Register 1¹

Bit	Name	R/W	Description
<3:2>	V _{CCP}	Read-only	V _{CCP} LSBs. Holds the 2 LSBs of the 10-bit V _{CCP} measurement.
<5:4>	V _{CC}	Read-only	V _{CC} LSBs. Holds the 2 LSBs of the 10-bit V _{CC} measurement.

¹If this register is read, this register and the registers holding the MSB of each reading are frozen until read.

Table 48. Register 0x77—Extended Resolution Register 2¹

Bit	Name	R/W	Description
<3:2>	TDM1	Read-only	Remote 1 temperature LSBs. Holds the 2 LSBs of the 10-bit Remote 1 temperature measurement.
<5:4>	LTMP	Read-only	Local temperature LSBs. Holds the 2 LSBs of the 10-bit local temperature measurement.
<7:6>	TDM2	Read-only	Remote 2 temperature LSBs. Holds the 2 LSBs of the 10-bit Remote 2 temperature measurement.

¹If this register is read, this register and the registers holding the MSB of each reading are frozen until read.

Table 49. Register 0x78—Configuration Register 3 (Power-On Default = 0x00)

Bit	Name	R/W ¹	Description
<0>	ALERT	Read/write	ALERT = 1, Pin 5 (PWM2/ $\overline{\text{SMBALERT}}$) is configured as an $\overline{\text{SMBALERT}}$ interrupt output to indicate out-of-limit error conditions.
<1>	$\overline{\text{THERM}}$	Read/write	$\overline{\text{THERM}}$ Enable = 1 enables $\overline{\text{THERM}}$ timer monitoring functionality on Pin 9. Also determined by Bits 0 and 1 (PIN9FUNC) of Configuration Register 4. When $\overline{\text{THERM}}$ is asserted, if the fans are running and the boost bit is set, the fans run at full speed. Alternatively, $\overline{\text{THERM}}$ can be programmed so that a timer is triggered to time how long $\overline{\text{THERM}}$ has been asserted.
<2>	BOOST	Read/write	When $\overline{\text{THERM}}$ is an input and BOOST = 1, assertion of $\overline{\text{THERM}}$ causes all fans to run at the maximum programmed duty cycle for fail-safe cooling.
<3>	FAST	Read/write	FAST = 1, enables fast TACH measurements on all channels. This increases the TACH measurement rate from once per second to once every 250 ms (4 ×).
<4>	DC1	Read/write	DC1 = 1, enables TACH measurements to be continuously made on TACH1. Fans must be driven by dc. Setting this bit prevents pulse stretching, because it is not required for DC-driven motors.
<5>	DC2	Read/write	DC2 = ,1 enables TACH measurements to be continuously made on TACH2. Fans must be driven by dc. Setting this bit prevents pulse stretching, because it is not required for DC-driven motors.
<6>	DC3	Read/write	DC3 = 1, enables TACH measurements to be continuously made on TACH3. Fans must be driven by dc. Setting this bit prevents pulse stretching, because it is not required for DC-driven motors.
<7>	DC4	Read/write	DC4 = 1, enables TACH measurements to be continuously made on TACH4. Fans must be driven by dc. Setting this bit prevents pulse stretching, because it is not required for DC-driven motors.

¹This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 50. Register 0x79— $\overline{\text{THERM}}$ Timer Status Register (Power-On Default = 0x00)

Bit	Name	R/W	Description
<7:1>	TMR	Read-only	Times how long $\overline{\text{THERM}}$ input is asserted. These seven bits read zero until the $\overline{\text{THERM}}$ assertion time exceeds 45.52 ms.
<0>	ASRT/ TMRO	Read-only	This bit is set high on the assertion of the $\overline{\text{THERM}}$ input, and is cleared on read. If the $\overline{\text{THERM}}$ assertion time exceeds 45.52 ms, this bit is set and becomes the LSB of the 8-bit TMR reading. This allows $\overline{\text{THERM}}$ assertion times from 45.52 ms to 5.82 s to be reported back with a resolution of 22.76 ms.

Table 51. Register 0x7A— $\overline{\text{THERM}}$ Timer Limit Register (Power-On Default = 0x00)

Bit	Name	R/W	Description
<7:0>	LIMIT	Read/write	Sets maximum $\overline{\text{THERM}}$ assertion length allowed before an interrupt is generated. This is an 8-bit limit with a resolution of 22.76 ms allowing $\overline{\text{THERM}}$ assertion limits of 45.52 ms to 5.82 s to be programmed. If the $\overline{\text{THERM}}$ assertion time exceeds this limit, Bit 5 (F4P) of Interrupt Status Register 2 (Reg. 0x42) is set. If the limit value is 0x00, then an interrupt is generated immediately on the assertion of the $\overline{\text{THERM}}$ input.

Table 52. Register 0x7B—TACH Pulses per Revolution Register (Power-On Default = 0x55)

Bit	Name	R/W	Description
<1:0>	FAN1	Read/write	Sets number of pulses to be counted when measuring Fan 1 speed. Can be used to determine fan pulses per revolution for unknown fan type.
			Pulses Counted 00 = 1 01 = 2 (default) 10 = 3 11 = 4
<3:2>	FAN2	Read/write	Sets number of pulses to be counted when measuring Fan 2 speed. Can be used to determine fan pulses per revolution for unknown fan type.
			Pulses Counted 00 = 1 01 = 2 (default) 10 = 3 11 = 4
<5:4>	FAN3	Read/write	Sets number of pulses to be counted when measuring Fan 3 speed. Can be used to determine fan pulses per revolution for unknown fan type.
			Pulses Counted 00 = 1 01 = 2 (default) 10 = 3 11 = 4
<7:6>	FAN4	Read/write	Sets number of pulses to be counted when measuring Fan 4 speed. Can be used to determine fan pulses per revolution for unknown fan type.
			Pulses Counted 00 = 1 01 = 2 (default) 10 = 3 11 = 4

Table 53. Register 0x7C—Configuration Register 5 (Power-On Default = 0x00)

Bit	Name	R/W ¹	Description
<0>	2sC	Read/write	2sC = 1, sets the temperature range to twos complement temperature range. 2sC = 0, changes the temperature range to Offset 64. When this bit is changed, the ADT7467 interprets all relevant temperature register values as defined by this bit.
<1>	HF/LF		Sets the PWM drive frequency to high frequency mode (0) or low frequency mode (1).
<2>	GPIOD		GPIO direction. When GPIO function is enabled, this determines whether the GPIO is an input (0) or an output (1).
<3>	GPIOP		GPIO polarity. When the GPIO function is enabled and is programmed as an output, this bit determines whether the GPIO is active low (0) or high (1).
<4:7>	RES		Unused.

¹This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

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Table 54. Register 0x7D—Configuration Register 4 (Power-On Default = 0x00)

Bit	Name	R/W ¹	Description
<1:0>	Pin9FUNC	Read/write	These bits set the functionality of Pin 9: 00 = TACH4 (default) 01 = Bidirectional $\overline{\text{THERM}}$ 10 = $\overline{\text{SMBALERT}}$ 11 = GPIO
<3:2>	AINL	Read/write	These two bits define the input threshold for 2-wire fan speed measurements (low frequency mode only): 00 = ± 20 mV 01 = ± 40 mV 10 = ± 80 mV 11 = ± 130 mV
<4:7>	RES		Unused.
<5>	BpAttV _{CCP}		Bypass V _{CCP} attenuator. When set, the measurement scale for this channel changes from 0 V (0x00) to 2.2965V (0xFF) .
<6:7>	RES		Unused.

¹This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

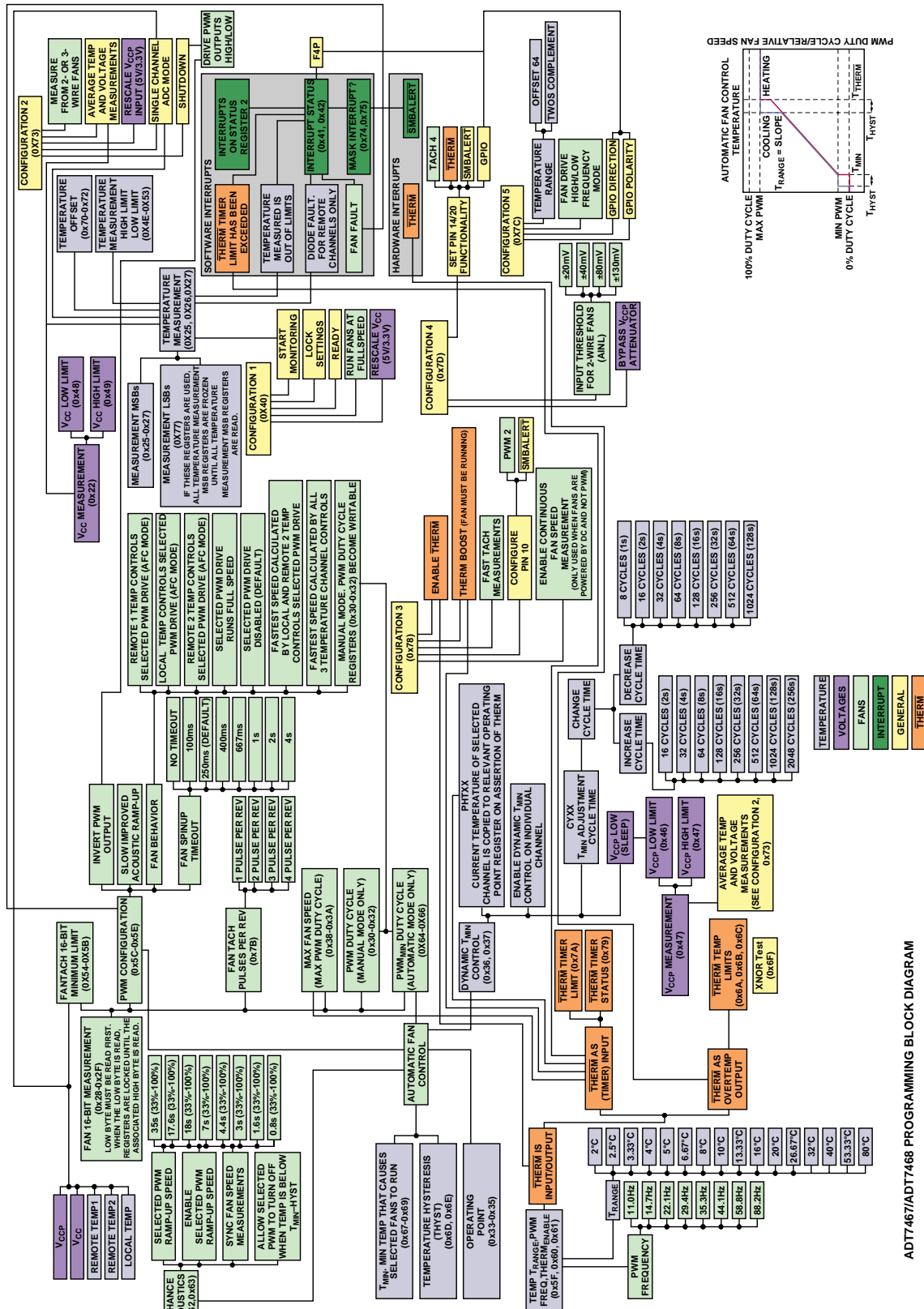
Table 55. Register 0x7E—Manufacturer’s Test Register 1 (Power-On Default = 0x00)

Bit	Name	R/W	Description
<7:0>	Reserved	Read-only	Manufacturer’s test register. These bits are reserved for manufacturer’s test purposes and should <i>not</i> be written to under normal operation.

Table 56. Register 0x7F—Manufacturer’s Test Register 2 (Power-On Default = 0x00)

Bit	Name	R/W	Description
<7:0>	Reserved	Read-only	Manufacturer’s test register. These bits are reserved for manufacturer’s test purposes and should <i>not</i> be written to under normal operation.

ADT7467 PROGRAMMING BLOCK DIAGRAM

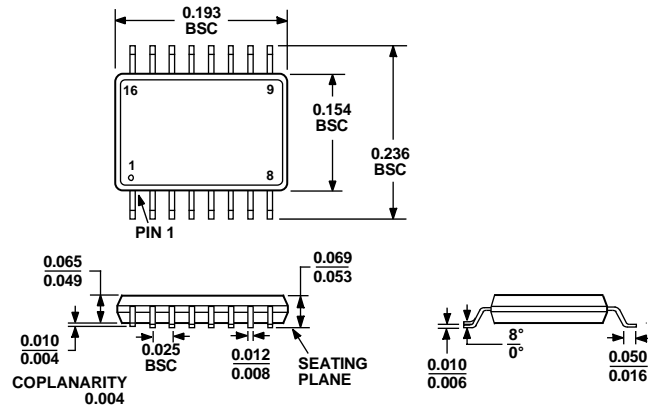


ADT7467/ADT7468 PROGRAMMING BLOCK DIAGRAM

Figure 55.

048930-044

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-137AB

Figure 86. 16-Lead Shrink Small Outline Package [QSOP] (RQ-16)
Dimensions shown in inches

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADT7467ARQ	-40°C to +120°C	16-Lead QSOP	RQ-16
ADT7467ARQ-REEL	-40°C to +120°C	16-Lead QSOP	RQ-16
ADT7467ARQ-REEL7	-40°C to +120°C	16-Lead QSOP	RQ-16

NOTES

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